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FME-MB88121-1.48E

Automotive Solutions

CMOS

FlexRay ASSP

MB88121/MB88121A/MB88121B/MB88121C

■ DESCRIPTION

The MB88121 Series FlexRay ASSP (application specific standard product) facilitates to add FlexRay connectivity to 8-bit, 16-bit and 32-bit microcontrollers that do not comprise embedded FlexRay protocol cores. The device features a FlexRay communication controller based on the ERAY*1 IP core provided by Bosch. The most recent FlexRay communication controller complies to the protocol definition 2.1 of the FlexRay consortium. Fujitsu intends to update the communications controller when new protocol definitions are released. Please, refer to the chapter 'product lineup' for a cross reference between device version and protocol version supported. Several parallel and serial interfaces provide connectivity to a vast number of host processors.

All types of host interfaces are selectable by mode pins that supersede any programming by the user. The configurable parallel host interface connects to most 16-bit and 32-bit microcontrollers while SPI offers serial interfacing options. A DMA support unit avoids that the application on the host processor has to wait until the input buffer becomes available for writing.

The version suffix 'B/C' of the ASSP is operated from a single 3.3V or 5.0 V supply and includes an on board voltage regulator that provides 1.8 V to the internal core. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 80 MHz clock from an external 4 MHz, 5 MHz, 8 MHz, 10 MHz, 16 MHz*2 or 20 MHz*2 clock. Alternatively the user may choose to drive the clock input with a square wave signal from the host processor.

*1 : License of Robert Bosch GmbH

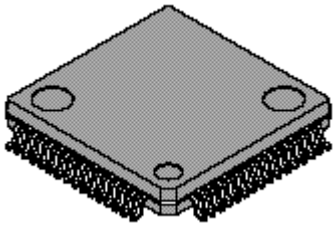
*2 : MB88121C only

rev 1.48 29/Jan/2013

FUJITSU

■ PACKAGE

64-pin Plastic LQFP



(FPT-64P-M03/M24)

The device is offered in a standard 64-pin quad flatpack package with a pin pitch of 0.5 mm.

■ FEATURES

- FlexRay communication controller based on ERAY*1 IP core from Bosch
  - Data rates of up to 10 Mbit/s on each channel
  - Up to 128 message buffers configurable
  - 8 Kbyte of Message RAM for storage of e.g. 128 message buffers with max. 48 byte data section or up to 30 message buffers with 254 byte data section
  - Configuration of message buffers with different payload lengths possible
  - One configurable receive FIFO
  - Each message buffer can be configured as receive buffer, as transmit buffer or as part of the receive FIFO
  - Host access to message buffers via Input and Output Buffer
    Input Buffer: Holds message to be transferred to the Message RAM
    Output Buffer: Holds message read from the Message RAM
  - Filtering for slot counter, cycle counter, and channel
  - Maskable module interrupts
  - Network Management supported
- Configurable parallel host interface
- SPI interface (8 Mbit/s) (MB88121B/C only)
- DMA support unit (MB88121A/B/C only)
- 0.18μm CMOS Process Technology
- Single voltage supply (5.0 V / 3.3 V), internal voltage regulator for 1.9 V core voltage offering low EMI and low power consumption (MB88121B/C only)
- Package : 64-pin*2 plastic LQFP;

*1 : License of Robert Bosch GmbH

*2: Other packages such as 48-pin plastic LQFP featuring only SPI host interface are under consideration.

■ PRODUCT LINEUP

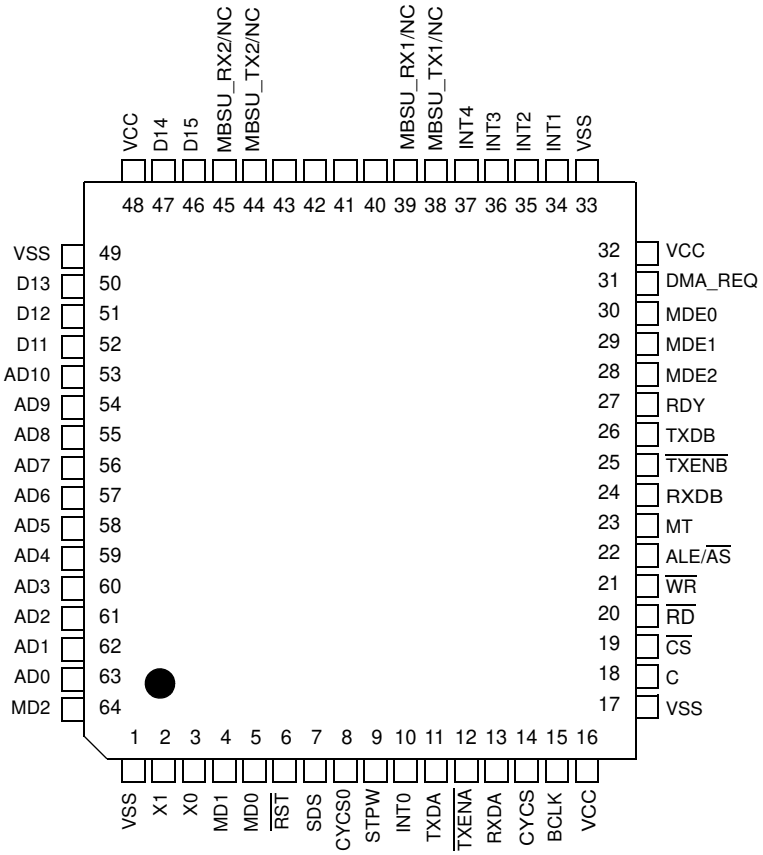
Part Number / Parameter	MB88121	MB88121A	MB88121B	MB88121C
System clock	Direct clock input: 80MHz (or 40MHz for 5Mbit/s). On-chip PLL (evaluation pending): External clock 10 MHz, internal clock 80 MHz (50% duty cycle).		On-chip PLL (jitter evaluation pending) External clock input 4/5/8/10 MHz	Direct clock input: 80MHz. On-chip PLL (jitter evaluation pending) External clock input 4/5/8/10/16/20 MHz
Technology	0.18µm CMOS with triple voltage supply (5.0V, 3.3V, 1,8V).		0.18µm CMOS with on-chip voltage regulator for internal power supply.	
Operating voltage range	5.0V±0.5V, 3.3V±0.3V, 1.8V±0.15V		3.0 V - 5.5 V	
Temperature range	T_A = -40 °C to +85 °C		T_A = -40 °C to +105 °C	T_A = -40 °C to +125 °C
Package	LQFP-64			
FlexRay Protocol version	2.0	2.1	V2.1	
Parallel host interface	Configurable parallel host interface compatible with Fujitsu 32-bit FR microcontrollers. Maximum frequency 33MHz (target)		Configurable parallel host interface compatible with Fujitsu 16-bit 16FX and 32-bit FR microcontrollers.	
SPI interface	-		Configurable clocking schemes and bit direction.	
DMA support unit	-	Generates DMA request signal for host processor for writing the input buffer. Thus the possibility that the input buffer is busy does not produce any waiting time at the host that can issue other tasks during the buffer writing.		
Low voltage interrupt (tbd)	-		Generates an interrupt when internal or external operating voltage drops below certain limits.	

.

■ PIN ASSIGNMENTS

1. Pin assignment in 16 bit multiplexed parallel mode (MB88121B/C only)

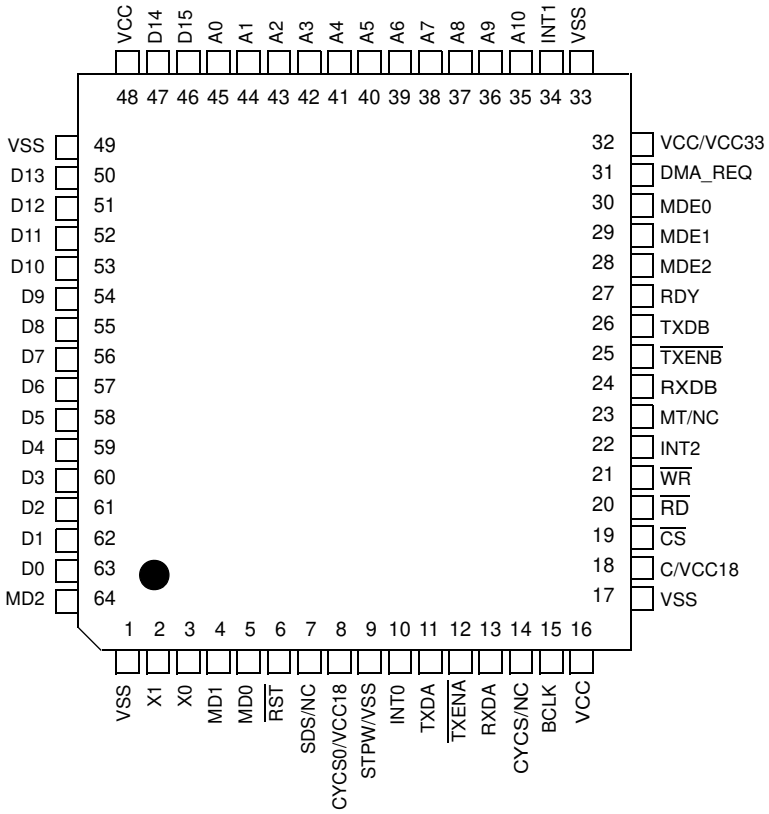
(TOP VIEW)



(FPT-64P-M03/M24)

2. Pin assignment in 16 bit non-multiplexed parallel mode

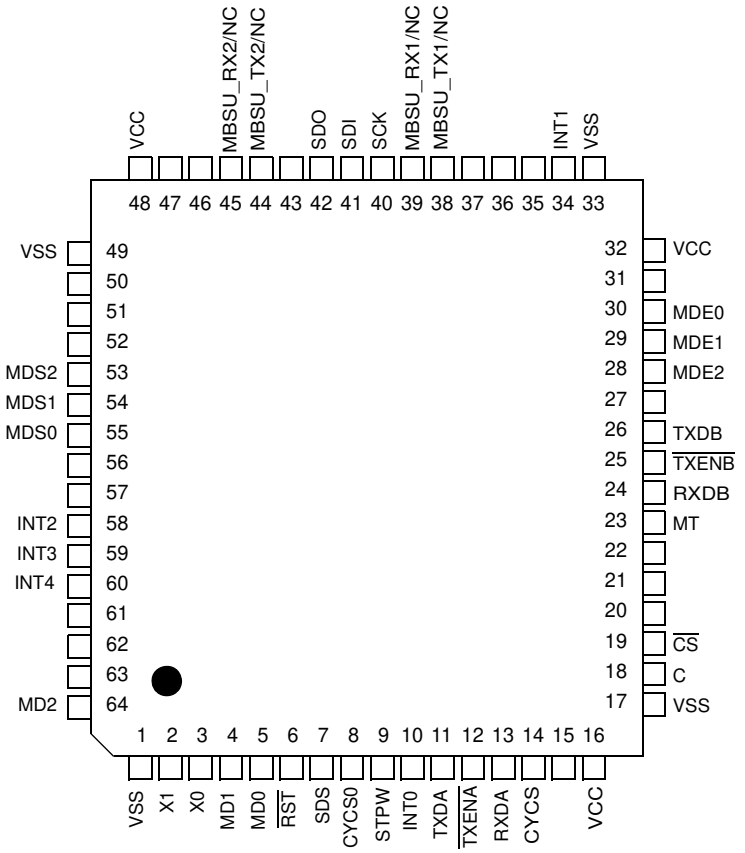
(TOP VIEW)



(FPT-64P-M03/M24)

3. Pin assignment in SPI mode (MB88121B/C only)

(TOP VIEW)



(FPT-64P-M03/M24)

■ PIN DESCRIPTION

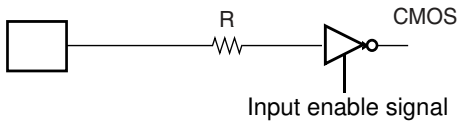
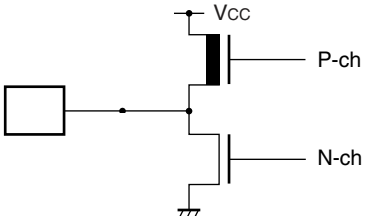
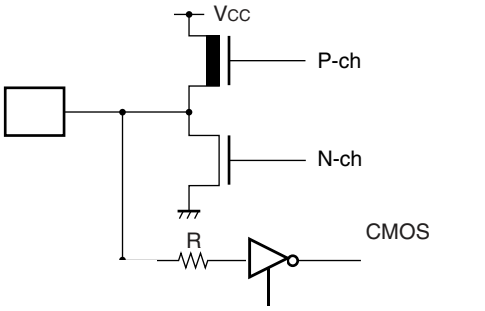
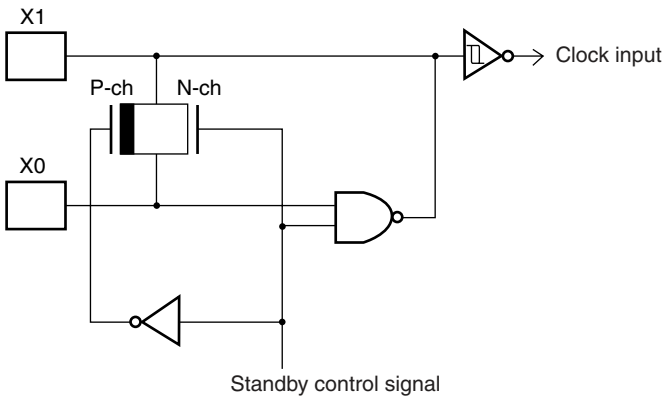
Pin No.	Pin name	Circuit type	Function
1, 17, 33, 49	VSS	—	These are power supply ground (0 V) input pins
16, 48	VCC	—	MB88121B/C: These are power supply (3.3 - 5.0 V) input pins. MB88121(A): These are power supply (5.0 V) input pins
32	VCC/VCC33	—	MB88121B/C: This is a power supply (3.3 - 5.0 V) input pin. MB88121(A): 3.3V supply voltage for the level converters.
18	C/VCC18	—	MB88121B/C: This is the power supply stabilization capacitor pin. It should be connected to higher than or equal to 0.1 µF ceramic capacitor. MB88121(A): 1.8V core supply input pin.
2	X1	D	Oscillation output pin.
3	X0		Oscillation input pin. If external clock is used, it is connected here.
4 - 5	MD1 - MD0	A	Input pins for the mode selection.
6	$\overline{RST}$	A	Reset input pin.
7	SDS/NC	B/-	MB88121B/C: Debug pin: Start of dynamic segment, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
8	CYCS0/VCC18	B/-	MB88121B/C: Debug pin: Cycle 0 start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): 1.8V core supply input pin.
9	STPWT/VSS	C/-	MB88121B/C: Stop Watch Trigger Input pin MB88121(A): Power supply ground (0 V) input pin.
10	INT0	B	Output pin for the Interrupt 0 output.
11	TXDA	B	Output pin for the data transmitter output channel A.
12	$\overline{TXENA}$	B	Output pin for the transmission enable output channel A.
13	RXDA	A	Input pin for the data receiver input channel A.
14	CYCS/NC	B/-	MB88121B/C: Debug pin: Cycle start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
15	BCLK	A	Input pin for the Bus Clock input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.
19	$\overline{CS}$	A	Input pin for the chip select input.
20	$\overline{RD}$	A	Input pin for the read enable input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.
21	$\overline{WR}$	A	Input pin for the write enable input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.

Pin No.	Pin name	Circuit type	Function
22	ALE	C	Input pin for the address latch enable input (high active). This function is enabled in the multiplexed parallel modes for 16FX and for other devices to be defined later.
	$\overline{AS}$		Input pin for the address strobe input (low active). This function is enabled in the multiplexed parallel modes. Timing meets FR core devices (460 series) and other devices.
	INT2		Output pin for the Interrupt 2 output. This function is enabled in 16-bit non-multiplexed parallel mode.
	-		This pin is Hi-Z in in SPI mode.
23	MT/NC	B/-	MB88121B/C: Debug pin; Macrotick start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
24	RXDB	A	Input pin for the data receiver input channel B.
25	$\overline{TXENB}$	B	Output pin for the transmission enable output channel B.
26	TXDB	B	Output pin for the data transmitter output channel B.
27	RDY	B	Output pin for the ready output. This function is enabled in all parallel modes.
	-		This pin is Hi-Z in SPI mode.
28-30	MDE2 - MDE0	A	Input pins for the extended mode selection.
31	DMA_REQ	B	Output pin for the DMA request output (MB88121A/B/C only). On MB88121, this pin outputs "L" level. This function is enabled in all parallel modes
	-	B	This pin is Hi-Z in SPI mode.
34	INT1	B	Output pin for the Interrupt 1 output.
35	A10	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	INT2		Output pin for the Interrupt 2 output. This function is enabled in 16-bit multiplexed parallel mode.
	-		This pin is Hi-Z in SPI mode.
36	A9	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	INT3		Output pin for the Interrupt 3 output. This function is enabled in 16-bit multiplexed parallel mode.
	-		This pin is Hi-Z in SPI mode.
37	A8	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed multiplexed parallel mode.
	INT4		Output pin for the Interrupt 4 output This function is enabled in 16-bit multiplexed parallel mode
	-		This pin is Hi-Z inSPI mode.

Pin No.	Pin name	Circuit type	Function
38	A7	C	Input pins for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	MBSU_TX1		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.
39	A6	C	Input pins for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	MBSU_RX1		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.
40	A5	A	Input pin for the address bus. This function is enabled 16-bit non-multiplexed parallel modes.
	SCK		Input pin for the serial clock input. This function is enabled in SPI mode.
	-		This pin is unused in 16-bit multiplexed parallel modes.
41	A4	A	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	SDI		Input pin for the serial data input. This function is enabled in SPI mode.
	-		This pin is unused in 16-bit multiplexed parallel modes.
42	A3	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	SDO		Output pin for the serial data output. When CS is "H" SDO is High-Z. This function is enabled in SPI mode.
	-		This pin is Hi-Z in 16-bit multiplexed parallel modes.
43	A2	A	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	-		This pin is unused in 16-bit multiplexed parallel mode and in SPI mode.
44	A1	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	MBSU_TX2		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.

Pin No.	Pin name	Circuit type	Function
45	A0	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	MBSU_RX2		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.
46 - 47	D15 - D14	C	I/O pins for the data bus. This function is enabled in 16-bit multiplexed and non-multiplexed parallel modes.
	-		These pins are Hi-Z in SPI mode.
50 - 52	D13 - D11	C	I/O pins for the data bus. This function is enabled in 16-bit multiplexed and non-multiplexed parallel modes.
	-		These pins are Hi-Z in SPI mode.
53 - 55	AD10 - AD8	C	I/O pins for the address/data bus. This function is enabled in 16-bit multiplexed parallel mode.
	D10 - D8		I/O pins for the data bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	MDS2 - MDS0		Input pins for specific settings of serial interfaces. This function is only enabled when serial mode was selected by MD / MDE.
56 - 57	AD7 - AD6	C	I/O pins for the address/data bus. This function is enabled in 16-bit multiplexed parallel mode.
	D7 - D6		I/O pins for the data bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	-		These pins are Hi-Z in SPI mode.
58 - 60	AD5 - AD3	C	I/O pins for the address/data bus. This function is enabled in 16-bit multiplexed parallel mode.
	D5 - D3		I/O pins for the data bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	INT2 - INT4		Output pins for the Interrupt 2 - 4 outputs. This function is enabled in SPI mode.
61 - 63	AD3 - AD0	C	I/O pins for the address/data bus. This function is enabled in 16-bit multiplexed parallel mode.
	D2 - D0		I/O pins for the data bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	-		These pins are Hi-Z in SPI mode.
64	MD2	A	Input pin for the mode selection.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• CMOS hysteresis input
B		• CMOS output
C		• CMOS output • CMOS hysteresis input with input enable signal
D		• Oscillation feedback resistor : 1 MΩ approx.

■ PIN FUNCTIONS VS. MODES

Pin No.	16bit mux mode (MB88121B/C only)	16bit non mux mode	SPI mode (MB88121B/C only)
1	VSS		
2	X1		
3	X0		
4	MD1		
5	MD0		
6	$\overline{RST}$		
7	MB88121B/C: SDS; MB88121(A):NC		
8	MB88121B/C: CYCS0 ; MB88121(A): VCC18		
9	MB88121B/C: STPWT; MB88121(A): VSS		
10	INT0		
11	TXDA		
12	$\overline{TXENA}$		
13	RXDA		
14	MB88121B/C: CYCS; MB88121(A): NC		
15	BCLK		-
16	VCC		
17	VSS		
18	MB88121B/C: C; MB88121(A): VCC18		
19	$\overline{CS}$		
20	$\overline{RD}$		-
21	$\overline{WR}$		-
22	ALE/$\overline{AS}$	INT2	-
23	MB88121B/C: MT; MB88121(A): NC		
24	RXDB		
25	$\overline{TXENB}$		
26	TXDB		
27	RDY		-
28	MDE2		
29	MDE1		
30	MDE0		
31	DMA_REQ		-
32	MB88121B/C: VCC; MB88121(A): VCC33		
33	VSS		

Pin No.	16bit mux mode (MB88121B/C only)	16bit non mux mode	SPI mode (MB88121B/C only)
34	INT1		
35	INT2	A10	-
36	INT3	A9	-
37	INT4	A8	-
38	MBSU_TX1	A7	MBSU_TX1;
39	MBSU_RX1;	A6	MBSU_RX1;
40	-	A5	SCK
41	-	A4	SDI
42	-	A3	SDO
43	-	A2	-
44	MBSU_TX2;	A1	MBSU_TX2
45	MBSU_RX2;	A0	MBSU_RX2
46	D15		-
47	D14		-
48	VCC		
49	VSS		
50	D13		-
51	D12		-
52	D11		-
53	AD10	D10	MDS2
54	AD9	D9	MDS1
55	AD8	D8	MDS0
56	AD7	D7	-
57	AD6	D6	-
58	AD5	D5	INT2
59	AD4	D4	INT3
60	AD3	D3	INT4
61	AD2	D2	-
62	AD1	D1	-
63	AD0	D0	-
64	MD2		

■ MODE SELECTION

MD2	MD1	MD0	Mode	MDE2	MDE1	MDE0	Mode Expansion	
0	X	X	Reserved(Set-prohibitd)					
1	0	0	16-bit (Oscillator)	0	0	0	FR (460)*1	mux
				0	0	1	16FX*1	
				0	1	0	reserved (Set-prohibitd)	
				0	1	1	reserved (Set-prohibitd)	
				1	0	0	FR (460)	non mux
				1	0	1	16FX*2	
				1	1	0	FR (360)	
				1	1	1	reserved (Set-prohibitd)	
1	0	1	16-bit*2 (External Clock Input)	0	0	0	FR (460)	mux
				0	0	1	16FX	
				0	1	0	reserved (Set-prohibitd)	
				0	1	1	reserved (Set-prohibitd)	
				1	0	0	FR (460)	non mux
				1	0	1	16FX	
				1	1	0	FR (360)	
				1	1	1	reserved (Set-prohibitd)	
1	1	0	Serial*1	Refer to tables for - frequency selection - serial type selection				
1	1	1	Reserved(Set-prohibitd)	X	X	X		

The table above describes the encoding of host interface options by mode pins. Basically these mode pins (MD[2:0]) select between the different bus types, parallel or serial, and in case of parallel type, their width. For 32-bit modes, the swapping of low word with high word for non-Intel style access is implicit part of the selected mode. The multiplex style for 16-bit modes is encoded in the mode expansion bits MDE[2:0].

The selection of the serial interface is encoded in MDE[2:0]. Implicitly type and operating frequency are encoded as well here. The specific settings of the selected serial interface are encasuplated in the special mode expansion pins MDS[2:0], that become available for MD[2:0] = 110B (select serial) only.

*1: MB88121B/C only

*2: MB88121C only

■ Used Clock for X0/X1

Input frequency of X0 and X1 is described Table below.

	MD[2:0]		
	100	101	110
Oscillator	4MHz/5MHz/8MHz	-	4MHz/5MHz/8MHz
External Clock	-	4MHz/5MHz/8MHz/ 10MHz/16MHz/20MHz/ 80MHz	4MHz/5MHz/8MHz/ 10MHz

■ FREQUENCY SELECTION IN SERIAL MODE

When operating the device via serial interface, the frequency set up according the table below needs to match the externally supplied clock.

MDE2	MDE1	Frequency
0	0	4 MHz
0	1	5 MHz
1	0	8 MHz
1	1	10 MHz

■ SERIAL INTERFACE TYPE SELECTION

The table below applies when MD[2:0] = 110B.

MDE0	Serial interface type
0	SPI (tbd)
1	Reserved

■ SPI SETTINGS

The table below applies when MD[2:0] = 110B and MDE0 = 0.

MDS2	MDS1	MDS0	Specific SPI Mode Settings
0	0	0	MDS2=LSBFE: Bit Direction 1: Data is transferred least significant bit first. 0: Data is transferred most significant bit first. MDS1=CPOL: Clock Polarity 1: Active-low clock. In idle state SCK is high. 0: Active-high clock. In idle state SCK is low. MDS0=CPHA: Clock Phase 1: Sampling of data occurs at even edges of SCK. 0: Sampling of data occurs at odd edges of SCK.
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Notes on Energization
- Caution on Operation with PLL

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

3. Treatment of unused pins

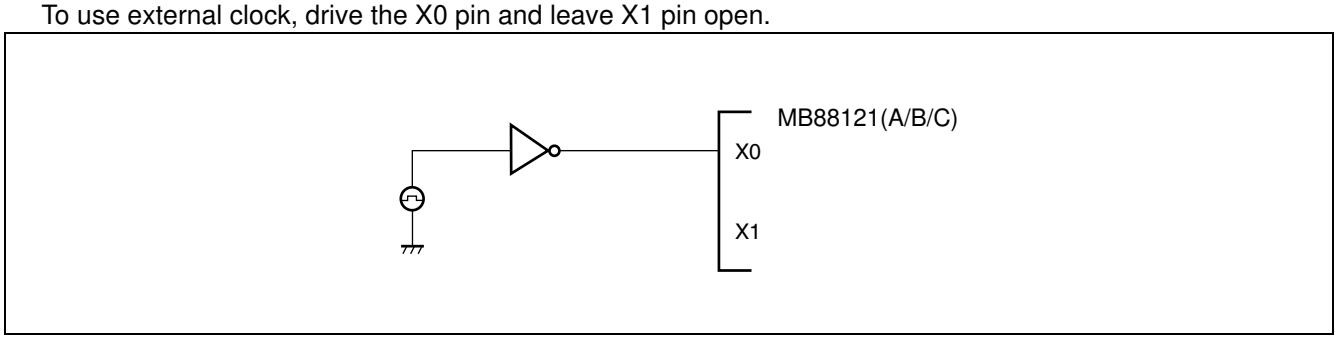
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

Unused inputs that feature an internal pull up resistor, or unused inputs that have been disabled by a particular operational mode can be left open. Make sure that at least one condition is explicitly mentioned for the respective pin.

4. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.

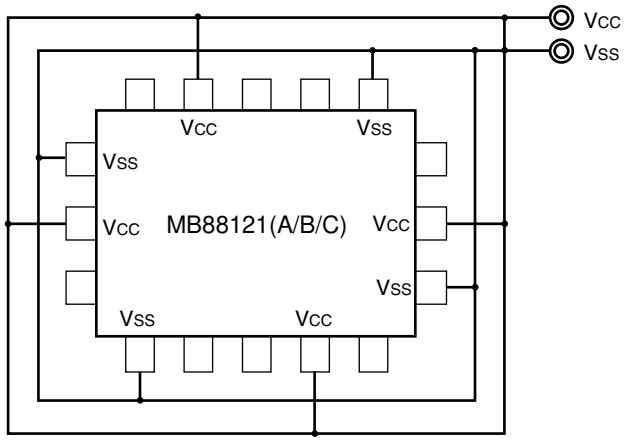


5. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.

- Connect V_{CC} and V_{SS} to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} in the vicinity of V_{CC} and V_{SS} pins of the device.



6. Pull-up/down resistors

MB88121(A/B/C) does not provide internal pull-up/down resistors unless explicitely mentioned in the pin list. Use external components where needed.

7. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

8. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V) .

9. Caution on Operation with PLL

As the device operates with an internal PLL clock, it attempts to be working with the self-oscillating circuit even when there is no external oscillator present or when the external clock input stopped. Performance of this operation, however, cannot be guaranteed.

10. Interrupt pin Assignment

The MB88121/A/B/C series supports interrupt pins. In the differrent operation interface modes the interrupt pin assignment is different.

For 16-bit none multiplexed mode (MD[2:0] = 1,0,0; MDE[2:0] = 1,x,x) the interrupt pin assignment is:

-

Pin name	Internal E-Ray signal	Description
INT0	eray_int0	Signal is activate if Interrupt line 0 is activated via ILE Register (ILE.0 = 1). All E-Ray interrupts set to Interrupt line0 and activated will be signaled via this pin (EILS, SILS EIES, SIES Register).
INT1	eray_int1	Signal is activate if Interrupt line 1 is activated via ILE Register(ILE.1 = 1) All E-Ray interrupts set to Interrupt line1 and activated will be signaled via this pin. (EILS, SILS EIES, SIES Register).
INT2	Timer 0 or Timer 1 interrupt, Low voltage detection	Timer0 and Timer 1 interrupts are signaled via this pins. They are logical or combined In case of low voltage detection it is indicated by INT2

For 16-bit multiplexed mode (MD[2:0] = 1,0,0; MDE[2:0] = 0,x,x) and SPI mode (MD[2:0] = 1,1,0) the interrupt pin assignment is:

Pin name	Internal E-Ray signal	Description
INT0	eray_int0	Signal is activate if Interrupt line is activated via ILE Register (ILE.0 = 1). All E-Ray interrupts set to Interrupt line0 and activated will be signaled via this pin (EILS, SILS EIES, SIES Register).
INT1	eray_int1	Signal is activate if Interrupt line is activated via ILE Register(ILE.1 = 1) All E-Ray interrupts set to Interrupt line1 and activated will be signaled via this pin. (EILS, SILS EIES, SIES Register).
INT2	Timer Interrupt 0	Timer0 Interrupt is signaled via this pins.
INT3	Timer interrupt 1	Timer1 Interrupt is signaled via this pins.
INT4	Low voltage detection	In case of low voltage detection it is indicated by INT4 pin.

11. Pin level at interrupt pins

In case that the interrupt pin is enabled following level is output

Level	Description
0	default value, no interrupt request is pending
1	Interrupt request is pending

The output changes to Low-Level when the corresponding flag in the E-Reay register is cleared.

For timer0 and timer1 interrupt pin(s) the High level is output only a dedicated time and set back to Low-Level.

See E-Ray User Manual for details. It is recommended to use egde detection at host side for these pins.

12. Data Accessing of MB88121 series

The MB88121 series includes a parallel bus Interface using 16-bit data width. However the internal Communication Controller requires a 32-bit data access. Therefore always access the MB88121 using 32-bit data access. The Bus Interface expect two 16-bit data transfer from the Host MCU.

The order of the transfer is important, otherwise data can be lost.

First 16-bit write cycle must be the lower, the second 16-bit write cycle the higher 16-bit address of the 32-bit address. As soon as data is written to the higher 16-bit Address, the Communication Controller is writing the 32-bit value to the address.

Example:

Write access to Input buffer: First 32-bit register WRDS1: (Address: 0x400 - 0x403)

Value of WRDS1 register: 0x0000 0000

First 16-bit write cycle via Bus interface to address 0x400-401: Value: 1234

Value of WRDS1 register: 0x0000 0000

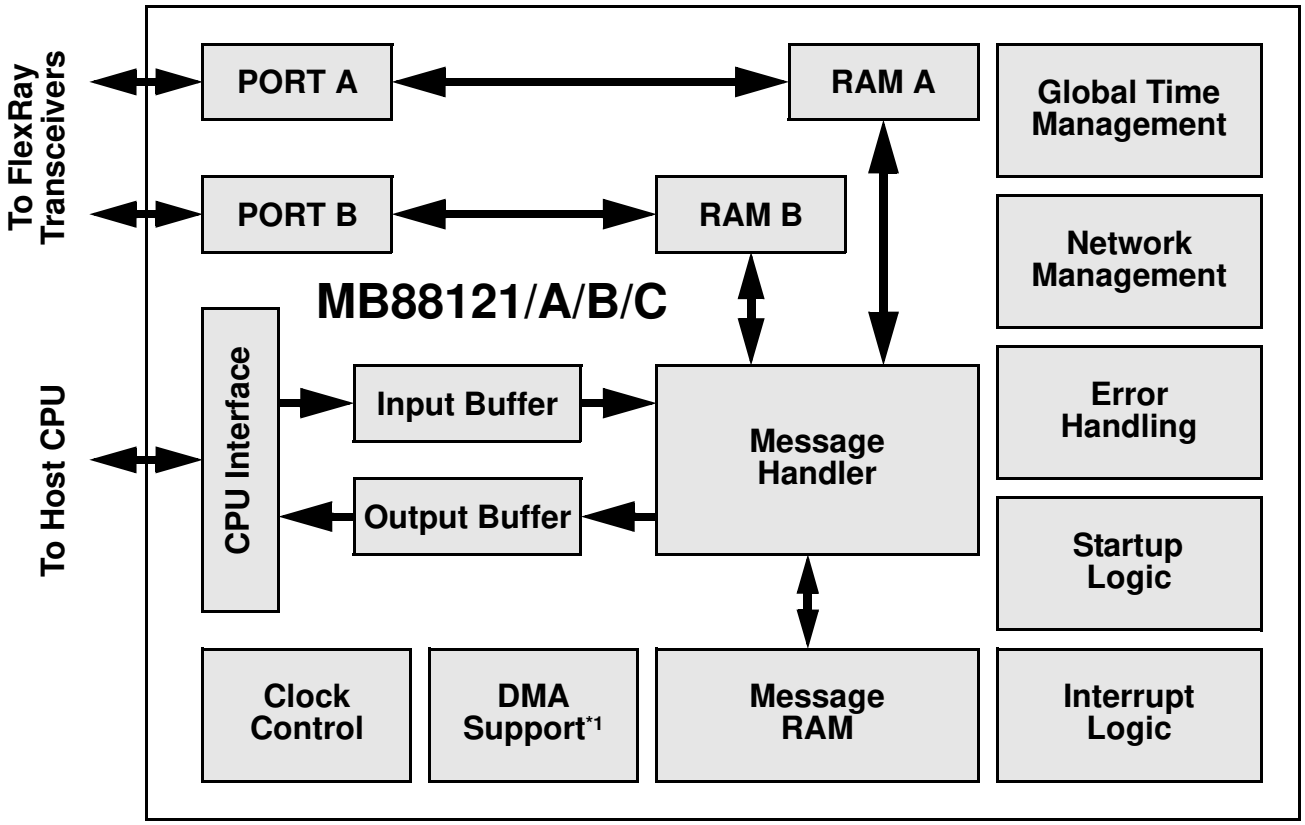
Second 16 bit write cycle via Bus Interface to address 0x402 - 0x403: Value 5678

32-bit data written to WRDS1 address.

Value of WRDS1 register: 0x1234 5678

■ BLOCK DIAGRAM

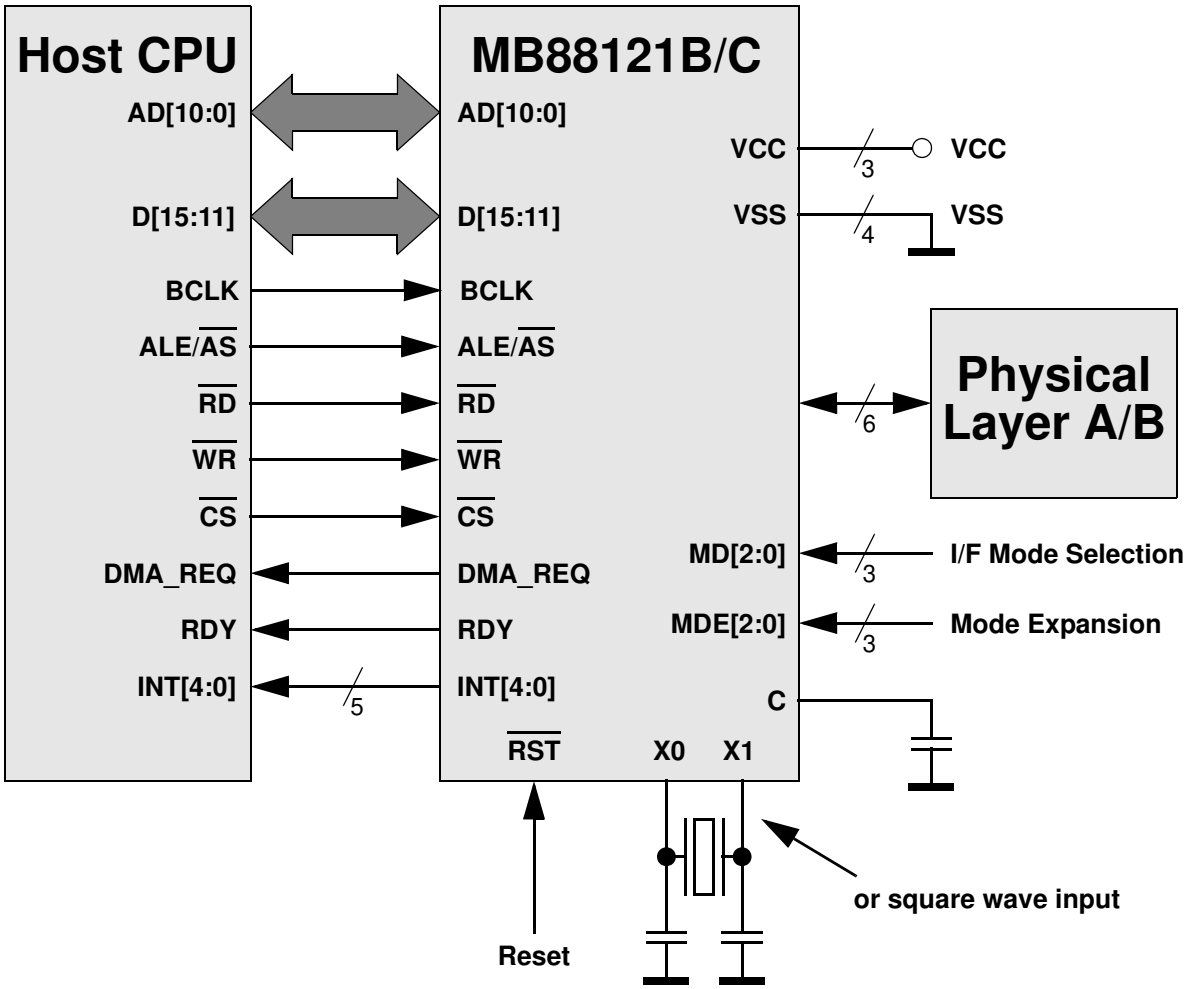
MB88121/MB88121A/MB88121B/MB88121C



*1: DMA support is only available on MB88121A/B/C

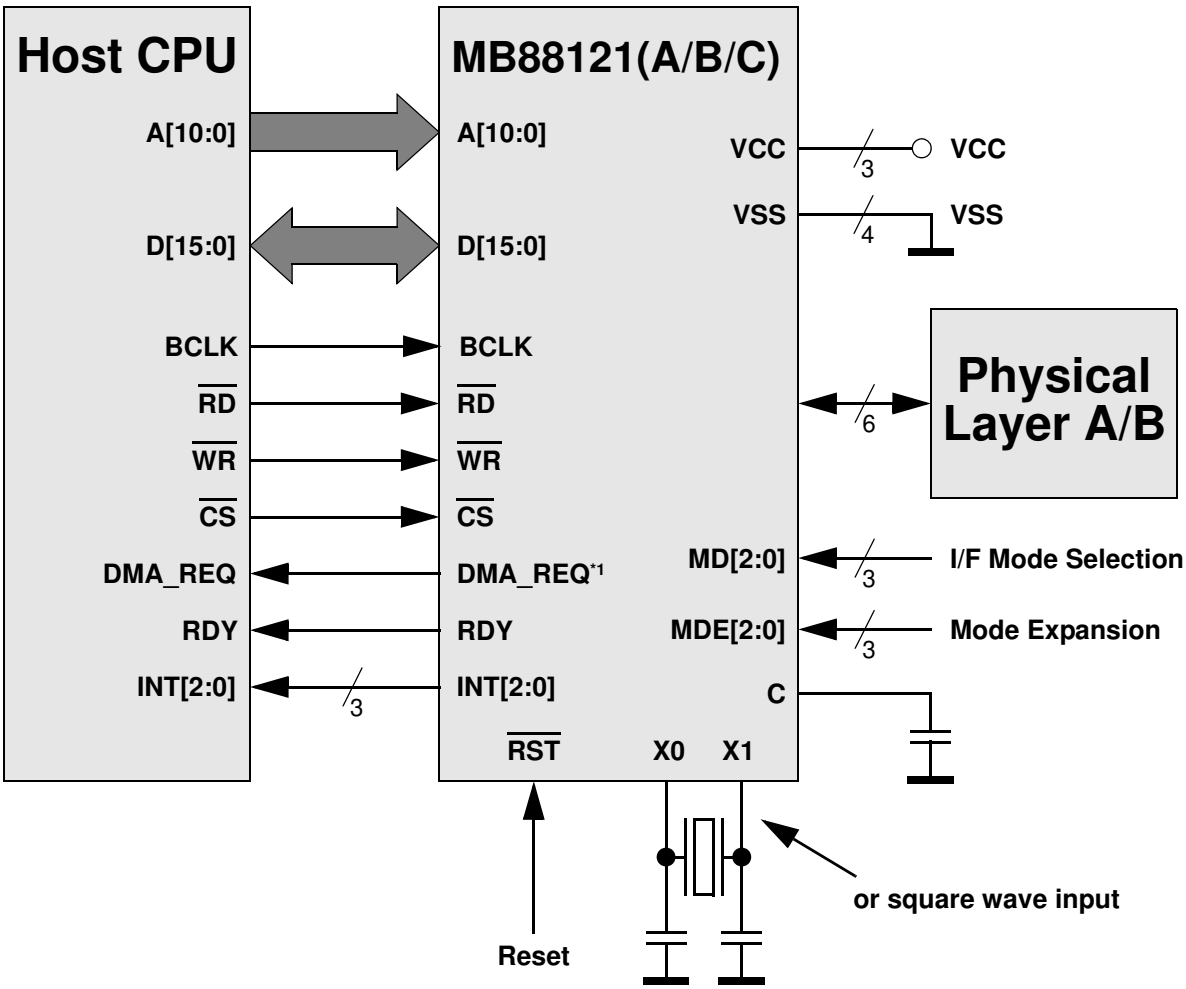
■ HOST INTERFACES

Connection to Host CPU in 16-bit multiplexed Mode (MB88121B/C only)



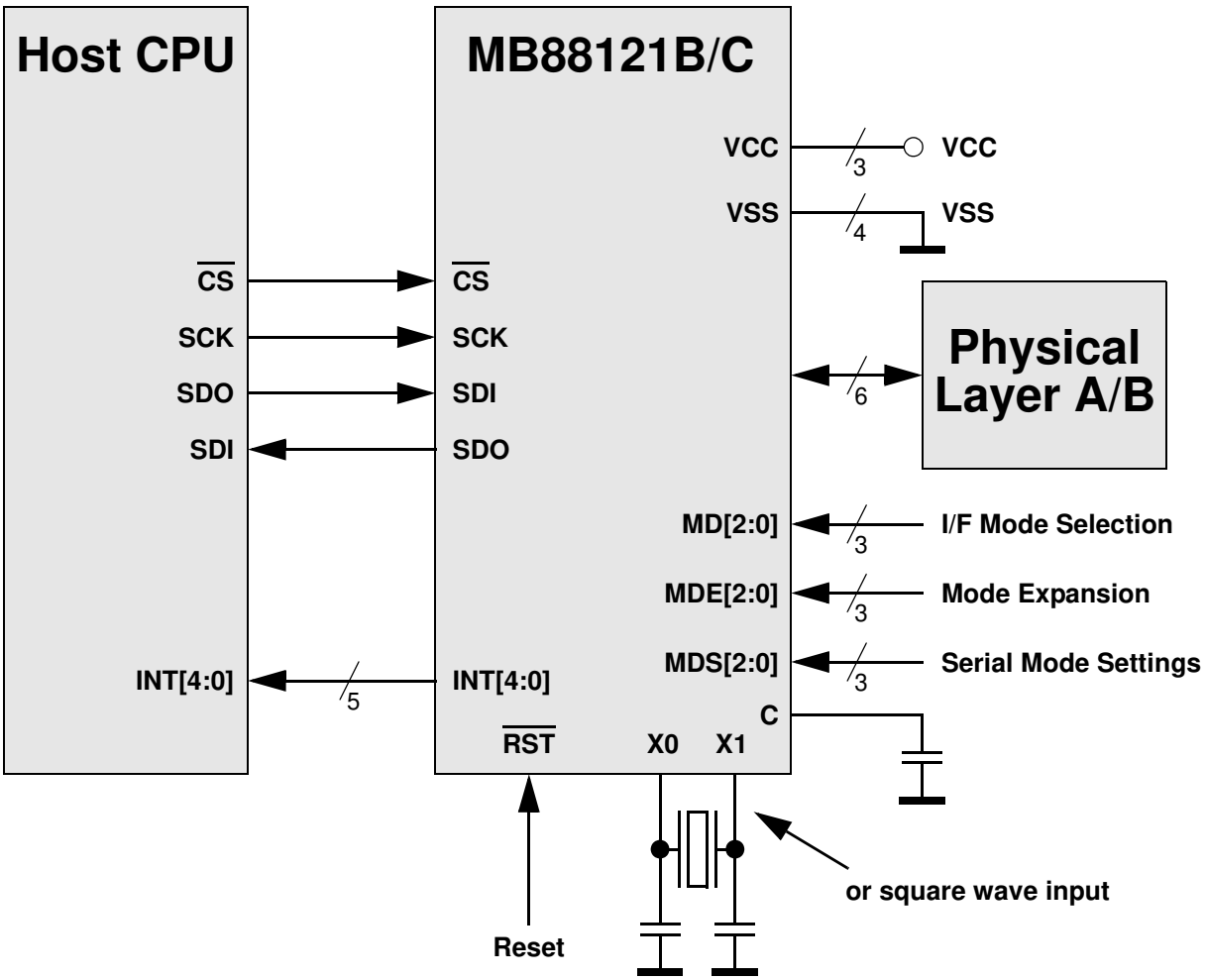
*1: DMA_REQ can only be used if RDY is not used, e.g. with automatic wait states.
The initial function of the RDY/DMA_REQ pin is RDY.

Connection to Host CPU in 16-bit non-multiplexed Mode



*1: MB88121A/B/C only

Connection to Host CPU in SPI Mode (MB88121B/C only)



■ I/O MAP

Address	Symbol	Name	Reset	Access
Customer Registers				
0x0000	VER	Version Information Register	MB88121: 0410 7905 MB88121A: 0420 7906 MB88121B: 0430 79FF MB88121C: 0440 79FF	r
0x0004	CCNT	Clock Control Register	0000 0000	r/w
0x0008	CUS2	*reserved* Customer 2 Register (DBGS & DMAS)	MB88121: 0000 0000 MB88121A/B/C:0000 0000	r r/w
0x000C	- INT	*reserved* Interrupt Register	MB88121(A): 0000 0000 MB88121B/C: 0000 0000	r r/w
Special Registers				
0x0010	-	*reserved (1) (don't write)*	MB88121: 0000 0000 MB88121A/B/C: 0000 0300	r
0x0014	-	*reserved (1) (don't write)*	0000 0000	r
0x0018	-	*reserved (1)*	0000 0000	r
0x001C	LCK	Lock Register	0000 0000	r/w
Interrupt Registers				
0x0020	EIR	Error Interrupt Register	0000 0000	r/w
0x0024	SIR	Status Interrupt Register	0000 0000	r/w
0x0028	EILS	Error Interrupt Line Select	0000 0000	r/w
0x002C	SILS	Status Interrupt Line Select	MB88121: 0303 7FFF MB88121A/B/C: 0303 FFFF	r/w
0x0030	EIES	Error Interrupt Enable Set	0000 0000	r/w
0x0034	EIER	Error Interrupt Enable Reset	0000 0000	r/w
0x0038	SIES	Status Interrupt Enable Set	0000 0000	r/w
0x003C	SIER	Status Interrupt Enable Reset	0000 0000	r/w
0x0040	ILE	Interrupt Line Enable	0000 0000	r/w
0x0044	T0C	Timer 0 Configuration	0000 0000	r/w
0x0048	T1C	Timer 1 Configuration	0002 0000	r/w
0x004C	STPW STPW1	Stop Watch Register Stop Watch Register 1	MB88121/A: 0000 0000 MB88121B/C: 0000 0000	r/w
0x0050	- STPW2	*reserved* Stop Watch Register 2	MB88121/A: 0000 0000 MB88121B/C: 0000 0000	r
0x0054 - 0x007C	-	*reserved (11)*	0000 0000	r

(Continued)

Address	Symbol	Name	Reset	Access
CC Control Registers				
0x0080	SUCC	SUC Configuration Register 1	MB88121: 0C40 0000 MB88121A/B/C: 0C40 1000	r/w
0x0084	SUCC2	SUC Configuration Register 2	MB88121: 0100 05A4 MB88121A/B/C: 0100 0504	r/w
0x0088	SUCC3	SUC Configuration Register 3	0000 0011	r/w
0x008C	NEMC	NEM Configuration Register	0000 0000	r/w
0x0090	PRTC1	PRT Configuration Register 1	MB88121: 084C 0005 MB88121A/B/C: 084C 0633	r/w
0x0094	PRTC2	PRT Configuration Register 2	MB88121: 0F2D 0E0E MB88121A/B/C:0F2D 0A0E	r/w
0x0098	MHDC	MHD Configuration Register	MB88121: 0001 0000 MB88121A/B/C: 0000 0000	r/w
0x009C	-	*reserved (1)*	0000 0000	r
0x00A0	GTUC1	GTU Configuration Register 1	MB88121: 0000 02D0 MB88121A/B/C: 0000 0280	r/w
0x00A4	GTUC2	GTU Configuration Register 2	MB88121: 0002 000C MB88121A/B/C: 0002 000A	r/w
0x00A8	GTUC3	GTU Configuration Register 3	MB88121: 0001 0000 MB88121A/B/C: 0202 0000	r/w
0x00AC	GTUC4	GTU Configuration Register 4	MB88121: 000A 0009 MB88121A/B/C: 0008 0007	r/w
0x00B0	GTUC5	GTU Configuration Register 5	MB88121: 0A01 0000 MB88121A/B/C: 0E00 0000	r/w
0x00B4	GTUC6	GTU Configuration Register 6	0002 0000	r/w
0x00B8	GTUC7	GTU Configuration Register 7	MB88121: 0002 0005 MB88121A/B/C: 0002 0004	r/w
0x00BC	GTUC8	GTU Configuration Register 8	0000 0002	r/w
0x00C0	GTUC9	GTU Configuration Register 9	MB88121: 0001 0101 MB88121A/B/C: 0000 0101	r/w
0x00C4	GTUC10	GTU Configuration Register 10	MB88121: 0002 0001 MB88121A/B/C: 0002 0005	r/w
0x00C8	GTUC11	GTU Configuration Register 11	0000 0000	r/w
0x00CC - 0x00FC	-	*reserved (13)*	0000 0000	r

Address	Symbol	Name	Reset	Access
CC Status Registers				
0x0100	CCSV	CC Status Vector	MB88121: 0000 4000 MB88121A/B/C: 0010 4000	r
0x0104	CCEV	CC Error Vector	0000 0000	r
0x0108 - 0x010C	-	*reserved (2)*	0000 0000	r
0x0110	SCV	Slot Counter Value	MB88121: 03FF 03FF MB88121A/B/C: 0000 0000	r
0x0114	MTCCV	Macrotick and Cycle Counter Value	0000 0000	r
0x0118	RCV	Rate Correction Value	0000 0000	r
0x011C	OCV	Offset Correction Value	0000 0000	r
0x0120	SFS	Sync Frame Status	0000 0000	r
0x0124	SWNIT	Symbol Window and NIT Status	0000 0000	r
0x0128	ACS	Aggregated Channel Status	0000 0000	r/w
0x012C	-	*reserved (1)*	0000 0000	r
0x0130 - 0x0168	ESIDn	Even Sync ID [1 ...15]	0000 0000	r
0x016C	-	*reserved (1)*	0000 0000	r
0x0170 - 0x01A8	OSIDn	Odd Sync ID [1 ...15]	0000 0000	r
0x01AC	-	*reserved (1)*	0000 0000	r
0x01B0 - 0x01B8	NMVn	Network Management Vector [1... 3]	0000 0000	r
0x01BC - 0x02FC	-	*reserved (81)*	0000 0000	r
Message Buffer Control Registers				
0x0300	MRC	Message RAM Configuration	MB88121: 0080 0000 MB88121A/B/C: 0180 0000	r/w
0x0304	FRF	FIFO Rejection Filter	0180 0000	r/w
0x0308	FRFM	FIFO Rejection Filter Mask	0000 0000	r/w
0x030C	- FCL	*reserved (1)* FIFO critical level	MB88121/A: 0000 0000 MB88121B/C: 0000 0080	r r/w

Address	Symbol	Name	Reset	Access
Message Buffer Status Registers				
0x0310	MHDS	Message Handler Status	0000 0000	r/w
0x0314	LDTS	*reserved* Last Dynamic Transmit Slot	MB88121: 0000 0000 MB88121A/B/C: 0000 0000	r r
0x0318	- FSR	*reserved* FIFO Status Register	MB88121/A: 0000 0000 MB88121B/C: 0000 0000	r
0x031C	- MHDF	*reserveds* Message Handler Constraints Flags	MB88121/A: 0000 0000 MB88121B/C: 0000 0000	r r/w
0x0320	TXRQ1	Transmission Request 1	0000 0000	r
0x0324	TXRQ2	Transmission Request 2	0000 0000	r
0x0328	TXRQ3	Transmission Request 3	0000 0000	r
0x032C	TXRQ4	Transmission Request 4	0000 0000	r
0x0330	NDAT1	New Data 1	0000 0000	r
0x0334	NDAT2	New Data 2	0000 0000	r
0x0338	NDAT3	New Data 3	0000 0000	r
0x033C	NDAT4	New Data 4	0000 0000	r
0x0340	MBSC1	Message Buffer Status Changed 1	0000 0000	r
0x0344	MBSC2	Message Buffer Status Changed 2	0000 0000	r
0x0348	MBSC3	Message Buffer Status Changed 3	0000 0000	r
0x034C	MBSC4	Message Buffer Status Changed 4	0000 0000	r
0x0350 - 0x03EC	-	*reserved (40)*	0000 0000	r
Identification Registers				
0x03F0	- CREL	*reserved* Core Release Endian Register	MB88121/A: 0000 0000 MB88121B: 0726 0412 MB88121C: 1027 1031	r
0x03F4	- ENDN	*reserved* Endian Register	MB88121/A: 0000 0000 MB88121B/C: 8765 4321	r
0x03F8 - 0x03FC	-	*reserved*	0000 0000	r

(Continued)

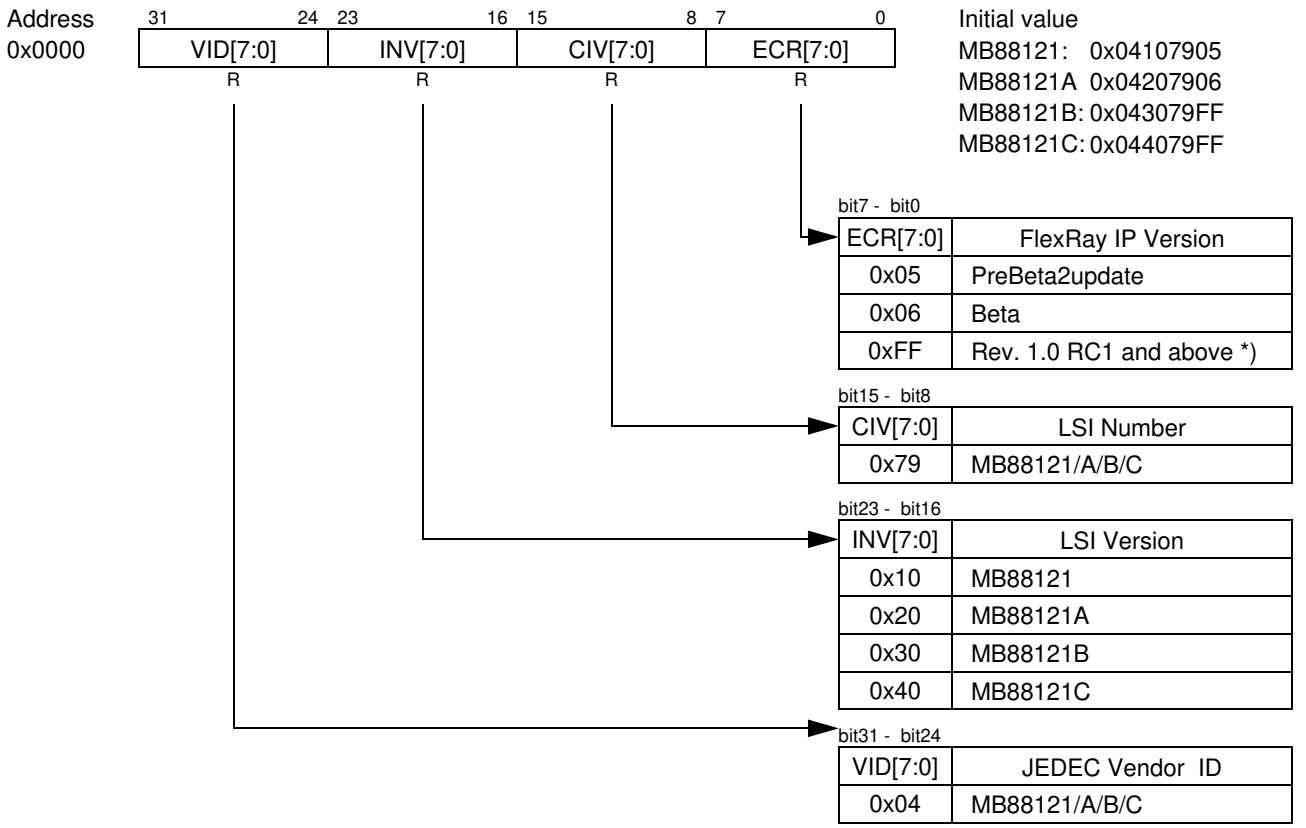
(Continued)

Address	Symbol	Name	Reset	Access
Input Buffer				
0x0400 - 0x04FC	WRDSn	Write Data Section [1...64]	0000 0000	r/w
0x0500	WRHS1	Write Header Section 1	0000 0000	r/w
0x0504	WRHS2	Write Header Section 2	0000 0000	r/w
0x0508	WRHS3	Write Header Section 3	0000 0000	r/w
0x050C	-	*reserved (1)*	0000 0000	r/w
0x0510	IBCM	Input Buffer Command Mask	0000 0000	r/w
0x0514	IBCR	Input Buffer Command Request	0000 0000	r/w
0x0518 - 0x05FC	-	*reserved (58)*	0000 0000	r
Output Buffer				
0x0600 - 0x06FC	RDDSn	Read Data Section [1 ...64]	0000 0000	r
0x0700	RDHS1	Read Header Section 1	0000 0000	r
0x0704	RDHS2	Read Header Section 2	0000 0000	r
0x0708	RDHS3	Read Header Section 3	0000 0000	r
0x070C	MBS	Message Buffer Status	0000 0000	r
0x0710	OBCM	Output Buffer Command Mask	0000 0000	r/w
0x0714	OBCR	Output Buffer Command Request	0000 0000	r/w
0x0718 - 0x07FC	-	*reserved (58)*	0000 0000	r

- Explanation on read/write
  r/w: Readable and Writable
  r: Read only
  w: Write only

Note : Any write access to reserved addresses in I/O map may result in unexpected behaviour. A read access to reserved address results in reading “X”.

■ VERSION INFORMATION REGISTER (VER)



Bit	Name	Function
bit31 - bit24	VID: JEDEC Vendor ID Code	The JEDEC Vendor ID Code is shown. The value of MB88121, MB88121A , MB88121B and MB88121C is 0x04. Writing is invalid.
bit23 - bit16	INV: LSI Version	The LSI Version information is shown. The value of MB88121 is 0x10, the value of MB88121A is 0x20 and the value of MB88121B is 0x30 and the value of MB88121C is 0x40. Writing is invalid.
bit15 - bit8	CIV: LSI Number	The LSI Number information is shown. The value of MB88121, MB88121A , MB88121B and MB88121C is 0x79. Writing is invalid.
bit7 - bit0	ECR: FlexRay IP Version	The FlexRay IP Version information is shown. The value of MB88121 is 0x05, the value of MB88121A is 0x06. All other the value is 0xFF, the CREL register contains the IP version. Writing is invalid.

■ CLOCK CONTROL REGISTER (CCNT)

The CLOCK CONTROL Register (except SRST[1:0]) is writeable in DEFAULT_CONFIG (CCSV[5:0] = 00 0000) or CONFIG state (CCSV[5:0] = 00 1111), only. SRST[1:0] is always writeable.

Address 0x0004

31 14	13 12	11	10 9	8 7	6	5	4	3 2	1	0
RSV	SRST[1:0]	PMUL[2]	RSV	SDIV[1:0]	RSV	STOP	RCLK	PMUL[1:0]	SSEL	PON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value 0x00000000

bit0

PON	PLL Oscillator Enable
0	Stop PLL oscillator
1	Enable PLL oscillator

bit1

SSEL	System Clock Selection
0	Select the oscillation clock (X0/X1)
1	Select the PLL clock

bit11,bit3 - bit2

PMUL[2:0]			PLL Multiplier Selection
0	0	0	X0/X1 (4MHz) x 20 (80MHz)
0	0	1	X0/X1 (5MHz) x 16 (80MHz)
0	1	0	X0/X1 (8MHz) x 10 (80MHz)
0	1	1	X0/X1 (10MHz) x 8 (80MHz)
1	0	0	X0/X1 (16MHz) x 5 (80MHz)
1	0	1	X0/X1 (20MHz) x 4 (80MHz)

bit4

RCLK	RAM Clock Selection (MB88121A/B only)
0	Select System Clock
1	Select System Clock divided by 2

bit5

STOP	Clock Stop
0	Supply the system clock for FlexRay Controller
1	Stop the system clock for FlexRay Controller

bit8 - bit7

SDIV[1:0]		Division for system clock (MB88121A/B only)
0	0	System clock is divided by 1
0	1	System clock is divided by 2
1	0	System clock is divided by 4
1	1	System clock is divided by 8

bit13 - bit12

SRST[1:0]	Software Reset
See after sheet	

bit31 - bit14, bit10 - bit9, bit6

RSV	Reserved
These bits are reserved. Always write “0”. “0” is read.	

R: Read only
R/W: Read/Write

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>bit31 - bit14</td><td>RSV: Reserved</td><td>These bits are reserved. “0” is read. Write “0”.</td></tr>
<tr><td>bit13 - bit12</td><td>SRST[1:0]</td><td>These bits initialize Communication Controller. When "00", "01", "10", "11" are written to these bits continuously, Communication Controller is initialized.
First : write "00" to SRST[1:0]
Second: Write "01" to SRST[1:0]
Third : Write "10" to SRST[1:0]
Forth : Write "11" to SRST[1:0] <- Initialize
If the condition isn't full, Communication Controller isn't initialized.
These bits are invalid for MB88121, MB88121A and MB88121B.</td></tr>
<tr><td>bit10 - bit 9</td><td>RSV Reserved</td><td>This bit is reserved. Always write “0”.</td></tr>
<tr><td>bit8 - bit7</td><td>SDIV[1:0]:
Division for system clock</td><td>These bits control the division for system clock. This function is supported in MB88121A, MB88121B and MB88121C. These bits are reserved in MB88121. In MB88121, “0” is read and write “0”.

<table><tr><th>SDIV[1]</th><th>SDIV[0]</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>System clock is divided by 1</td></tr><tr><td>0</td><td>1</td><td>System clock is divided by 2</td></tr><tr><td>1</td><td>0</td><td>System clock is divided by 4</td></tr><tr><td>1</td><td>1</td><td>System clock is divided by 8</td></tr></table>
<<Note>>
When FlexRay controller can receive or transmit data, these bits must not be changed.</td></tr>
<tr><td>bit6</td><td>RSV: Reserved</td><td>This bit is reserved. Always write “0”.</td></tr>
</table>

Bit	Name	Function
bit5	STOP: Clock Stop	This bit stops the system clock. If this bit set to “1”, the system clock is stopped. But the oscillator is active. When this bit is set to “1”, please carry out the following procedures. - PLL On 1) Stop receiving and transmitting for FlexRay controller. 2) Set “0” to SSEL bit. 3) Set “0” to PON bit. 4) Set “1” to STOP bit. - PLL Off 1) Stop receiving and transmitting for FlexRay controller. 2) Set “1” to STOP bit. When this bit is changed into “0” from “1”, please carry out in the following procedures. - PLL On 1) Set “1” to PON bit. 2) Set “0” to STOP bit. 3) Set “1” to SSEL bit after PLL lock up time (600us). 4) Enable to receive and transmit data for FlexRay controller. - PLL Off 1) Set “0” to STOP bit. <<Note>> When FlexRay controller can receive or transmit data, these bits must not be changed.
bit4	RCLK: RAM Clock Selection	This bit selects the RAM clock in MB88121A, MB88121B. If this bit is “0”, the system clock is selected as the RAM clock. If this bit is “1”, the system clock divided by 2 is selected as the RAM clock. In MB88121, this bit is reserved. Write “0”. “0” is read. <<Note>> When FlexRay controller can receive or transmit data, these bits must not be changed.

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>bit 11
bit3 – bit2</td><td>PMUL[2:0]:
PLL Multiplier Selection</td><td>These bits control the PLL multiplier. These bits must set up so that the PLL clock is set to 80MHz.

In MB88121 and MB88121A, the functionality of the PLL is not guaranteed.

For MB88121B/C, the evaluation of the PLL performance is pending. For this reason, do not use other settings than PMUL[1:0] = “11”.

<table>
<tr><th>PMUL[2]</th><th>PMUL[1]</th><th>PMUL[0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X0/X1 (4MHz) x 20 (80MHz)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>X0/X1 (5MHz) x 16 (80MHz)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>X0/X1 (8MHz) x 10 (80MHz)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>X0/X1 (10MHz) x 8 (80MHz)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>X0/X1 (16MHz) x 5 (80MHz)*1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>X0/X1 (20MHz) x 4 (80MHz)*1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>reserved</td></tr>
</table>
*1: MB88121C only

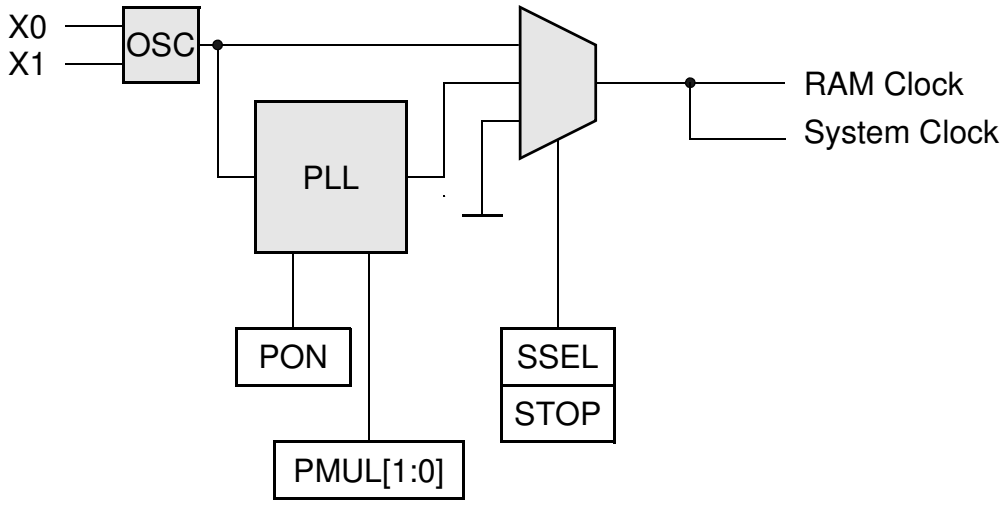
<<Note>>
These bits must be changed before PON bit is set to “1”.
When 16 bit parallel bus and external clock are used(MD2="1", MD1="0", MD0=“1"), the clock for X0/X1 pins can be used from 4MHz to 20MHz.
When 16 bit parallel bus and oscillator are used(MD2="1", MD1="0", MD0="0”), the clock for X0/X1 pins can be used from 4MHz to 8MHz.
When serial bus is used(MD="1", MD1="1", MD0="0") on external clock, the clock for X0/X1 pins can't be used at 16MHz and 20MHz, and on oscillator, the clock for X0/X1 pins can be used from 4MHz to 8MHz. And PMUL[2:0] bits shouldn’t be set to ”100” and “101”.
Setting to be resered is prohibition.</td></tr>
<tr><td>bit1</td><td>SSEL:
System Clock Selection</td><td>This bit selects the system clock.
"0": Select the clock of X0/X1
"1": Select the clock of PLL

In MB88121 and MB88121A, the functionality of the PLL is not guaranteed.

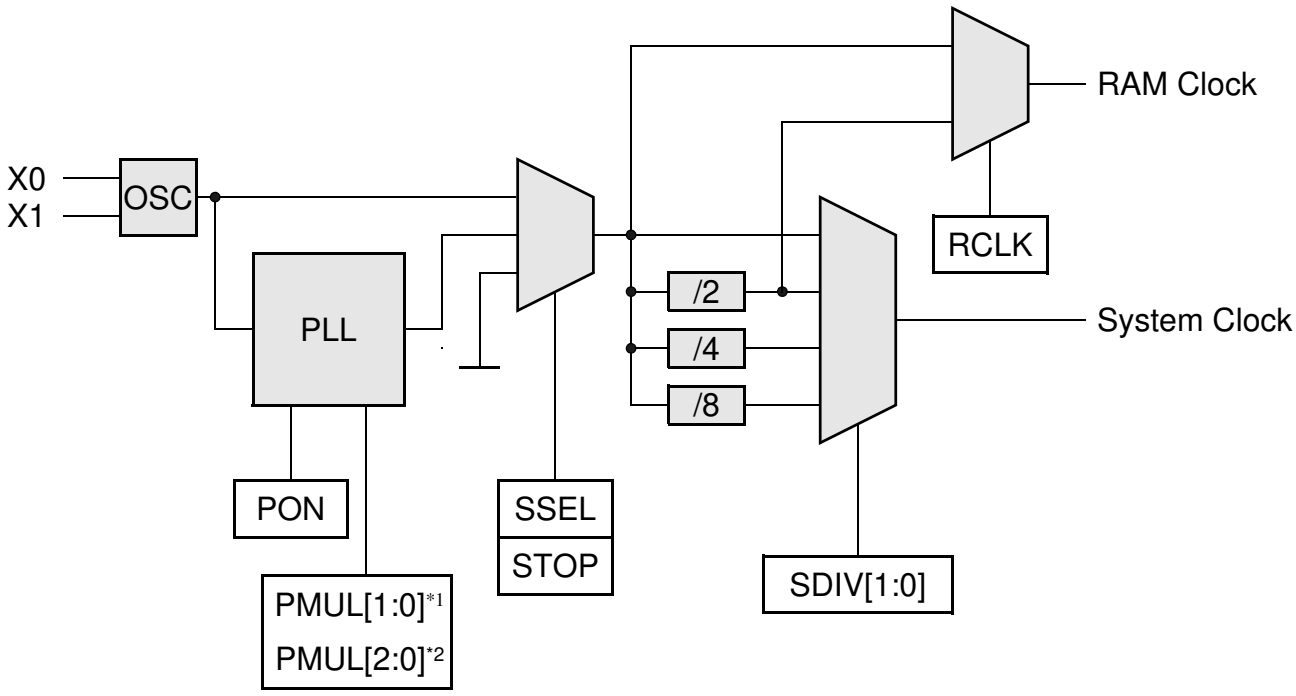
<<Note>>
• Must be changed into "1" from "0" after "1" is set as a PON bit and PLL lock-up time (600us) passes.
• If the oscillater of PLL is stopped, PON bit is set to "0" after this bit is changed to "0".
• When FlexRay controller can receive or transmit data, these bits must not be changed.</td></tr>
</table>

Bit	Name	Function
bit0	PON: PLL Oscillator Enable	This bit controls PLL oscillator. "0": Stop PLL oscillator "1": PLL oscillator enable In MB88121 and MB88121A, the functionality of the PLL is not guaranteed. <<Note>> This bit must be changed when SSEL bit is "0".

Clock supply circuit of MB88121

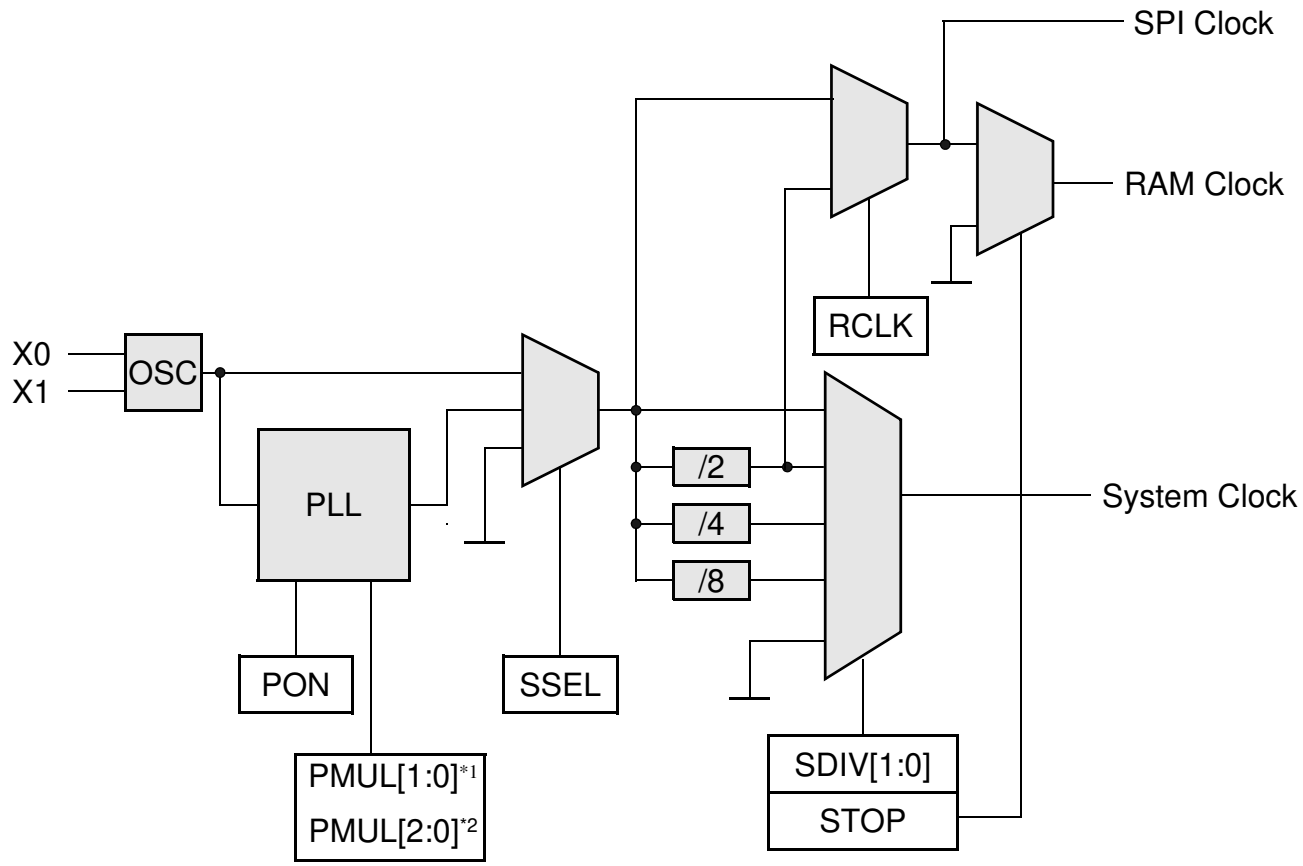


Clock supply circuit of MB88121A/B/C (MD[2:0] = 1 0 0)



*1 **MB88121A/B**
*2 **MB88121C**

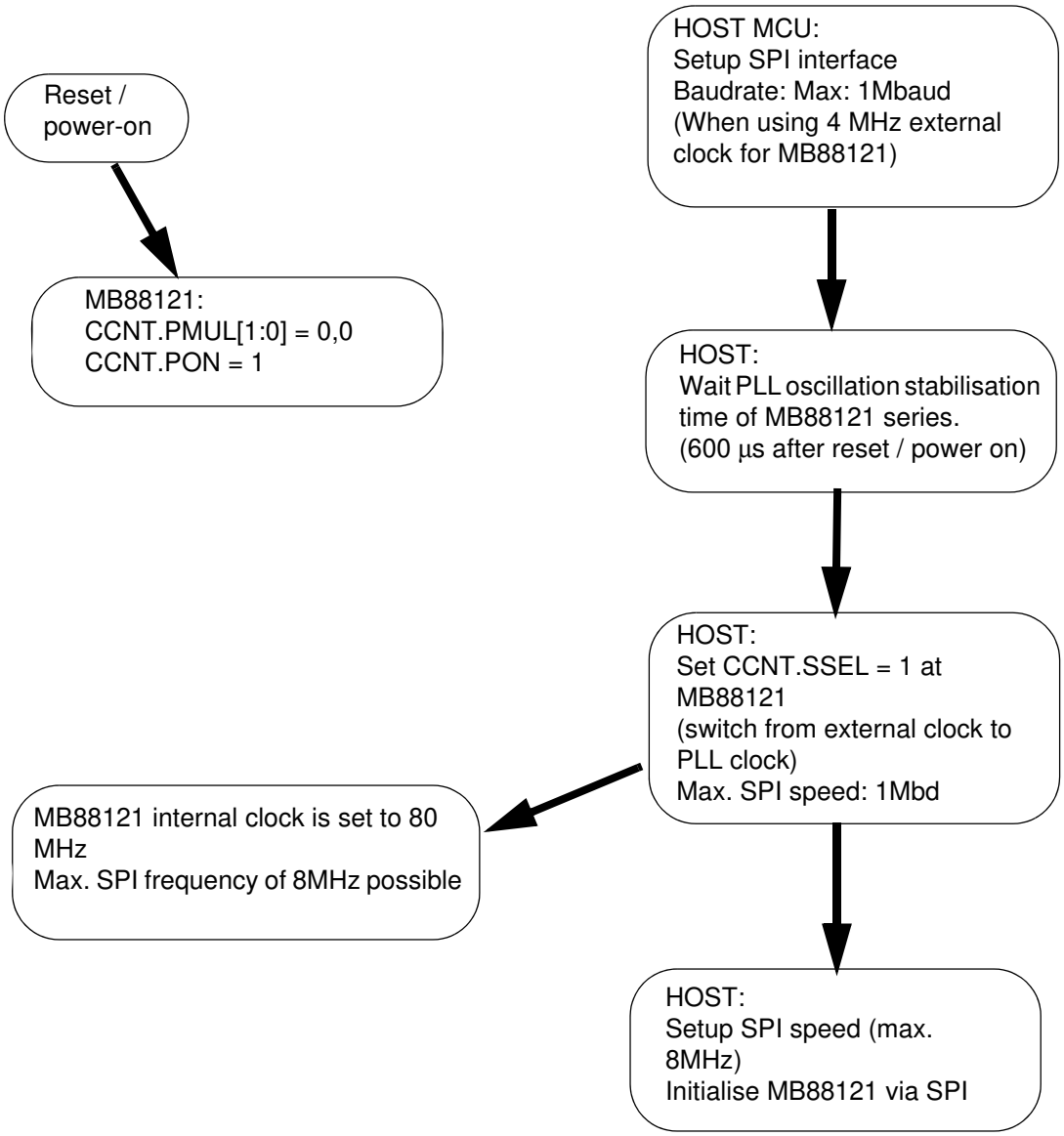
Clock supply circuit of MB88121B/C for SPI mode (MD[2:0] = 1 1 0)



*1 **MB88121B**
*2 **MB88121C**

Clock Settings after power-on / reset in SPI mode

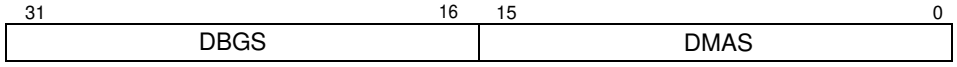
Use of 4 MHz external crystal



■ Customer 2 Register

The Customer2 Register (CUS2) is a 32-bit register, at address 0x0008.
The upper 16 bit (B16..31) are called Debug support Register (DBGS).
The lower 16 bit (Bit 0..15) are called DMA support register (DMAS)
Always access the customer 2 register 32-bit wise

Address
0x0008



13. Debug support Register (DBGS)

The Debug support register is available only in MB88121B/C. It is reserved in MB88121(A).
Bits 31 - 27 are available in MB88121B/C, only. For MB88121(A) they are reserved

Address
0x0008

31	30	29	28	27	26 ... 16
MBSUE	CYCSE	MTE	SDSE	CYCS0E	RSV
R/W	R/W	R/W	R/W	R/W	R/W

bit26 - bit16

RSV	Reserved
Write “0”. “0” is read.	

bit27

CYCS0E	Cycle Start 0 Enable
0	Output “L“
1	Output start of cycle 0

bit28

SDSE	Start of Dynamic Segment Enable
0	Output “L“
1	Output start of dynamic segment

bit29

MTE	Macrotick start enable
0	Output “L“
1	Output start of Macrotick

bit30

CYCSE	Cycle start enable
0	Output “L“
1	Output start of cycle

bit31

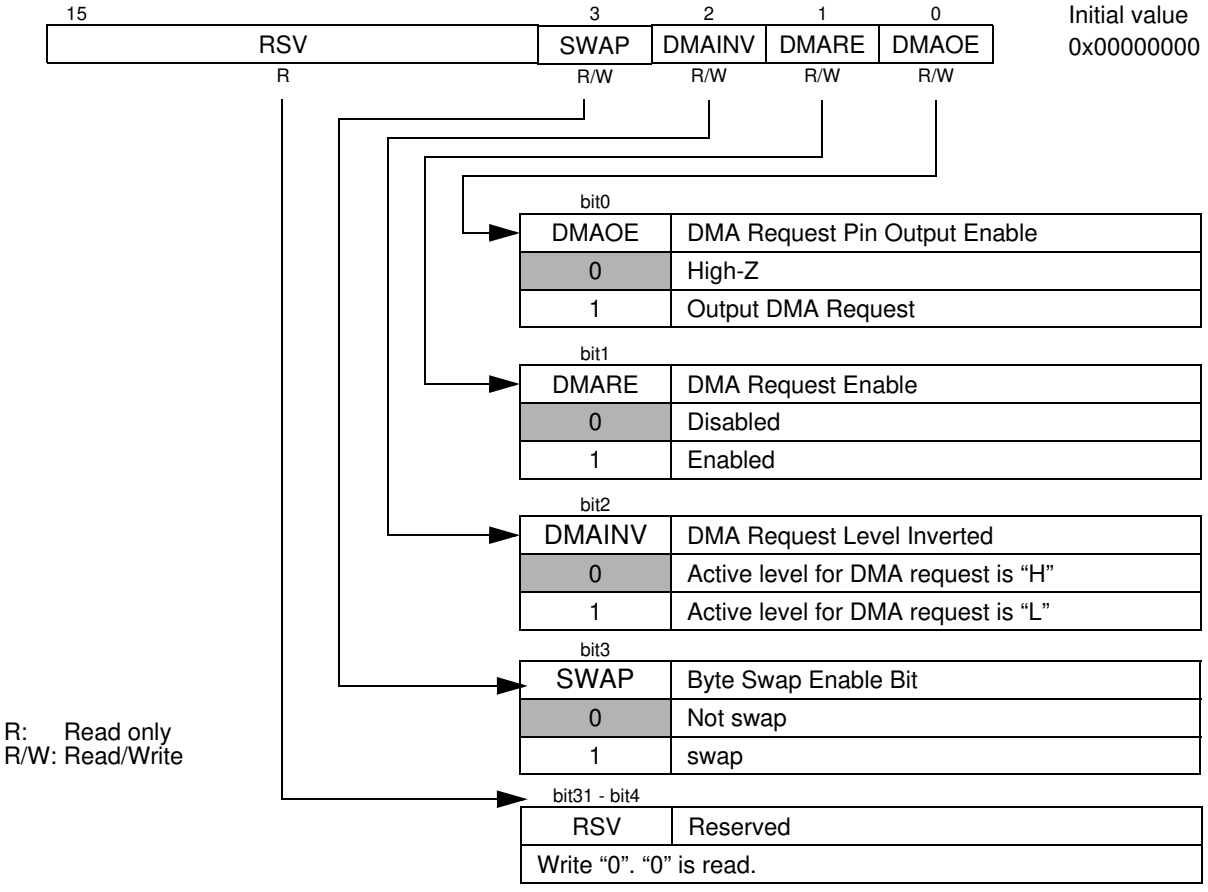
MBUSE	Message buffer status enable
0	Output “L“
1	Output Message buffer status updated

R: Read only
R/W: Read/Write

Bit	Name	Function
bit31	MBSUE: Message buffer Status update enable	This bit controls the Message buffer status update ports: MBSU_RX1; MBSU_TX1, MBSU_TX2, MBSU_RX2 "0": Disabled "1": Enabled <<Note>> If enabled output “High” at every Message buffer status update. High duration: One RAM clock cycle. If “0“ is set outputs “L” at pin.
bit30	CYCSE: Cycle start output enable	This bit controls the Cycle start output "0": Disabled "1": Enabled <<Note>> If enabled output “High” at every cycle start. High duration: One RAM clock cycle If “0“ is set outputs “L” at pin.
bit29	MTE: Start of Macrotick output enable	This bit controls the Macrotick start output "0": Disabled "1": Enabled <<Note>> If enabled output “High” at every Macrotick start. High duration: One RAM clock cycle If “0“ is set outputs “L” at pin.
bit28	SDSE: Start of dynamic segment output enable	This bit controls the start of dynamic segment output "0": Disabled "1": Enabled <<Note>> If enabled Output “High” at every start of dynamic segment. High duration: One RAM clock cycle If “0“ is set outputs “L” at pin.
bit27	CYCS0E: Start of cycle 0 output enable	This bit controls the Cycle 0 start output "0": Disabled "1": Enabled <<Note>> If enabled output “High” at every cycle 0 start. High duration: One RAM clock cycle If “0“ is set outputs “L” at pin.
bit26 - bit16	RSV: Reserved	These bits are reserved. "0" is read. Write "0".

14. DMA SUPPORT REGISTER (DMAS)

The DMA support register is available only in MB88121A/B/C. It is reserved in MB88121.



bit0

DMAOE	DMA Request Pin Output Enable
0	High-Z
1	Output DMA Request

bit1

DMARE	DMA Request Enable
0	Disabled
1	Enabled

bit2

DMAINV	DMA Request Level Inverted
0	Active level for DMA request is “H”
1	Active level for DMA request is “L”

bit3

SWAP	Byte Swap Enable Bit
0	Not swap
1	swap

bit31 - bit4

RSV	Reserved
Write “0”. “0” is read.	

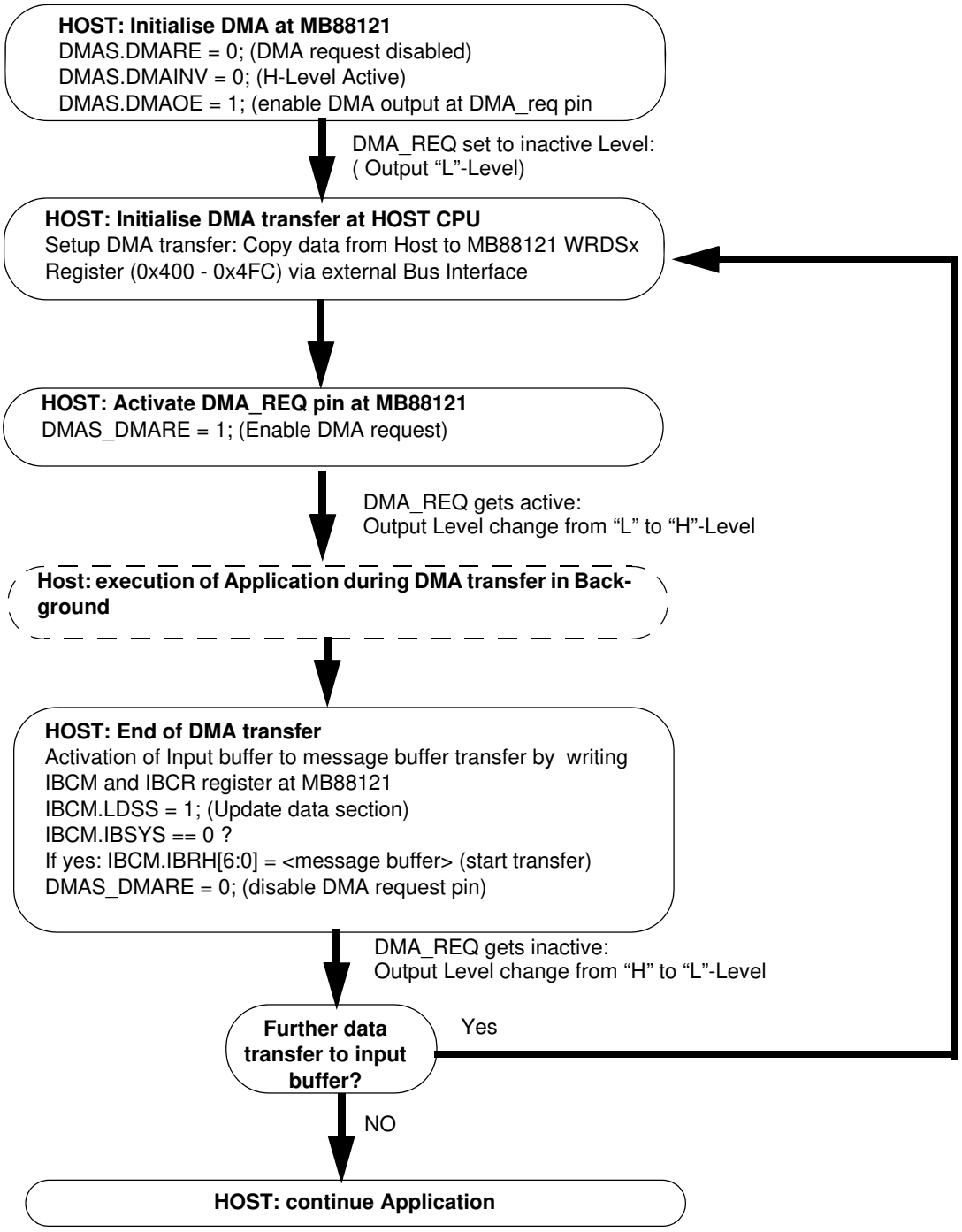
Bit	Name	Function
bit15 - bit4	RSV: Reserved	These bits are reserved. "0" is read. Write "0".
bit3	SWAP: Byte Swap Enable Bit	This bit selects whether to exchange the data handled with input/output buffer by each byte.In the case of MB88121A and MB88121B, this bit is dealt with for "0". When this bit set to "0": In this case, writing and reading are done as it is. When this bit set to "1": <460, 360 mode> When writing it in the input buffer, the data of bit 7-0 is written in bit31-24 in the input buffer. The data of bit 15-8 is written in bit23-16 in the input buffer. The data of bit 23-16 is written in bit15-8 in the input buffer. The data of bit 31-24 is written in bit7-0 in the input buffer. When it is read from the input/output buffer, the data of bit 7-0 of the input/output buffer is read as bit 31-24. The data of bit 15-8 of the input/output buffer is read as bit 23-16. The data of bit 23-16 of the input/output buffer is read as bit 15-8. The data of bit 31-24 of the input/output buffer is read as bit 7-0 <16FX mode> When writing it in the input buffer, the data of bit 7-0 is written in bit15-8 in the input buffer. The data of bit 15-8 is written in bit7-0 in the input buffer. The data of bit 23-16 is written in bit31-24 in the input buffer. The data of bit 31-24 is written in bit23-16 in the input buffer. When it is read from the input/output buffer, the data of bit 7-0 of the input/output buffer is read as bit 15-8. The data of bit 15-8 of the input/output buffer is read as bit 7-0. The data of bit 23-16 of the input/output buffer is read as bit 31-24. The data of bit 31-24 of the input/output buffer is read as bit 23-16 <<Note>> This bit is invalid serial bus mode. This bit is valid for the 16-bit parallel (non-multiplex and multiplex).
bit2	DMAINV: DMA Request Level Inverted	This bit controls the DMA request level. "0": Active level for DMA request is "H" "1": Active level for DMA request is "L" <<Note>> It is valid when DMAOE bit is "1".
bit1	DMARE: DMA Request enable	This bit controls the DMA request. "0": Disabled "1": Enabled <<Note>> It is valid when DMAOE bit is "1".

Bit	Name	Function
bit0	DMAOE: DMA Request Pin Output Enable	This bit controls output enable for DMA request pin. "0": High-Z at DMA_REQ pin "1": Output DMA request at DMA_REQ pin

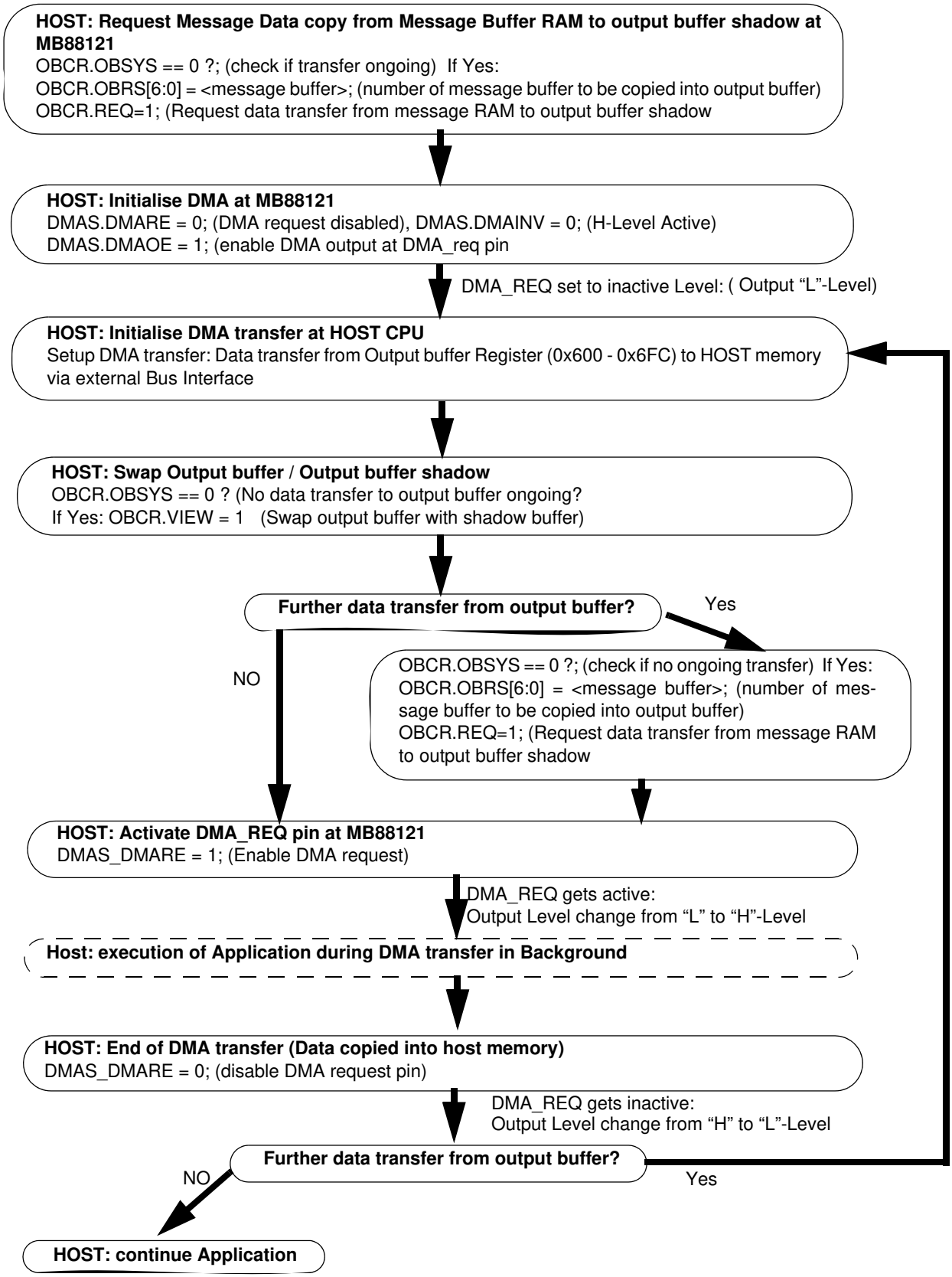
Application flow

The MB88121 support DMA transfer option for Input buffer and Output buffer data tranfer. In case the Host MCU is able to use DMA transfer via the external bus interface the DMA_req pin of MB88121 have to be connected to the DMA request input pin of host MCU.

DMA usage for Input buffer data transfer

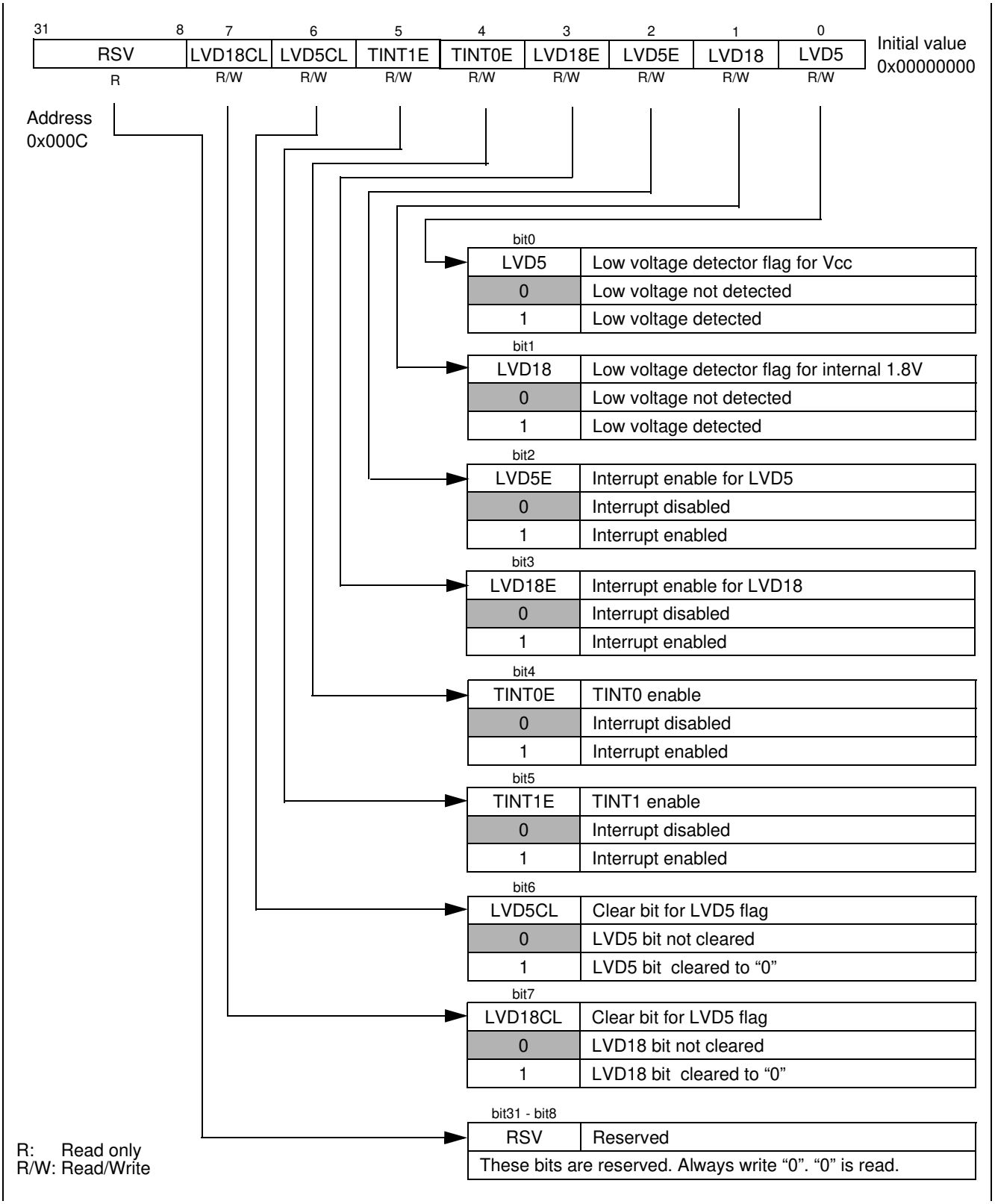


DMA usage for Ouput buffer data transfer


HOST: Request Message Data copy from Message Buffer RAM to output buffer shadow at MB88121
OBCR.OBSYS == 0 ?; (check if transfer ongoing) If Yes:
OBCR.OBRS[6:0] = <message buffer>; (number of message buffer to be copied into output buffer)
OBCR.REQ=1; (Request data transfer from message RAM to output buffer shadow
HOST: Initialise DMA at MB88121
DMAS.DMARE = 0; (DMA request disabled), DMAS.DMAINV = 0; (H-Level Active)
DMAS.DMAOE = 1; (enable DMA output at DMA_req pin
DMA_REQ set to inactive Level: (Output "L"-Level)
HOST: Initialise DMA transfer at HOST CPU
Setup DMA transfer: Data transfer from Output buffer Register (0x600 - 0x6FC) to HOST memory via external Bus Interface
HOST: Swap Output buffer / Output buffer shadow
OBCR.OBSYS == 0 ? (No data transfer to output buffer ongoing?
If Yes: OBCR.VIEW = 1 (Swap output buffer with shadow buffer)
Further data transfer from output buffer?
Yes
NO
OBCR.OBSYS == 0 ?; (check if no ongoing transfer) If Yes:
OBCR.OBRS[6:0] = <message buffer>; (number of message buffer to be copied into output buffer)
OBCR.REQ=1; (Request data transfer from message RAM to output buffer shadow
HOST: Activate DMA_REQ pin at MB88121
DMAS_DMARE = 1; (Enable DMA request)
DMA_REQ gets active:
Output Level change from "L" to "H"-Level
Host: execution of Application during DMA transfer in Background
HOST: End of DMA transfer (Data copied into host memory)
DMAS_DMARE = 0; (disable DMA request pin)
DMA_REQ gets inactive:
Output Level change from "H" to "L"-Level
Further data transfer from output buffer?
NO
Yes
HOST: continue Application

■ Interrupt Register (INT)

The Interrupt Register (INT) is available in MB88121B/C. For MB88121(A) this Register is reserved.



Bit	Name	Function
Bit 31-8	*reserved*	These bits are reserved. "0" is read. Write "0".
Bit 7	LVD18CL: LVD18 clear bit	This bit clears the LVD18 bit by writing “1” “0”: LVD18 Flag not changed “1”: LVD18 Flag cleared to “0” <<Note>>: This Bit is always read as “0”
Bit 6	LVD5CL: LVD5 clear bit	This bit clears the LVD5 bit by writing “1” “0”: LVD5 Flag not changed “1”: LVD5 Flag cleared to “0” <<Note>>: This Bit is always read as “0”
Bit 5	TINTE1: TINT1 enable bit	This bit enables the Timer interrupt 1 (TINT1) signal output via the corresponding INT pin. “0”: Interrupt disabled “1”: Interrupt enabled
Bit 4	TINTE0: TINT0 enable bit	This bit enables the Timer interrupt 0 (TINT0) signal output via the corresponding INT pin. “0”: Interrupt disabled “1”: Interrupt enabled
Bit 3	LVD18E: Interrupt enable bit for LVD18	This bit enables the LVD18 flag signal output via the corresponding INT pin: “0”: Interrupt disabled “1”: Interrupt enabled
Bit 2	LVD5E: Interrupt enable bit for LVD5	This bit enables the LVD5 flag signal output via the corresponding INT pin: “0”: Interrupt disabled “1”: Interrupt enabled
Bit 1	LVD18: Low voltage detector Flag for 1.8V	This bit indicates a lov voltage detection of internal 1.8V: “0”: No undervoltage occured “1”: undervoltage occured <<Note>> This Flag is cleared by writing “1” to Bit 7 LVD18CL
Bit 0	LVD5: Low voltage detector Flag for 5V	This bit indicates a lov voltage detection of Vcc input voltage: “0”: No undervoltage occured “1”: undervoltage occured <<Note>> This Flag is cleared by writing “1” to Bit 6 LVD5CL

Note: In 16/bit none-multiplexed mode the LVD5, LVD18, TINT0 and TINT1 are assigned to INT2 pin. In 16 bit multiplexed or SPI mode the assignment is: TINT0 to INT2; TINT1 to INT3, LVD5 and LVD18 to INT4 pin. See also chapter “Handling Devices” topic 10 Interrupt pin assignment

■ OTHER REGISTERS

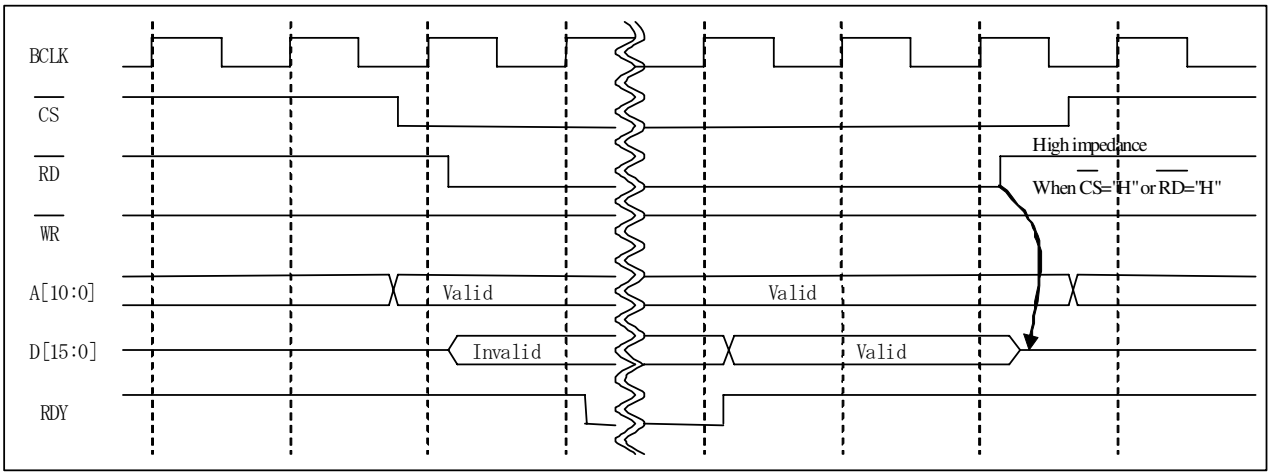
Please refer to the E-Ray User's manual for a description of the other registers.

■ OPERATION IN 16-BIT NON-MULTIPLEXED PARALLEL BUS MODE

The 16bit non-multiplexed parallel bus is divided by an address bus and 16 bits data bus. As the register of the FlexRay Controller is 32bit, it must be accessed at 16bit twice continuously.

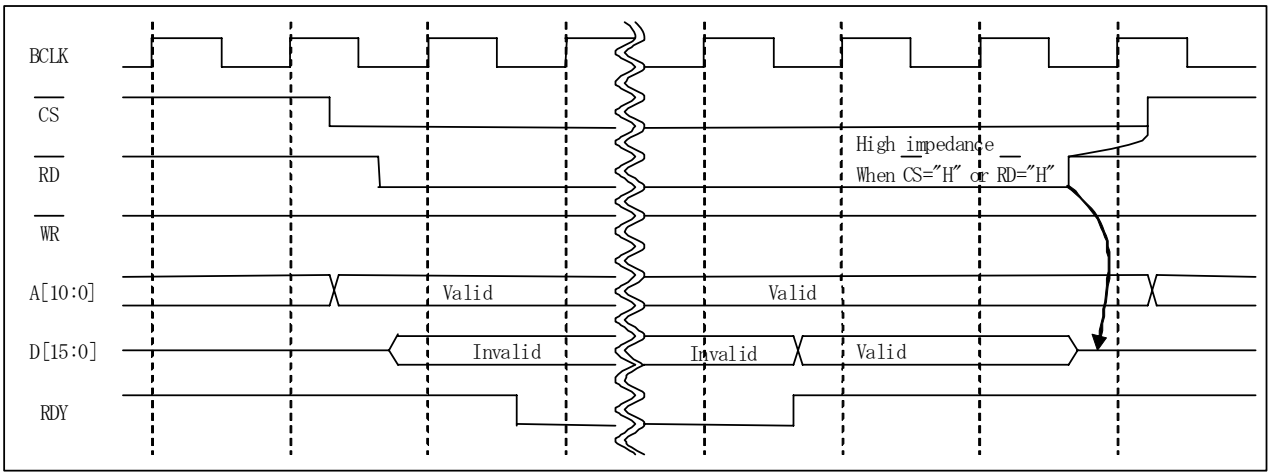
1. 16bit non-multiplexed parallel bus timing

Read timing in FR460 mode



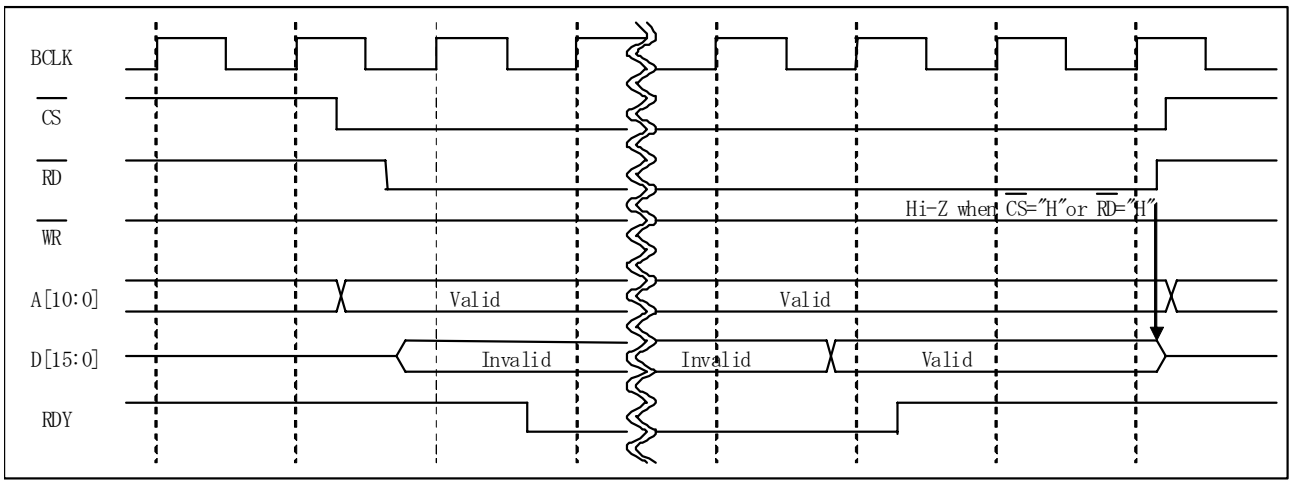
When the CS pin and the RD pin become "L", invalid data is output from the D[15:0] pins, and the RDY pin becomes "L" at the next rising edge of the BCLK pin, causing the CPU to wait. After several BCLK cycles, the RDY pin becomes "H" at the rising edge of the BCLK pin and valid data is output from the D[15:0] pins. When the RD pin becomes "H", the D[15:0] pins become Hi-Z.

Read timing in FR360 mode



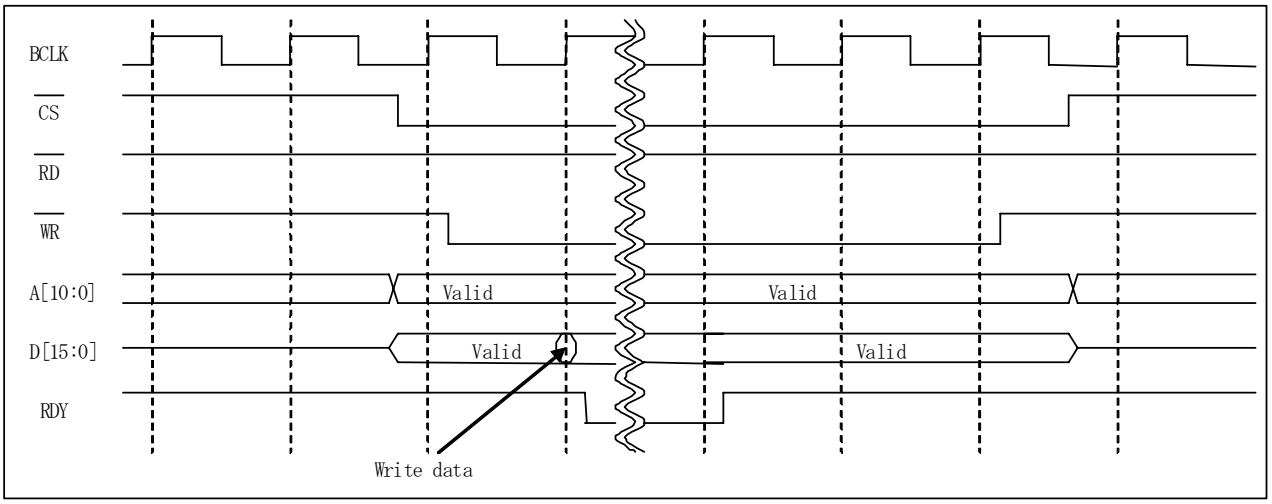
When the CS pin and the RD pin become "L", invalid data is output from the D[15:0] pins, and the RDY pin becomes "L" at the next falling edge of the BCLK pin, causing the CPU to wait. After several BCLK cycles, the RDY pin becomes "H" at the falling edge of the BCLK pin and valid data is output from the D[15:0] pins. When the RD pin becomes "H", the D[15:0] pins become Hi-Z.

Read timing in 16FX mode



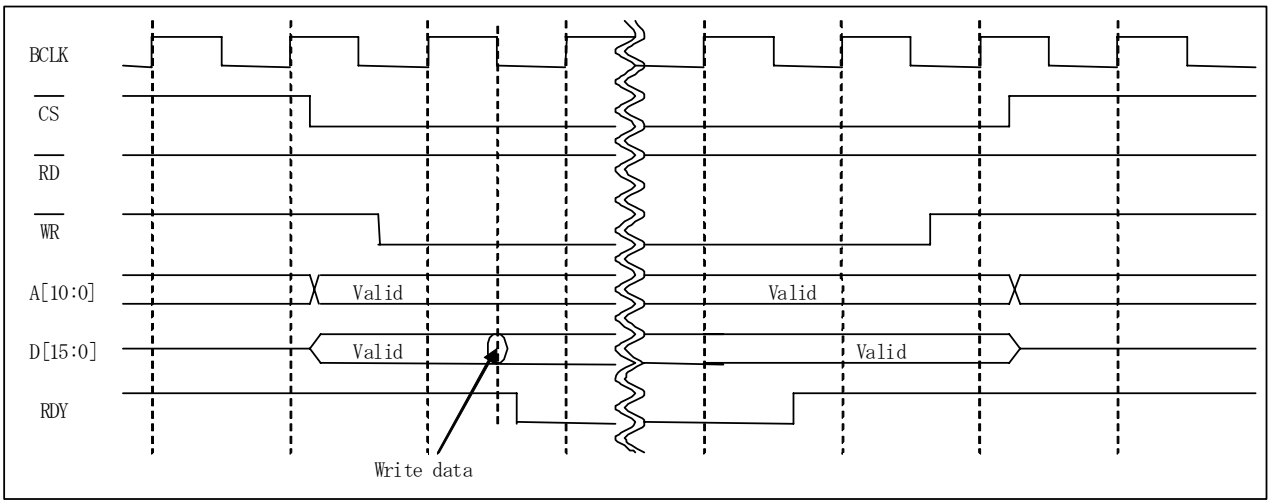
When the CS pin and RD pin become "L", data is output to the D15 to D0 pins, the RDY pin is set to "L" at the falling of the next BCLK pin and waits for the CPU. When data in the register is ready, the data is synchronized with the falling edge of the BCLK pin. When the next rising edge of the BCLK pin, the RDY pin is set to "H".When the CS or RD pin is set to "H", the D15 to D0 pins are set to high impedance.

Write timing in FR460 mode



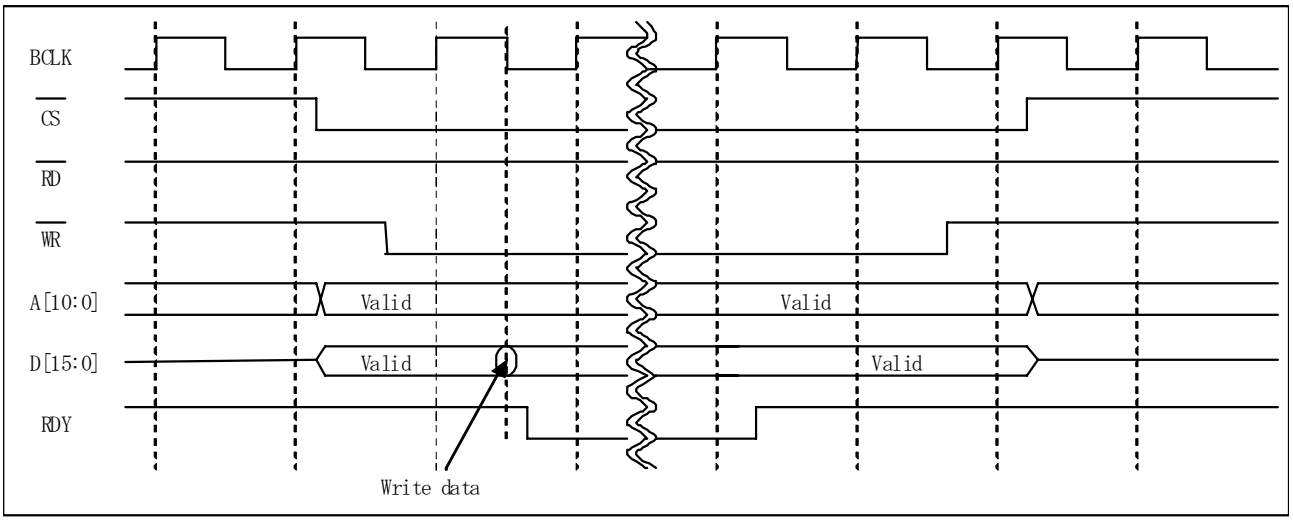
When the CS pin and the WR pin become "L", the data on the D[15:0] pins is written to a temporary register at the next rising edge of the BCLK pin, and the RDY pin becomes "L", causing the CPU to wait. When the data of the temporary register is written to the register addressed by the A[10:0] pins, the RDY pin becomes "H".

Write timing in FR360 mode



When the CS pin and the WR pin become "L", the data on the D[15:0] pins is written to a temporary register at the next falling edge of the BCLK pin, and the RDY pin becomes "L", causing the CPU to wait. When the data of the temporary register is written to the register addressed by the A[10:0] pins, the RDY pin becomes "H".

Write timing in 16FX mode



When the CS pin and the WR pin become "L", the data on the D[15:0] pins is written to a temporary register at thenext falling edge of the BCLK pin, and the RDY pin becomes "L", causing the CPU to wait. When the data of the temporary register is written to the register addressed by the A[10:0] pins, the RDY pin becomes "H" at the rising of the next BCLK pin.

2. Wait states caused by the RDY pin

The maximum low width of RDY is as follows.

1) BCLK=32MHz, RAM clock=80MHz

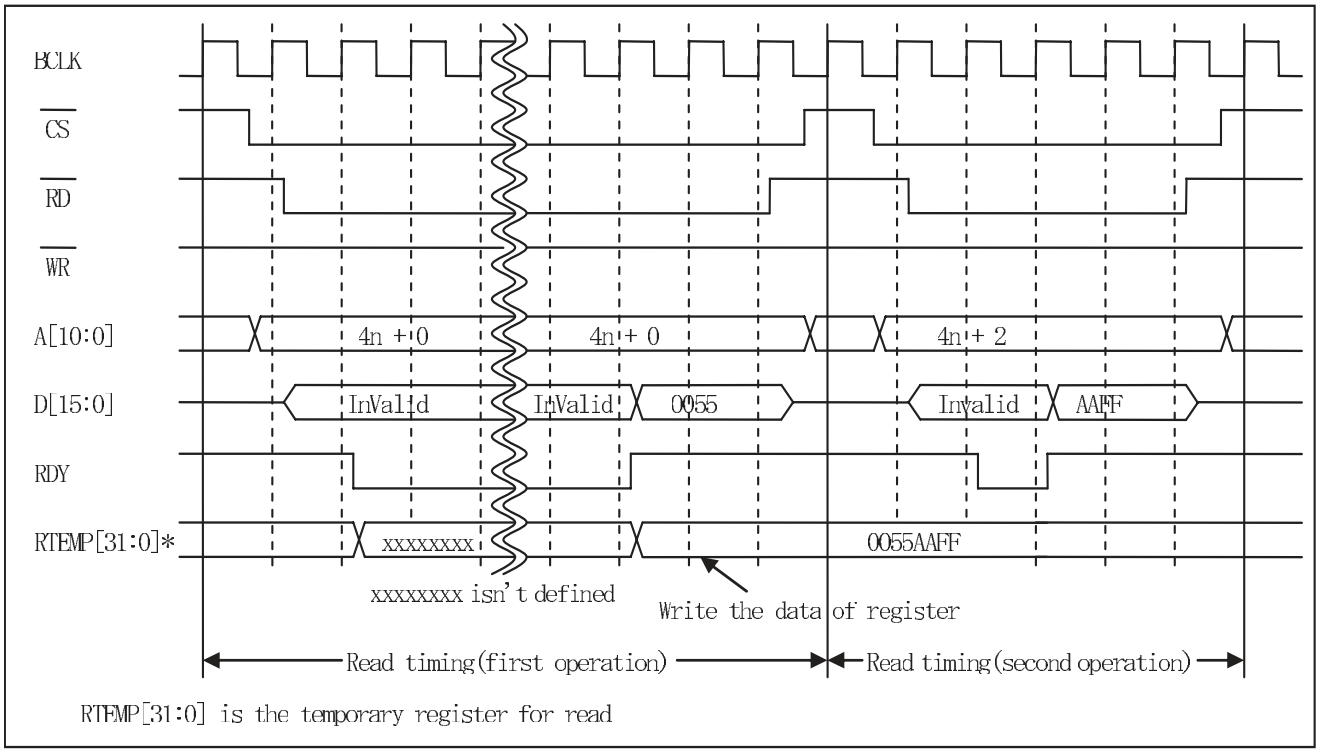
Device	Low width of RDY during read operation	Low width of RDY during writing operation
MB88121	Maximum 5 BCLK	Maximum 4 BCLK
MB88121A/ MB88121B/ MB88121C	Maximum 5 BCLK	Maximum 5 BCLK

2) BCLK=32MHz, RAM clock=40MHz

Device	Low width of RDY during read operation	Low width of RDY during writing operation
MB88121	Maximum 7 BCLK	Maximum 6 BCLK
MB88121A/ MB88121B/ MB88121C	Maximum 7 BCLK	Maximum 7 BCLK

3. The read timing for the register

The FlexRay Controller registers have a width of 32bit. A 32bit temporary read register is available to save read data. In the case of reading in 16bit non-multiplexed parallel bus mode, data of the register selected by A[10:0] pins is written to the temporary register by the first read access, and data of of the16bit upper temporary register is output to the D[15:0] pins. Data of the16bit lower temporary register is output to the D[15:0] pins by the second read access.

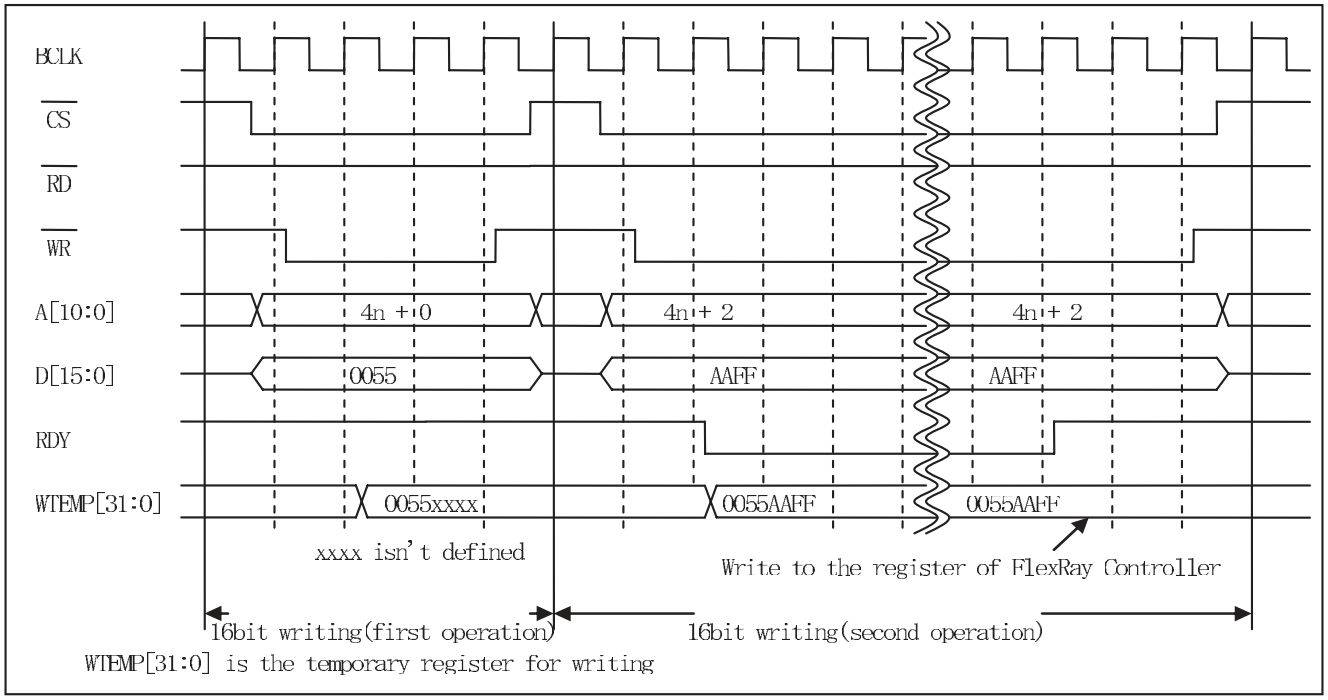


Read timing for FlexRay Controller (FR460 mode)

<<Note>>
As the register of the FlexRay Controller is 32bit, it must be accessed at 16bit twice continuously.

4. The write timing for the register

The FlexRay Controller registers have a width of 32bit. A 32bit temporary write register is available to save write data. In the case of writing in 16bit non-multiplexed parallel bus mode, data of the D[15:0] pins is written to the 16bit upper temporary register by the first write access, and data of the D[15:0] pins is written to the 16bit lower temporary register by the second write access. Then data of the temporary register is written to the register of the FlexRay controller.



Write timing for FlexRay Controller (FR460 mode)

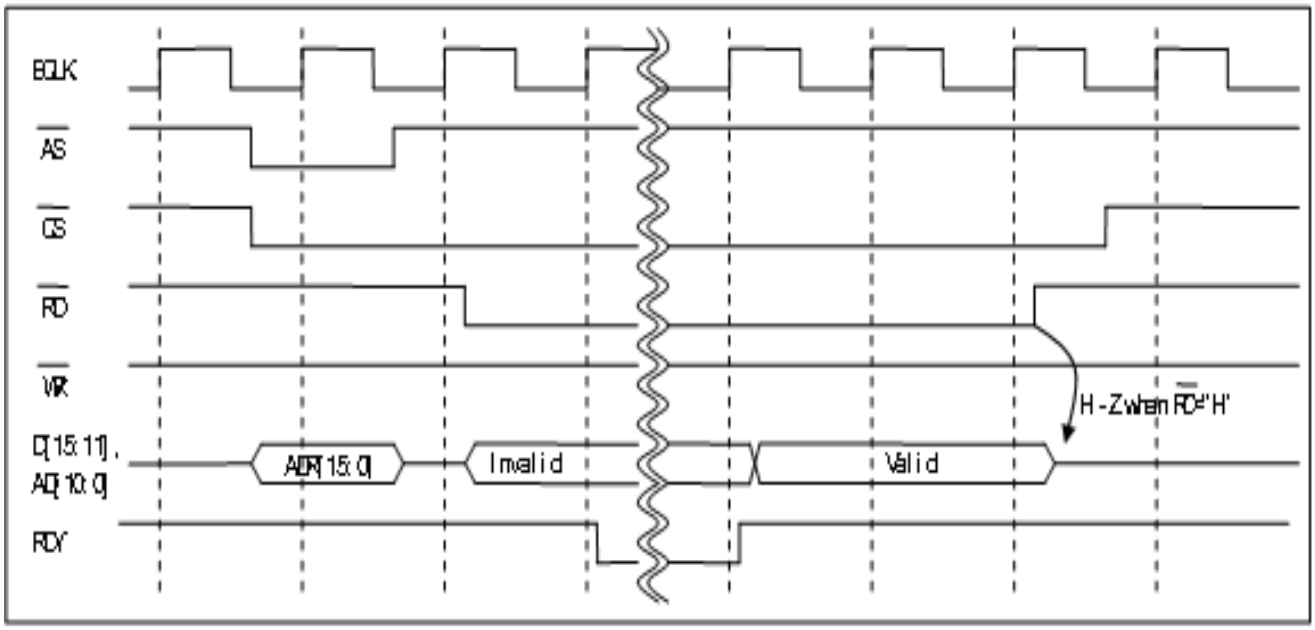
<<Note>>
As the register of the FlexRay Controller is 32bit, it must be accessed at 16bit twice continuously.

■ OPERATION IN 16-BIT MULTIPLEXED PARALLEL BUS MODE

The 16bit multiplexed parallel bus is is sharing the lower 11 bus lines for address (A[0..10]) and data (D0..10). As the register of the FlexRay Controller is 32bit wide, it must be accessed with two 16bit operations in consecue-tive manner.

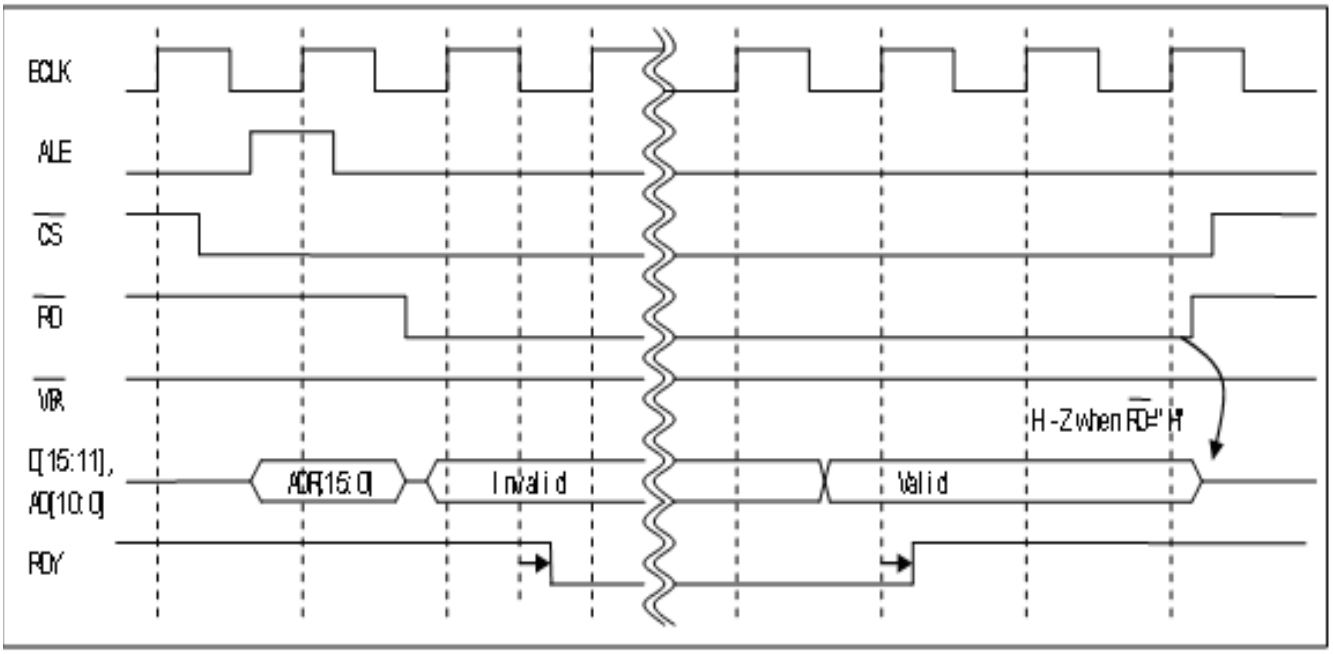
1. 16bit multiplexed parallel bus timing

Read timing in FR460 mode



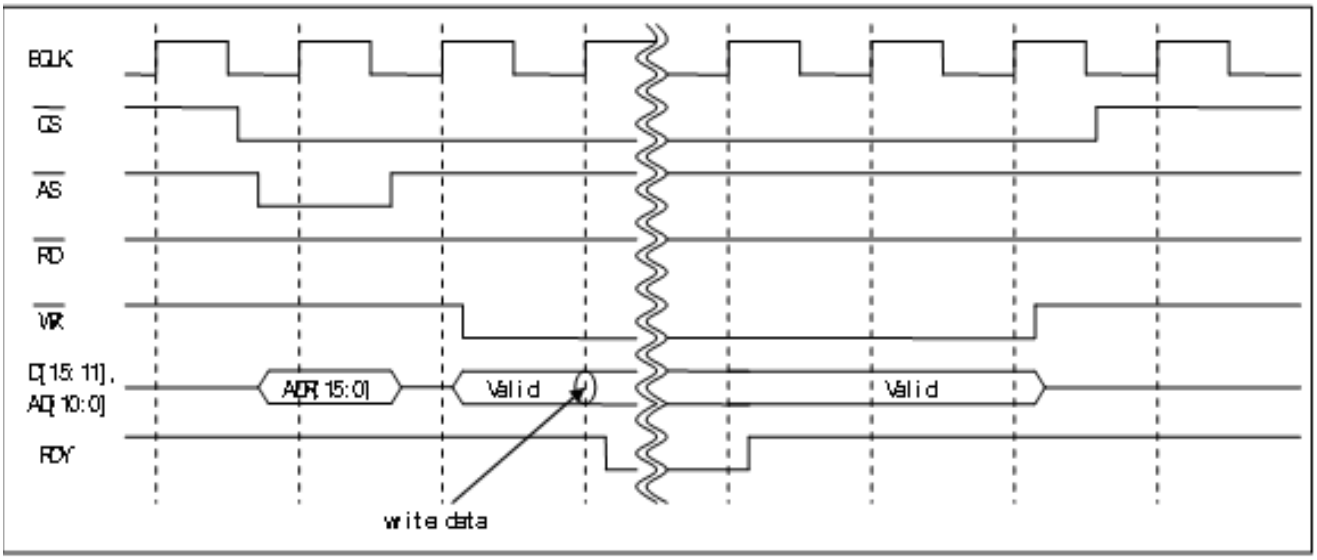
The address data is latched by the rising edge of AS pin. When the CS pin and RD pin become "L", invalid data is output from the D[15:11] pins and AD[10:0] pins, and the RDY pin becomes "L" at the next rising edge of BCLK pin, causing the CPU to wait. After several BCLK cycles, the RDY pin becomes "H" at the rising edge of the BCLK pin and valid data is output from the D[15:11] pins and AD[10:0] pins. When the RD pin becomes "H", the D[15:11] pins and AD[10:0] pins become Hi-Z.

Read timing in 16FX mode



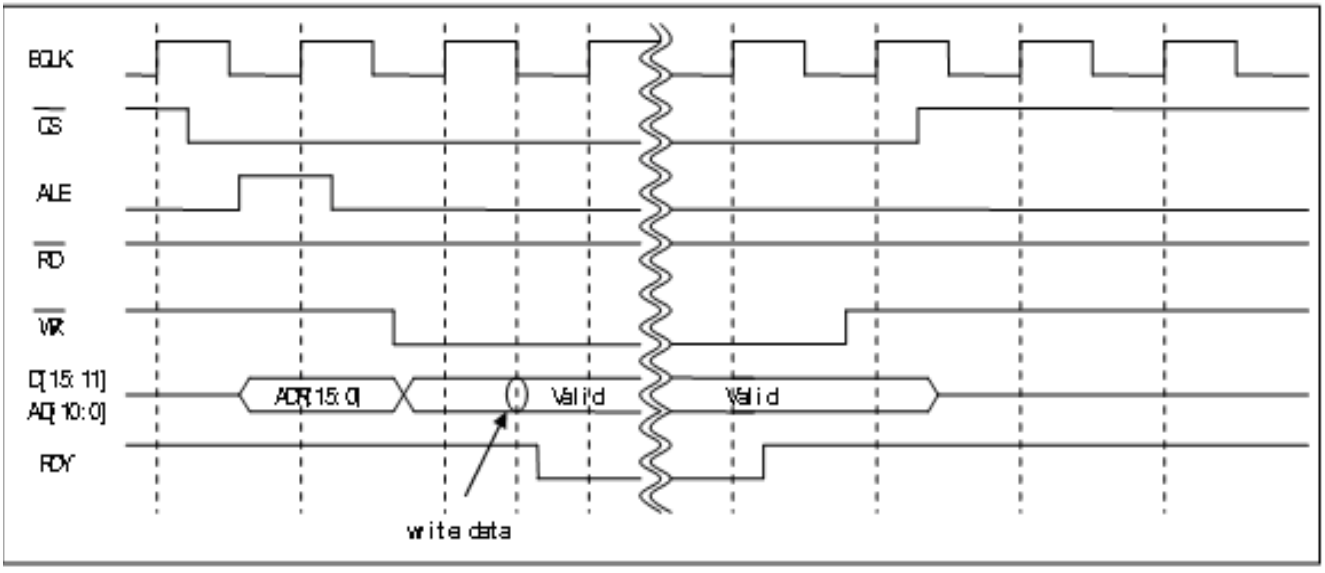
The address data is latched by the falling edge of ALE pin. When the CS pin and RD pin become "L", invalid data is output from the D[15:11] pins and AD[10:0] pins, and the RDY pin becomes "L" at the next falling edge of BCLK pin, causing the CPU to wait. After several BCLK cycles, the RDY pin becomes "H" at the rising edge of the BCLK pin and valid data is output from the D[15:11] pins and AD[10:0] pins. When the RD pin becomes "H", the D[15:11] pins and AD[10:0] pins become Hi-Z.

Writing timing in FR460 mode



The address data are latched by the rising edge of AS pin. When the CS pin and the WR pin become "L", the data on the D[15:11] pins and AD[10:0] pins is written to a temporary register at the next rising edge of the BCLK pin, and the RDY pin becomes "L", causing the CPU to wait. When the data of the temporary register is written to the register is written to the register addressed by the address data, the RDY pin becomes "H".

Writing timing in 16FX mode



The address data are latched by the falling edge of ALE pin. When the CS pin and the WR pin become "L", the data on the D[15:11] pins and AD[10:0] pins is written to a temporary register at the next falling edge of the BCLK pin, and the RDY pin becomes "L", causing the CPU to wait. When the data of the temporary register is written to the register is written to the register addressed by the address data, the RDY pin becomes "H".

2. Wait states caused by the RDY pin

The maximum low width of RDY is as follows.

1) BCLK=32MHz, RAM clock=80MHz

MODE	Low width of RDY during read operation	Low width of RDY during writing operation
FR460	Maximum 5BCLK	Maximum 5BCLK
16FX	Maximum 5BCLK + Low width of BCLK	Maximum 5BCLK + Low width of BCLK

2) BCLK=32MHz, RAM clock=40MHz

MODE	Low width of RDY during read operation	Low width of RDY during writing operation
FR460	Maximum 7BCLK	Maximum 7BCLK
16FX	Maximum 7BCLK + Low width of BCLK	Maximum 7BCLK + Low width of BCLK

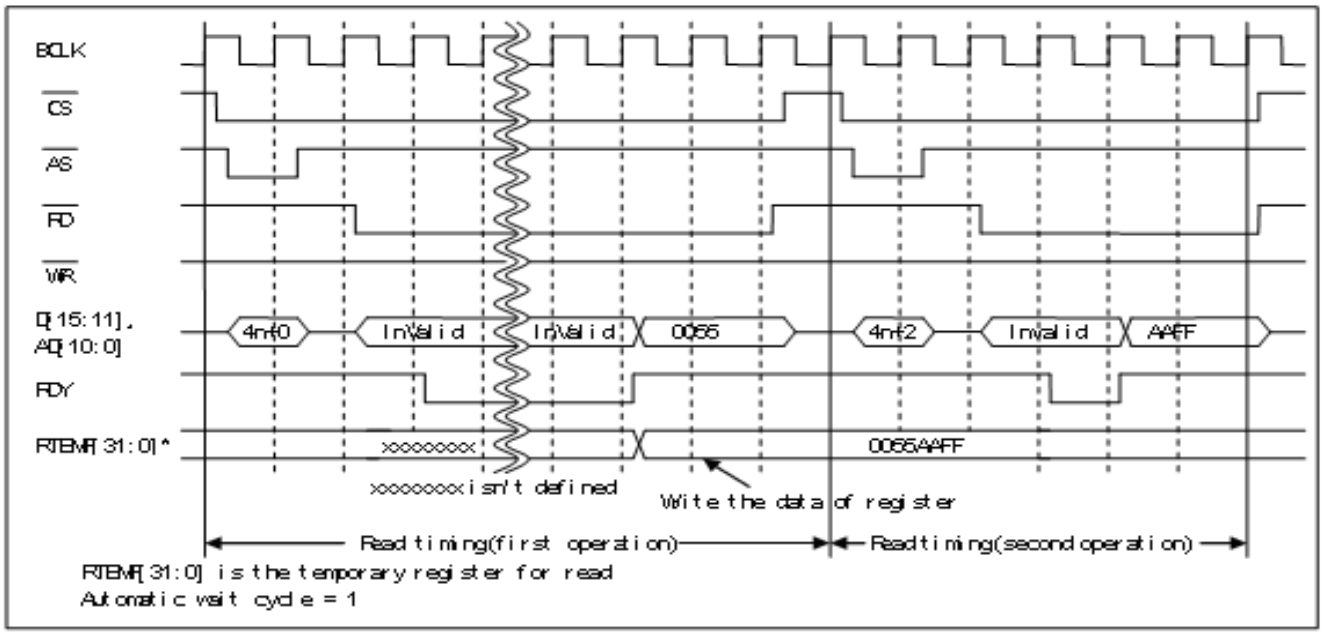
3. The read timing for the register

The FlexRay Controller registers have a width of 32bit. A 32bit temporary read register is available to save read data. In the case of reading in 16bit multiplexted parallel bus mode, data of the register selected by the address data latched by the AS pin or ALE pin is written to the temporary register by the first read access, and the data of temporary register is output to the D[15:11] pins and AD[10:0] pins as follows.

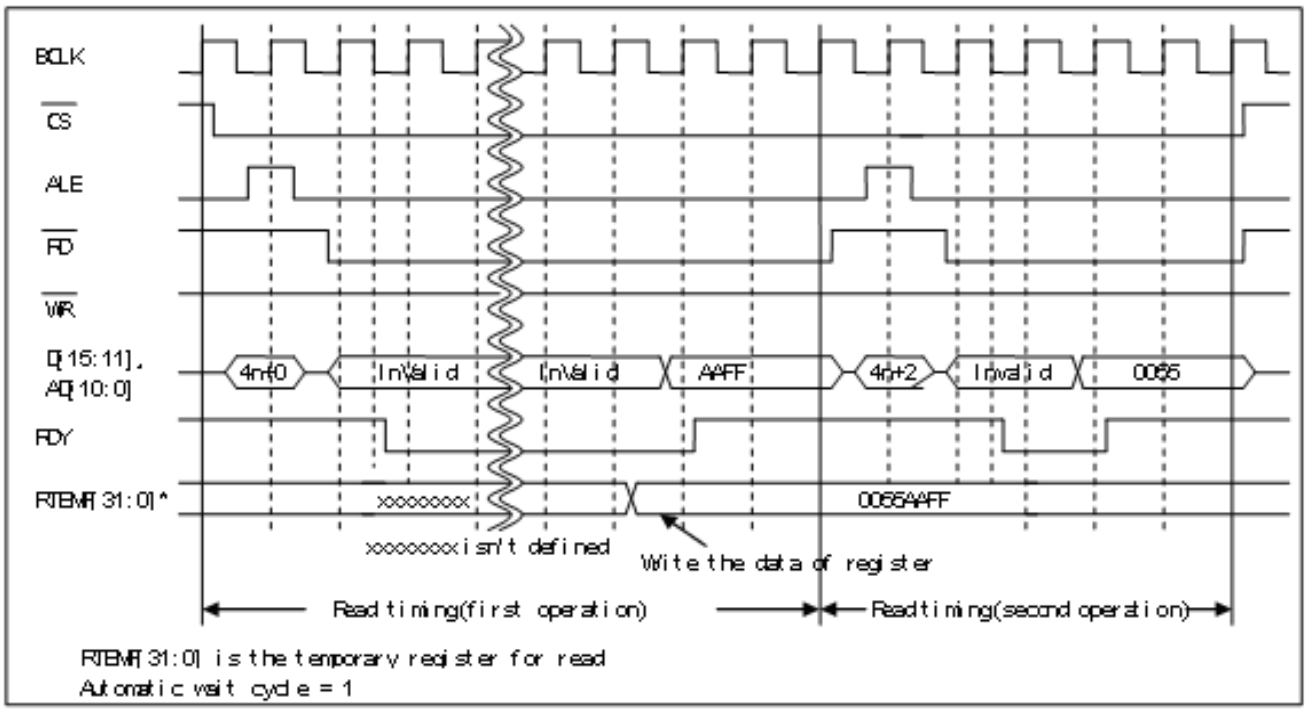
FR460 mode: Data of the 16bit upper temporary register is output to the D[15:11] pins and AD[10:0] in case of the first read access, and data of the 16bit lower temporary register is output to the D[15:11] pins and AD[10:0] pins in case of the second read access.

16FX mode: Data of the 16bit lower temporary register is output to the D[15:11] pins and AD[10:0] in case of the first read access, and data of the 16bit upper temporary register is output to the D[15:11] pins and AD[10:0] pins in case of the second read access.

Read operation in FR460 mode



Read operation in 16FX mode



<<Note>>
As the register of the FlexRay Controller is 32bit, it must be accessed at 16bit twice continuously

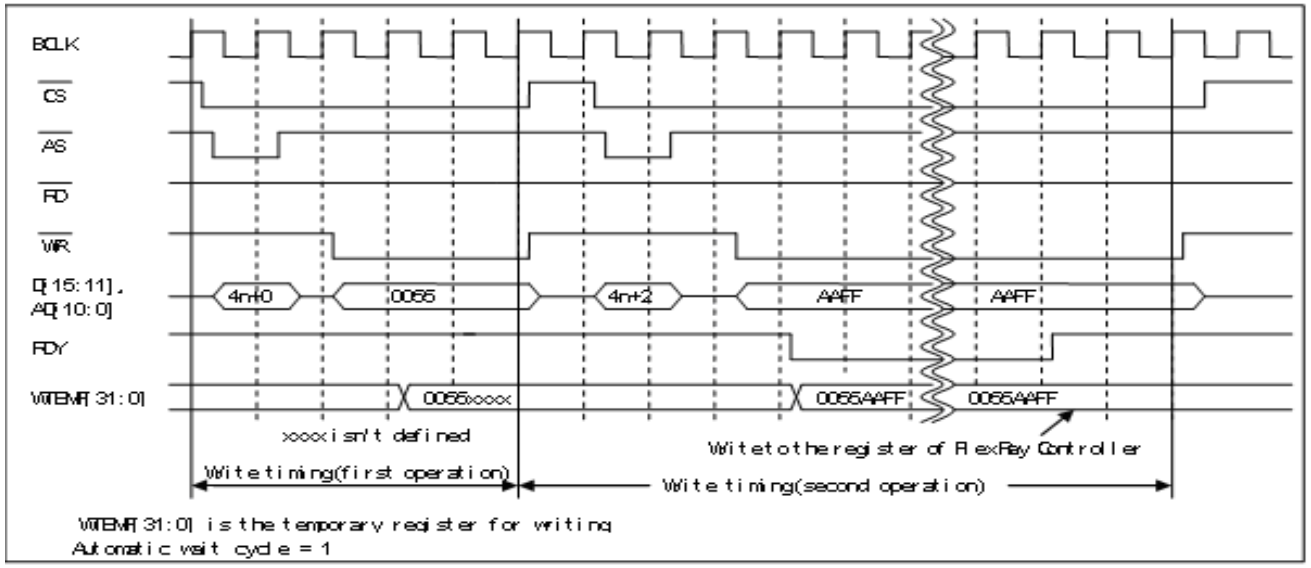
4. The write timing for the register

The FlexRay Controller registers have a width of 32bit. A 32bit temporary read register is available to save write data. In the case of writing in 16bit multiplexted parallel bus mode, the temporary register is written as follows.

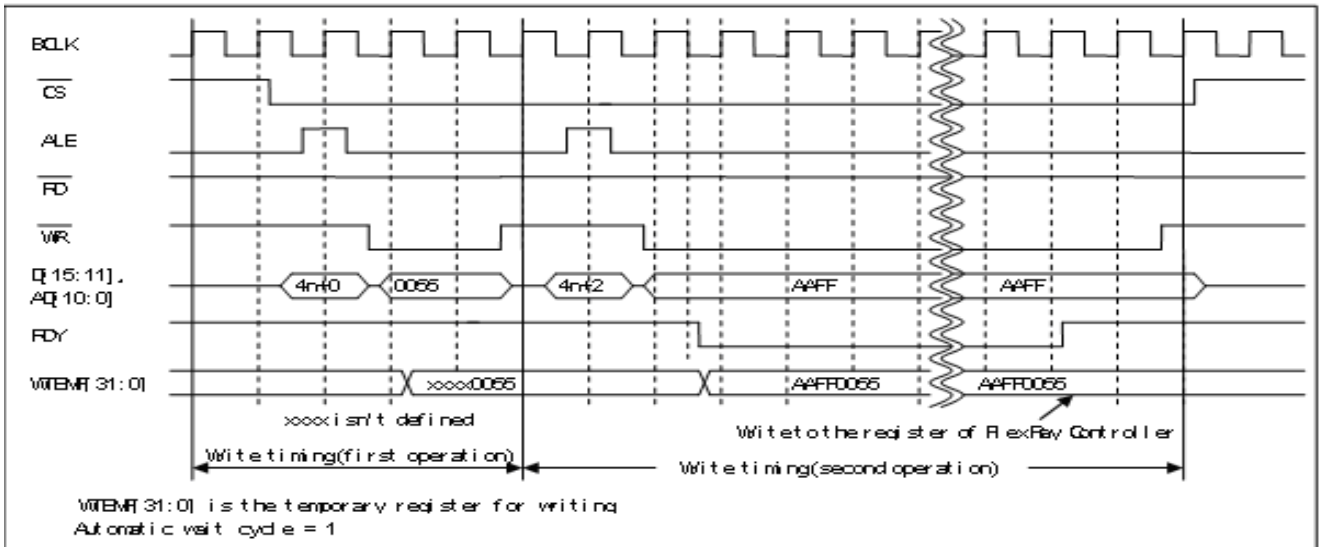
FR460 mode: Data of the D[15:11] pins and AD[10:0] pins is written to the 16bit upper temporary register in case of the first write access, and it is written to the 16 bit lower temporary register in case of the second write access. Then the data of the temporary register is written to the register of FlexRay controller.

16FX mode: Data of the D[15:11] pins and AD[10:0] pins is written to the 16bit lower temporary register in case of the first write access, and it is written to the 16 bit upper temporary register in case of the second write access. Then the data of the temporary register is written to the register of FlexRay controller.

Write operation in FR460 mode



Write operation in 16FX mode



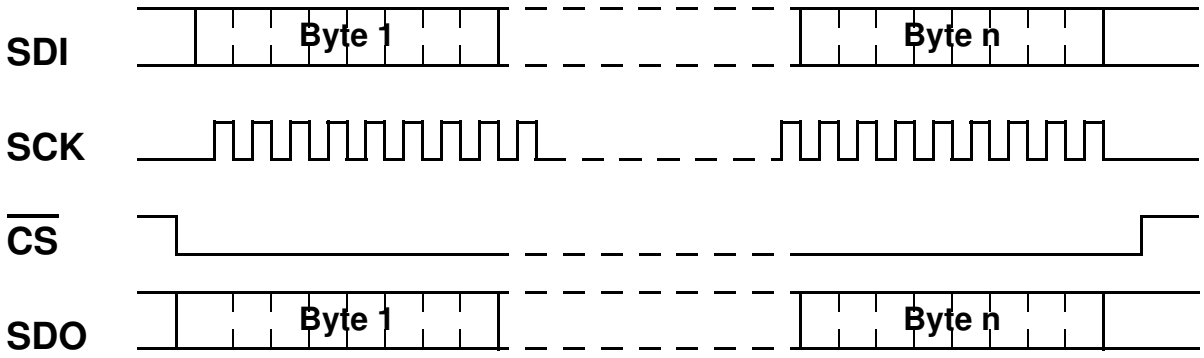
<<Note>>
As the register of the FlexRay Controller is 32bit, it must be accessed at 16bit twice continuously.

■ OPERATION IN SPI MODE

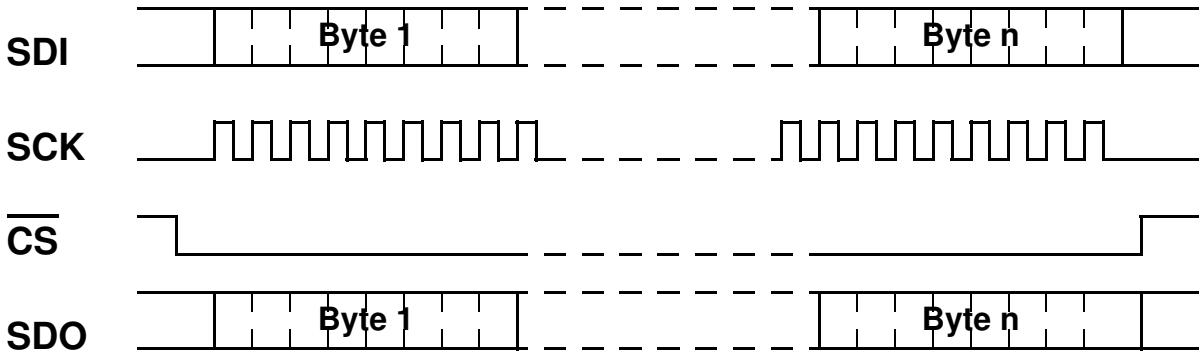
1. Basic SPI Modes

In SPI mode, MB88121 acts as an SPI slave. When Chip Select $\overline{CS}$ becomes “High-level“, SDO changes to HIGH Z state and data on SDI is not read by MB88121. Depending on MDS[2:0], the following formats are possible:

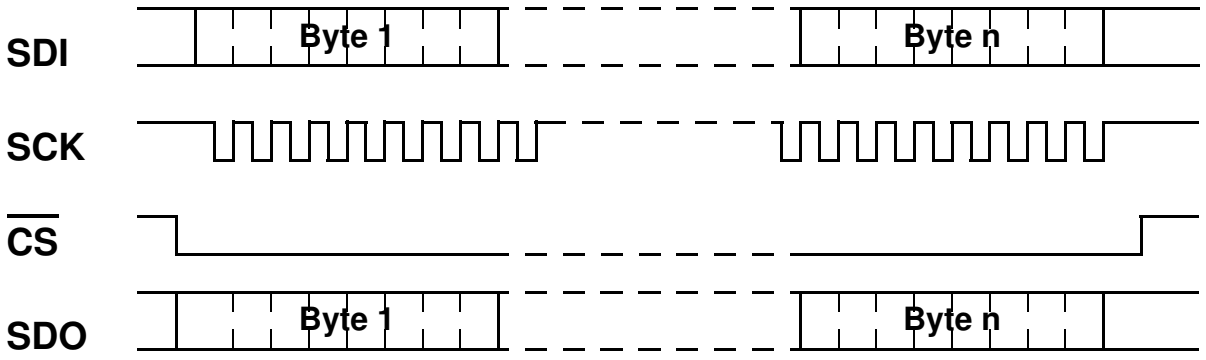
MDS[1:0] = 00: Active-high clock, sampling on odd (rising) edge



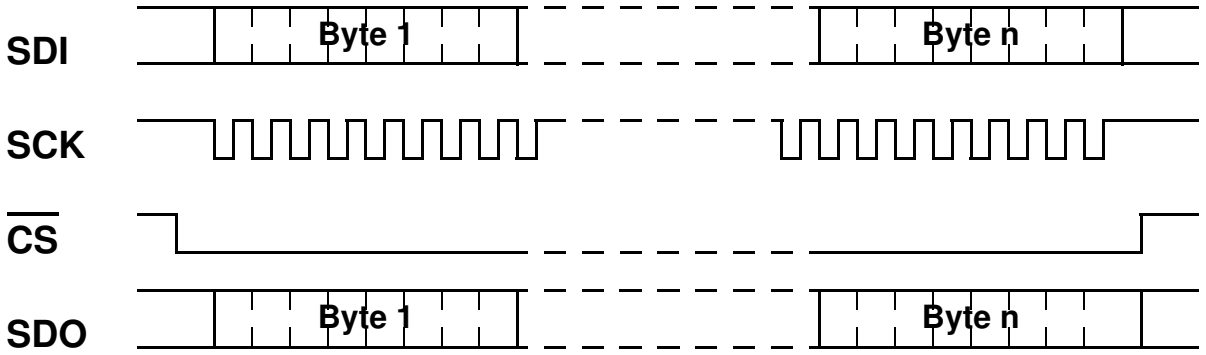
MDS[1:0] = 01: Active-high clock, sampling on even (falling) edge



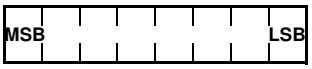
MDS[1:0] = 10: Active-low clock, sampling on odd (falling) edge



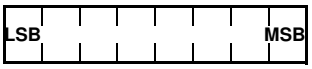
MDS[1:0] = 11: Active-low clock, sampling on even (rising) edge



MDS[2] = 0: MSB first



MDS[2] = 1: LSB first



2. Specific Protocol Definition

Communication via the SPI interface is performed by command frames. Between two command frames, $\overline{CS}$ must be dis asserted to '1'. A command frame consists of a command byte according to the following table and several additional bytes (refer to the command descriptions).

The format of the command byte is as follows.

7	6	5	4	3	2	1	0
C4	C3	C2	C1	C0	'0'	P	*

*: Bit 0 of the command byte is used as the address bit A[10] for the WR, RD and RDN commands. For other commands, Bit 0 is '0'.

C4 = 0:

Opcode	C4	C3 = RD1	C2 = RD0	C1 = WR1	C0 = WR0	P	Mnemonic	Command
00h	0	0	0	0	0	0	NOP	No Operation
0Ah/09h	0	0	0	0	1	1/0	WR	Write Word
12h	0	0	0	1	0	1	WBI	Write Input Buffer, Initialize
18h	0	0	0	1	1	0	WBC	Write Input Buffer, Continue
22h/21h	0	0	1	0	0	1/0	RD	Read Word
	0	0	1	0	1	0		reserved
	0	0	1	1	0	0		reserved
	0	0	1	1	1	1		reserved
42h	0	1	0	0	0	1	RBI	Read Output Buffer, Initialize
	0	1	0	0	1	0		reserved
50h	0	1	0	1	0	0	RBIWBI	Combination of RBI and WBI
5Ah	0	1	0	1	1	1	RBIWBC	Combination of RBI and WBC
60h	0	1	1	0	0	0	RBC	Read Output Buffer, Continue
	0	1	1	0	1	1		reserved
72h	0	1	1	1	0	1	RBCWBI	Combination of RBC and WBI
78h	0	1	1	1	1	0	RBCWBC	Combination of RBC and WBC

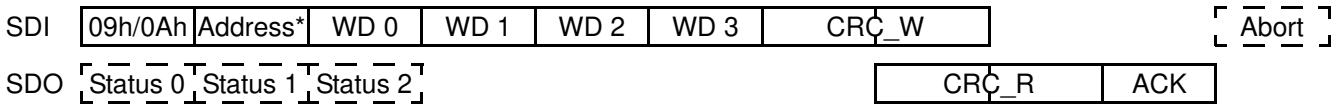
C4 = 1:

Opcode	C4	C3	C2	C1	C0	P	Mnemonic	Command
82h	1	0	0	0	0	1	WIP	Write Input Buffer Pointer
88h	1	0	0	0	1	0	WOP	Write Output Buffer Pointer
90h	1	0	0	1	0	0	WRIBC	Write Input Buffer Control
9Ah	1	0	0	1	1	1	WROBC	Write Output Buffer Control
A0h/A3h	1	0	1	0	0	0/1	RDN	Read n Words
AAh	1	0	1	0	1	1	WRHS	Write Input Buffer Header Section WRHS1-3
B2h	1	0	1	1	0	1		reserved
B8h	1	0	1	1	1	0		reserved
C0h	1	1	0	0	0	0		reserved
CAh	1	1	0	0	1	1		reserved
D2h	1	1	0	1	0	1		reserved
D8h	1	1	0	1	1	0		reserved
E2h	1	1	1	0	0	1		reserved
E8h	1	1	1	0	1	0		reserved
F0h	1	1	1	1	0	0		reserved
FAh	1	1	1	1	1	1		reserved

These opcodes are subject to change.

Opcodes listed as ‘reserved’ in the table will be interpreted as NOP commands. The P bit is defined such that each valid command has even parity, resulting in a Hamming distance of 2 between valid opcodes. One bit error within the command byte can never cause a valid command to be interpreted as another valid command except NOP.

WR: Write one Word, Command Byte = 09h/0Ah

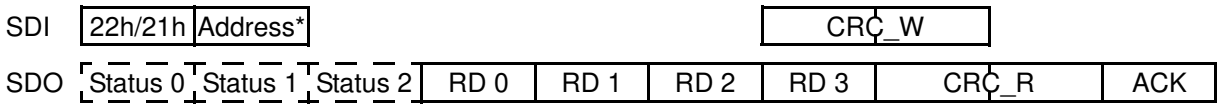


*: A[10] = bit 0 of command byte, A[9:2] = Address byte, A[1:0] = 00.

After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, 32bit of data WD[3:0] is written to the address A[10:0] if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, data is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write the data.

Payload:	4 bytes
Command length:	10 bytes
Overhead:	150%
Efficiency:	40%

RD: Read one Word, Command Byte = 22h/21h

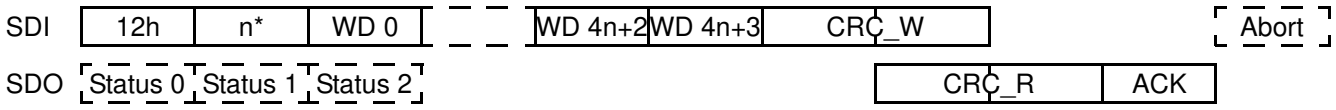


*: A[10] = bit 0 of command byte, A[9:2] = Address byte, A[1:0] = 00.

Data RD[3:0] is read from address A[10:0].
After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent.

Payload:	4 bytes
Command length:	10 bytes
Overhead:	150%
Efficiency:	40%

WBI: Write Input Buffer, Initialize IBP, Command Byte = 12h

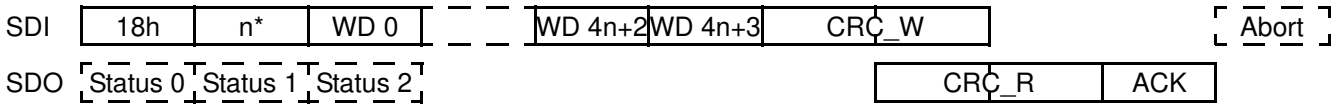


*: n = word count - 1; 0 ≤n ≤63

Clear IBP and write data starting at address 400h (IBP = Input Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP is incremented by n+1 if CS has a rising edge immediately after ACK. If there is no rising CS edge immediately after ACK, IBP is not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising CS edge and will not increment IBP.

Payload:	4*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	150% / (n+1)
Efficiency:	100% * (1 - 3/(2n+5))

WBC: Write Input Buffer, Continue, Command Byte = 18h

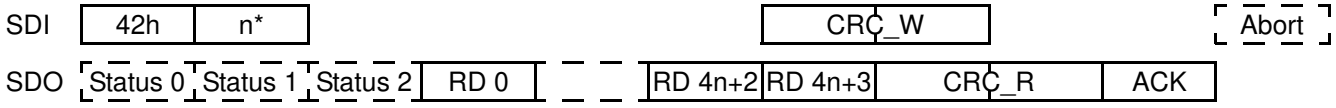


*: n = word count - 1; 0 ≤n ≤63

Write data starting at address 400h+4*IBP (IBP = Input Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP is incremented by n+1 if CS has a rising edge immediately after ACK. If there is no rising CS edge immediately after ACK, IBP is not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising CS edge and will not increment IBP.

Payload:	4*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	150% / (n+1)
Efficiency:	100% * (1 - 3/(2n+5))

RBI: Read Output Buffer, Initialize OBP, Command Byte = 42h

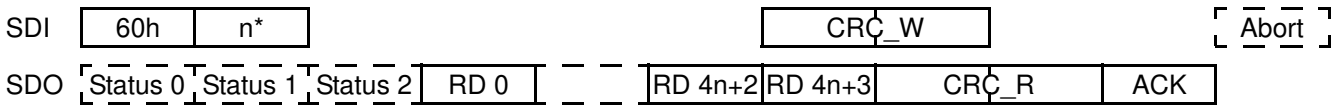


*: n = word count - 1; 0 ≤n ≤63

Clear OBP and read data starting at address 600h (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, OBP is incremented by n+1 if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, OBP is not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not increment OBP.

Payload:	4*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	150% / (n+1)
Efficiency:	100% * (1 - 3/(2n+5))

RBC: Read Output Buffer, Continue, Command Byte = 60h

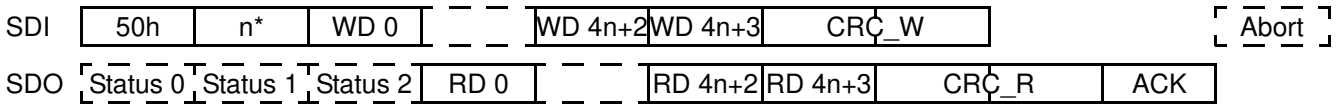


*: n = word count - 1; 0 ≤n ≤63

Read data starting at address 600h+4*OBP (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, OBP is incremented by n+1 if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, OBP is not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not increment OBP.

Payload:	4*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	150% / (n+1)
Efficiency:	100% * (1 - 3/(2n+5))

RBIWBI: Combination of RBI and WBI, Command Byte = 50h

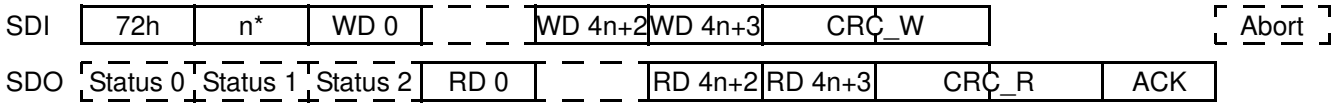


*: n = word count - 1; 0 ≤n ≤63

Clear IBP and write data starting at address 400h (IBP = Input Buffer Pointer). Clear OBP and read data starting at address 600h (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP and OBP are incremented by n+1 if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, IBP and OBP are not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not increment IBP and OBP.

Payload:	8*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	75% / (n+1) - 50%
Efficiency:	200% * (1 - 3/(2n+5))

RBCWBI: Combination of RBC and WBI, Command Byte = 72h

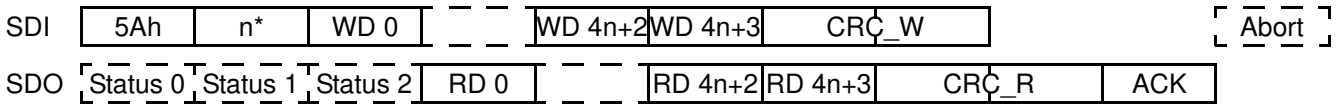


*: n = word count - 1; 0 ≤n ≤63

Clear IBP and write data starting at address 400h (IBP = Input Buffer Pointer). Read data starting at address 600h+4*OBP (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP and OBP are incremented by n+1 if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, IBP and OBP are not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not increment IBP and OBP.

Payload:	8*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	75% / (n+1) - 50%
Efficiency:	200% * (1 - 3/(2n+5))

RBIWBC: Combination of RBI and WBC, Command Byte = 5Ah

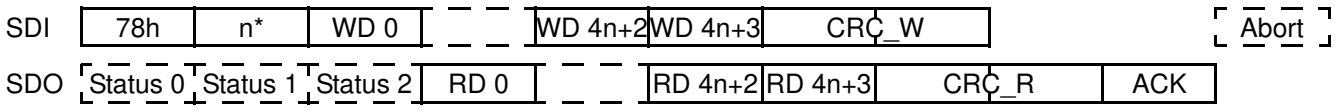


*: n = word count - 1; 0 ≤n ≤63

Write data starting at address 400h+4*IBP (IBP = Input Buffer Pointer). Clear OBP and read data starting at address 600h (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP and OBP are incremented by n+1 if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, IBP and OBP are not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not increment IBP and OBP.

Payload:	8*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	75% / (n+1) - 50%
Efficiency:	200% * (1 - 3/(2n+5))

RBCWBC: Combination of RBC and WBC, Command Byte = 78h

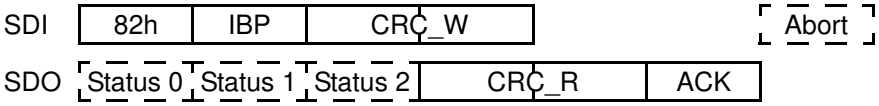


*: n = word count - 1; 0 ≤n ≤63

Write data starting at address 400h+4*IBP (IBP = Input Buffer Pointer). Read data starting at address 600h+4*OBP (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP and OBP are incremented by n+1 if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, IBP and OBP are not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not increment IBP and OBP.

Payload:	8*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	75% / (n+1) - 50%
Efficiency:	200% * (1 - 3/(2n+5))

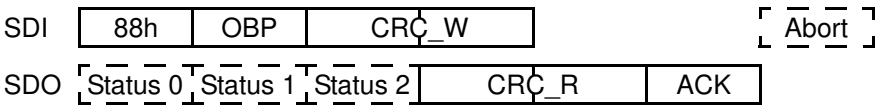
WIP: Write Input Buffer Pointer, Command Byte = 82h



After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP is written if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, IBP is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write IBP. IBP is used by commands WBC, RBIWBC and RBCWBC.

Payload:	0 bytes
Command length:	6 bytes
Overhead:	6 bytes
Efficiency:	0%

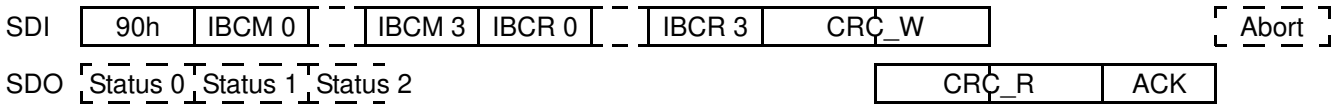
WOP: Write Output Buffer Pointer, Command Byte = 88h



After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, OBP is written if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, OBP is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write OBP. OBP is used by commands RBC, RBCWBI and RBCWBC.

Payload:	0 bytes
Command length:	6 bytes
Overhead:	6 bytes
Efficiency:	0%

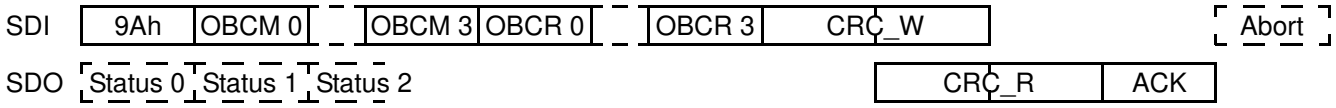
WRIBC: Write Input Buffer Command, Command Byte = 90h



Write IBCM[3:0] to IBCM register. After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBCR[3:0] is written to IBCR register if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, the IBCR register is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write the IBCR register.
It is no problem that IBCM register may be written even in the case of a communication problem: IBCM is only a configuration register, it does not trigger an action. On the other hand, writing the IBCR register triggers an action. For this reason, IBCR is written only after it has been confirmed that there has been no communication problem.

Payload:	8 bytes
Command length:	13 bytes
Overhead:	62.5%
Efficiency:	61.5%

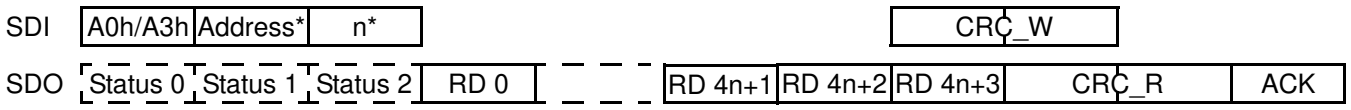
WROBC: Write Output Buffer Command, Command Byte = 9Ah



Write OBCM[3:0] to OBCM register. After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, OBCR[3:0] is written to OBCR register if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, the OBCR register is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write the OBCR register.
It is no problem that OBCM register may be written even in the case of a communication problem: OBCM is only a configuration register, it does not trigger an action. On the other hand, writing the OBCR register triggers an action. For this reason, OBCR is written only after it has been confirmed that there has been no communication problem.

Payload:	8 bytes
Command length:	13 bytes
Overhead:	62.5%
Efficiency:	61.5%

RDN: Read n Words, Command Byte = A0h/A3h

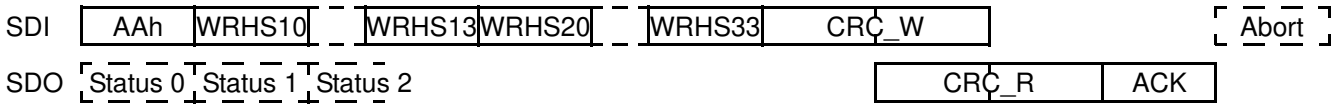


*: A[10] = bit 0 of command byte, A[9:2] = Address byte, A[1:0] = 00.
n = word count - 1; 0 ≤n ≤63

For i = 0 to n, data RD[4i+3:4i] is read from address A[10:0]+4i.
After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent.

Payload:	4*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	150% / (n+1)
Efficiency:	100% * (1 - 3/(2n+5))

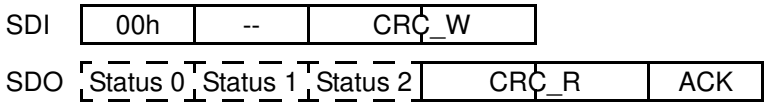
WRHS: Write Input Buffer Header Section WRHS1-3, Command Byte = AAh



Write WRHS1[3:0] to WRHS1 register. Write WRHS2[3:0] to WRHS2 register. After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, WRHS3[3:0] is written to WRHS3 register if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, the WRHS3 register is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write the WRHS3 register.
It is no problem that WRHS1 and WRHS2 registers may be written even in the case of a communication problem: WRHS1-3 are only configuration registers, writing to them does not trigger an action.

Payload:	12 bytes
Command length:	17 bytes
Overhead:	41.7%
Efficiency:	70.6%

NOP: No Operation (Read Status), Command Byte = 00h



Payload:	0 bytes
Command length:	6 bytes
Overhead:	6 bytes
Efficiency:	0%

3. Data Security Algorithms

CRC_x: The CRC_W and CRC_R fields are used for error detection. They consist of 16 bits. For the generation of the CRC_W and CRC_R fields, the polynomial 0x1021 is used.

ACK: The ACK field consists of 8 bits. By the ACK field, MB88121 signals to the host that the CRC check of the CRC_W field has been successful. A successful check of CRC_W is acknowledged by ACK = FFh, a CRC error of CRC_W is signalled by ACK = 00h.
The host can apply an error correction to the ACK field by checking the binary cross sum cs(ACK).

$$cs(ACK) = \sum_{i=0}^{7} ACK[i]$$

For example, the error corrected acknowledge ACK_ecc could be calculated as follows:
ACC_ecc = “OK” if cs(ACK) ≥ 6. In this case the host can assume that the transmission was successful.
ACC_ecc = “NG” if cs(ACK) ≤5. In this case the host should transmit an extra byte (Abort), dis assert $\overline{CS}$ and start a new transmission.

Abort: MB88121 will perform its action (writing a register or updating IBP/OBP) only after it has received the correct CRC_W and after it has detected the rising $\overline{CS}$ edge exactly after the last bit of the ACK byte (but writing to the Input buffer is always performed immediately, word by word as they are received). If another clock edge is detected when the rising $\overline{CS}$ edge is expected, or if the rising $\overline{CS}$ edge is detected when another clock edge is expected, MB88121 will not perform its action. If several bits of the ACK byte are corrupted, the host does not know if MB88121 has correctly received the message or not. In this case, the host can send an extra byte (Abort) which will be interpreted by MB88121 as extra clocks when the rising $\overline{CS}$ edge is expected. In this case, it will ignore the message, i.e. it will not write the register or not update IBP/OBP).

4. Default Status Read Out

With this protocol MB88121 transmits 24 bits of status information at the beginning of each command frame.

Status Byte Overview:

STATUS 0

7	6	5	4	3	2	1	0
ST07	ST06	ST05	ST04	ST03	ST02	ST01	ST00

STATUS 1

7	6	5	4	3	2	1	0
ST17	ST16	ST15	ST14	ST13	ST12	ST11	ST10

STATUS 2

7	6	5	4	3	2	1	0
ST27	ST26	ST25	ST24	ST23	ST22	ST21	ST20

STATUS 0 Definition

Bit	Name	Function
7	ST07	reserved
6	ST06	reserved
5	ST05	reserved
4	ST04	reserved
3	ST03	reserved
2	ST02	reserved
1	ST01	eray_obusy ‘1’: Output buffer busy flag. If it is set, the output buffer is busy (0x600-0x6fc).Write access to OBCR register should not be performed. After confirming this bit is '0' by NOP command, write it in the OBCM and OBCR registers. ‘0’: Output buffer not busy
0	ST00	eray_ibusy ‘1’: Input buffer busy flag.If it is when input buffer is busy.(0x400-0x4fc).Write access to the input buffer shoud not be performed. After confirming this bit is '0' by NOP command, write it in the IBCM and IBCR registers. ‘0’: Input buffer not busy

Note: STATUS 0 register shows status of e-ray core(bit2-bit7=0). The status value is changed at falling edge of CSX.

STATUS 1 Definition

Bit	Name	Function
7	ST17	Parity error ‘1’: Parity error occured during last tranmission. ‘0’: No parity error.

Bit	Name	Function
6	ST16	Command format error ‘1’: Command format error occured at last transmission. (ie. bit2/bit0 of command first byte) is 1 (exception : command that has A[10] bit)) ‘0’: No command format error.
5	ST15	reserved
4	ST14	Undefined error ‘1’: Undifiened Command used at last transmission. ‘0’: no undefiened error.
3	ST13	Busy error ‘1’: E-Ray Communication Controller was busy and command is not executed. ‘0’: No tbusy error.
2	ST12	Long message error ‘1’: Message was too long at last transmission. ‘0’: No long message error occured
1	ST11	Short message error ‘1’: Message was too short at last transmission. ‘0’: No short message error.
0	ST10	Crc error ‘1’: CRC error at last transmission ‘0’: No CRC error.

Note: STATUS 1 register shows the status of previous SPI session. This status is cleared by eray_reset.

STATUS 2 Definition

Bit	Name	Function
7	ST27	reserved
6	ST26	reserved
5	ST25	E-Ray timer 1 interrupt flag (tint1) ‘1’: E-Ray timer 1 interrupt flag is set ‘0’: No E-Ray timer 1 flag is set
4	ST24	E-Ray timer 0 interrupt flag (tint0) ‘1’: E-Ray timer 0 interrupt flag is set ‘0’: No E-Ray timer 0 flag is set
3	ST23	E-Ray interrupt lin1 (int1) flag ‘1’: E-Ray interrupt line 1 flag is set. At least one of the E-Ray line 1 assigned interrupt (EILS, SILS, EIES, SIES,ILE) flag is set. ‘0’: No E-Ray line1 interrupt.
2	ST22	E-Ray interrupt line0 (int0) flag ‘1’: E-Ray interupt line 0 flag is set. At least one of the E-Ray line 0 assigned interrupt (EILS, SILS, EIES, SIES,ILE) flag is set. ‘0’: No E-Ray line0 interrupt.
1	ST21	Status Interrupt register (SIR) flag ‘1’: At least one flag int the E-Ray Satuts interrupt register (SIR) is set to “1”. ‘0’: No SIR interrupt flag is set.

Bit	Name	Function
0	ST20	Error interrupt register flag (EIR) ‘1’: At least one flag in the E-Ray Error interrupt register (EIR) is set to “1”. ‘0’: No EIR interrupt flag is set.

Note: STATUS 2 This register shows status of interrupt request(bit6, bit7=0). The status value is changed at falling edge of CSX.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remark
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} –0.3	V_{SS} +6.0	V	*2
Input voltage*1	V_I	V_{SS} –0.3	V_{CC} +0.3	V	
Output voltage*1	V_O	V_{SS} –0.3	V_{CC} +0.3	V	
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum total output current	ΣI_{OL}	—	150	mA	
“L” level average total output current	ΣI_{OLAV}	—	75	mA	*5
“H” level maximum output current	I_{OH}	—	–10	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level maximum total output current	ΣI_{OH}	—	200	mA	
“H” level average total output current	ΣI_{OHAV}	—	100	mA	*5
Power consumption	P_D	—	200	mW	
Storage temperature	T_{STG}	–55	+150	°C	

*1 : The parameter is based on V_{SS} = 0 V.

*2 : V_{CC} must not exceed V_{SS} –0.3 V.

*3 : The maximum output current is defined as the peak value for a single pin.

*4 : The average output current specifies the mean value of the current flowing through one of the corresponding pins over the period of 100 ms.

*5 : The average total output current specifies the mean value of the currents flowing through all of the corre sponding pins over the period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter		Symbol	Value			Unit	Remarks
			Min	Typ	Max		
Supply voltage	External	V_{CC}	4.5	5.0	5.5	V	MB88121, MB88121A
			3.0		5.5	V	MB88121B/C
	-	V_{CC33}	3.0	3.3	3.6	V	MB88121, MB88121A
	Internal	V_{CC18}	1.65	1.8	1.95	V	MB88121, MB88121A
Smoothing capacitor		C_S	1.0* (within tolerance ± 50%)			µF	MB88121B/C
Operating temperature		T_A	–40	—	+ 85	°C	MB88121/A
			–40	—	+105	°C	MB88121B
			–40	—	+125	°C	MB88121C

*Use a ceramic capacitor or a capacitor with similar frequency characteristics.
Use capacitors with a larger capacitance than C_S for the smoothing capacitors on the V_{CC} pins.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application ouside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. Cautions concerning handling the power supply

This section explains cautions concerning the power supply, for example the handling and processing of pins, when turning the power on.

- Turning the power on

It is necessary to perform the setting initialization reset at the RST pin straight after turning the power on. Also, keep "L" level input to the RST pin for the stabilization waiting time requested by the oscillation circuit straight after turning the power on in order to retain the oscillation stabilization waiting time for the PLL oscillation circuit.

- External clock input when turning the power on

Input the external clock before the PLL oscillation stabilization waiting time is released when turning the power on.

4. DC Characteristics

(MB88121/MB88121A: T_A = − 40 °C to + 85 °C, V_{CC} = 5.0 V ±0.5V, V_{CC33} = 3.3 V ±0.3V, V_{CC18} = 1.8 V ±0.15V)
(MB88121B: T_A = − 40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = − 40 °C to + 125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remark
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Pins other than X0, $\overline{RST}$, MDE2 to MDE0, MD2 to MD0	—	V_{CC} × 0.7	—	V_{CC} +0.3	V	With hysteresis
		X0, $\overline{RST}$, MDE2 to MDE0, MD2 to MD0		V_{CC} × 0.8				
"L" level input voltage	V_{IL}	Pins other than X0, $\overline{RST}$, MDE2 to MDE0, MD2 to MD0	—	V_{SS} –0.3	—	V_{CC} × 0.3	V	
		X0, $\overline{RST}$, MDE2 to MDE0, MD2 to MD0				V_{CC} × 0.2		
"H" level output voltage	V_{OH}	—	I_{OH} = –4mA	V_{CC} –0.4	—	V_{CC}	V	
"L" level output voltage	V_{OL}	—	I_{OL} = 4mA	V_{SS}	—	0.4	V	
Power supply current	I_{CC}	—	V_{CC} = 5.0 V	—	—	30	mA	Under operating conditions
Power Con-sumption	W_P	V_{CC}	V_{CC} = 5.0 V	—	120	135	mW	MB88121
		V_{CC}	V_{CC} = 5.0 V	—	120	135	mW	MB88121A
		V_{CC}	V_{CC} = 5.0 V	—	120	135	mW	MB88121B
		V_{CC}	V_{CC} = 5.0 V	—	120	135	mW	MB88121C
		V_{CC}	V_{CC} = 3.3 V	—	67	100	mW	MB88121C

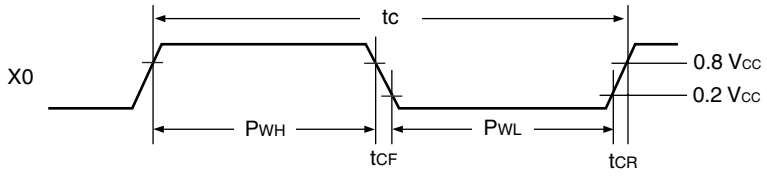
5. AC Characteristics

(1) Input Clock Timing

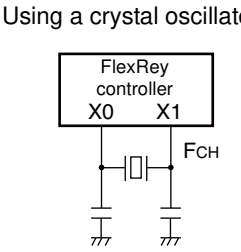
(MB88121/MB88121A: T_A = − 40 °C to + 85 °C, V_{CC} = 5.0 V ±0.5V, V_{CC33} = 3.3 V ±0.3V, V_{CC18} = 1.8 V ±0.15V)
(MB88121B: T_A = − 40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = − 40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remark
				Min	Typ	Max		
Input clock frequency	F_{CH}	X0, X1	At oscillation clock input	4	—	8	MHz	
		X0	At external clock input	4	—	80	MHz	When using an internal PLL 20 MHz Max at SPI mode 10 MHz Max
Input clock cycle time	tc	X0, X1	—	12.5	—	250	ns	
Input clock cycle width	P_{WH}, P_{WL}	X0		4	—	—	ns	When using an external clock, use a duty ratio of 30% to 70% as a guide.
Input clock rise time and fall time	t_{CR}, t_{CF}	X0		—	—	4	ns	When using an external clock

- X0, X1 Clock Timing



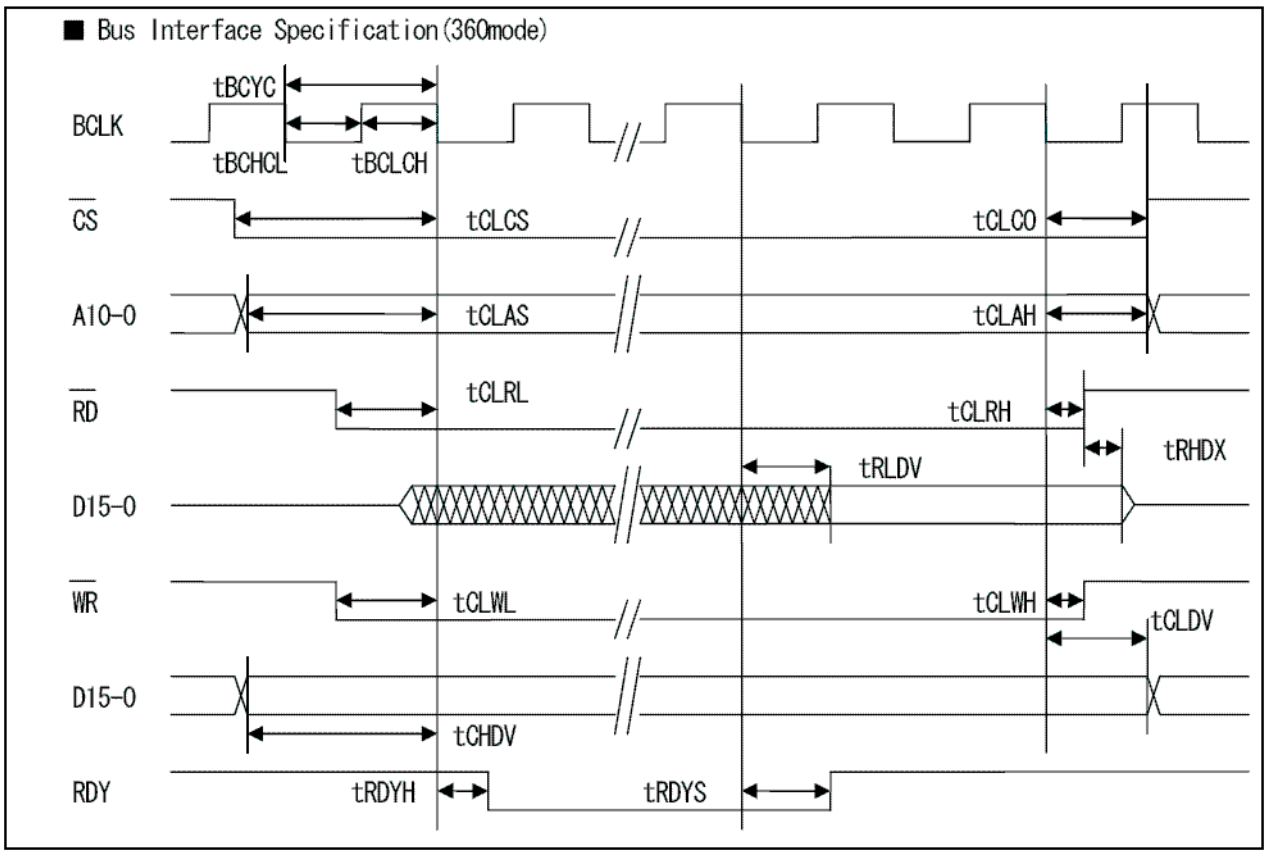
- Clock Input Pin Connection Circuit



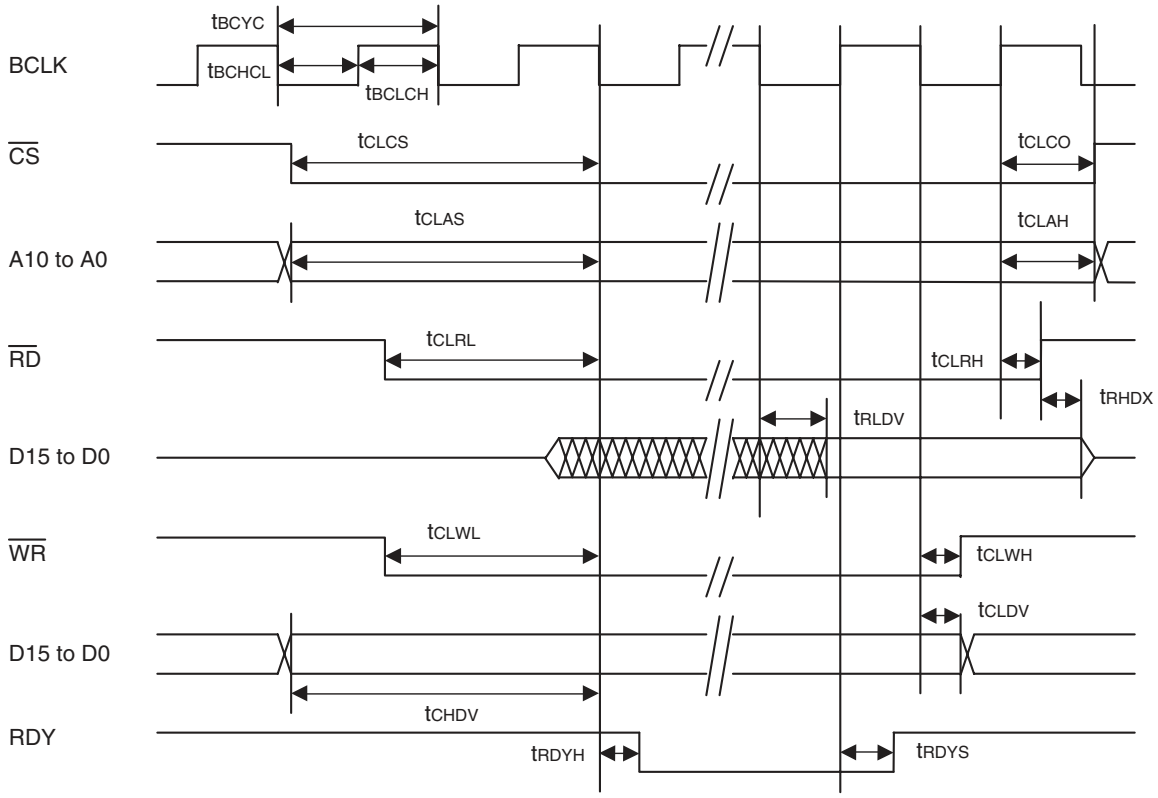
(2) 16 bit non-multiplexed mode

(MB88121/MB88121A: T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±0.5V, V_{CC33} = 3.3 V ±0.3V, V_{CC18} = 1.8 V ±0.15V)
(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

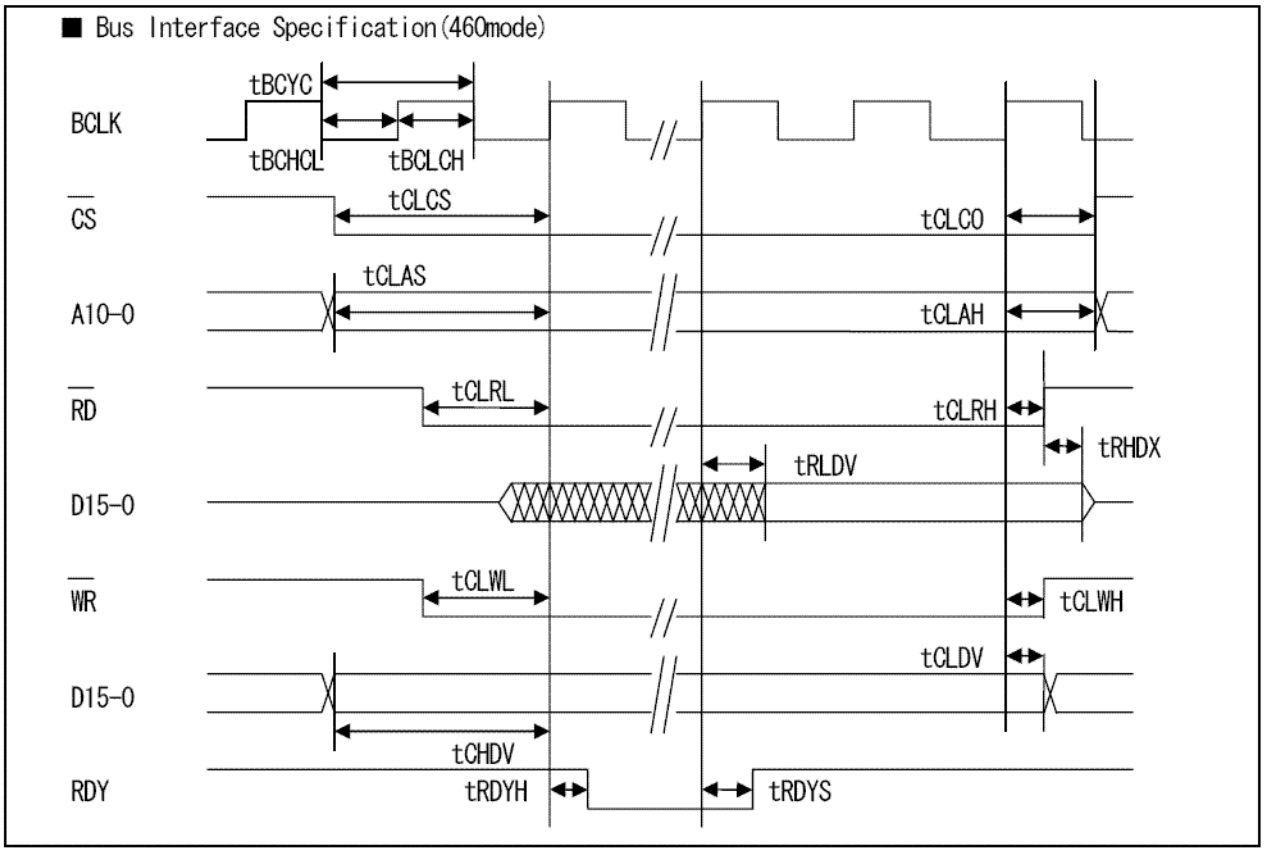
Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Bus Clock Cycle	t_{BCYC}	—	31.25	—	ns
High width of BCLK	t_{BCLCH}	—	5.0	—	ns
Low width of BCLK	t_{BCHCL}	—	5.0	—	ns
System Clock Cycle	t_{SCYC}	MB88121, MB88121A	12.5	100	ns
		MB88121B	100	250	ns
		MB88121C(Oscillator)	125	250	ns
		MB88121C(External Clock Input)	12.5	250	ns
High width of SCLK	t_{SCLCH}	MB88121, MB88121A	4.8	—	ns
		MB88121B	10	—	ns
		MB88121C(Oscillator)	10	—	ns
		MB88121C(External Clock Input)	4.8	—	ns
Low width of SCLK	t_{SCHCL}	MB88121, MB88121A	4.8	—	ns
		MB88121B	10	—	ns
		MB88121C(Oscillator)	10	—	ns
		MB88121C(External Clock Input)	4.8	—	ns
CS setup	t_{CLCS}	—	18.0	—	ns
CS hold	t_{CLCO}	—	0	—	ns
Address setup	t_{CLAS}	—	13.0	—	ns
Address hold	t_{CLAH}	—	0	—	ns
RD setup time	t_{CLRL}	—	14.0	—	ns
RD hold time	t_{CLRH}	—	0	—	ns
Data Valid delay	t_{RLDV}	C_f = 20pF (VCC = 5V)	3.0	19.0	ns
		C_f = 20pF (VCC = 3V)	3.0	30.0	ns
Data Valid hold	t_{RHDX}	C_f = 20pF	3.0	18.5	ns
WR setup time	t_{CLWL}	—	14.0	—	ns
WR hold time	t_{CLWH}	—	0	—	ns
Data setup	t_{CHDV}	—	18.0	—	ns
Data hold	t_{CLDV}	—	0	—	ns
RDY output delay	t_{RDYS}	C_f = 20pF (VCC = 5V)	—	15.4	ns
	t_{RDYS}	C_f = 20pF (VCC = 3V)	—	25.4	ns
RDY output hold	t_{RDYH}	C_f = 20pF	3.0	—	ns
RST input time	t_{RSTL}	—	200.0	—	ns


■ Bus Interface Specification(360mode)
BCLK
tBCYC
tBCHCL
tBCLCH
CS
tCLCS
tCLCO
A10-0
tCLAS
tCLAH
RD
tCLRL
tCLRH
tRHDX
tRLDV
D15-0
WR
tCLWL
tCLWH
tCLDV
D15-0
tCHDV
RDY
tRDYH
tRDYS

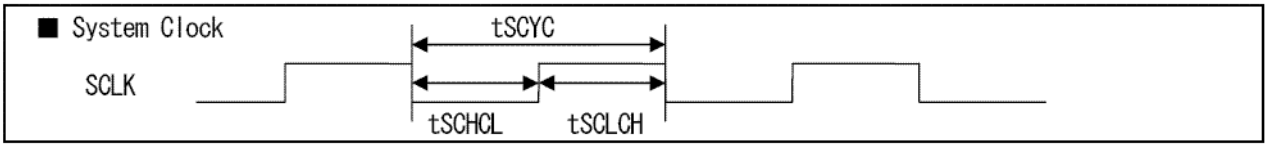
■ 16bit non-multiplexed mode(16fx)



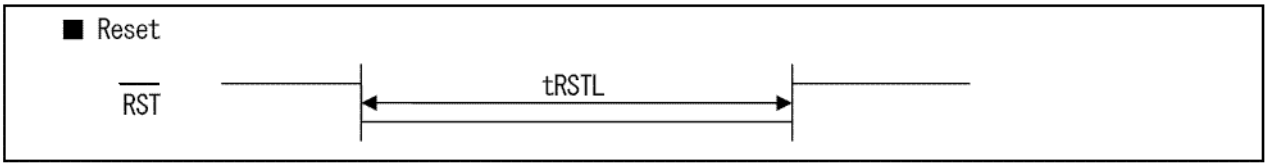
■ Bus Interface Specification(460mode)



■ System Clock



■ Reset

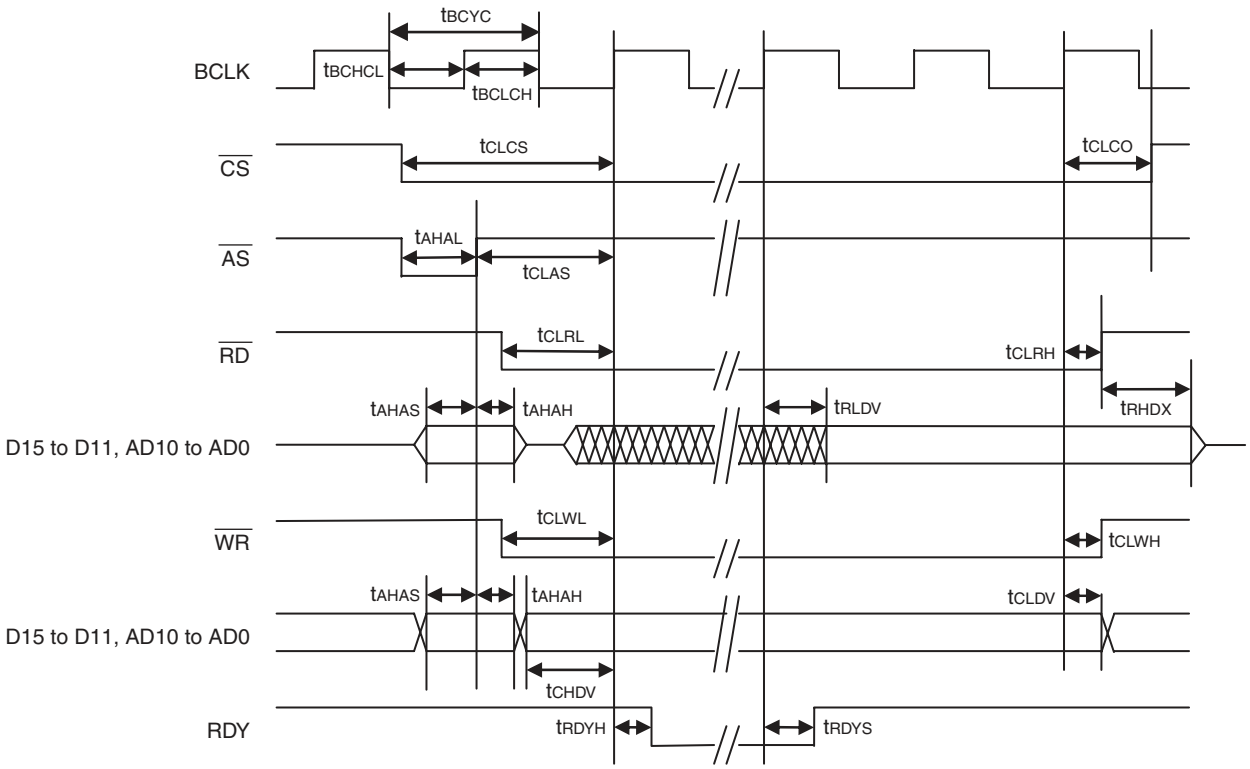


(3) 16 bit multiplexed mode

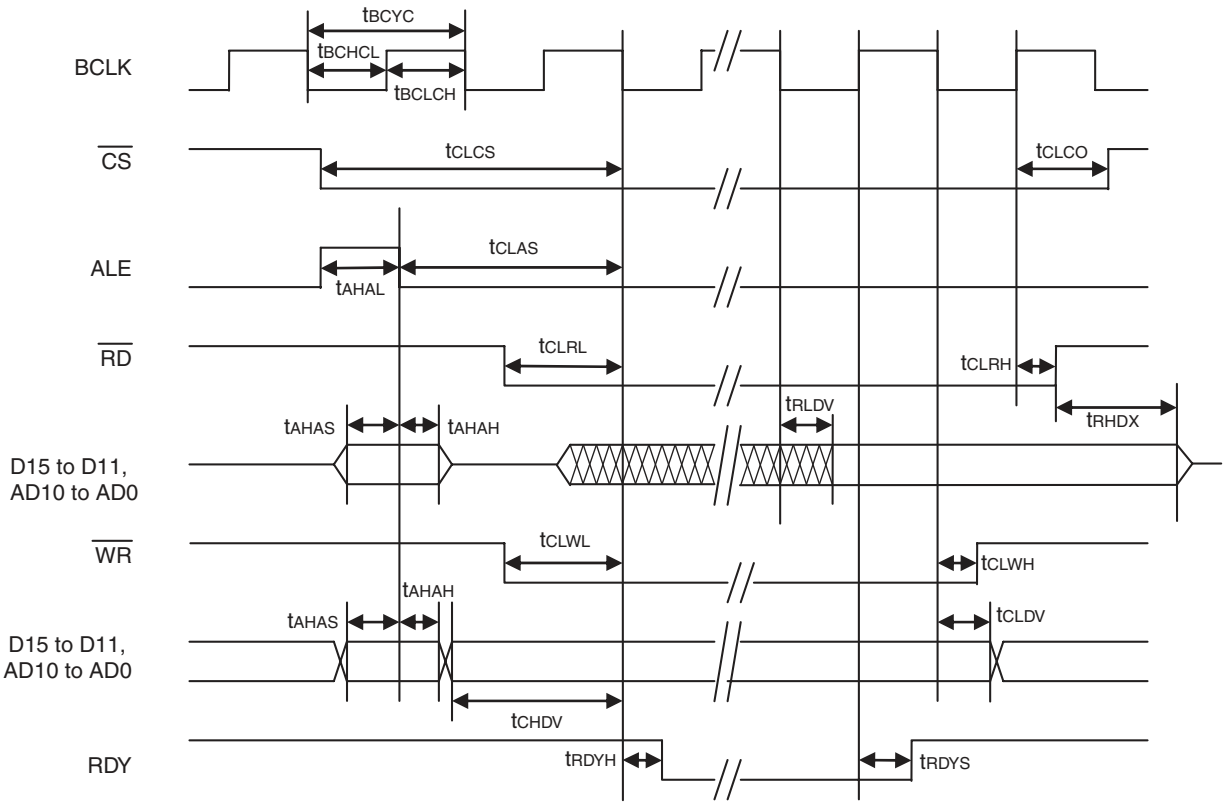
(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Bus Clock Cycle	t_{BCYC}	—	31.25	—	ns
High width of BCLK	t_{BCLCH}	—	5.0	—	ns
Low width of BCLK	t_{BCHCL}	—	5.0	—	ns
System Clock Cycle	t_{SCYC}	MB88121B	100	250	ns
		MB88121C(Oscillator)	125	250	ns
		MB88121C(External Clock Input)	12.5	250	ns
High width of SCLK	t_{SCLCH}	MB88121B	10	—	ns
		MB88121C(Oscillator)	10	—	ns
		MB88121C(External Clock Input)	4.8	—	ns
Low width of SCLK	t_{SCHCL}	MB88121B	10	—	ns
		MB88121C(Oscillator)	10	—	ns
		MB88121C(External Clock Input)	4.8	—	ns
CS setup	t_{CLCS}	—	18.0	—	ns
CS hold	t_{CLCO}	—	0	—	ns
Address setup	t_{AHAS}	—	5.0	—	
Address hold	t_{AHAH}	—	3.0	—	
Address strobe/Latch setup	t_{CLAS}	—	10.0	—	ns
Address strobe/Latch width	t_{CLAH}	—	10.00	—	ns
RD setup time	t_{CLRL}	—	6.0	—	ns
RD hold time	t_{CLRH}	—	0	—	ns
Data Valid delay	t_{RLDV}	C_f = 20pF (VCC = 5V)	3.0	19.0	ns
		C_f = 20pF (VCC = 3V)	3.0	30.0	ns
Data Valid hold	t_{RHDX}	C_f = 20pF	3.0	18.5	ns
WR setup time	t_{CLWL}	—	14.0	—	ns
WR hold time	t_{CLWH}	—	0	—	ns
Data setup	t_{CHDV}	—	18.0	—	ns
Data hold	t_{CLDV}	—	0	—	ns
RDY output delay	t_{RDYS}	C_f = 20pF (VCC = 5V)	—	15.4	ns
	t_{RDYS}	C_f = 20pF (VCC = 3V)	—	25.4	ns
RDY output hold	t_{RDYH}	C_f = 20pF	3.0	—	ns
RST input time	t_{RSTL}	—	200.0	—	ns

■16bit multiplexed mode(460mode)



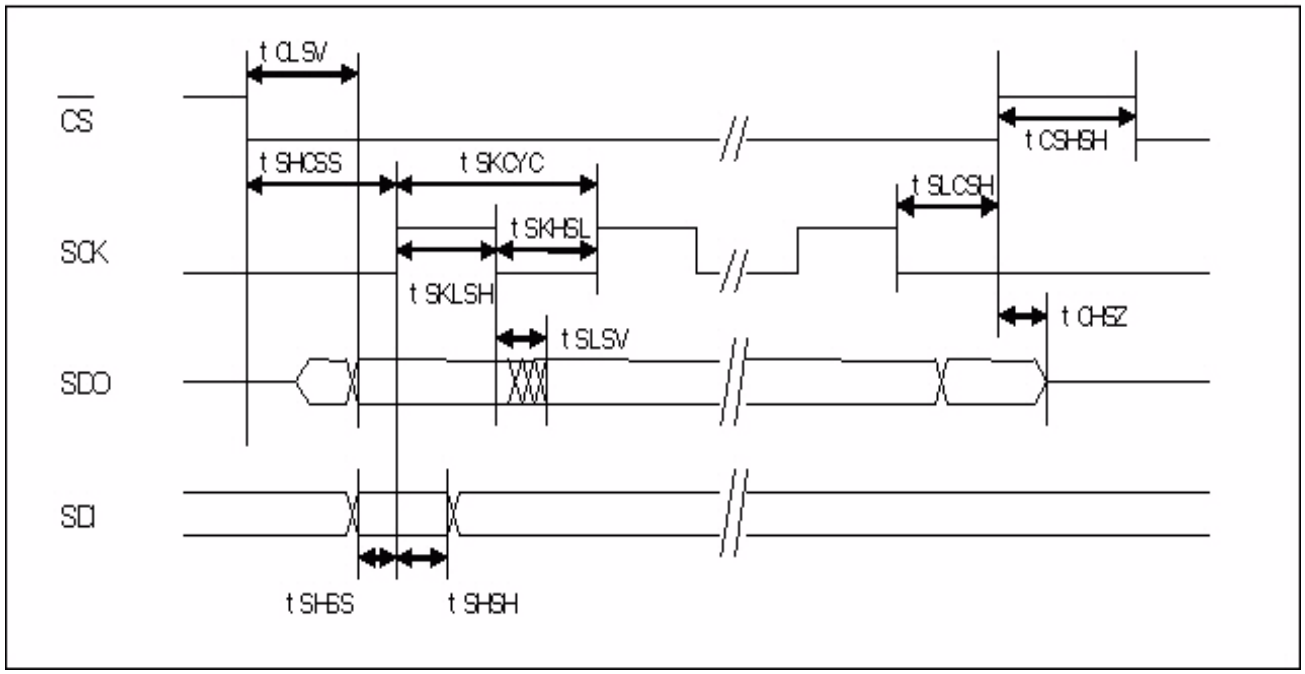
■16bit multiplexed mode(16FX mode)



- SPI mode

MDS1 = 0, MDS0 = 0

(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

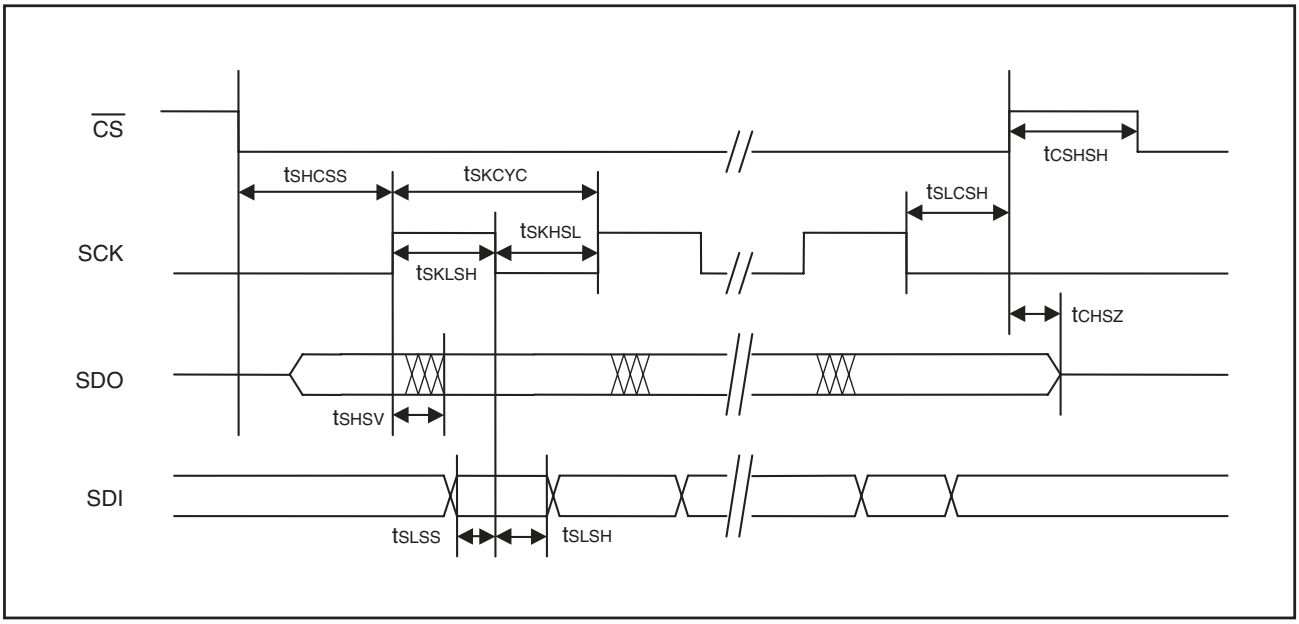


Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Cycle of SCK	t_{SKCYC}	—	6trp	—	ns
			100	—	ns
Low width of SCK	t_{SKHSL}	—	30	—	ns
High width of SCK	t_{SKLSH}	—	30	—	ns
SDO valid delay for CS	t_{CLSV}	C_f = 20pF	—	25	ns
SDO valid delay for SCK	t_{SLSV}		—	20	ns
SDI setup time	t_{SHSS}	—	20	—	ns
SDI hold time	t_{SHSH}	—	20	—	ns
CS setup	t_{SHCSS}	—	30	—	
CS hold time	t_{SLCSH}	—	30	—	
SDO Hi-impedance delay	t_{CHSZ}	—	—	30	ns
CS recovery time	t_{CSHSH}	—	50	—	ns

*1: trp shows the RAM cycle for FlexRay

MDS1 = 0, MDS0 = 1

(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

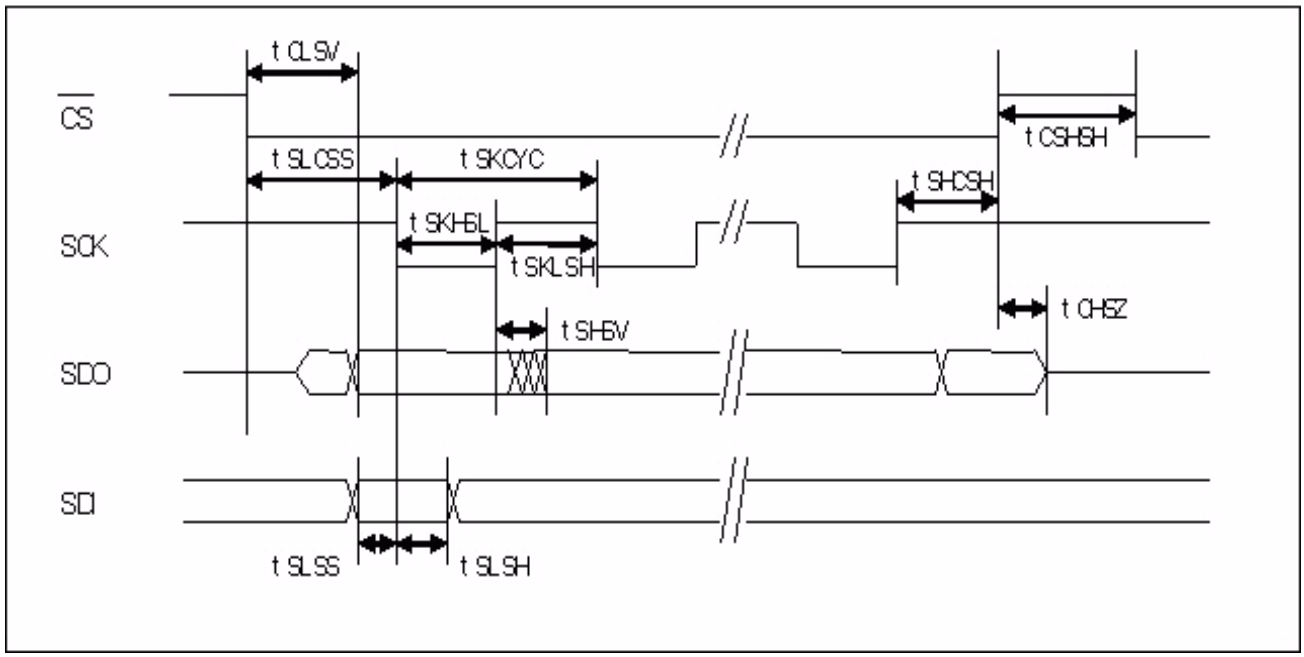


Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Cycle of SCK	t_{SKCYC}	—	6trp	—	ns
			100	—	ns
Low width of SCK	t_{SKHSL}	—	30	—	ns
High width of SCK	t_{SKLSH}	—	30	—	ns
SDO valid delay for SCK	t_{SHSV}	C_f = 20pF	—	20	ns
SDI setup time	t_{SLSS}	—	20	—	ns
SDI hold time	t_{SLSH}	—	20	—	ns
CS setup	t_{SHCSS}	—	30	—	
CS hold time	t_{SLCSH}	—	30	—	
SDO Hi-impedance delay	t_{CHSZ}	—	—	30	ns
CS recovery time	t_{CSHSH}	—	50	—	ns

*1: trp shows the RAM cycle for FlexRay

MDS1 = 1, MDS0 = 0

(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

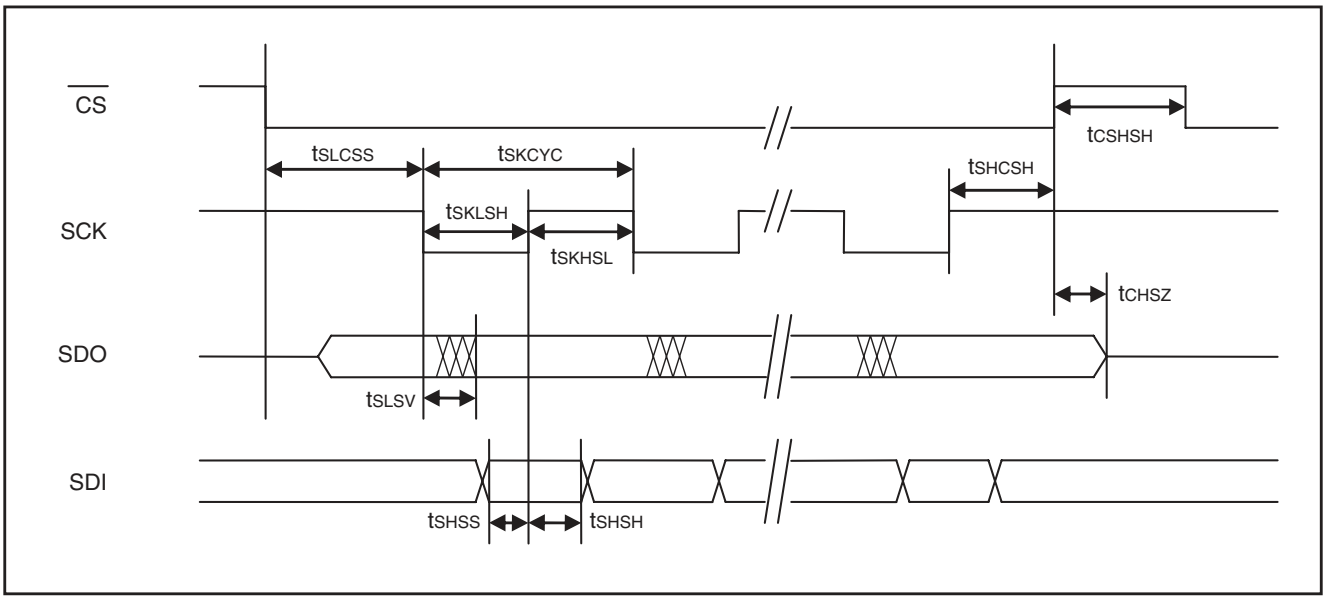


Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Cycle of SCK	t_{SKCYC}	—	6trp	—	ns
			100	—	ns
Low width of SCK	t_{SKHSL}	—	30	—	ns
High width of SCK	t_{SKLSH}	—	30	—	ns
SDO valid delay for CS	t_{CLSV}	C_f = 20pF	—	25	ns
SDO valid delay for SCK	t_{SHSV}		—	20	ns
SDI setup time	t_{SLSS}	—	20	—	ns
SDI hold time	t_{SLSH}	—	20	—	ns
CS setup time	t_{SLCSS}	—	30	—	
CS hold time	t_{SHCSH}	—	30	—	
SDO Hi-impedance delay	t_{CHSZ}	—	—	30	ns
CS recovery time	t_{CSHSH}	—	50	—	ns

*1: trp shows the RAM cycle for FlexRay

MDS1 = 1, MDS0 = 1

(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)



Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Cycle of SCK	t_{SKCYC}	—	6trp	—	ns
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SDI hold time	t_{SHSH}	—	20	—	ns
CS setup	t_{SLCSS}	—	30	—	
CS hold time	t_{SHCSH}	—	30	—	
SDO Hi-impedance delay	t_{CHSZ}	—	—	30	ns
CS recovery time	t_{CSHSH}	—	50	—	ns

*1: trp shows the RAM cycle for FlexRay

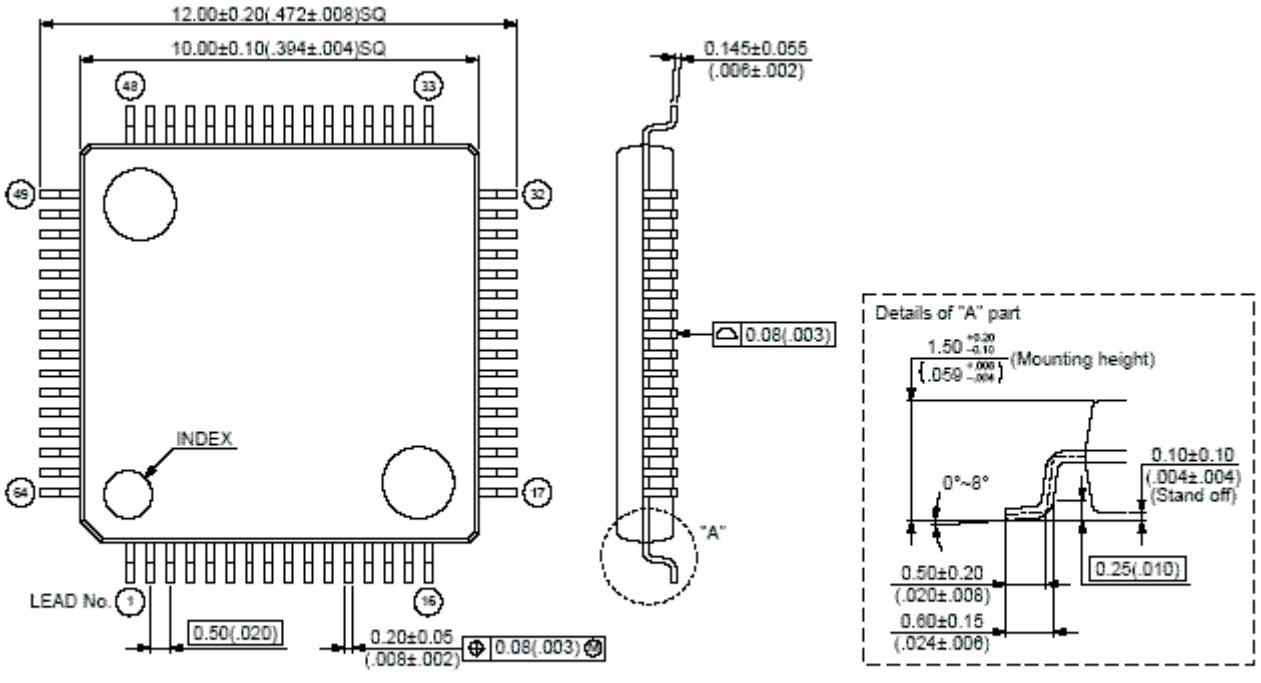
■ ORDERING INFORMATION

Part number	Package	Remarks
MB88121BPFV	64-pin Plastic LQFP (FPT-64P-M03)	ES only
MB88121BPMC1	64-pin Plastic LQFP (FPT-64P-M24)	ES only
MB88121CPMC1	64-pin Plastic LQFP (FPT-64P-M24)	

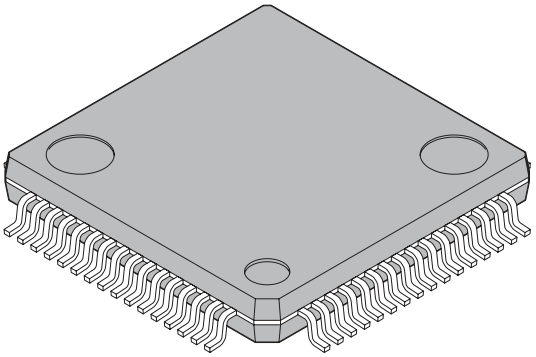
■ PACKAGE DIMENSION

64-pin Plastic LQFP
(FPT-64P-M03)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness including plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

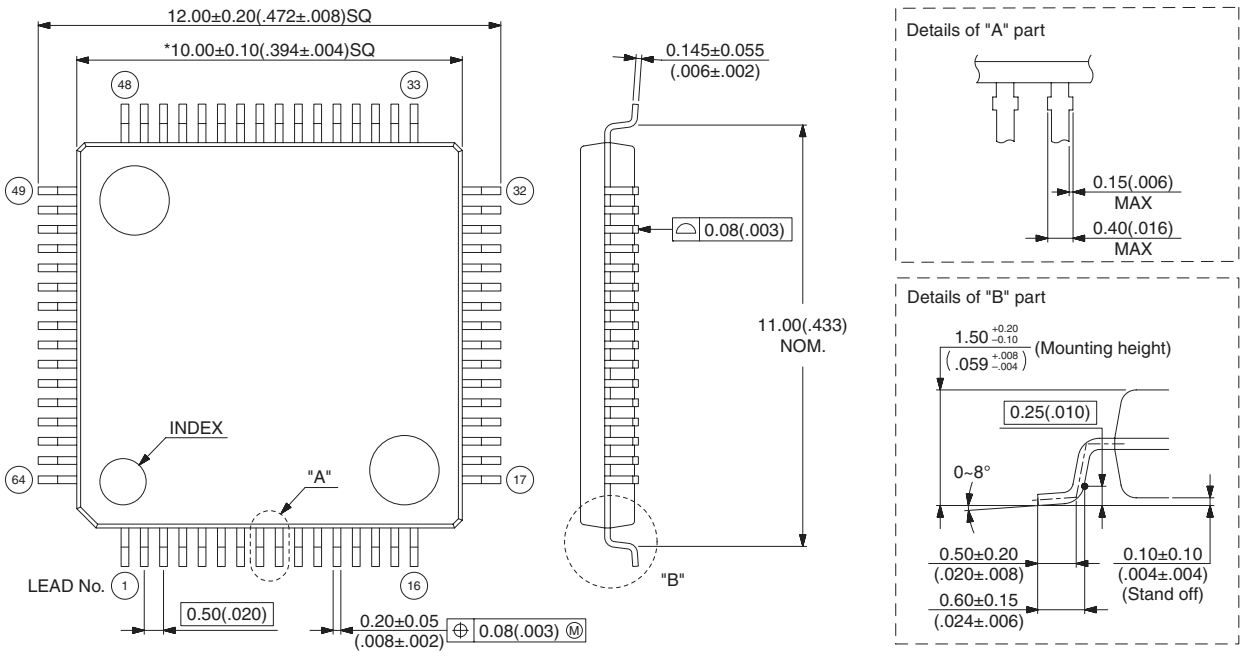


Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

64-pin plastic LQFP		
 (FPT-64P-M24)	Lead pitch	0.50 mm
	Package width × package length	10.0 mm × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

For further information please contact:

FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47,
D-63225 Langen,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu.com/emea/services/microelectronics/

mail: flexray_info@fme.fujitsu.com

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