LOW I_Q, SINGLE-BOOST, FIXED-VOLTAGE DUAL SYNCHRONOUS BUCK CONTROLLER

Check for Samples: TPS43337-Q1

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C2
- Two Synchronous Buck Controllers
- BuckA: Fixed Output Voltage of 3.4 V
- BuckB: Fixed Output Voltage of 1.235 V
- One Pre-Boost Controller
- Input Range up to 40 V, (Transients up to 60 V), Operation Down to 2 V When Boost Is Enabled
- Low-Power Mode I_Q: 34 µA (One Buck On), 43 µA (Two Bucks On)
- Low Shutdown Current I_{sh} < 4 µA
- Boost Output Selectable: 7 V, 8.85 V, or 10 V
- Programmable Frequency and External Synchronization Range: 150 to 600 kHz
- Separate Enable Inputs (ENA, ENB, ENC)
- Selectable Forced Continuous Mode or Automatic Low-Power Mode at Light Loads
- Sense Resistor or Inductor DCR Sensing for Buck Controllers
- Out-of-Phase Switching Between Buck Channels
- Peak Gate Drive Current 1.5 A
- Thermally Enhanced 38-Pin HTSSOP (DAP) PowerPAD™ Package

APPLICATIONS

- Automotive Start-Stop, Infotainment, Navigation Instrument Cluster Systems
- Industrial and Automotive Multi-Rail DC Power-Distribution Systems and Electronic Control Units

DESCRIPTION

The TPS43337-Q1 includes two current-mode synchronous buck controllers and a voltage-mode boost controller. The device is ideally suited as a pre-regulator stage with low I_Q requirements and for systems that must survive supply drops due to cranking events. The integrated boost controller allows the device to operate down to 2 V at the input without seeing a drop on the buck regulator output stages. At light loads, the buck controllers enable to operate automatically in low power-mode, consuming just 34 µA of quiescent current.

The buck controllers have independent soft-start capability and power-good indicators. Current foldback in the buck controllers and cycle-by-cycle current limitation in the boost controller provide external MOSFET protection. The switching frequency is programable over 150 to 600 kHz or is synchronized to an external clock in the same range

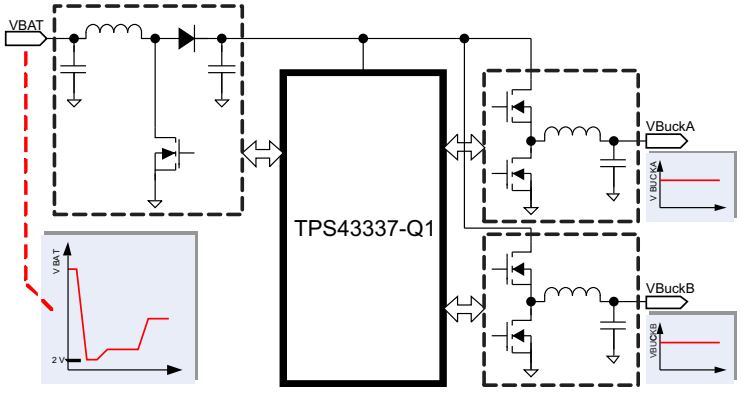

Figure 1. Typical Application Diagram

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

			MIN	MAX	UNIT
Voltage	Input voltage: VIN, VBAT		–0.3	60	V
Voltage (buck function: BuckA and BuckB)	Enable inputs: ENA, ENB		–0.3	60	V
	Bootstrap inputs: CBA, CBB		–0.3	68	V
	Phase inputs: PHA, PHB		–0.7	60	V
	Phase inputs: PHA, PHB (for 150 ns)		–1		V
	Feedback inputs: FBA, FBB		–0.3	13	V
	Error amplifier outputs: COMPA, COMPB		–0.3	13	V
	High-side MOSFET driver: GA1–PHA, GB1–PHB		–0.3	8.8	V
	Low-side MOSFET drivers: GA2, GB2		–0.3	8.8	V
	Current-sense voltage: SA1, SA2, SB1, SB2		–0.3	13	V
	Soft start: SSA, SSB		–0.3	13	V
	Power-good output: PGA, PGB		–0.3	13	V
	Power-good delay: DLYAB		–0.3	13	V
	Switching-frequency timing resistor: RT		–0.3	13	V
	SYNC, EXTSUP		–0.3	13	V
Voltage (boost function)	Low-side MOSFET driver: GC1		–0.3	8.8	V
	Error amplifier output: COMPC		–0.3	13	V
	Enable input: ENC		–0.3	13	V
	Current-limit sense: DS		–0.3	60	V
	Output-voltage select: DIV		–0.3	8.8	V
Voltage (PMOS driver)	P-channel MOSFET driver: GC2		–0.3	60	V
	P-channel MOSFET driver: VIN–GC2		–0.3	8.8	V
	Gate-driver supply: VREG		–0.3	8.8	V
Temperature	Junction temperature: T_J		–40	150	°C
	Operating temperature: T_A		–40	125	°C
	Storage temperature: T_S		–55	165	°C
Electrostatic discharge ratings	Human-body model (HBM) AEC-Q100 Classification Level H2		±2		kV
	Charged-device model (CDM) AEC-Q100 Classification Level C2	VBAT, ENC, SYNC, VIN	±750		V
		All other pins	±500		
	Machine model (MM)	PGA, PGB	±150		
		All other pins	±200		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.

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THERMAL INFORMATION

THERMAL METRIC(1)		TPS43337-Q1 HTSSOP-DAP 38 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	27.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	19.6	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	15.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.24	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	6.6	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Buck function: BuckA and BuckB voltage	Input voltage: VIN, VBAT	4	40	V
	Enable inputs: ENA, ENB	0	40	
	Boot inputs: CBA, CBB	4	48	
	Phase inputs: PHA, PHB	–0.6	40	
	Current-sense voltage: SA1, SA2, SB1, SB2	0	11	
	Power-good output: PGA, PGB	0	11	
	SYNC, EXTSUP	0	9	
Boost function	Enable input: ENC	0	9	V
	Voltage sense: DS		40	
	DIV	0	VREG	
	Operating Temperature: T_A	–40	125	°C

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DC ELECTRICAL CHARACTERISTICS

VIN = 8 to 18 V, T_J = –40°C to +150°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.0	**Input Supply**						
1.1	V_{BAT}	Supply voltage	Boost controller enabled, after initial start-up condition is satisfied	2		40	V
1.2	V_{IN}	Input voltage required for device on initial start-up		6.5		40	V
		Buck regulator operating range after initial start-up		4		40	
1.3	$V_{IN\ UV}$	Buck undervoltage lockout	V_{IN} falling. After a reset, initial start-up conditions may apply.(1)	3.5	3.6	3.8	V
			V_{IN} rising. After a reset, initial start-up conditions may apply.(1)		3.8	4	V
1.4	V_{BOOST_UNLOCK}	Boost unlock threshold	V_{BAT} rising	8.2	8.5	8.8	V
1.5	I_{Q_LPM}	LPM quiescent current:(2)	V_{IN} = 13 V, BuckA: LPM, BuckB: off, T_A = 25°C		34	46	µA
			V_{IN} = 13 V, BuckB: LPM, BuckA: off, T_A = 25°C				
			V_{IN} = 13 V, BuckA, B: LPM, T_A = 25°C		43	57	µA
1.6	I_{Q_LPM}	LPM quiescent current:(2)	V_{IN} = 13 V, BuckA: LPM, BuckB: off, T_A = 125°C		44	56	µA
			V_{IN} = 13 V, BuckB: LPM, BuckA: off, T_A = 125°C				
			V_{IN} = 13 V, BuckA and BuckB: LPM, T_A = 125°C		53	67	µA
1.7	I_{Q_NRM}	Quiescent current: normal (PWM) mode(2)	SYNC = 5 V, T_A = 25°C				mA
			V_{IN} = 13 V, BuckA: CCM, BuckB: off, T_A = 25°C		4.85	5.3	
			V_{IN} = 13 V, BuckB: CCM, BuckA: off, T_A = 25°C				
			V_{IN} = 13 V, BuckA and BuckB: CCM, T_A = 25°C		7	7.6	
1.8	I_{Q_NRM}	Quiescent current: normal (PWM) mode(2)	SYNC = 5 V, T_A = 125°C				mA
			V_{IN} = 13 V, BuckA: CCM, BuckB: off, T_A = 125°C		5	5.5	
			V_{IN} = 13 V, BuckB: CCM, BuckA: off, T_A = 125°C				
			V_{IN} = 13 V, BuckA, B: CCM, T_A = 125°C		7.5	8	
1.9	I_{bat_sh}	Shutdown current	BuckA and BuckB: off, VBat = 13 V , T_A = 25°C		2.5	4	µA
1.10	I_{bat_sh}	Shutdown current	BuckA and BuckB: off, VBat = 13 V, T_A = 125°C		3	5	µA
1.11	$VIN_{LPMexit}$	VIN level to exit LPM	V_{IN} falling	7.7	8	8.3	V
1.12	$VIN_{LPMentry}$	VIN level to enable entering LPM	V_{IN} rising	8.2	8.5	8.8	V
1.13	VIN_{LPMhys}	Hysteresis	V_{IN} rising or falling	0.4	0.5	0.6	V
2.0	**Input Voltage V_{BAT} - Undervoltage Lockout**						
2.1	V_{BATUV}	Boost-input undervoltage	V_{BAT} falling. After a reset, initial start-up conditions may apply.(1)	1.8	1.9	2	V
			V_{BAT} rising. After a reset, initial start-up conditions may apply.(1)	2.4	2.5	2.6	V
2.2	$UVLO_{Hys}$	Hysteresis		500	600	700	mV
2.3	$UVLO_{filter}$	Filter time			5		µs
3.0	**Input Voltage V_{IN} - Overvoltage Lockout**						
3.1	V_{OVLO}	Overvoltage shutdown	V_{IN} rising	45	46	47	V
			V_{IN} falling	43	44	45	
3.2	$OVLO_{Hys}$	Hysteresis		1	2	3	V
3.3	$OVLO_{filter}$	Filter time			5		µs

(1) If VBAT and VREG remain adequate, the buck can continue to operate if VIN is > 3.8 V.
(2) Quiescent current specification includes the current in the internal-feedback resistor divider.

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DC ELECTRICAL CHARACTERISTICS (continued)

VIN = 8 to 18 V, T_J = –40°C to +150°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.0	**Boost Controller**						
4.1	$V_{boost7\text{-}VIN}$	Boost V_{OUT} = 7 V	DIV = low, V_{BAT} = 2 to 7 V	6.8	7	7.3	V
4.2	$V_{boost7\text{-}th}$	Boost-enable threshold	Boost V_{OUT} = 7 V, V_{BAT} falling	7.5	8	8.5	V
		Boost-disable threshold	Boost V_{OUT} = 7 V, V_{BAT} rising	8	8.5	9	
		Boost hysteresis	Boost V_{OUT} = 7 V, V_{BAT} rising or falling	0.4	0.5	0.6	
4.3	$V_{boost10\text{-}VIN}$	Boost V_{OUT} = 10 V	DIV = open, V_{BAT} = 2 to 10 V	9.7	10	10.4	V
4.4	$V_{boost10\text{-}th}$	Boost-enable threshold	Boost V_{OUT} = 10 V, V_{BAT} falling	10.5	11	11.5	V
		Boost-disable threshold	Boost V_{OUT} = 10 V, V_{BAT} rising	11	11.5	12	
		Boost hysteresis	Boost V_{OUT} = 10 V, V_{BAT} rising or falling	0.4	0.5	0.6	
4.5	$V_{boost8.85\text{-}VIN}$	Boost V_{OUT} = 8.85 V	DIV = V_{REG}, V_{BAT} = 2 to 8.85 V	8.35	8.85	9.35	V
4.6	$V_{boost8.85\text{-}th}$	Boost-enable threshold	Boost V_{OUT} = 8.85 V, V_{BAT} falling	9.15	9.85	10.45	V
		Boost-disable threshold	Boost V_{OUT} = 8.85 V, V_{BAT} rising	9.65	10.35	10.85	
		Boost hysteresis	Boost V_{OUT} = 8.85 V, V_{BAT} rising or falling	0.4	0.5	0.6	
	Boost-Switch Current Limit						
4.7	V_{DS}	Current-limit sensing	DS input with respect to PGNDA	0.175	0.2	0.225	V
4.8	t_{DS}	Leading-edge blanking			200		ns
	Gate Driver for Boost Controller						
4.9	$I_{GC1\ Peak}$	Gate-driver peak current			1.5		A
4.10	$r_{DS(on)}$	Source and sink driver	V_{REG} = 5.8 V, IGC1 current = 200 mA			2	Ω
	Gate Driver for PMOS						
4.11	$r_{DS(on)}$	PMOS OFF			10	20	Ω
4.12	I_{PMOS_ON}	Gate current	V_{IN} = 13.5 V, Vgs = –5 V	10			mA
4.13	t_{delay_ON}	Turnon delay	C = 10 nF		5	10	µs
	Boost-Controller Switching Frequency						
4.14	$f_{sw\text{-}Boost}$	Boost switching frequency				f_{SW_Buck} / 2	kHz
4.15	D_{Boost}	Boost duty cycle				90%	
	Error Amplifier (OTA) for Boost Converters						
4.16	Gm_{BOOST}	Forward transconductance	V_{BAT} = 12 V	0.8		1.35	mS
			V_{BAT} = 5 V	0.35		0.65	
5.0	**Buck Controllers**						
5.1a	V_{BuckA_NRM}	Fixed output voltage in normal mode	Included resistor-feedback-divider, measured at FBA pin	3.345	3.396	3.447	V
5.1b	V_{BuckA_LPM}	Fixed output in low-power mode		3.311	3.396	3.481	
5.2a	V_{BuckB_NRM}	Fixed output voltage in normal mode	Included resistor-feedback-divider, measured at FBB pin	1.216	1.235	1.253	V
5.2b	V_{BuckB_LPM}	Fixed output voltage in low-power mode		1.204	1.235	1.266	
5.4	V_{sense}	V sense for forward-current limit in CCM	Measured across Sx1 and Sx2, FBx at 94% of typical value (low duty-cycle)	60	75	90	mV
5.5		V sense for reverse-current limit in CCM	Measured across Sx1 and Sx2, FBx at 125% of typical value	–65	–37.5	–23	mV
5.6	$V_{I\text{-}Foldback}$	V sense for output short	Measured across Sx1 and Sx2, FBx = 0 V	17	32.5	48	mV
5.7	t_{dead}	Shoot-through delay, blanking time			20		ns
5.8	DC_{NRM}	High-side minimum on-time			100		ns
		Maximum duty cycle (digitally controlled)			98.75%		
5.9	DC_{LPM}	Duty cycle, LPM				80%	

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DC ELECTRICAL CHARACTERISTICS (continued)

VIN = 8 to 18 V, T_J = –40°C to +150°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.10	I_{LPM_Entry}	LPM entry-threshold load current as fraction of maximum set load current			1%	(3)	
	I_{LPM_Exit}	LPM exit-threshold load current as fraction of maximum set load current		(3)	10%		
	High-Side External NMOS Gate Drivers for Buck Controller						
5.11	I_{GX1_peak}	Gate-driver peak current			1.5		A
5.12	$r_{DS(on)}$	Source and sink driver	V_{REG} = 5.8 V, I_{GX1} current = 200 mA			2	Ω
	Low-Side NMOS Gate Drivers for Buck Controller						
5.13	I_{GX2_peak}	Gate driver peak current			1.5		A
5.14	$R_{DS\ ON}$	Source and sink driver	V_{REG} = 5.8 V, I_{GX2} current = 200 mA			2	Ω
	Error Amplifier (OTA) for Buck Converters						
5.15	Gm_{BUCK}	Transconductance	COMPA, COMPB = 0.8 V, source/sink = 5 µA, test in feedback loop	0.72	1	1.35	mS
6.0	**Digital Inputs: ENA, ENB, ENC, SYNC**						
6.1	V_{IH}	Higher threshold	V_{IN} = 13 V	1.7			V
6.2	V_{IL}	Lower threshold	V_{IN} = 13 V			0.7	V
6.3	R_{IH_SYNC}	Pulldown resistance on SYNC	V_{SYNC} = 5 V		500		kΩ
6.4	R_{IL_ENC}	Pulldown resistance on ENC	V_{ENC} = 5 V		500		kΩ
6.5	I_{IL_ENx}	Pullup current source on ENA, ENB	V_{ENx} = 0 V		0.5	2	µA
7.0	**Boost Output Voltage: DIV**						
7.1	V_{IH_DIV}	Higher threshold	V_{REG} = 5.8 V	Vreg – 0.2			V
7.2	V_{IL_DIV}	Lower threshold				0.2	V
7.3	V_{oz_DIV}	Voltage on DIV if unconnected	Voltage on DIV if unconnected		Vreg / 2		V
8.0	**Switching Parameter – Buck DC-DC Controllers**						
8.1	f_{SW_Buck}	Buck switching frequency	RT pin: GND	360	400	440	kHz
8.2	f_{SW_Buck}	Buck switching frequency	RT pin: 60-kΩ external resistor	360	400	440	kHz
8.3	f_{SW_adj}	Buck adjustable range with external resistor	RT pin: external resistor	150		600	kHz
8.4	f_{SYNC}	Buck synchronization range	External clock input	150		600	kHz
9.0	**Internal Gate-Driver Supply**						
9.1	V_{REG}	Internal regulated supply	V_{IN} = 8 to 18 V, V_{EXTSUP} = 0 V, SYNC = high	5.5	5.8	6.1	V
		Load regulation	I_{VREG} = 0 to 100 mA, V_{EXTSUP} = 0 V, SYNC = high		0.2%	1%	
9.2	$V_{REG(EXTSUP)}$	Internal regulated supply	V_{EXTSUP} = 8.5 V	7.2	7.5	7.8	V
		Load regulation	I_{EXTSUP} = 0 to 125 mA, SYNC = High V_{EXTSUP} = 8.5 to 13 V		0.2%	1%	
9.3	$V_{EXTSUP\text{-}th}$	EXTSUP switch-over voltage threshold	I_{VREG} = 0 to 100 mA, V_{EXTSUP} ramping positive	4.4	4.6	4.8	V
9.4	$V_{EXTSUP\text{-}Hys}$	EXTSUP switch-over hysteresis		150		250	mV
9.5	$I_{REG\text{-}Limit}$	Current limit on VREG	V_{EXTSUP} = 0 V, normal mode as well as LPM	100		400	mA
9.6	$I_{REG\_EXTSUP\text{-}Limit}$	Current limit on VREG when using EXTSUP	I_{VREG} = 0 to 100 mA, V_{EXTSUP} = 8.5 V, SYNC = High	125		400	mA
10.0	**Soft Start**						
10.1	I_{SSx}	Soft-start source current	V_{SSA} and V_{SSB} = 0 V	40	50	60	µA
11.0	**Oscillator (RT)**						
11.1	V_{RT}	Oscillator reference voltage			1.2		V

(3) The exit threshold specification must always higher than the entry threshold.

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DC ELECTRICAL CHARACTERISTICS (continued)

VIN = 8 to 18 V, T_J = –40°C to +150°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
12.0	**Power Good / Delay**						
12.1a	PG_{thA}	Power-good threshold	FBA falling	3.09	3.158	3.226	V
12.1b	PG_{thB}		FBB falling	1.124	1.148	1.173	
12.2	PG_{hys}	Hysteresis			2%		
12.3	PG_{drop}	Voltage drop	I_{PGA} = 5 mA			450	mV
12.4			I_{PGA} = 1 mA			100	mV
12.5	PG_{leak}	Power-good leakage	Sx2 = PGx = 13 V			1	µA
12.6	$t_{deglitch}$	Power-good deglitch time		2		16	µs
12.7	t_{delay}	Reset delay	External capacitor = 1 nF $V_{BUCKx} < PG_{thx}$		1		ms
12.8	t_{delay_fix}	Fixed reset delay	No external capacitor, pin open		20	50	µs
12.9	I_{OH}	Activate current source (current to charge external capacitor)		30	40	50	µA
12.10	I_{IL}	Activate current sink (current to discharge external capacitor)		30	40	50	µA
13.0	**Overtemperature Protection**						
13.1	$T_{shutdown}$	Junction-temperature shutdown threshold		150	165		°C
13.2	T_{hys}	Junction-temperature hysteresis			15		°C

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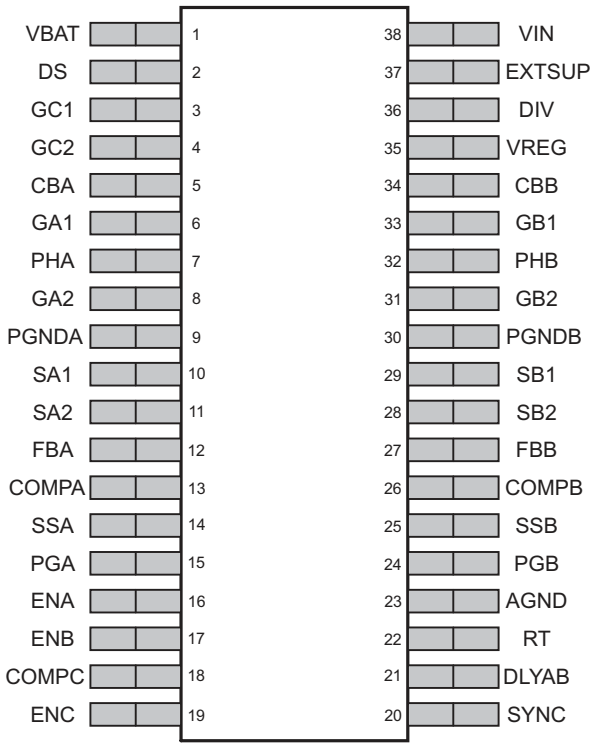
DEVICE INFORMATION

DAP PACKAGE
(TOP VIEW)



PIN FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
AGND	23	O	Analog ground reference
CBA	5	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckA. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
CBB	34	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckB. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
COMPA	13	O	Error-amplifier output of BuckA and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of BuckA. Clamping this voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.
COMPB	26	O	Error-amplifier output of BuckB and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of BuckB. Clamping this voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.
COMPC	18	O	Error-amplifier output and loop-compensation node of the boost regulator
DIV	36	I	The status of this pin defines the output voltage of the boost regulator. A high input regulates the boost converter at 8.85 V, a low input sets the value at 7 V, and a floating pin sets 10 V.
DLYAB	21	O	The capacitor at the DLYAB pin sets the power-good delay interval used to de-glitch the outputs of the power-good comparators. Leaving this pin open sets the power-good delay to an internal default value of 20 µs, typical.
DS	2	I	This input monitors the voltage on the external boost-converter low-side MOSFET for overcurrent protection. An alternative connection for better noise immunity is to place a sense resistor between the source of the low-side MOSFET and ground via a filter network.
ENA	16	I	Enable inputs for BuckA (active-high with an internal pullup current source). An input voltage higher than 1.5 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller. When both ENA and ENB are low, the device shuts down and consumes less than 4 µA of current.

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PIN FUNCTIONS (continued)

NAME	NO.	I/O	DESCRIPTION
ENB	17	I	Enable inputs for BuckB (active-high with an internal pullup current source). An input voltage higher than 1.5 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller. When both ENA and ENB are low, the device shuts down and consumes less than 4 µA of current.
ENC	19	I	This input enables and disables the boost regulator. An input voltage higher than 1.5 V enables the controller. Voltages lower than 0.7 V disable the controller. When enabled, the controller starts switching as soon as VBAT falls below the boost threshold, depending upon the programmed output voltage.
EXTSUP	37	I	One uses EXTSUP to supply the VREG regulator from one of the TPS43337-Q1 buck regulator rails to reduce power dissipation in cases where there is an expectation of high VIN. When EXTSUP is open or lower than 4.6 V, the regulator power comes from VIN.
FBA	12	I	Feedback voltage pin for BuckA. The buck controller regulates this feedback voltage to 3.4 V through the internal resistor-divider network. Connect FBA to the output voltage of BuckA.
FBB	27	I	Feedback voltage pin for BuckB. The buck controller regulates this feedback voltage to 1.235 V through the internal resistor-divider network. Connect FBB to the output voltage of BuckB.
GA1	6	O	This output drives an external high-side N-channel MOSFET for buck regulator BuckA. The output provides high peak currents to drive capacitive loads. The gate-drive reference is to a floating ground provided by PHA that has a voltage swing provided by CBA.
GA2	8	O	This output drives an external high-side N-channel MOSFET for buck regulator BuckA. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GB1	33	O	This output drives an external high-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. The gate-drive reference is to a floating ground provided by PHB that has a voltage swing provided by CBB.
GB2	31	O	This output drives an external high-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GC1	3	O	This output drives an external low-side N-channel MOSFET for the boost regulator. This output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GC2	4	O	This pin makes a floating output drive available to control the external P-channel MOSFET. This MOSFET bypasses the boost rectifier diode or a reverse-protection diode when the boost status is non-switching or disabled, and thus reduces power losses.
PGA	15	O	Open-drain power-good indicator pin for BuckA. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls below 93% of the set value, or if either VIN or VBAT drops below the respective undervoltage threshold.
PGB	24	O	Open-drain power-good indicator pin for BuckB. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls below 93% of the set value, or if either VIN or VBAT drops below the respective undervoltage threshold.
PGNDA	9	O	Power-ground connection to the source of the low-side N-channel MOSFETs of BuckA.
PGNDB	30	O	Power-ground connection to the source of the low-side N-channel MOSFETs of BuckB.
PHA	7	O	Switching terminal of buck regulator BuckA; provides a floating ground reference for the high-side MOSFET gate-driver circuitry and senses current reversal in the inductor when discontinuous-mode operation is desired.
PHB	32	O	Switching terminal of buck regulator BuckB; provides a floating ground reference for the high-side MOSFET gate-driver circuitry and senses current reversal in the inductor when discontinuous-mode operation is desired.
RT	22	O	Connecting a resistor to ground on this pin sets the operating switching frequency of the buck and boost controllers. A short circuit to ground on this pin defaults operation to 400 kHz for the buck controllers and 200 kHz for the boost controller.
SA1	10	I	High-impedance differential-voltage inputs from the current-sense element (sense resistor or inductor DCR) for each buck controller. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and VIN. (SA1 positive node, SA2 negative node)
SA2	11	I	
SB1	29	I	High-impedance differential voltage inputs from the current-sense element (sense resistor or inductor DCR) for each buck controller. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and VIN. (SB1 positive node, SB2 negative node)
SB2	28	I	
SSA	14	O	Soft-start or tracking input for buck controller BuckA. The buck controller regulates the FBA voltage to the lower of 0.8 V or the SSA pin voltage. An internal pullup current source of 50 µA is present at the pin. Connect an appropriate capacitor here to set the soft-start ramp interval, or connect a resistor divider connected to another supply to provide a tracking input to this pin.
SSB	25	O	Soft-start or tracking input for buck controller BuckB. The buck controller regulates the FBA voltage to the lower of 0.8 V or the SSA pin voltage. An internal pullup current source of 50 µA is present at the pin. Connect an appropriate capacitor here to set the soft-start ramp interval, or connect a resistor divider connected to another supply to provide a tracking input to this pin.

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PIN FUNCTIONS (continued)

NAME	NO.	I/O	DESCRIPTION
SYNC	20	I	If an external clock is present on this pin, the device detects it, and the internal PLL locks on to the external clock. This overrides the internal oscillator frequency. The device can synchronize to frequencies from 150 kHz to 600 kHz. A high logic level on this pin ensures forced continuous-mode operation of the buck controllers and inhibits transition to low-power mode. An open or low allows discontinuous-mode operation and entry into low-power mode at light loads.
VBAT	1	I	Battery input sense for the boost controller. With the boost controller enabled, if the voltage at VBAT falls below the boost threshold, the device activates the boost controller and regulates the voltage at VIN to the programmed boost output voltage.
VIN	38	I	Main input pin. This is the buck controller input pin as well as the output of the boost regulator. Additionally, VIN powers the internal control circuits of the device.
VREG	35	O	This pin requires an external capacitor to provide a regulated supply for the gate drivers of the buck and boost controllers. TI recommends a capacitance on the order of 4.7 µF. Either VIN or EXTSUP can power the regulator. This pin has current-limit protection, so do not use it to drive any other loads.

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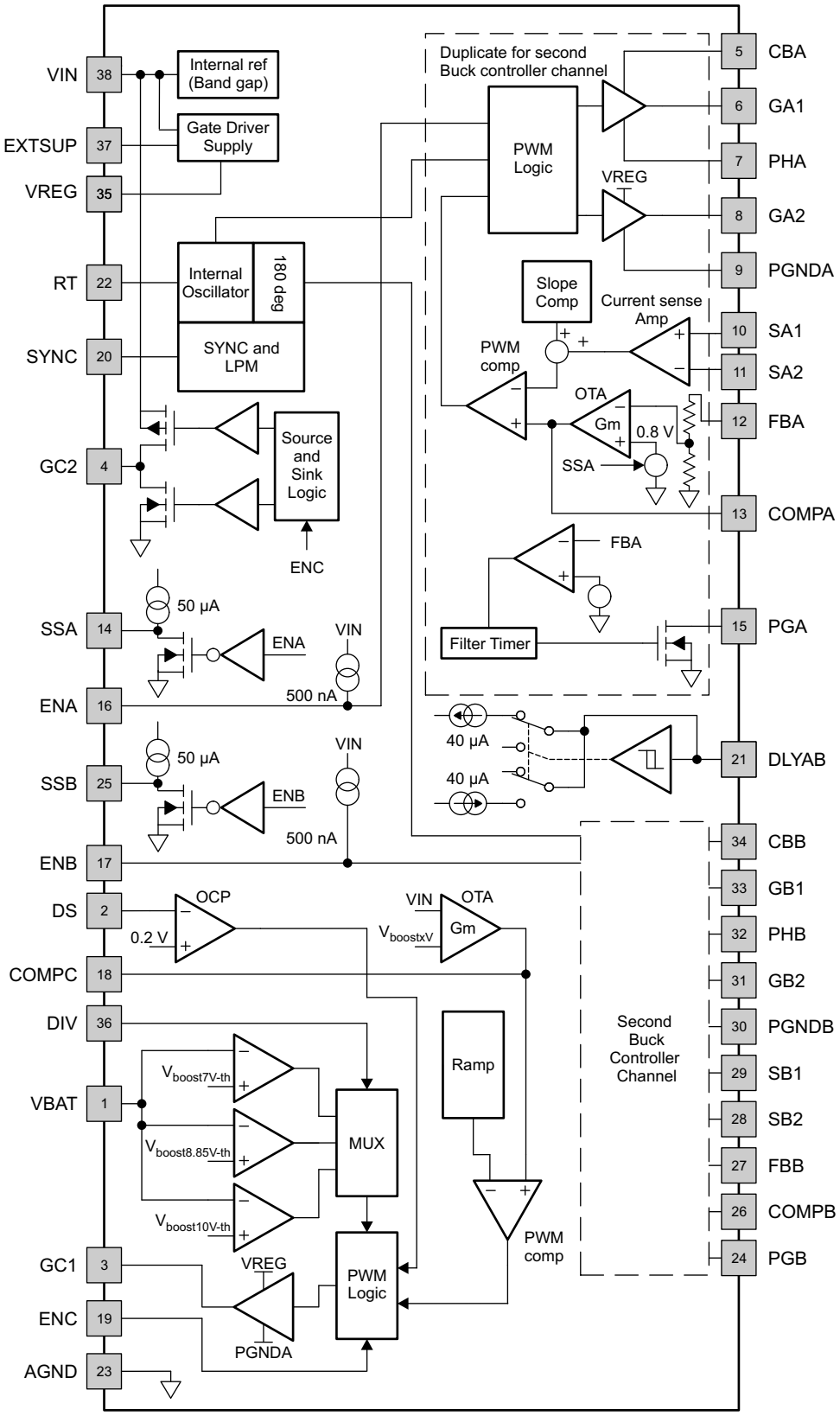

Figure 2. Functional Block Diagram

TYPICAL CHARACTERISTICS

BuckA EFFICIENCY AND POWER LOSSES
V_{IN} = 12 V, Inductor = 10 µH, R_{sense} = 20 mΩ, Switching Frequency = 400 kHz, EXTSUP open

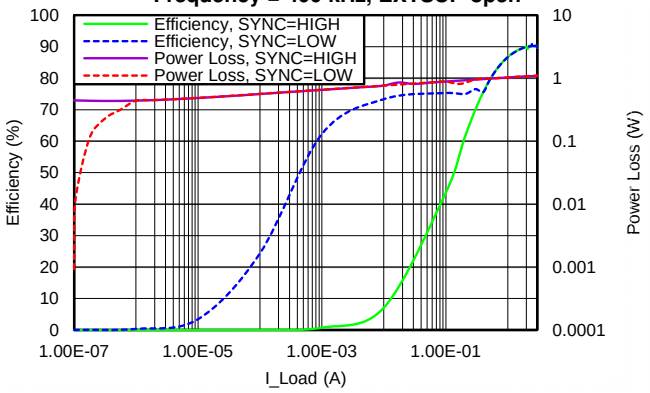

Figure 3.

BuckB EFFICIENCY AND POWER LOSSES
V_{IN} = 12 V, Inductor = 4.7 µH, R_{sense} = 10 mΩ, Switching Frequency = 400 kHz, EXTSUP open

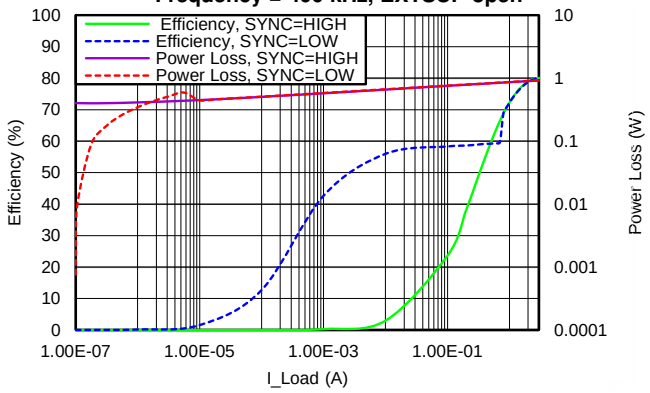

Figure 4.

BuckA LOAD STEP 1 A - 2 A
V_{IN} = 12 V, Inductor = 10 µH, R_{sense} = 20 mΩ, C_{OUT} = 100 µF, Switching Frequency = 400 kHz

Figure 5.

BuckB LOAD STEP 1 A - 2 A
V_{IN} = 12 V, Inductor = 4.7 µH, R_{sense} = 10 mΩ, C_{OUT} = 320 µF, Switching Frequency = 400 kHz

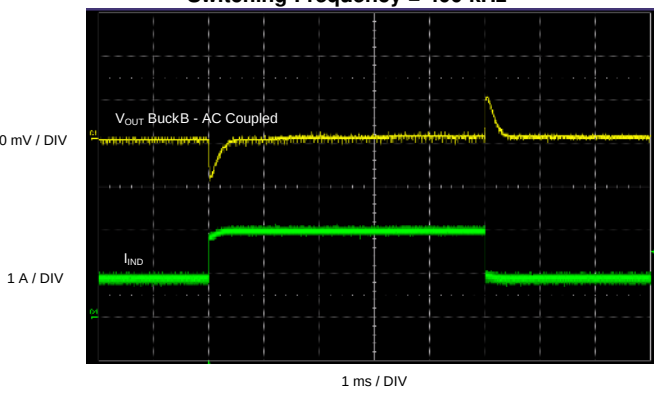

Figure 6.

BuckB LOAD STEP UP 0 A - 1 A
V_{IN} = 12 V, Inductor = 4.7 µH, R_{sense} = 10 mΩ, C_{OUT} = 320 µF, Switching Frequency = 400 kHz

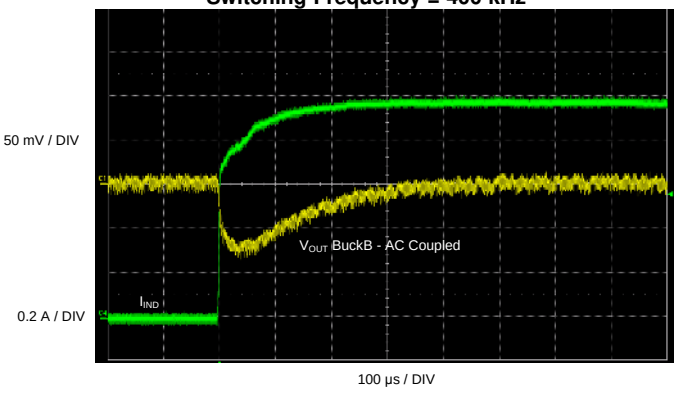

Figure 7.

BuckB LOAD STEP DOWN 1 A - 0 A
V_{IN} = 12 V, Inductor = 4.7 µH, R_{sense} = 10 mΩ, C_{OUT} = 320 µF, Switching Frequency = 400 kHz

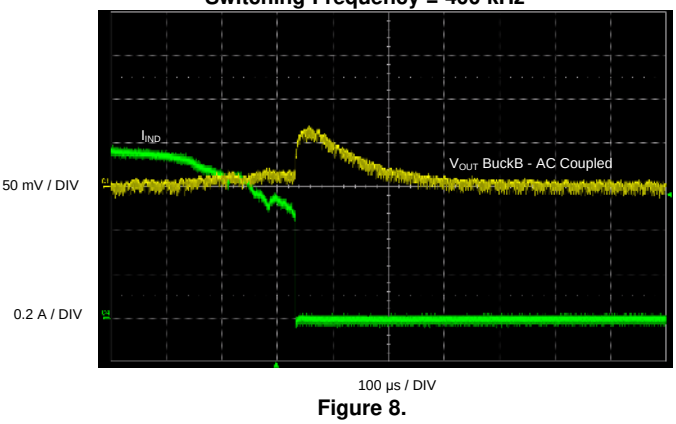

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

SOFT-START OUTPUTS
BuckA and BuckB

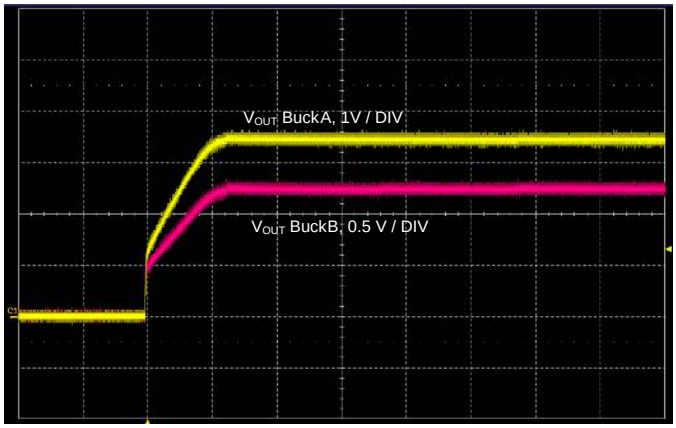

Figure 9.

VIN (BOOST OUTPUT) = 10 V, SWITCHING FREQUENCY = 200 kHz, INDUCTOR = 1 µH, RSENSE = 7.5 mΩ

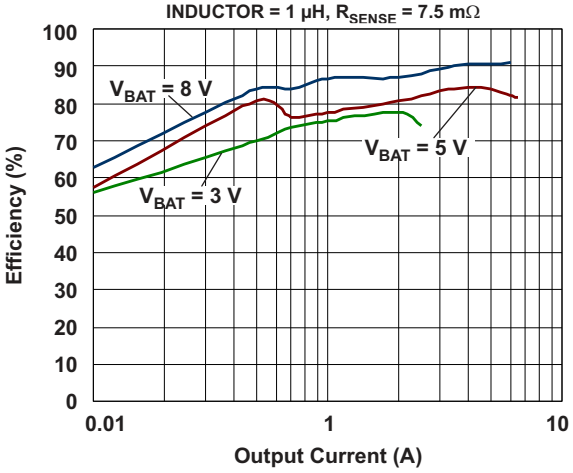

Figure 10.

VBAT (BOOST INPUT) = 5 V, VIN (BOOST OUTPUT) = 10 V, SWITCHING FREQUENCY = 200 kHz, INDUCTOR = 1 µH, RSENSE = 7.5 mΩ, CIN = 440 µF, COUT = 660 µF

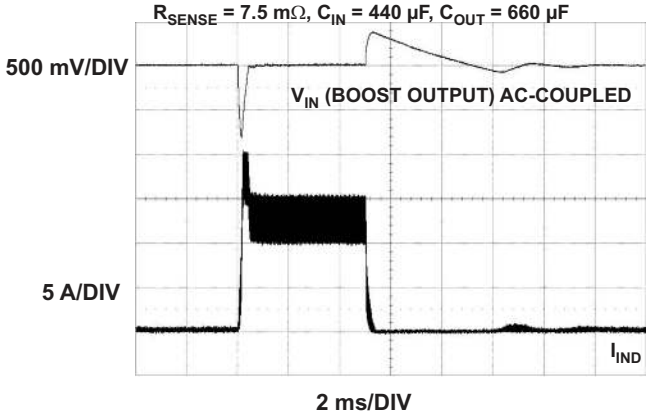

Figure 11.

VIN (BOOST OUTPUT) = 10 V, BuckA = 5 V AT 1.5 A, BuckB = 3.3 V AT 3.5 A, SWITCHING FREQUENCY = 200 kHz, INDUCTOR = 1 µH, RSENSE = 7.5 mΩ, CIN = 440 µF, COUT = 660 µF

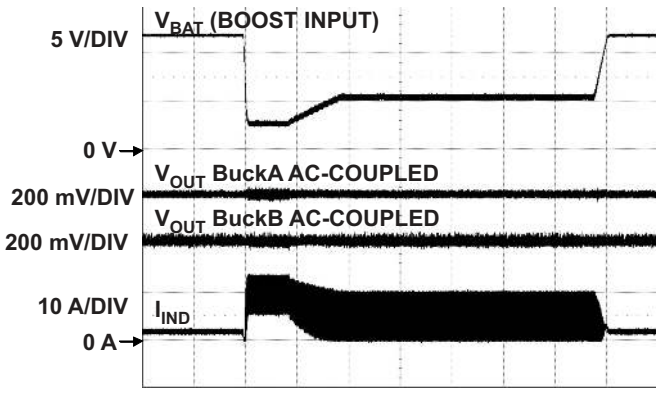

Figure 12.

VIN (BOOST OUTPUT) = 10 V, BuckA = 5 V AT 1.5 A, BuckB = 3.3V AT 3.5A, SWITCHING FREQUENCY = 200 kHz, INDUCTOR = 1 µH, RSENSE = 7.5 mΩ, CIN = 440 µF, COUT = 660 µF

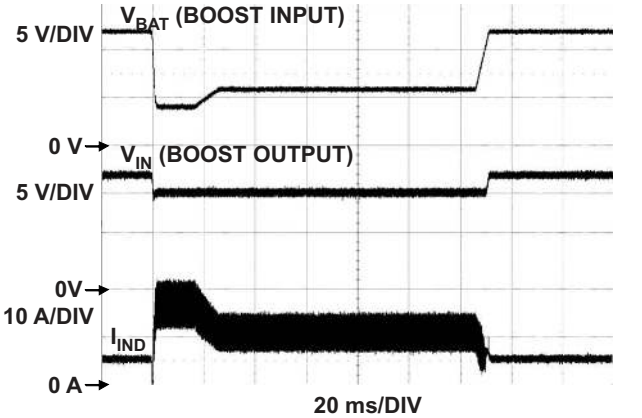

Figure 13.

VBAT (BOOST INPUT) = 5 V, VIN (BOOST OUTPUT) = 10 V, SWITCHING FREQUENCY = 200 kHz, INDUCTOR = 1 µH, RSENSE = 7.5 mΩ, CIN = 440 µF, COUT = 660 µF

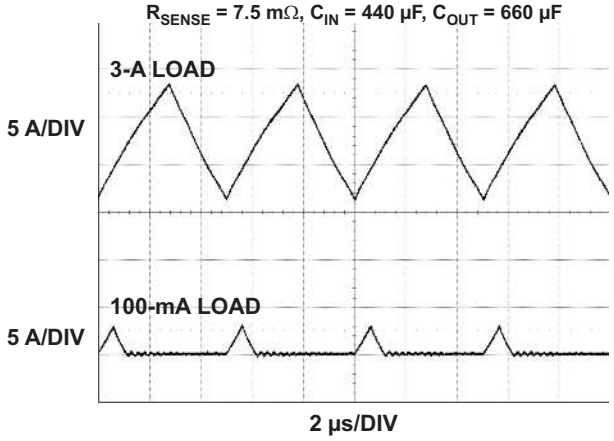

Figure 14.

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TYPICAL CHARACTERISTICS (continued)

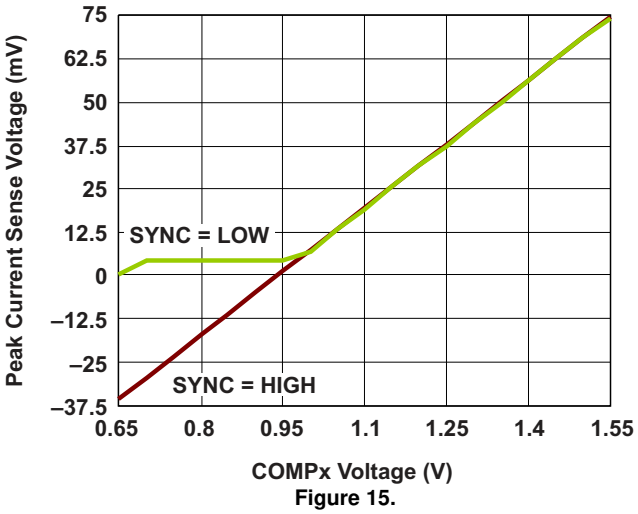

Figure 15.

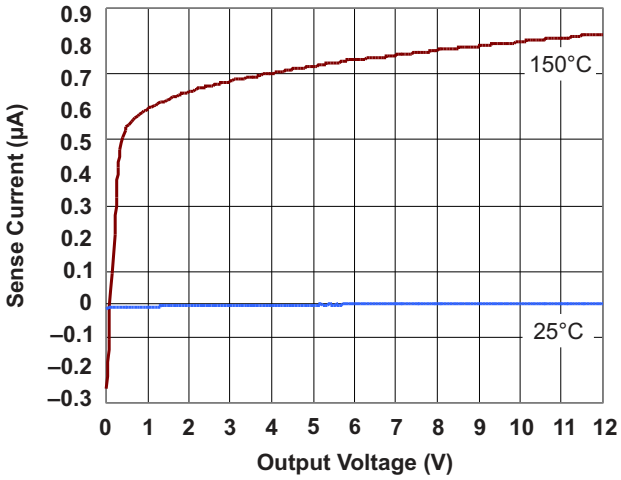

Figure 16.

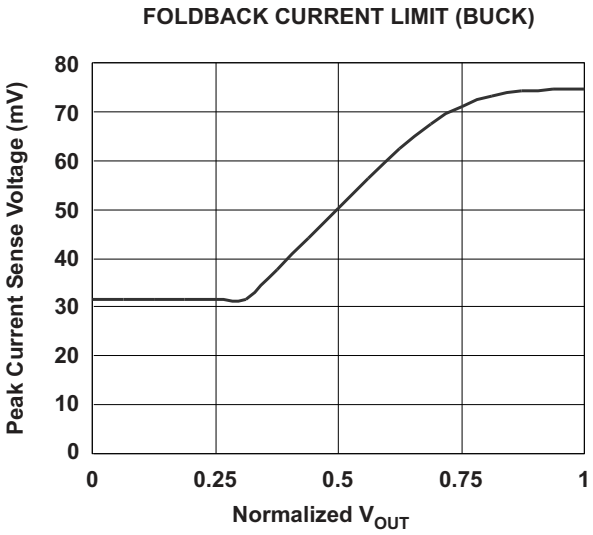

Figure 17.

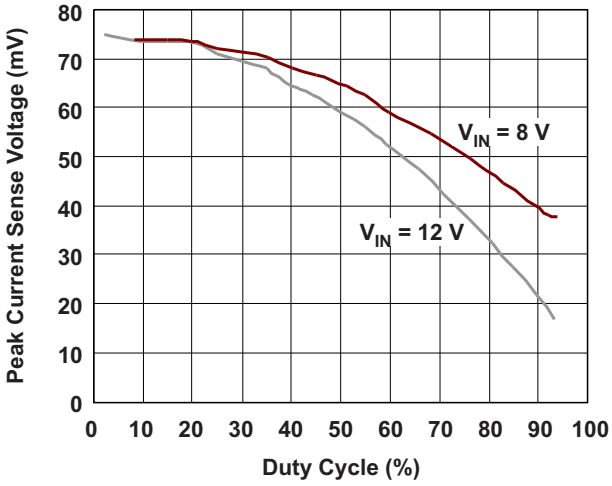

Figure 18.

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DETAILED DESCRIPTION

BUCK CONTROLLERS: NORMAL-MODE PWM OPERATION

Frequency Selection and External Synchronization

The buck controllers operate using constant-frequency peak-current-mode control for optimal transient behavior and ease of component choices. The switching frequency is programmable between 150 kHz and 600 kHz, depending upon the resistor value at the RT pin. A short circuit to ground at this pin sets the default switching frequency to 400 kHz. the frequency is also set by a resistor at RT according to Equation 1.

$$f_{SW} = \frac{X}{RT} \quad (X = 24\ k\Omega \times MHz)$$

$$f_{SW} = 24 \times \frac{10^9}{RT} \tag{1}$$

For example,

600 kHz requires 40 kΩ.

150 kHz requires 160 kΩ.

Synchronizing to an external clock at the SYNC pin in the same frequency range of 150 to 600 kHz is also possible. The device detects clock pulses at this pin, and an internal PLL locks on to the external clock within the specified range. The device also detects a loss of clock at this pin, and on detecting this loss, the device sets the switching frequency to the internal oscillator. The two buck controllers operate at identical switching frequencies, 180 degrees out of phase.

Enable Inputs

Independent enable inputs from the ENA and ENB pins enable the buck controllers. These are high-voltage pins, with a threshold of 1.5 V for high level, and with direct connection directly to the battery for self-bias. The low threshold is 0.7 V. Both these pins have internal pullup currents of 0.5 µA (typical). As a result, an open circuit on these pins enables the respective buck controllers. When both buck controllers are disabled, the device shuts down and consumes a current less than 4 µA.

Feedback Inputs

An internal voltage divider presets the output voltage. Connect each FBx pin to the output of the respective regulator of the pin.

Soft-Start Inputs

In order to avoid large inrush currents, each buck controller has an independent, programmable soft-start timer. The voltage at the SSx pins acts as the soft-start reference voltage. A 50-µA pullup current available at the SSx pins, in combination with a suitably chosen capacitor, generates a ramp of the desired soft-start speed. After start-up, the pullup current ensures that this node is higher than the internal reference of 0.8 V; 0.8 V then becomes the reference for the buck controllers. Equation 2 calculates the soft-start ramp time.

$$C_{SS} = \frac{I_{SS} \times \Delta t}{\Delta V} \quad \text{(Farads)}$$

where,

- I_{SS} = 50 µA (typical)
- ΔV = 0.8 V
- C_{SS} is the required capacitor for Δt, the desired soft-start time. (2)

Alternatively, the soft-start pins are used as tracking inputs. In this case, connect these pins to the supply to be tracked via a suitable resistor-divider network.

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Current-Mode Operation

Peak-current-mode control regulates the peak current through the inductor to maintain the output voltage at the set value. The error between the feedback voltage at FBx and the internal voltage divider produces a signal at the output of the error amplifier (COMPx), which serves as the target for the peak inductor current. The device senses the current through the inductor as a differential voltage at Sx1–Sx2 and compares the voltage with this target during each cycle. A fall or rise in load current produces a fall or rise in voltage at FBx, causing COMPx to fall or rise respectively, thus increasing or decreasing the current through the inductor until the average current matches the load. This process maintains the output voltage in regulation.

The top N-channel MOSFET turns on at the beginning of each clock cycle and stays on until the inductor current reaches the peak value. When this MOSFET turns off, and after a small delay (shoot-through delay), the lower N-channel MOSFET turns on until the start of the next clock cycle. In dropout operation, the high-side MOSFET stays on continuously. In every fourth clock cycle, there is a limit on the duty cycle of 95% in order to charge the bootstrap capacitor at CBx, which allows a maximum duty cycle of 98.75% for the buck regulators. During dropout, the buck regulator switches at one-fourth of its normal frequency.

Current Sensing and Current Limit With Foldback

Clamping of the maximum value of COMPx is such as to limit the maximum current through the inductor to a specified value. When the output of the buck regulator (and hence the feedback value at FBx) falls to a low value due to a short-circuit or overcurrent condition, the clamped voltage at COMPx successively decreases, thus providing current foldback protection, which protects the high-side external MOSFET from excess current (forward-direction current limit).

Similarly, if due to a fault condition the output is shorted to a high voltage and the low-side MOSFET turns fully on, the COMPx node drops low. A clamp is on the lower end as well, in order to limit the maximum current in the low-side MOSFET (reverse-direction current limit).

An external resistor senses the current through the inductor. Choose the sense resistor such that the maximum forward-peak current in the inductor generates a voltage of 75 mV across the sense pins. This specified typical value is for low duty cycles only. At typical duty-cycle conditions around 28% (assuming 3.4 V output and 12 V input), 55 mV is a more reasonable value, considering tolerances and mismatches. The typical characteristics (see Figure 18) provide a guide for using the correct current-limit sense voltage.

The current-sense pins Sx1 and Sx2 are high-impedance pins with low leakage across the entire output range, thus allowing DCR current sensing using the dc resistance of the inductor for higher efficiency. Figure 19 shows DCR sensing. Here, the series resistance (DCR) of the inductor is the sense element. Place the filter components close to the device for noise immunity. Remember that while the DCR sensing gives high efficiency, it is inaccurate due to the temperature sensitivity and a wide variation of the parasitic inductor series resistance. Hence using the more-accurate sense resistor for current sensing is advantageous.

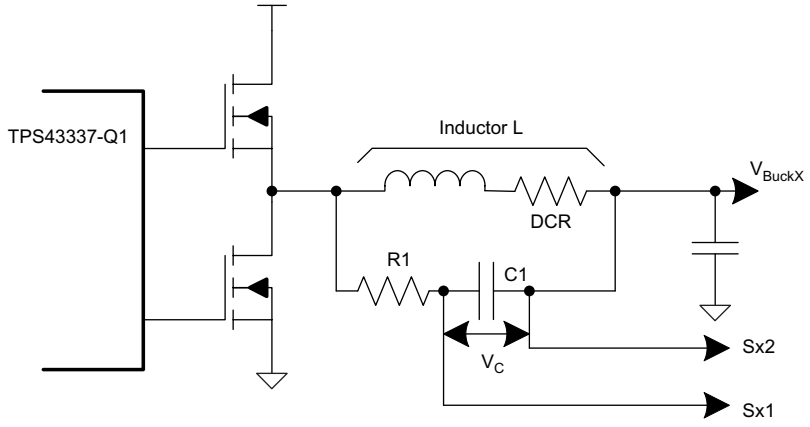

Figure 19. DCR Sensing Configuration

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Slope Compensation

Optimal slope compensation, which is adaptive to changes in input voltage and duty cycle, allows stable operation at all conditions. For optimal performance of this circuit, choose the inductor and sense resistor according to Equation 3.

$$\frac{L \times f_{SW}}{R_S} = 200 \quad (3)$$

where

- L is the buck regulator inductor in henries.
- R_S is the sense resistor in ohms.
- f_{sw} is the buck regulator switching frequency in hertz.

Power-Good Outputs and Filter Delays

Each buck controller has an independent power-good comparator monitoring the feedback voltage at the FBx pins and indicating whether the output voltage has fallen below a specified power-good threshold. This threshold has a typical value of 93% of the regulated output voltage. The power-good indicator is available as an open-drain output at the PGx pins. Shutdown of a buck controller causes an internal pulldown of the power-good indicator. Connecting the external pullup resistor to a rail other than the output of that particular buck channel causes a constant current flow through the external resistor during a powered-down state of the buck controller.

In order to avoid triggering the power-good indicators due to noise or fast transients on the output voltage, the device uses an internal delay circuit for de-glitching. Similarly, when the output voltage returns to the set value after a long negative transient, assertiohn of the power-good indicator (release of the open-drain pin) occurs after the same delay. Use of this delay can pause the reset of circuits powered from the buck regulator rail. Program the delay of this circuit by using a suitable capacitor at the DLYAB pin according to Equation 4.

$$\frac{t_{DELAY}}{C_{DLYAB}} = \frac{1\ msec}{1\ nF} \quad (4)$$

When the DLYAB pin is open, the delay is set to a default value of 20 µs (typical). The power-good delay timing is common to both the buck rails, but the power-good comparators and indicators function independently.

Light-Load PFM Mode

An external clock or a high level on the SYNC pin results in forced continuous-mode operation of the bucks. When the SYNC pin is low or open, the buck controllers are allowed to operate in discontinuous mode at light loads by turning off the low-side MOSFET whenever a zero-crossing in the inductor current is detected.

In discontinuous mode, as the load decreases, the duration of the clock-period when both the high-side as well the low-side MOSFET is turned-off, increases (deep discontinuous mode). In case the duration exceeds 60% of the clock period and VBAT > 8 V, the buck controller switches to a low-power operation mode. The design ensures that this typically occurs at 1% of the set full-load current if the inductor and the sense resistor have been chosen appropriately as recommended in the *Slope Compensation* section.

In low-power PFM mode, the buck monitors the FBx voltage and compares it with the 0.8 V internal reference voltage through the internal voltage divider. Whenever the FBx value falls below the internal threshold, the high-side MOSFET is turned on for a pulse duration inversely proportional to the difference VIN – Sx2. At the end of this on-time, the high-side MOSFET is turned off and the current in the inductor decays until it becomes zero. The low-side MOSFET is not turned on. The next pulse occurs the next time FBx falls below the threshold value which results in a constant volt-second t_{on} hysteretic operation with a total-device quiescent-current consumption of 34 µA when a single buck channel is active and 43 µA when both channels are active.

As the load increases, the pulses become more and more frequent and move closer to each other until the current in the inductor becomes continuous. At this point, the buck controller returns to normal fixed-frequency current-mode control. Another criterion to exit the low-power mode is when VIN falls low enough to require higher than 80% duty cycle of the high-side MOSFET.

During low-power mode, the TPS43337-Q1 supports the full-current load until the transition to normal mode takes place. The design ensures the low-power-mode exit occurs at 10% (typical) of full-load current if the inductor and sense resistor have been chosen as recommended. Moreover, there is always a hysteresis between the entry and exit thresholds to avoid oscillating between the two modes.

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In the event that both buck controllers are active, low-power mode is only possible when both buck controllers have light loads that are low enough for entry into low-power mode. When the boost controller is enabled, low-power mode is possible only if VBAT is high enough to prevent the boost from switching and if DIV is open or set to GND. If DIV is high (VREG), low-power mode is inhibited.

Boost Controller

The boost controller has a fixed-frequency voltage-mode architecture and includes a cycle-by-cycle current-limit protection for the external N-channel MOSFET. The switching frequency is derived from and set to one-half of the buck-controller switching frequency. The output voltage of the boost controller at the VIN pin is set by an internal resistor-divider network and is programmable to 7 V, 8.85 V, and 10 V based on the low, open, and high status of the DIV pin, respectively. A change of the DIV setting is not recognized while the device is in low-power mode.

The boost controller is enabled by the active-high ENC pin and is active when the input voltage at the VBAT pin has crossed the unlock threshold of 8.5 V at least once. After that, the boost controller is armed and starts switching as soon as VIN falls below the value set by the DIV pin, and regulates the VIN voltage. Thus, the boost regulator maintains a stable input voltage for the buck regulators during transient events such as a cranking pulse at VBAT.

Whenever the voltage at the DS pin exceeds 200 mV, the boost-external MOSFET is turned off by pulling the CG1 pin low. By connecting the DS pin to the drain of the MOSFET or to a sense resistor between the MOSFET source and ground, cycle-by-cycle overcurrent protection for the MOSFET can be achieved. The on-resistance of the MOSFET or the value of the sense resistor must be chosen in such a way that the on-state voltage at DS does not exceed 200 mV at the maximum load and minimum input-voltage conditions. When a sense resistor is used, connecting a filter network between the DS pin and the sense resistor is recommended for better noise immunity.

The boost output (VIN) is also used to supply other circuits in the system, however, they should be high-voltage tolerant. The boost output is regulated to the programmed value only when VIN is low, and so VIN can reach battery levels.

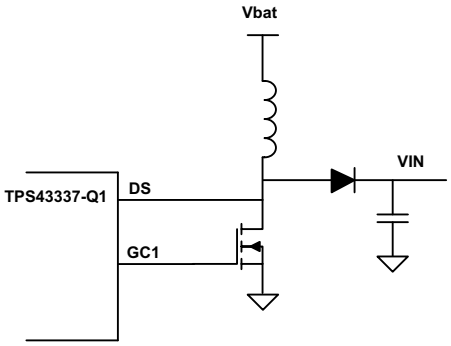

Figure 20. External Drain-Source Voltage Sensing

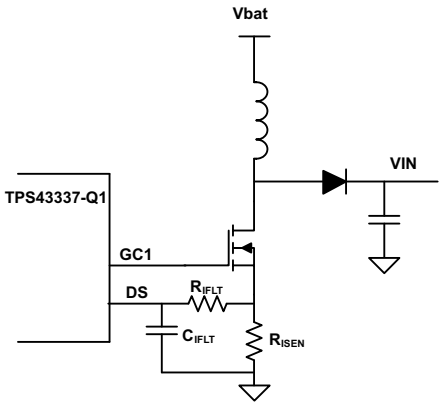

Figure 21. External Current Shunt Resistor

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Table 1. Mode Control

SYNC Terminal	Comments
External clock	Device in forced into continuous mode, internal PLL locks into the external clock between 150 kHz and 600 kHz
Low or open	Device can enter discontinuous mode. Automatic LPM entry and exit, depending on load conditions
High	Device in forced into continuous mode

Table 2. Mode of Operation

ENABLE AND INHIBIT PINS				DRIVER STATUS		DEVICE STATUS	QUIESCENT CURRENT
ENA	ENB	ENC	SYNC	BUCK CONTROLLERS	BOOST CONTROLLER		
Low	Low	Low	X	Shutdown	Disabled	Shutdown	Approximately 4 µA
Low	High	Low	Low	BuckB running	Disabled	BuckB: LPM enabled	Approximately 34 µA (light loads)
			High			BuckB: LPM inhibited	mA range
High	Low	Low	Low	BuckA running	Disabled	BuckA: LPM enabled	Approximately 34 µA (light loads)
			High			BuckA: LPM inhibited	mA range
High	High	Low	Low	BuckA and BuckB running	Disabled	BuckA and BuckB: LPM enabled	Approximately 43 µA (light loads)
			High			BuckA and BuckB: LPM inhibited	mA range
Low	Low	Low	X	Shutdown	Disabled	Shutdown	Approximately 4 µA
Low	High	High	Low	BuckB running	Boost running for VIN < set boost output	BuckB: LPM enabled	Approximately 54 µA (no boost, light loads)
			High			BuckB: LPM inhibited	mA range
High	Low	High	Low	BuckA running	Boost running for VIN < set boost output	BuckA: LPM enabled	Approximately 54 µA (no boost, light loads)
			High			BuckA: LPM inhibited	mA range
High	High	High	Low	BuckA and BuckB running	Boost running for VIN < set boost output	BuckA and BuckB: LPM enabled	Approximately 68 µA (no boost, light loads)
			High			BuckA and BuckB: LPM inhibited	mA range

Gate Driver Supply (VREG, EXTSUP)

The gate drivers of the buck and boost controllers are supplied from an internal linear regulator whose output (5.8 V, typical) is available at the VREG pin and requires decoupling with a ceramic capacitor in the range of 3.3 µF to 10 µF. This pin has internal current-limit protection and should not be used to power any other circuits.

The VREG linear regulator is powered from VIN by default when the EXTSUP voltage is lower than 4.6 V (typical). In case VIN is expected to go to high levels, there can be excessive power dissipation in this regulator, especially at high switching frequencies and when using large external MOSFETs. In this case, powering this regulator from the EXTSUP pin is advantageous, which can be connected to a supply lower than VIN but high enough to provide the gate drive. When EXTSUP is connected to a voltage greater than 4.6 V, the linear regulator automatically switches to EXTSUP as its input to provide this advantage. Efficiency improvements are possible when one of the switching regulator rails from the TPS43337-Q1 or any other voltage available in the system is used to power EXTSUP. The maximum voltage that should be applied to EXTSUP is 9 V.

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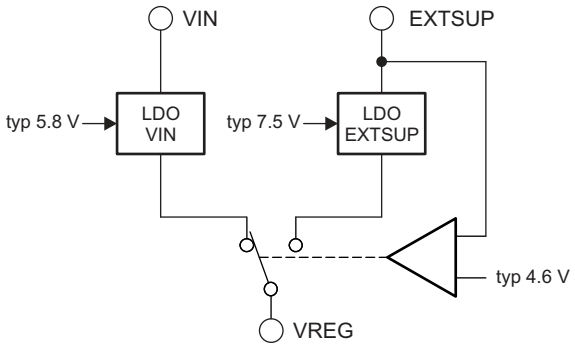

Figure 22. Internal Gate-Driver Supply

Using a voltage above 5.8 V (sourced by VIN) for EXTSUP is advantageous as it provides a large gate drive and therefore better on-resistance of the external MOSFETs.

During low-power mode, the EXTSUP functionality is not available. The internal regulator operates as a shunt regulator powered from VIN and has a typical value of 7.5 V. Current-limit protection for VREG is available in low-power mode as well. If EXTSUP is unused, leave the pin open without a capacitor installed.

External P-Channel Drive (GC2) and Reverse Battery Protection

The TPS43337-Q1 includes a gate driver for an external P-channel MOSFET, which can be connected across the rectifier diode of the boost regulator which is useful to reduce power losses when the boost controller is not switching. The gate driver provides a swing of 6 V typical below the VIN voltage in order to drive a P-channel MOSFET. When VBAT falls below the boost enable threshold, the gate driver turns off the P-channel MOSFET, and the diode is no longer bypassed.

The gate driver can also be used to bypass any additional protection diodes connected in series as shown in Figure 23. Figure 24 also shows a different scheme of reverse battery protection which may require only a smaller-sized diode to protect the N-channel MOSFET, as the diode conducts only for a part of the switching cycle. Because the diode is not always in the series path, the system efficiency improves.

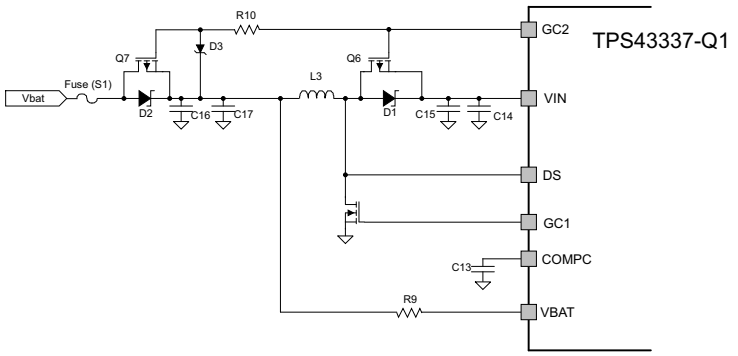

Figure 23. Reverse-Battery-Protection Option for Buck-Boost Configuration

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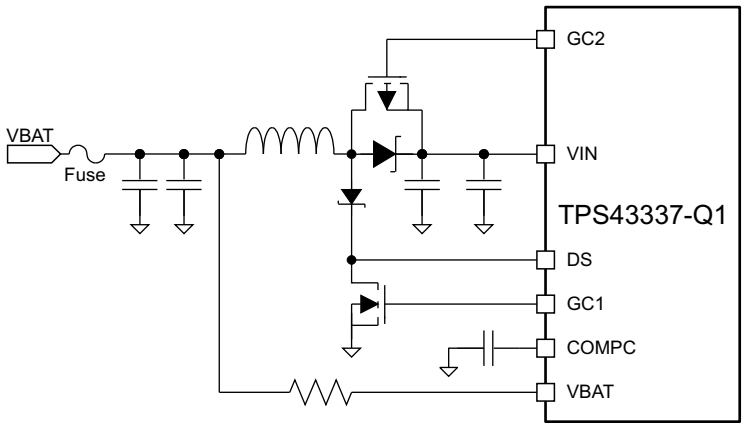

Figure 24. Reverse-Battery-Protection Option for Buck-Boost Configuration

Undervoltage Lockout and Overvoltage Protection

The TPS43337-Q1 starts up at a VIN voltage of 6.5 V (minimum), required for the internal supply (VREG). Once the has started up, it operates down to a VIN voltage of 3.6 V; below this voltage level, the undervoltage lockout disables the device.

NOTE

If V_{IN} drops, V_{REG} drops as well, reducing the gate-drive voltage, while the digital logic remains fully functional. Even if ENC is high, exceeding the boost-unlock voltage of typically 8.5 V one time is required before boost activation takes place (see the Boost Controller section).

A voltage of 46 V at VIN triggers the overvoltage comparator, which shuts down the device. In order to prevent transient spikes from shutting down the device, the undervoltage and overvoltage protection have filter times of 5 µs (typical).

When the voltages return to the normal-operating region, the enabled switching regulators start including a new soft-start ramp for the buck regulators.

When the boost controller is enabled, a voltage less than 1.9 V (typical) on VBAT triggers an undervoltage lockout and pulls the boost gate driver (GC1) low (this action has a filter delay of 5 µs, typical). As a result, VIN falls at a rate dependent on the capacitor and load, eventually triggering VIN undervoltage. A short falling transient at VBAT even lower than 2 V can thus be survived, if VBAT returns above 2.5 V before VIN is discharged to the undervoltage threshold.

Thermal Protection

The TPS43337-Q1 protects itself from overheating using an internal thermal shutdown circuit. If the die temperature exceeds the thermal shutdown threshold of 165°C due to excessive power dissipation (for example, due to fault conditions such as a short circuit at the gate drivers or VREG), the controllers are turned off, and then restarted when the temperature has fallen by 15°C.

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APPLICATION INFORMATION

The following example illustrates the design process and component selection for the TPS43337-Q1. The design goal parameters are given in Table 3.

Table 3. Design Goal Parameters Example

PARAMETER	V_{BUCKA}	V_{BUCKB}	BOOST
Input voltage	V_{IN} 6 to 30 V 12 V - typical	V_{IN} 6 to 30 V 12 V - typical	V_{BAT} = 5 (cranking pulse input) to 30 V
Output voltage, V_{OUTx}	3.396 V	1.235 V	10 V
Maximum output current, I_{OUTx}	3 A	2 A	2.5 A
Load step output tolerance, ΔV_{OUT} + $\Delta V_{OUT(Ripple)}$	±0.2 V	±0.12 V	±0.5 V
Current output load step, ΔI_{OUTx}	0.1 to 3 A	0.1 to 2 A	0.1 to 2.5 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz	200 kHz

This example is a starting point and theoretical representation of the values to be used for the application; further optimization of the components derived may be required to improve the performance of the device.

Boost Component Selection

A boost converter operating in continuous-conduction mode (CCM) has a right-half-plane (RHP) zero in the transfer function. The RHP zero is inversely related to the load current and inductor value and directly related to the input voltage. The RHP zero limits the maximum bandwidth achievable for the boost regulator. If the bandwidth is too close to the RHP zero frequency, the regulator may become unstable.

Thus, for high-power systems with low input voltages, a low inductor value is chosen. This value increases the amplitude of the ripple currents in the N-channel MOSFET, the inductor and the capacitors for the boost regulator. They must be designed with the ripple/RHP zero trade-off in mind and considering the power dissipation effects in the components due to parasitic series resistance.

A boost converter that operates in the discontinuous mode does not contain the RHP-zero in transfer function. However, designing for the discontinuous mode demands an even lower inductor value that has high ripple currents. Also, ensure that the regulator never enters the continuous-conduction mode; otherwise, the regulator becomes unstable.

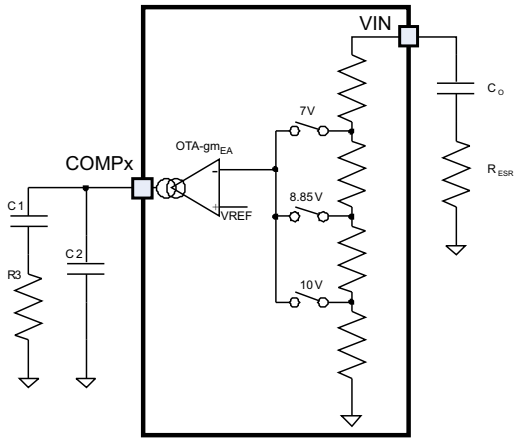

Figure 25. Boost Compensation Components

This design is done assuming continuous-conduction mode. During light load conditions, the boost converter operates in discontinuous mode without affecting stability. Hence, the assumptions here cover the worst case for stability.

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Boost Maximum Input Current I_{IN_MAX}

The maximum input current is drawn at the minimum input voltage and maximum load. The efficiency for VBAT = 5 V at 2.3 A is 80%, based on the typical characteristics plot.

$$P_{INmax} = \frac{P_{OUT}}{Efficiency} = \frac{25\ W}{0.8} = 31.3\ W \tag{5}$$

Hence,

$$I_{INmax}(at\ V_{BAT} = 5\ V) = \frac{31.3\ W}{5\ V} = 6.3\ A \tag{6}$$

Boost Inductor Selection, L

Allow input ripple current of 40% of $I_{IN\ max}$ at V_{BAT} = 5 V

$$L = \frac{V_{BAT} \times t_{ON}}{I_{INripplemax}} = \frac{V_{BAT}}{I_{INripplemax} \times 2 \times f_{SW}} = \frac{5\ V}{2.52\ A \times 2 \times 200\ kHz} = 4.9\ \mu H \tag{7}$$

Choose a lower value of 3.9 µH in order to ensure a high RHP-zero frequency while making a compromise that expects a high current ripple. This inductor selection also makes the boost converter operate in discontinuous conduction mode, where it is easier to compensate.

The inductor saturation current must be higher than the peak inductor current and some percentage higher than the maximum current-limit value set by the external resistive sensing element.

This rating should be determined at the minimum input voltage, maximum output current, and maximum core temperature for the application.

Inductor Ripple Current, I_{RIPPLE}

Based on an Inductor value of 3.9 µH, the ripple current is approximately 3.1 A.

Peak Current in Low-Side FET, I_{PEAK}

$$I_{PEAK} = I_{INmax} + \frac{I_{RIPPLE}}{2} = 6.3\ A + \frac{3.1\ A}{2} = 7.85\ A \tag{8}$$

Based on this peak current value (see Equation 8), the external current-sense resistor R_{SENSE} is calculated in .

$$R_{SENSE} = \frac{0.2\ V}{7.85\ A} = 25\ m\Omega$$

Select 20 mΩ, allowing for tolerance.

The filter component values R_{IFLT} and C_{IFLT} for current sense are 1.5 kΩ and 1 nF, respectively, which allows for good noise immunity.

Right Half-Plane Zero RHP Frequency, f_{RHP}

$$f_{RHP} = \frac{V_{BAT\,min}}{2\pi \times I_{In\,max} \times L} = 32\ kHz \tag{9}$$

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Output Capacitor, C_O

To ensure stability, the output capacitor C_O is chosen such that

$$f_{LC} \le \frac{f_{RHP}}{10}$$

$$\frac{10}{2\pi \times \sqrt{L \times C_{OUTx}}} \le \frac{V_{BATmin}}{2\pi \times I_{INmax} \times L}$$

$$C_{OUTx} \ge \left(\frac{10 \times I_{INmax}}{V_{BATmin}} \right)^2 \times L = \left(\frac{10 \times 6.3\ A}{5\ V} \right)^2 \times 3.9\ \mu H$$

$$C_{OUTxmin} \ge 635\ \mu F \quad (10)$$

Select C_{OUTx} = 680 µF.

This capacitor is usually aluminum electrolytic with ESR in the tens-of-milliohms which is good for loop stability, because it provides a phase boost due to the ESR. The output filter components L and C create a double pole (180 degree phase-shift) at a frequency f_{LC}, and the ESR of the output capacitor R_{ESR} creates a *zero* for the modulator at frequency f_{ESR}. These frequencies can be determined by Equation 11.

$$f_{ESR} = \frac{1}{2\pi \times C_{OUTx} \times R_{ESR}} Hz, \quad \text{assume } R_{ESR} = 40\ m\Omega$$

$$f_{ESR} = \frac{1}{2\pi \times 680\ \mu F \times 0.04} = 6\ kHz$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUTx}}} = \frac{1}{2\pi \times \sqrt{4\ \mu H \times 680\ \mu F}} = 3.1\ kHz \quad (11)$$

This satisfies $f_{LC} \le 0.1\ f_{RHP}$.

Bandwidth of Boost Converter, f_C

Use the following guidelines to set the frequency poles, zeroes, and crossover values for the trade-off between stability and transient response:

$f_{LC} < f_{ESR} < f_C < f_{RHP\ Zero}$

$f_C < f_{RHP\ Zero} / 3$

$f_C < f_{SW} / 6$

$f_{LC} < f_C / 3$

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Output Ripple Voltage Due to Load Transients, ΔV_O

Assume a bandwidth of f_C = 10 kHz.

$$\Delta V_{OUTx} = R_{ESR} \times \Delta I_{OUTx} + \frac{\Delta I_{OUTx}}{4 \times C_{OUTx} \times f_C}$$

$$= 0.04\ \Omega \times 2.5\ A + \frac{2.5\ A}{4 \times 660\ \mu F \times 10\ kHz} = 0.19\ V \quad (12)$$

Because the boost converter is active only during brief events such as a cranking pulse, and the buck converters are high-voltage tolerant, a higher excursion on the boost output may be tolerable in some cases. In such cases, smaller component choices for the boost output may be used.

Selection of Components for Type II Compensation

The required loop gain for unity gain bandwidth (UGB) is shown in Equation 13.

$$G = 40 \log\left(\frac{f_C}{f_{LC}}\right) - 20 \log\left(\frac{f_C}{f_{ESR}}\right)$$

$$G = 40 \log\left(\frac{10\ kHz}{3.1\ kHz}\right) - 20 \log\left(\frac{10\ kHz}{6\ kHz}\right) = 15.9\ dB \quad (13)$$

The boost converter error amplifier (OTA) has a Gm that is proportional to the V_{BAT} voltage which allows a constant loop response across the input voltage range and makes it easier to compensate by removing the dependency on V_{BAT}.

$$R3 = \frac{10^{G/20}}{85 \times 10^{-6}\ A/V^2 \times V_{OUTx}} = 7.2\ k\Omega$$

$$C1 = \frac{10}{2\pi \times f_C \times R3} = \frac{10}{2\pi \times 10\ kHz \times 7.2\ k\Omega} = 22\ nF$$

$$C2 = \frac{C1}{2\pi \times R3 \times C1 \times \left(\frac{f_{SW}}{2}\right) - 1} = \frac{22\ nF}{2\pi \times 7.2\ k\Omega \times 22nF \times \left(\frac{200\ kHz}{2}\right) - 1} = 223\ pF \quad \text{choose } 220\ pF \quad (14)$$

Input Capacitor, C_{IN}

The input ripple required is lower than 50 mV.

$$\Delta V_{C1} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{IN}} = 10\ mV$$

$$C_{IN} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times \Delta V_{C1}} = 194\ \mu F$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR} = 40\ mV \quad (15)$$

Therefore, TI recommends 220 µF with 10-mΩ ESR.

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Output Schottky Diode D1 Selection

A Schottky diode with low forward-conducting voltage V_F over temperature and fast switching characteristics is required to maximize efficiency. The reverse breakdown voltage should be higher than the maximum input voltage, and the component should have low reverse-leakage current. Additionally, the peak forward current should be higher than the peak inductor current. The power dissipation in the Schottky diode is given in Equation 16.

$$P_D = I_{D(PEAK)} \times V_F \times (1 - D)$$

$$D = 1 - \frac{V_{INMIN}}{V_{OUT} + V_F} = 1 - \frac{5V}{10V + 0.6V} = 0.53$$

$$P_D = 7.85\ A \times 0.6\ V \times (1 - 0.53) = 2.2\ W \quad (16)$$

Low-Side MOSFET (BOT_SW3)

$$P_{BOOSTFET} = (I_{Pk})^2 \times r_{DS(on)}(1 + TC) \times D + \left(\frac{V_I \times I_{Pk}}{2}\right) \times (t_r + t_f) \times f_{sw}$$

$$P_{BOOSTFET} = (7.85\ A)^2 \times 0.02\ \Omega \times (1 + 0.4) \times 0.53 + \left(\frac{V_I \times I_{Pk}}{2}\right) \times (20\ ns + 20\ ns) \times 200\ kHz = 1.07\ W \quad (17)$$

The times t_r and t_f denote the rising and falling times of the switching node and are related to the gate-driver strength of the TPS43337-Q1 and gate Miller capacitance of the MOSFET. The first term denotes the conduction losses, which are minimized when the on-resistance of the MOSFET is low. The second term denotes the transition losses which arise due to the full application of the input voltage across the drain-source of the MOSFET as it turns on or off. They are higher at high output currents and low input voltages (due to the large input peak current) and when the switching time is low.

NOTE: The on-resistance $r_{DS(on)}$ has a positive temperature coefficient, which produces the (TC = d × ΔT) term that signifies the temperature dependence. (Temperature coefficient d is available as a normalized value from MOSFET data sheets and can be assumed to be 0.005 / ºC as a starting value.)

BuckA Component Selection

Minimum ON Time, $t_{ON\ min}$

$$t_{ON\,min} = \frac{V_O}{V_{IN\,max} \times f_{SW}} = \frac{3.4\ V}{30\ V \times 400\ kHz} = 283\ ns \quad (18)$$

As shown in Equation 18, $t_{ON\ min}$ is higher than the minimum duty cycle specified (100 ns, typical). Hence the minimum duty cycle is achievable at this frequency.

Current-Sense Resistor R_{SENSE}

Based on the typical characteristics for V_{SENSE} limit with V_{IN} versus duty cycle, the sense limit is approximately 70 mV (at VIN = 12 V and duty cycle of 3.4 V / 12 V = 0.283). Allowing for tolerances and ripple currents, choose V_{SENSE} maximum of 55 mV.

$$R_{SENSE} = \frac{55\ mV}{3\ A} = 18\ m\Omega$$

Select 18 mΩ.

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Inductor Selection L

As explained in the description of the buck controllers (see Detailed Description), for optimal slope compensation and loop response, the inductor should be chosen such that:

$$L = K_{FLR} \times \frac{R_{SENSE}}{f_{SW}} = 200 \times \frac{18\ m\Omega}{400\ kHz} = 9.2\ \mu H \quad (19)$$

- K_{FLR} = Coil selection constant = 200

Choose a standard value of 10 µH. For the buck converter, the inductor saturation currents and core should be chosen to sustain the maximum currents.

Inductor Ripple Current I_{RIPPLE}

At the nominal input voltage of 12 V, this gives a ripple current of 25% of I_{OUTmax} ≈ 1 A.

Output Capacitor C_O

Select an output capacitance C_O of 100 µF with low ESR in the range of 10 mΩ. This gives $\Delta V_{O(Ripple)}$ ≈ 15 mV and ΔV drop of ≈ 180 mV during a load step, which does not trigger the power-good comparator and is within the required limits.

$$C_{OUTA} \approx \frac{2 \times \Delta I_{OUTA}}{f_{SW} \times \Delta V_{OUTA}} = \frac{2 \times 2.9\ A}{400\ kHz \times 0.2\ V} = 72.5\ \mu F \quad (20)$$

$$V_{OUTA(Ripple)} = \frac{I_{OUTA(Ripple)}}{8 \times f_{SW} \times C_{OUTA}} + I_{OUTA(Ripple)} \times ESR = \frac{1\ A}{8 \times 400\ kHz \times 100\ \mu F} + 1\ A \times 10\ m\Omega = 13.1\ mV \quad (21)$$

$$\Delta V_{OUTA} = \frac{\Delta I_{OUTA}}{4 \times f_C \times C_{OUTA}} + \Delta I_{OUTA} \times ESR = \frac{2.9\ A}{4 \times 50\ kHz \times 100\ \mu F} + 2.9\ A \times 10\ m\Omega = 174\ mV \quad (22)$$

Bandwidth of Buck Converter f_C

Use the following guidelines to set frequency poles, zeroes, and crossover values for the trade-off between stability and transient response.

- Crossover frequency f_C between f_{SW} / 6 and f_{SW} / 10. Assume f_C = 50 kHz.
- Select the zero $f_z \approx f_C$ / 10
- Make the second pole $f_{P2} \approx f_{SW}$ / 2

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Selection of Components for Type II Compensation

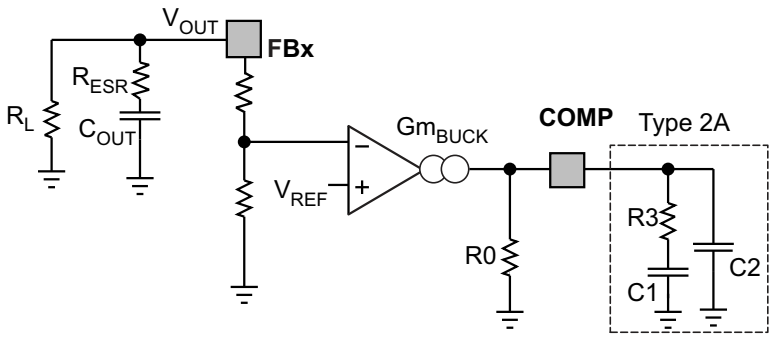

Figure 26. Buck Compensation Components

$$R3 = \frac{2\pi \times f_C \times V_{OUTA} \times C_{OUTA}}{Gm_{BUCK} \times K_{CFB} \times V_{REF}} = \frac{2\pi \times 50\ kHz \times 3.4\ V \times 100\ \mu F}{Gm_{BUCK} \times K_{CFB} \times V_{REF}} = 19\ k\Omega$$

Use standard value of R3 = 18 kΩ

where:

- V_O = 3.4 V
- C_O = 100 µF
- Gm = 1 mS
- V_{REF} = 0.8 V
- K_{CFB} = 0.125 / R_{SENSE} = 6.9 (0.125 is an internal constant)

(23)

$$C1 = \frac{10}{2\pi \times R3 \times f_C} = \frac{10}{2\pi \times 18\ k\Omega \times 50\ kHz} = 1.8\ nF$$

(24)

Use standard value of 1.8 nF.

$$C2 = \frac{C1}{2\pi \times R3 \times C1\left(\frac{f_{SW}}{2}\right) - 1} = \frac{1.8\ nF}{2\pi \times 18\ k\Omega \times 1.8\ nF\left(\frac{400\ kHz}{2}\right) - 1} = 45\ pF$$

(25)

Use standard value of 47 pF.

The resulting bandwidth of buck converter f_C

$$f_C = \frac{Gm_{BUCK} \times R3 \times K_{CFB}}{2\pi \times C_{OUTA}} \times \frac{V_{REF}}{V_{OUT}}$$

$$f_C = \frac{1\,mS \times 18\ k\Omega \times 6.9\ S \times 0.8\ V}{2\pi \times 100\ \mu F \times 3.4\ V} = 46.5\ kHz$$

(26)

f_C is close to the target bandwidth of 50 kHz.

The resulting zero frequency f_{Z1}

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} = \frac{1}{2\pi \times 18\ k\Omega \times 1.8\ nF} = 4.9\ kHz$$

(27)

f_{Z1} is close to the f_C / 10 guideline of 5 kHz

The second pole frequency f_{P2}

$$f_{P2} = \frac{1}{2\pi \times R3 \times C2} = \frac{1}{2\pi \times 18\ k\Omega \times 47\ pF} = 188\ kHz$$

(28)

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f_{P2} is close to the f_{SW} / 2 guideline of 200 kHz. Hence, all requirements for a good loop response are satisfied.

BuckB Component Selection

Using the same method as VBUCKA, the following parameters and components are realized in Equation 29.

$$t_{ON\,min} = \frac{V_{OUTB}}{V_{IN\,max} \times f_{SW}} = \frac{1.235\ V}{30\ V \times 400\ kHz} = 103\ ns \tag{29}$$

This t_{ONmin} is on the edge of the minimum duty cycle specified (100 ns, typical); expect pulse-skipping at high V_{IN}.

$$R_{SENSE} = \frac{60\ mV}{2A} = 30\ m\Omega$$

$$L = 200 \times \frac{30\ m\Omega}{400\ kHz} = 15\ \mu H$$

choose 30 mΩ, 15 µH.

- ΔI_{ripple} current ≈ 0.4 A (approx. 20% of $I_{O\ max}$)

Select an output capacitance C_O of 100 µF with low ESR in the range of 10 mΩ. This gives ΔV_O (ripple) ≈ 7.5 mV and ΔV drop of ≈ 120 mV during a load step.

Assume f_C = 50 kHz.

$$C_{OUTB} \approx \frac{2 \times \Delta I_{OUTB}}{f_{SW} \times \Delta V_{OUTB}} = \frac{2 \times 1.9\ A}{400\ kHz \times 0.12\ V} = 46\ \mu F \tag{30}$$

$$V_{OUTB(Ripple)} = \frac{I_{OUTB(Ripple)}}{8 \times f_{SW} \times C_{OUTB}} + I_{OUTB(Ripple)} \times ESR = \frac{0.4\ A}{8 \times 400\ kHz \times 100\ \mu F} + 0.4\ A \times 10\ m\Omega = 5.3\ mV \tag{31}$$

$$\Delta V_{OUTB} = \frac{\Delta I_{OUTB}}{4 \times f_C \times C_{OUTB}} + \Delta I_{OUTB} \times ESR = \frac{1.9\ A}{4 \times 50\ kHz \times 100\ \mu F} + 1.9\ A \times 10\ m\Omega = 114\ mV \tag{32}$$

$$R3 = \frac{2\pi \times f_C \times V_{OUTB} \times C_{OUTB}}{Gm_{BUCK} \times K_{CFB} \times V_{REF}}$$

$$= \frac{2\pi \times 50\ kHz \times 1.235\ V \times 100\ \mu F}{1\,mS \times 4.16S \times 0.8V} = 11.7\ k\Omega \tag{33}$$

Use standard value of R3 = 12 kΩ.

$$C1 = \frac{10}{2\pi \times R3 \times f_C} = \frac{10}{2\pi \times 12\ k\Omega \times 50\ kHz} = 2.7\ nF, \quad \text{choose } 2.7\,nF \tag{34}$$

$$C2 = \frac{C1}{2\pi \times R3 \times C1 \times \left(\frac{f_{SW}}{2}\right) - 1}$$

$$= \frac{2.7\ nF}{2\pi \times 12\ k\Omega \times 2.7\ nF \times \left(\frac{400\ kHz}{2}\right) - 1} = 68\ pF, \quad \text{choose } 68\ pF \tag{35}$$

$$f_C = \frac{Gm_{BUCK} \times R3 \times K_{CFB}}{2\pi \times C_{OUTB}} \times \frac{V_{REF}}{V_O}$$

$$f_C = \frac{1\,mS \times 12\ k\Omega \times 4.16 \times 0.8}{2\pi \times 100\ \mu F \times 1.235\ V} = 51.5\ kHz \tag{36}$$

f_C is close to the target bandwidth of 50 kHz.

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The resulting zero frequency f_{Z1}

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} = \frac{1}{2\pi \times 12\ k\Omega \times 2.7\ nF} = 4.9\ kHz$$

f_{Z1} is close to the f_C / 10 guideline of 5 kHz.

The second pole frequency f_{P2}

$$f_{P2} = \frac{1}{2\pi \times R3 \times C2} = \frac{1}{2\pi \times 12 k\Omega \times 68\ pF} = 195\ kHz \quad (37)$$

f_{P2} is close to the f_{SW} / 2 guideline of 200 kHz.

Hence, all requirements for a good loop response are satisfied.

BuckX High-Side and Low-Side N-Channel MOSFETs

The gate-drive supply for these MOSFETs is supplied by an internal supply which is 5.8 V (typical) under normal operating conditions. The output is a totem pole, allowing full voltage drive of V_{REG} to the gate with peak output current of 1.2 A. The high-side MOSFET is referenced to a floating node at the phase terminal (PHx) and the low-side MOSFET is referenced to the power ground (PGx) terminal. For a particular application, these MOSFETs should be selected with consideration for the following parameters: $r_{ds(on)}$, gate charge Qg, drain-to-source breakdown voltage BVDSS, maximum dc current IDC(max), and thermal resistance for the package.

The times t_r and t_f denote the rising and falling times of the switching node and are related to the gate-driver strength of the TPS43337-Q1 and gate Miller capacitance of the MOSFET. The first term denotes the conduction losses, which are minimized when the on-resistance of the MOSFET is low. The second term denotes the transition losses, which arise due to the full application of the input voltage across the drain-source of the MOSFET as it turns on or off. They are lower at low currents and when the switching time is low.

$$P_{BuckTOPFET} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times D + \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times (t_r + t_f) \times f_{SW} \quad (38)$$

$$P_{BuckLOWERFET} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times (1 - D) + V_F \times I_{OUT} \times (2 \times t_d) \times f_{SW} \quad (39)$$

In addition, during the dead time t_d when both the MOSFETs are off, the body diode of the low-side MOSFET conducts, increasing the losses which is denoted by the second term in the Equation 39. Using external Schottky diodes in parallel to the low-side MOSFETs of the buck converters helps to reduce this loss.

Note that $r_{DS(on)}$ has a positive temperature coefficient which is accounted for in the TC term for $r_{DS(on)}$, TC = d × ΔT[°C]. The temperature coefficient, d, is available as a normalized value from MOSFET data sheets and can be assumed to be 0.005 / ºC as a starting value.

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Schematic

The following section summarizes the previously calculated example and gives a schematic and component proposals.

Table 4. Application Example

PARAMETER	V_{BUCKA}	V_{BUCKB}	BOOST
Input voltage	V_{IN} = 6 to 30 V 12 V - typical	V_{IN} = 6 to 30 V 12 V - typical	V_{BAT} = 5 (cranking pulse input) to 30 V
Output voltage, V_{OUTx}	3.396 V	1.235 V	10 V
Maximum output current, I_{OUTx}	3 A	2 A	2.5 A
Load-step output tolerance, $\Delta V_{OUT} + \Delta V_{OUT(Ripple)}$	±0.2 V	±0.12 V	±0.5 V
Current output load step, ΔI_{OUTx}	0.1 to 3 A	0.1 to 2 A	0.1 to 2.5 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz	200 kHz

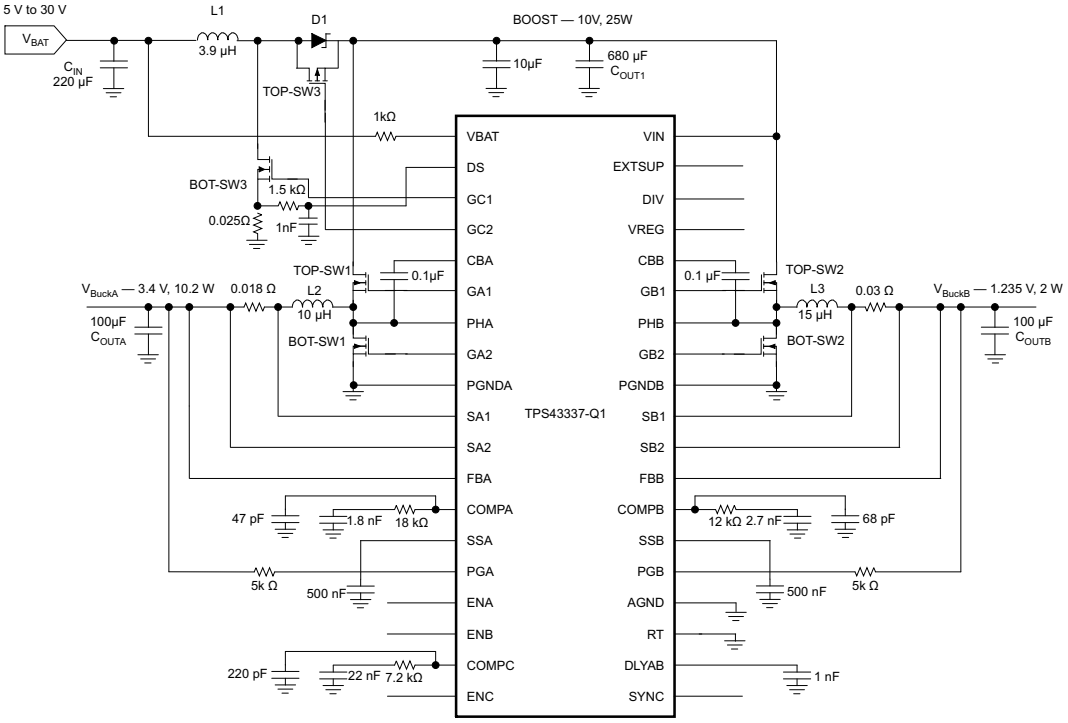

Figure 27. *Schematic - Application Example*

Table 5. Application Example - Component Proposals

Name	Component Proposal	Value
L1	MSS1278T-392NL (Coilcraft)	3.9 µH
L2	MSS1278T-103ML (Coilcraft)	10 µH
L3	MSS1278T-153ML (Coilcraft)	15 µH
D1	SK103 (Micro Commercial Components)	
TOP_SW3	IRF7416 (International Rectifier)	
TOP_SW1, TOP_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW1, BOT_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW3	IRFR3504ZTRPBF (International Rectifier)	
COUT1	EEVFK1J681M (Panasonic)	680 µF
C_{OUTA}, C_{OUTB}	ECASD91A107M010K00 (Murata)	100 µF
C_{IN}	EEVFK1J221Q (Panasonic)	220 µF

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Power Dissipation Derating Profile, 38-Pin HTTSOP Package With PowerPAD Package

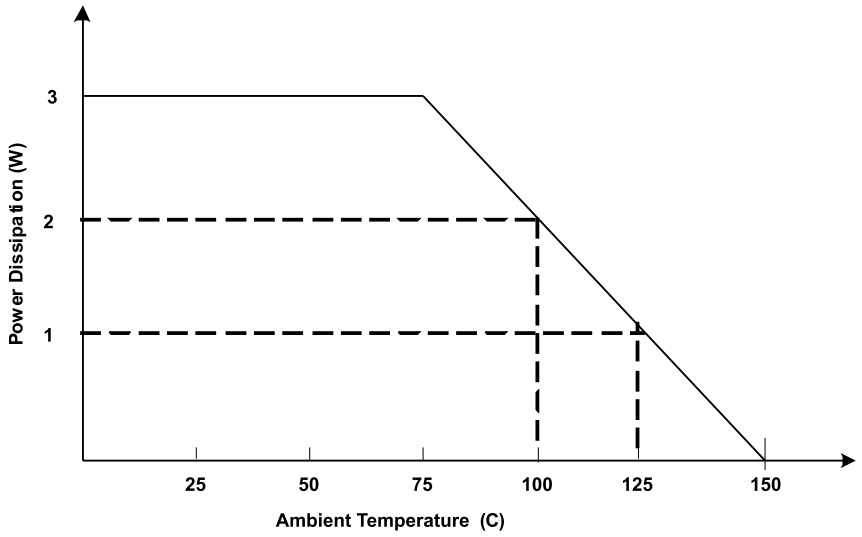

Figure 28. Power Dissipation Derating Profile Based on High-K JEDEC PCB

PCB Layout Guidelines

Grounding and PCB Circuit Layout Considerations

Boost Converter

1. The path formed from the input capacitor to the inductor and BOT_SW3 with the low-side current-sense resistor should have short leads and PC trace lengths. The same applies for the trace from the inductor to the Schottky diode D1 to the COUT1 capacitors. The negative terminal of the input capacitor and the negative terminal of the sense resistor must be connected together with short trace lengths.
2. The overcurrent-sensing shunt resistor may require noise filtering, and this capacitor should be close to the IC pin.

Buck Converter

1. Connect the drains of TOP_SW1 and TOP_SW2 together with the positive terminal of input capacitor COUT1. The trace length between these terminals should be short.
2. Connect a local decoupling capacitor between the drain of TOP_SWx and the source of BOT_SWx.
3. The Kelvin-current sensing traces for the shunt resistor should have minimum trace spacing and be routed parallel to each other. Any filtering capacitors for noise should be placed near the IC pins.
4. Connect the positive terminal of the respective output capacitor C_{OUTA} or C_{OUTB} to the respective feedback input FBA or FBB. Do not connect these traces near any switching nodes or high-current traces.

Other Considerations

1. PGNDx and AGND should be shorted to the thermal pad. Use a star-ground configuration if connecting to a non-ground-plane system. Use tie-ins for the EXTSUP capacitor, compensation-network ground, and voltage-sense-feedback ground networks to this star ground.
2. Connect a compensation network between the compensation pins and IC signal ground. Connect the oscillator resistor (frequency setting) between the RT pin and IC signal ground. These sensitive circuits should not be located near nodes showing high dv/dt; these include the gate-drive outputs, phase pins, and boost circuits (bootstrap).
3. Reduce the surface area of the high-current-carrying loops to a minimum, by ensuring optimal component placement. Ensure the bypass capacitors are located as close as possible to their respective power and ground pins.

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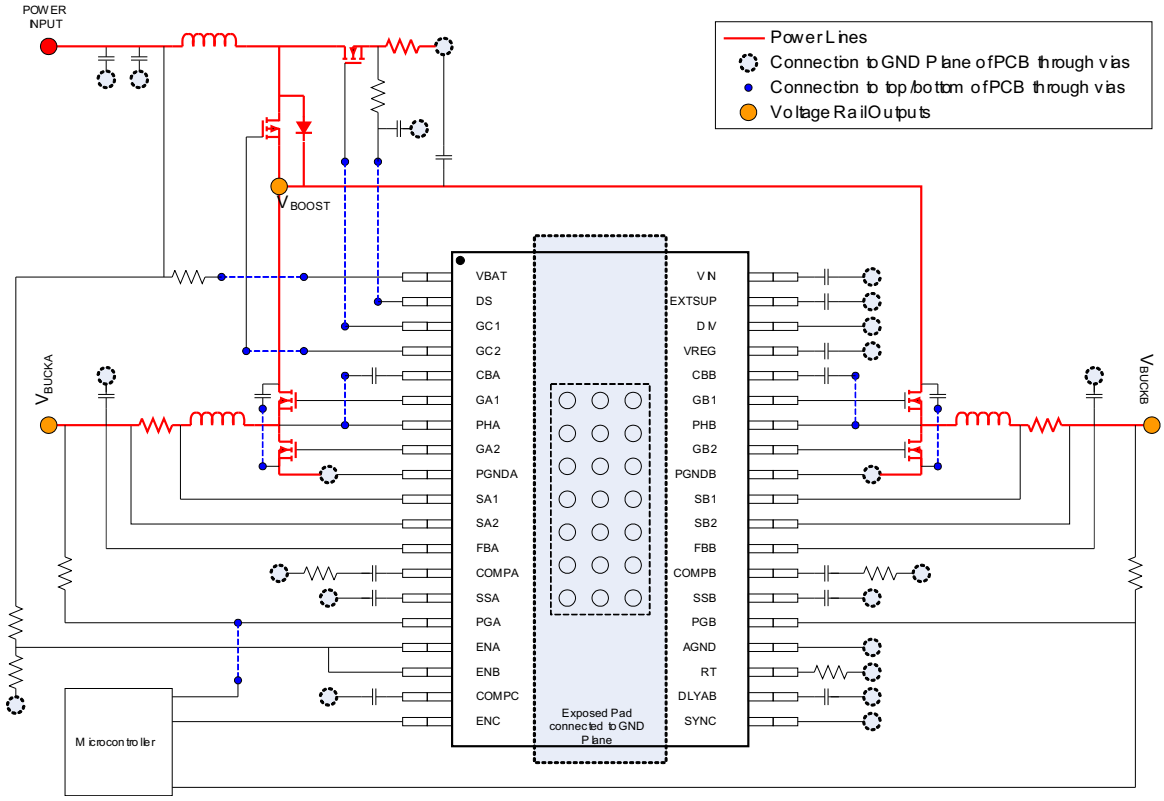
PCB Layout


POWER INPUT
Power Lines
Connection to GND Plane of PCB through vias
Connection to top/bottom of PCB through vias
Voltage Rail Outputs
VBOOST
VBUCKA
VBUCKB
VBAT
DS
GC1
GC2
CBA
GA1
PHA
GA2
PGNDA
SA1
SA2
FBA
COMPA
SSA
PGA
ENA
ENB
COMPC
ENC
VIN
EXTSUP
DIV
VREG
CBB
GB1
PHB
GB2
PGNDB
SB1
SB2
FBB
COMPB
SSB
PGB
AGND
RT
DLYAB
SYNC
Exposed Pad connected to GND Plane
Microcontroller

REVISION HISTORY

Changes from Original (August 2013) to Revision A	Page
• Changed document status from *Product Preview* to *Production Data*	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS43337QDAPRQ1	ACTIVE	HTSSOP	DAP	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS43337	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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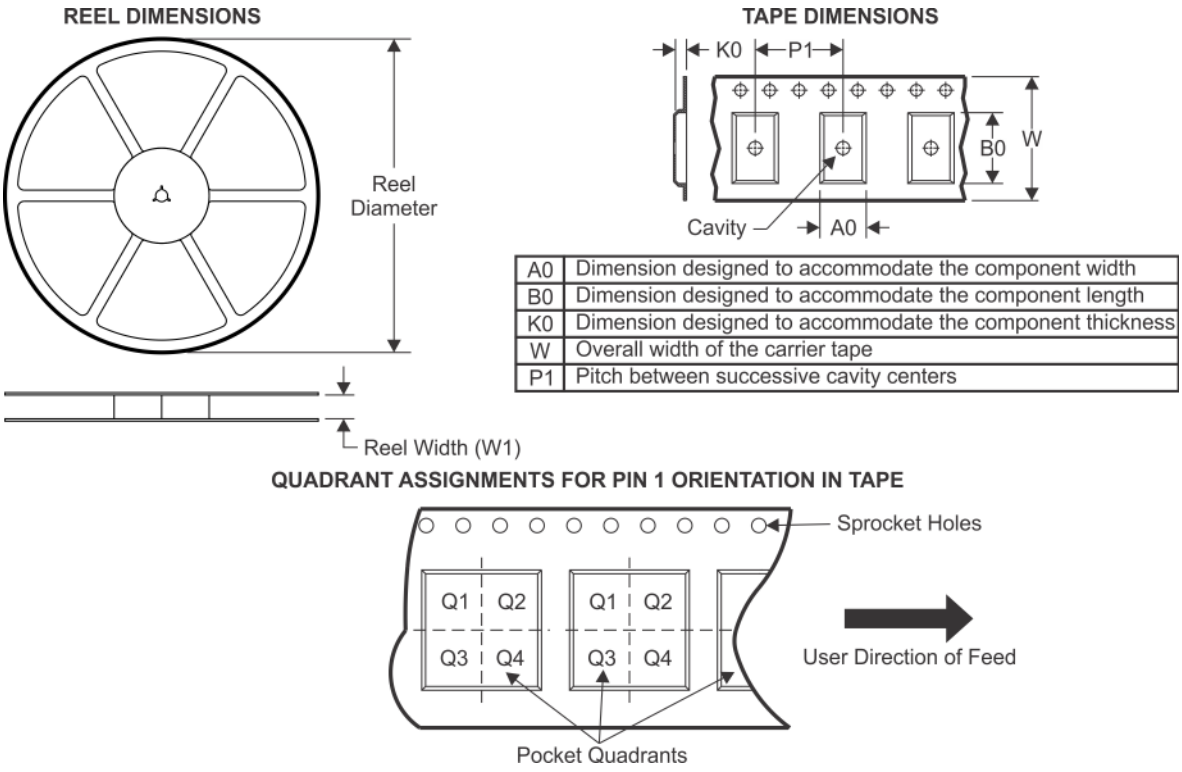
TAPE AND REEL INFORMATION

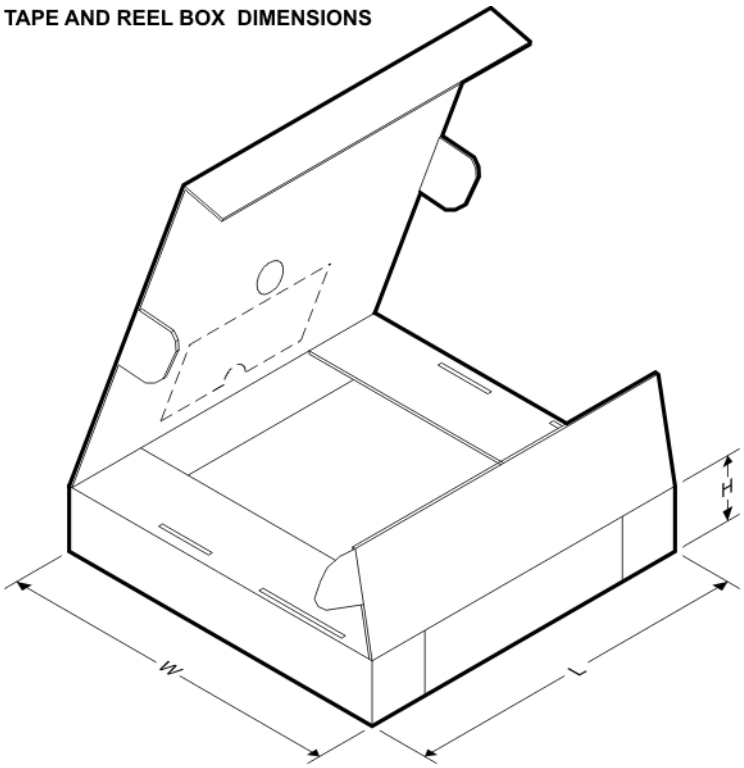


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS43337QDAPRQ1	HTSSOP	DAP	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

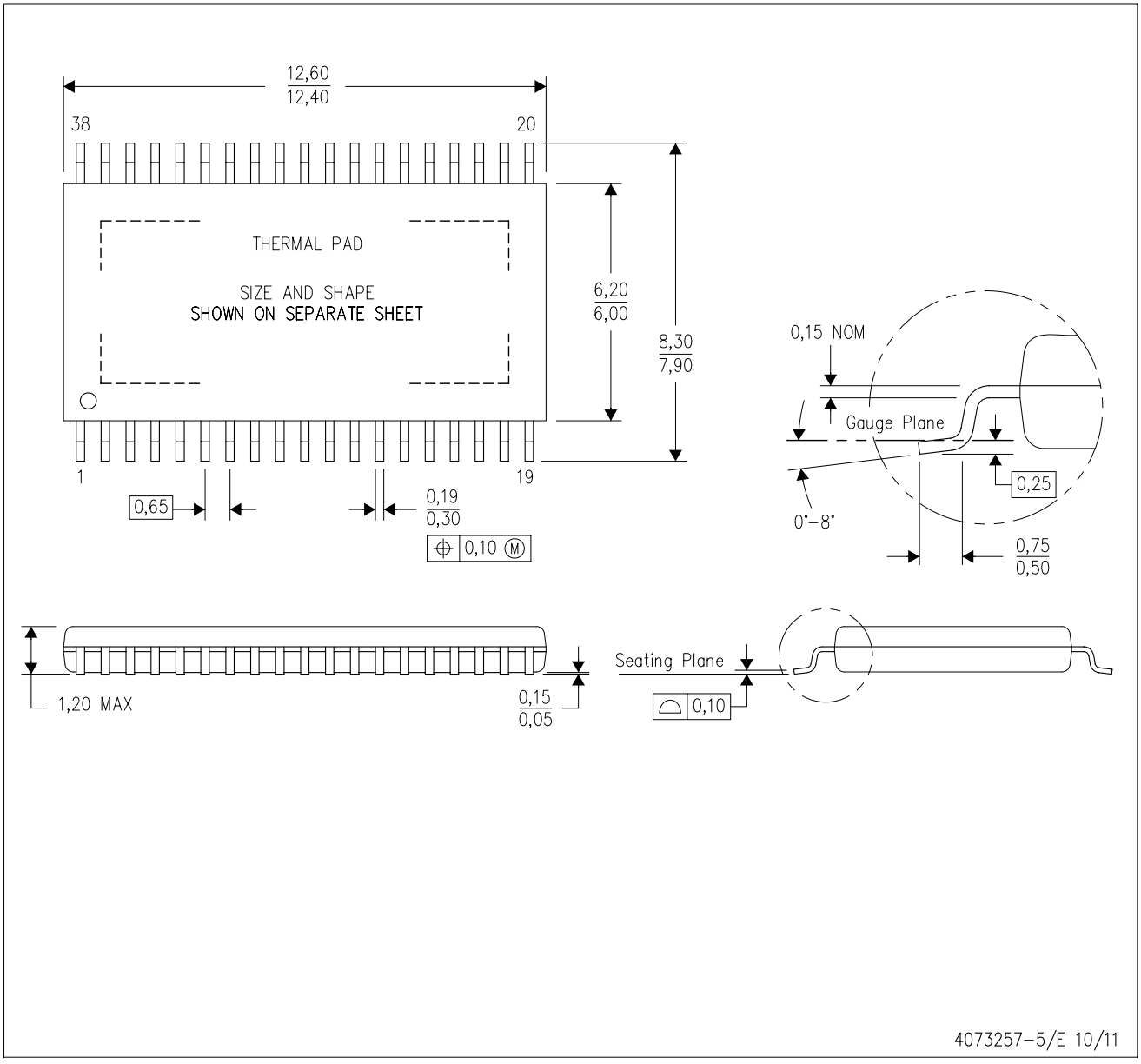
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS43337QDAPRQ1	HTSSOP	DAP	38	2000	350.0	350.0	43.0

DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153 Variation DDT–1.

PowerPAD is a trademark of Texas Instruments.

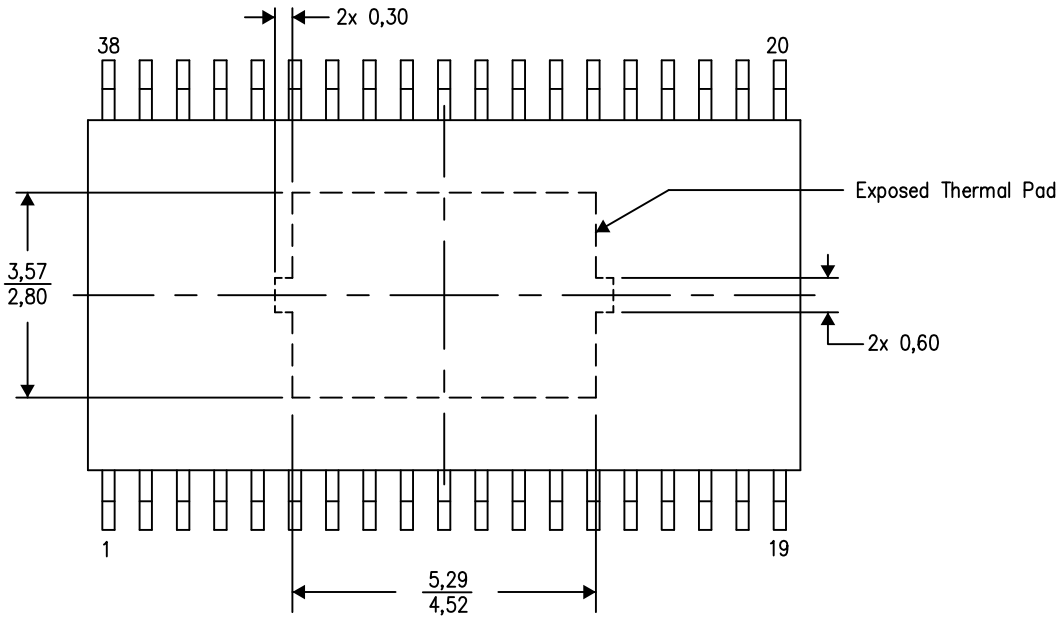
DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206319–9/M 09/13

NOTE: All linear dimensions are in millimeters

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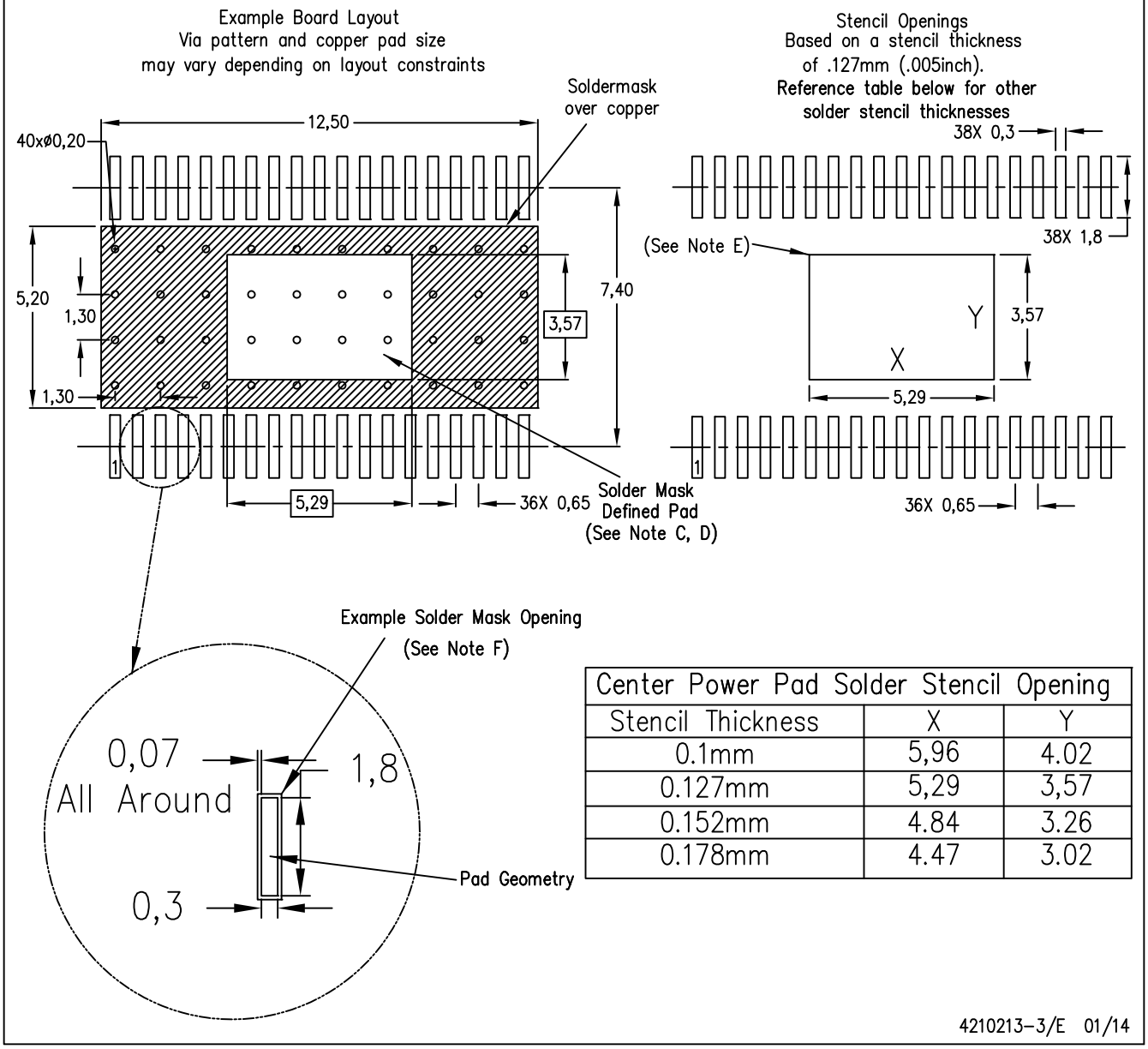
DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5,96	4.02
0.127mm	5,29	3,57
0.152mm	4.84	3.26
0.178mm	4.47	3.02

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

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