# TinyLogic UHS Dual Inverting Buffer with 3-STATE Outputs

## NC7WZ240

**MARKING DIAGRAMS**

UQFN8
1.6X1.6, 0.5P
CASE 523AY

U7KK
XYZ

US8
CASE 846AN

WZ40
ALYW

| U7, WZ40 | = Specific Device Code |
| KK | = 2−Digit Lot Run Traceability Code |
| XY | = 2−Digit Date Code Format |
| Z | = Assembly Plant Code |
| A | = Assembly Location |
| L | = Wafer Lot Number |
| YW | = Assembly Start Week |

### Description

The NC7WZ240 is a Dual Inverting Buffer with independent active LOW enables for the 3−STATE outputs. The Ultra High Speed device is fabricated with advanced CMOS technology to achieve superior switching performance with high output drive while maintaining low static power dissipation over a broad $V_{CC}$ operating range. The device is specified to operate over the 1.65 V to 5.5 V $V_{CC}$ operating range. The inputs and outputs are high impedance when $V_{CC}$ is 0 V. Inputs tolerate voltages up to 5.5 V independent of $V_{CC}$ operating range. Outputs tolerate voltages above $V_{CC}$ when in the 3−STATE condition.

### Features

- Space Saving US8 Surface Mount Package
- MicroPak™ Pb−Free Leadless Package
- Ultra High Speed: $t_{PD}$ = 2.3 ns Typ. into 50 pF at 5 V $V_{CC}$
- High Output Drive: ±24 mA at 3 V $V_{CC}$
- Broad $V_{CC}$ Operating Range: 1.65 V to 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V $V_{CC}$
- Power Down High Impedance Inputs / Outputs
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Outputs are Overvoltage Tolerant in 3−STATE Mode
- Proprietary Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
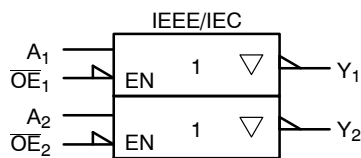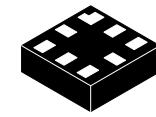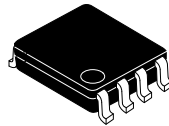
### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

**Figure 1. Logic Symbol**

**September, 2022 – Rev. 4**

Publication Order Number:
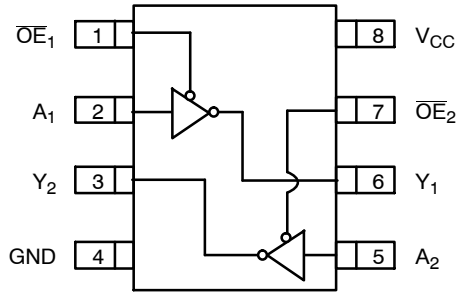**NC7WZ240/D**

# NC7WZ240

**Connection Diagrams**



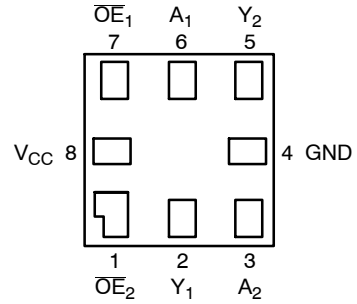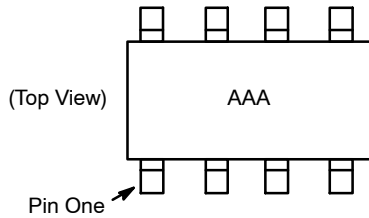**Figure 2. Pin Assignments for US8
(Top View)**



**Figure 4. Pad Assignments for MicroPak
(Top Thru View)**



AAA represents Product Code Top Mark – see ordering code

NOTE: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

**Figure 3. Pin One Orientation Diagram**

## PIN DESCRIPTIONS

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Enable Inputs for 3−STATE Outputs |
| $A_n$ | Inputs |
| $Y_n$ | 3−STATE Outputs |

## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| $\overline{OE}$ | $A_n$ | $Y_n$ |
| L | L | H |
| L | H | L |
| H | L | Z |
| H | H | Z |

H = HIGH Logic Level
L = LOW Logic Level
Z = 3−STATE

# NC7WZ240

**ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | −0.5 | 6.5 | V |
| $V_{IN}$ | DC Input Voltage (Note 1) | | −0.5 | 6.5 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 | 6.5 | V |
| $I_{IK}$ | DC Input Diode Current | $V_{IN} < 0$ V | − | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT} < 0$ V | − | −50 | mA |
| $I_{OUT}$ | DC Output Source / Sink Current | | − | ±50 | mA |
| $I_{CC}$ / $I_{GND}$ | DC $V_{CC}$ / Ground Current | | − | ±50 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 | +150 | °C |
| $T_J$ | Junction Lead Temperature under Bias | | − | +150 | °C |
| $T_L$ | Junction Lead Temperature (Soldering, 10 Seconds) | | − | +260 | °C |
| $P_D$ | Power Dissipation in Still Air | US8 | − | 500 | mW |
| | | MicroPak−8 | − | 539 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1.  The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage Operating | | 1.65 | 5.5 | V |
| | Supply Voltage Data Retention | | 1.5 | 5.5 | |
| $V_{IN}$ | Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | Output Voltage | Active State | 0 | $V_{CC}$ | V |
| | | 3−STATE | 0 | 5.5 | V |
| $T_A$ | Operating Temperature | | −40 | +85 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ @ 1.8 V ±0.15 V, 2.5 V ±0.2 V | 0 | 20 | ns/V |
| | | $V_{CC}$ @ 3.3 V ±0.3 V | 0 | 10 | |
| | | $V_{CC}$ @ 5.0 V ±0.5 V | 0 | 5 | |
| $\theta_{JA}$ | Thermal Resistance | US8 | − | 250 | °C/W |
| | | MicroPak−8 | − | 232 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2.  Unused inputs must be held HIGH or LOW. They may not float.

# NC7WZ240

## DC ELECTICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | | V_CC (V) | T_A = +25°C | | | T_A = −40 to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | | 1.65 to 1.95 | 0.65 $V_{CC}$ | – | – | 0.65 $V_{CC}$ | – | V |
| | | | | 2.3 to 5.5 | 0.7 $V_{CC}$ | – | – | 0.7 $V_{CC}$ | – | |
| $V_{IL}$ | LOW Level Input Voltage | | | 1.65 to 1.95 | – | – | 0.35 $V_{CC}$ | – | 0.35 $V_{CC}$ | V |
| | | | | 2.3 to 5.5 | – | – | 0.3 $V_{CC}$ | – | 0.3 $V_{CC}$ | |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -100\ \mu A$ | 1.65 | 1.55 | 1.65 | – | 1.55 | – | V |
| | | | | 2.3 | 2.2 | 2.3 | – | 2.2 | – | |
| | | | | 3.0 | 2.9 | 3.0 | – | 2.9 | – | |
| | | | | 4.5 | 4.4 | 4.5 | – | 4.4 | – | |
| | | | $I_{OH} = -4\ mA$ | 1.65 | 1.29 | 1.52 | – | 1.29 | – | |
| | | | $I_{OH} = -8\ mA$ | 2.3 | 1.9 | 2.15 | – | 1.9 | – | |
| | | | $I_{OH} = -16\ mA$ | 3.0 | 2.4 | 2.80 | – | 2.4 | – | |
| | | | $I_{OH} = -24\ mA$ | 3.0 | 2.3 | 2.68 | – | 2.3 | – | |
| | | | $I_{OH} = -32\ mA$ | 4.5 | 3.8 | 4.20 | – | 3.8 | – | |
| $V_{OL}$ | LOW Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 100\ \mu A$ | 1.65 | – | 0.0 | 0.10 | – | 0.10 | V |
| | | | | 2.3 | – | 0.0 | 0.10 | – | 0.10 | |
| | | | | 3.0 | – | 0.0 | 0.10 | – | 0.10 | |
| | | | | 4.5 | – | 0.0 | 0.10 | – | 0.10 | |
| | | | $I_{OL} = 4\ mA$ | 1.65 | – | 0.08 | 0.24 | – | 0.24 | |
| | | | $I_{OL} = 8\ mA$ | 2.3 | – | 0.10 | 0.3 | – | 0.3 | |
| | | | $I_{OL} = 16\ mA$ | 3.0 | – | 0.15 | 0.4 | – | 0.4 | |
| | | | $I_{OL} = 24\ mA$ | 3.0 | – | 0.22 | 0.55 | – | 0.55 | |
| | | | $I_{OL} = 32\ mA$ | 4.5 | – | 0.22 | 0.55 | – | 0.55 | |
| $I_{IN}$ | Input Leakage Current | $V_{IN} = 5.5$ V, GND | | 1.65 to 5.5 | – | – | ±0.1 | – | ±1 | μA |
| $I_{OZ}$ | 3–STATE Output Leakage | $V_{IN} = V_{IH}$ or $V_{IL}$ $0 \leq V_{OUT} \leq 5.5$ V | | 1.65 to 5.5 | – | – | ±0.5 | – | ±5 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{IN}$ or $V_{OUT} = 5.5$ V | | 0.0 | – | – | 1 | – | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{IN} = 5.5$ V, GND | | 1.65 to 5.5 | – | – | 1 | – | 10 | μA |

## NOISE CHARACTERISTICS

| Symbol | Parameter | Conditions | V_CC (V) | T_A = +25°C | | Unit |
|---|---|---|---|---|---|---|
| | | | | Typ | Max | |
| $V_{OLP}$ (Note 3) | Quiet Output Maximum Dynamic $V_{OL}$ | $C_L = 50$ pF | 5.0 | – | 1.0 | V |
| $V_{OLV}$ (Note 3) | Quiet Output Minimum Dynamic $V_{OL}$ | $C_L = 50$ pF | 5.0 | – | 1.0 | V |
| $V_{OHV}$ (Note 3) | Quiet Output Minimum Dynamic $V_{OH}$ | $C_L = 50$ pF | 5.0 | – | 4.0 | V |
| $V_{IHD}$ (Note 3) | Minimum HIGH Level Dynamic Input Voltage | $C_L = 50$ pF | 5.0 | – | 3.5 | V |
| $V_{ILD}$ (Note 3) | Maximum LOW Level Dynamic Input Voltage | $C_L = 50$ pF | 5.0 | – | 1.5 | V |

3. Parameter guaranteed by design.

# NC7WZ240

## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = +25°C | | | $T_A$ = −40 to +85°C | | Unit |
|--------|-----------|------------|--------------|-----|-----|-----|-----|-----|------|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay $A_n$ to $Y_n$ (Figure 5, 7) | $C_L$ = 15 pF $R_D$ = 1 MΩ S1 = Open | 1.8 ±0.15 | – | – | 12.0 | – | 13.0 | ns |
| | | | 2.5 ±0.2 | – | – | 7.5 | – | 8.0 | |
| | | | 3.3 ±0.3 | – | – | 5.2 | – | 5.5 | |
| | | | 5.0 ±0.5 | – | – | 4.5 | – | 4.8 | |
| | | $C_L$ = 50 pF, $R_D$ = 500 Ω S1 = Open | 3.3 ±0.3 | – | – | 5.7 | – | 6.0 | |
| | | | 5.0 ±0.5 | – | – | 5.0 | – | 5.3 | |
| $t_{OSLH}$, $t_{OSHL}$ | Output to Output Skew (Note 4) (Figure 5, 7) | $C_L$ = 50 pF, $R_D$ = 500 Ω S1 = Open | 3.3 ±0.3 | – | – | 1.0 | – | 1.0 | ns |
| | | | 5.0 ±0.5 | – | – | 0.8 | – | 0.8 | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time (Figure 5, 7) | $C_L$ = 50 pF $R_D$,$R_U$ = 500 Ω S1 = GND for $t_{PZH}$ S1 = $V_I$ for $t_{PZL}$ $V_I$ = 2 x $V_{CC}$ | 1.8 ±0.15 | – | – | 14.0 | – | 15.0 | ns |
| | | | 2.5 ±0.2 | – | – | 8.5 | – | 9.0 | |
| | | | 3.3 ±0.3 | – | – | 6.2 | – | 6.5 | |
| | | | 5.5 ±0.5 | – | – | 5.5 | – | 5.8 | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time (Figure 5, 7) | $C_L$ = 50 pF $R_D$,$R_U$ = 500 Ω S1 = GND for $t_{PZH}$ S1 = $V_I$ for $t_{PZL}$ $V_I$ = 2 x $V_{CC}$ | 1.8 ±0.15 | – | – | 12.0 | – | 13.0 | ns |
| | | | 2.5 ±0.2 | – | – | 8.0 | – | 8.5 | |
| | | | 3.3 ±0.3 | – | – | 5.7 | – | 6.0 | |
| | | | 5.0 ±0.5 | – | – | 4.7 | – | 5.0 | |
| $C_{IN}$ | Input Capacitance | | 0 | – | 2.5 | – | – | – | pF |
| $C_{OUT}$ | Output Capacitance | | 5.0 | – | 4 | – | – | – | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Figure 6) | (Note 5) | 3.3 | – | 10 | – | – | – | pF |
| | | | 5.0 | – | 12 | – | – | – | |

4. Parameter guaranteed by design. $t_{OSLH}$ = |$t_{PLHmax}$ − $t_{PLHmin}$|; $t_{OSHL}$ = |$t_{PHLmax}$ − $t_{PHLmin}$|.
5. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading and operating at 50% duty cycle. (see Figure 6) $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD}$ = ($C_{PD}$) ($V_{CC}$) ($f_{IN}$) + ($I_{CC}$static).

**AC Loading and Waveforms**
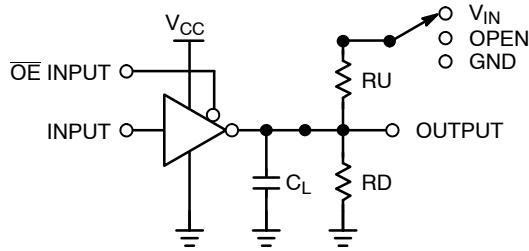


$C_L$ includes load and stray capacitance
Input PRR = 1.0 MHz; $t_W$ = 500 ns

**Figure 5. AC Test Circuit**
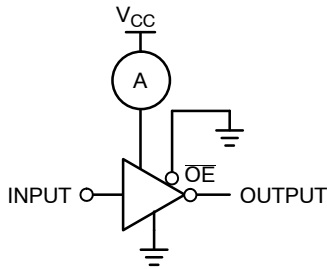


Input = AC Waveform; $t_r = t_f$ = 1.8 ns;
PRR = 10 MHz; Duty Cycle = 50%.

**Figure 6. I$_{CCD}$ Test Circuit**
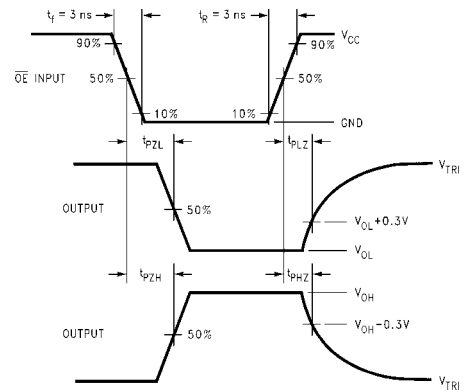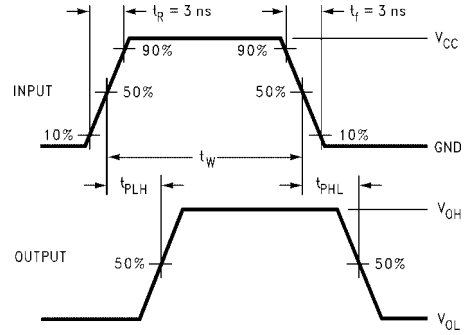


**Figure 7. AC Waveforms**

**ORDERING INFORMATION**

| Order Number | Top Mark | Package | Shipping† |
|---|---|---|---|
| NC7WZ240K8X | WZ40 | 8–Lead US8, JEDEC MO–187, Variation CA 3.1 mm Wide | 3000 / Tape & Reel |
| NC7WZ240K8X–L22236 | WZ40 | 8–Lead US8, JEDEC MO–187, Variation CA 3.1 mm Wide | 3000 / Tape & Reel |
| NC7WZ240L8X | U7 | 8–Lead MicroPak, 1.6 mm Wide (Pb–Free) | 5000 / Tape & Reel |
| NC7WZ240L8X–L22185 | U7 | 8–Lead MicroPak, 1.6 mm Wide (Pb–Free) | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
6.  Pb–Free package per JEDEC J–STD–020B.

**UQFN8 1.6X1.6, 0.5P**
CASE 523AY
ISSUE O

DATE 31 AUG 2016



PIN#1 IDENT

TOP VIEW
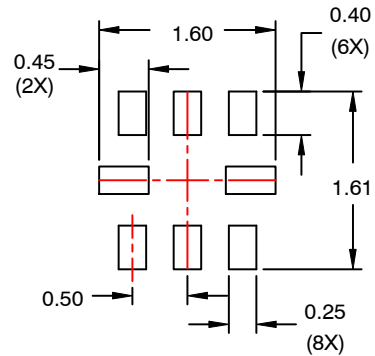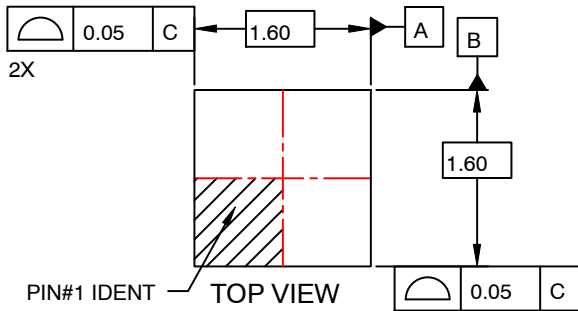


RECOMMENDED
LAND PATTERN



SEATING
PLANE
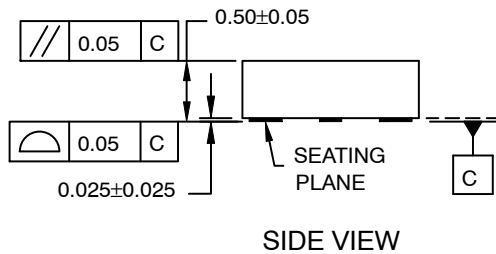
SIDE VIEW

NOTES:

A. PACKAGE CONFORMS TO JEDEC MO−255 VARIATION UAAD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
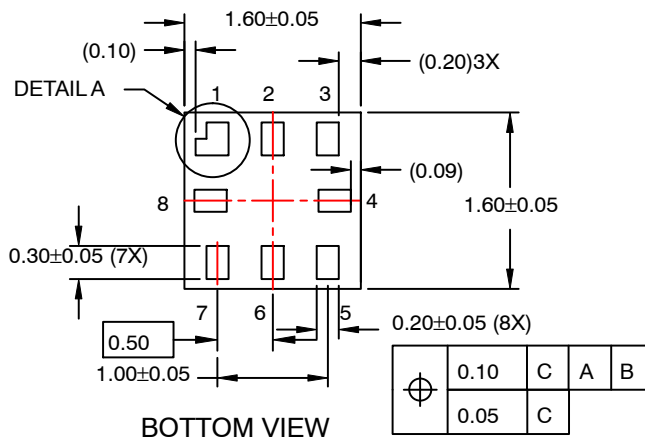


DETAIL A

BOTTOM VIEW
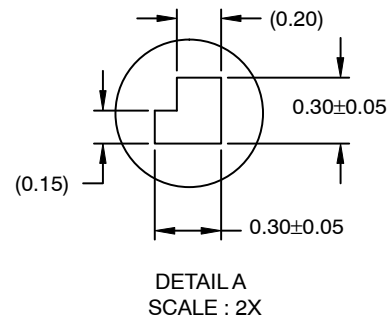


DETAIL A
SCALE : 2X

| DOCUMENT NUMBER: | 98AON13591G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| DESCRIPTION: | UQFN8 1.6X1.6, 0.5P | | PAGE 1 OF 1 |

**US8**
CASE 846AN
ISSUE O

DATE 31 DEC 2016

**TOP VIEW**

2.10 / 1.90

0.15

8    5

B

A

3.20 / 3.00

2.40 / 2.20

1.55

PIN 1 IDENT

1    4

⌒ 0.2 C B A

**ALL LEAD TIPS**

**RECOMMENDED LAND PATTERN**

1.80

(8X) 0.70

1.00

2.70    3.40

0.50    0.30 (8X)

**SIDE VIEW**

0.90 MAX

0.80 / 0.60

0.10 / 0.00

⌒ 0.1 C

**ALL LEAD TIPS**

SEATING PLANE

C

0.50    0.17-0.27 (8X)

⊕ 0.13 Ⓜ A BⓈ CⓈ
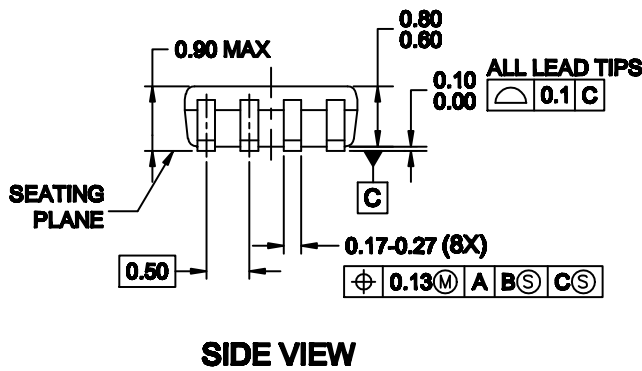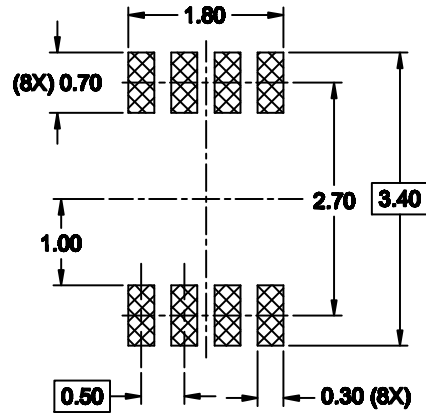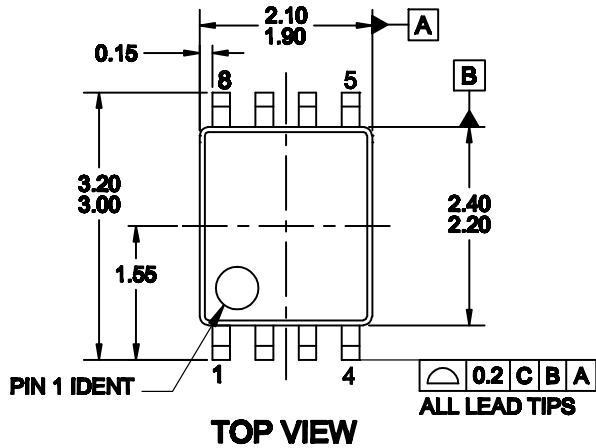
**NOTES:**

A. CONFORMS TO JEDEC REGISTRATION MO-187

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.

**DETAIL A**

0.4 TYP

GAGE PLANE

0.12

0°-8°

0.20-0.35

SEATING PLANE

DETAIL A

0.10-0.18
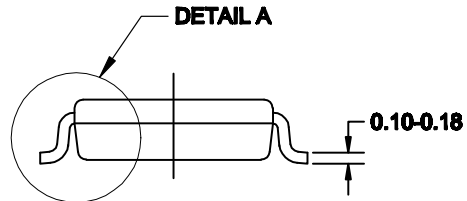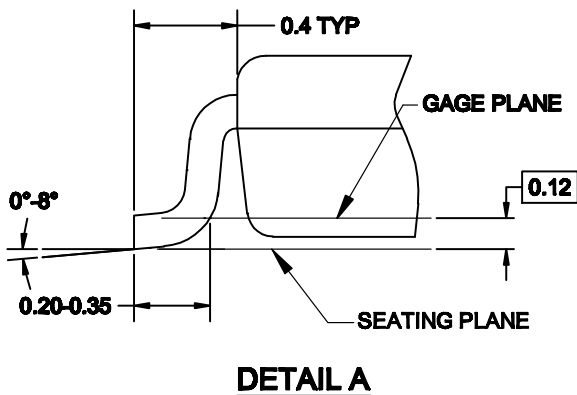
| DOCUMENT NUMBER: | 98AON13778G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| DESCRIPTION: | US8 | | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical–documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
www.onsemi.com/support/sales

◊