M8284A
CLOCK GENERATOR AND DRIVER

Military

- **Military Temperature Range: −55°C to +125°C (T_C)**
- **Generates the System Clock for the M8086, M8088, M8089, M8087**
- **Uses a Crystal or a TTL Signal for Frequency Source**
- **Provides Local READY and MULTIBUS® READY Synchronization**
- **Single +5V ±5% Power Supply**
- **Generates System Reset Output from Schmitt Trigger Input**
- **Capable of Clock Synchronization with Other M8284As**

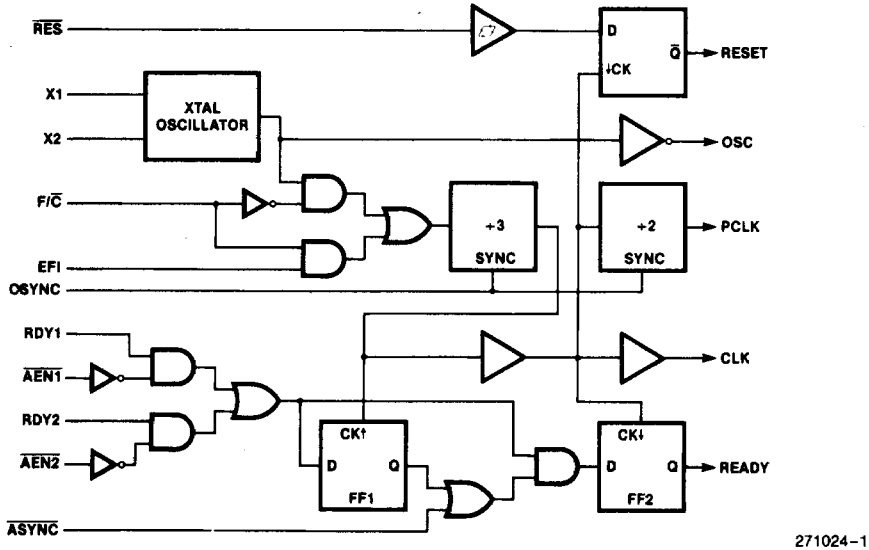

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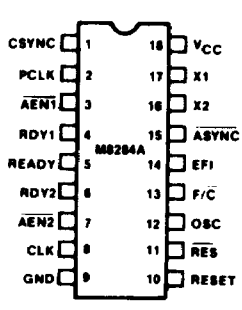
Figure 1. M8284A Block Diagram



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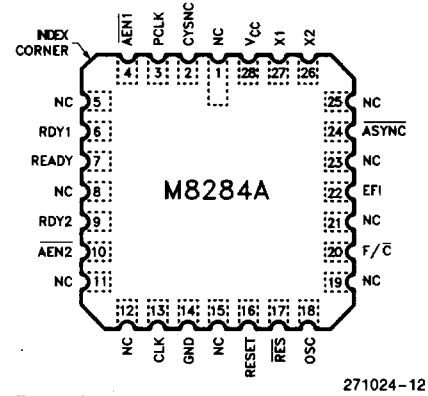

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Figure 2. M8284A Pin Configurations

November 1987
Order Number: 271024-002

Table 1. Pin Description

Symbol	I/O	Name and Function
$\overline{AEN1}$, $\overline{AEN2}$	I	**ADDRESS ENABLE:** $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	**BUS READY (TRANSFER COMPLETE):** RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	I	**READY SYNCHRONIZATION SELECT:** $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	O	**READY:** READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	**CRYSTAL IN:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	**FREQUENCY/CRYSTAL SELECT:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	**EXTERNAL FREQUENCY IN:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	O	**PROCESSOR CLOCK:** CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is ⅓ of the crystal or EFI input frequency and a ⅓ duty cycle. An output HIGH of 4.5 Volts (V_{CC} = 5V) is provided on this pin to drive MOS devices.
PCLK	O	**PERIPHERAL CLOCK:** PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK and has a 50% duty cycle.
OSC	O	**OSCILLATOR OUTPUT:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	**RESET IN:** $\overline{RES}$ is an active LOW signal which is used to generate RESET. The M8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	**RESET:** RESET is an active HIGH signal which is used to reset the M8086 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	I	**CLOCK SYNCHRONIZATION:** CSYNC is an active HIGH signal which allows multiple M8284As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		**GROUND:** Ground.
V_{CC}		**POWER:** +5V supply.

FUNCTIONAL DESCRIPTION

General

The M8284A is a single chip clock generator/driver for the M8086 microprocessor. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS "Ready" synchronization and reset logic. Refer to Figure 1 for Block Diagram and Figure 2 for Pin Configuration.

Oscillator

The oscillator circuit of the M8284A is designed primarily for use with an external series resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors ($R_1 = R_2 = 510\Omega$) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

For systems which have a V_{CC} ramp time $\geq$ 1 V/ms and/or have inherent board capacitance between X1 or X2, exceeding 10 pF (not including M8284A pin capacitance), the configuration in Figures 6 and 8 is recommended. This circuit provides optimum stability for the oscillator in such extreme conditions. It is advisable to limit stray capacitances to less than 10 pF on X1 and X2 to minimize deviation from operating at the fundamental frequency.

If EFI is used and no crystal is connected, it is recommended that X_1 or X_2 should be tied to V_{CC} through a 510Ω resistor to prevent the oscillator from free running which might produce HF noise and additional I_{CC} current.

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias(5) . −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages..... −1.0V to +5.5V
Power Dissipation 1W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_C(5) = −55°C to +125°C; V_{CC} = 5V ±5%

Symbol	Parameter	Min	Max	Units	Test Conditions
I_F	Forward Input Current ($\overline{ASYNC}$) Other Inputs		−1.3 −0.5	mA mA	V_F = 0.45V V_F = 0.45V
I_R	Reverse Input Current ($\overline{ASYNC}$) Other Inputs		50 50	μA μA	$V_R = V_{CC}$ V_R = 5.25V
V_C	Input Forward Clamp Voltage		−1.0	V	I_C = −5 mA
I_{CC}	Power Supply Current		162	mA	V_{CC} = 5.25V Freq = 25 MHz
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
V_{IHR}	Reset Input HIGH Voltage	2.6		V	
V_{OL}	Output LOW Voltage		0.45	V	I_{OL} = 5 mA
V_{OH}	Output HIGH Voltage CLK Other Outputs	4 2.4		V V	I_{OH} = −1 mA I_{OH} = −1 mA
V_{IHR}−V_{ILR}	$\overline{RES}$ Input Hysteresis	0.25		V	

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another M8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the M8284A. This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle MOS clock driver designed to drive the iAPX 86, 88 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK, PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the M8284A.

READY Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied low.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flop-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, T_{R1VCL}, on each bus cycle.

When $\overline{ASYNCH}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNCH}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

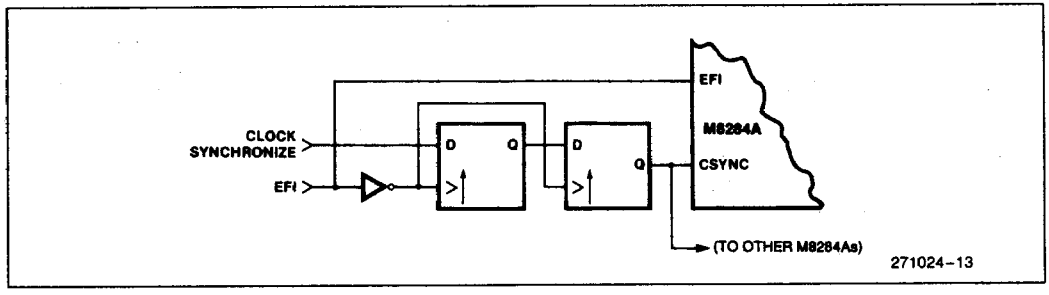

Figure 3. CSYNC Synchronization

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A.C. CHARACTERISTICS T_C[5] = −55°C to +125°C; V_{CC} = 5V ±5%

TIMING REQUIREMENTS

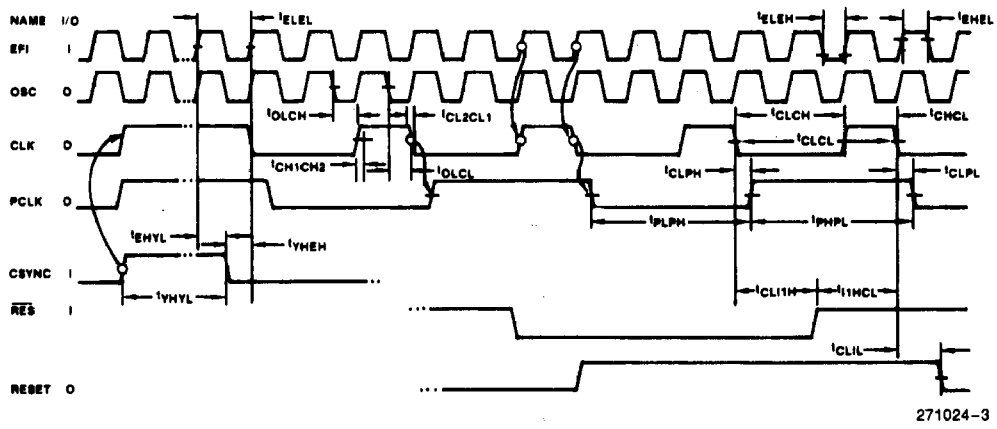
Symbol	Parameter	Min	Max	Units	Test Conditions
t_{EHEL}	External Frequency HIGH Time	13		ns	90% – 90% V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	10% – 10% V_{IN}
t_{ELEL}	EFI Period	$t_{EHEL} + t_{ELEH} + \delta$		ns	(Note 1)
	XTAL Frequency	12	25	MHz	
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50		ns	
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0		ns	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	20		ns	
t_{YHYL}	CSYNC Width	$2 \bullet t_{ELEL}$		ns	
t_{I1HCL}	$\overline{RES}$ Setup to CLK	65		ns	(Note 2)
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20		ns	(Note 2)

TIMING RESPONSES†

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125		ns	
t_{CHCL}	CLK HIGH Time	$(1/3\ t_{CLCL}) + 2.0$		ns	Fig. 6 and Fig. 7
t_{CLCH}	CLK LOW Time	$(2/3\ t_{CLCL}) - 15.0$		ns	Fig. 6 and Fig. 7
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time		10	ns	1.0V to 3.5V
t_{PHPL}	PCLK HIGH Time	$t_{CLCL} - 20$		ns	
t_{PLPH}	PCLK LOW Time	$t_{CLCL} - 20$		ns	
t_{RYLCL}	Ready Inactive to CLK (Note 4)	−8		ns	Fig. 8 and Fig. 9
t_{RYHCH}	Ready Active to CLK (Note 3)	$(2/3\ t_{CLCL}) - 15.0$		ns	Fig. 8 and Fig. 9
t_{CLIL}	CLK to Reset Delay		40	ns	
t_{CLPH}	CLK to PCLK HIGH Delay		22	ns	
t_{CLPL}	CLK to PCLK LOW Delay		22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	−5	27	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	40	ns	

NOTES:
1. δ = EFI rise (5 ns max) + EFI fall (5 ns max).
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 and TW states.
4. Applies only to T2 states.
5. Case temperatures are "instant on".

†Figure 10 illustrates test load measurement condition.



NOTE:
All timing measurements are made at 1.5V, unless otherwise noted.

Figure 3. Waveforms for Clocks and Reset Signals

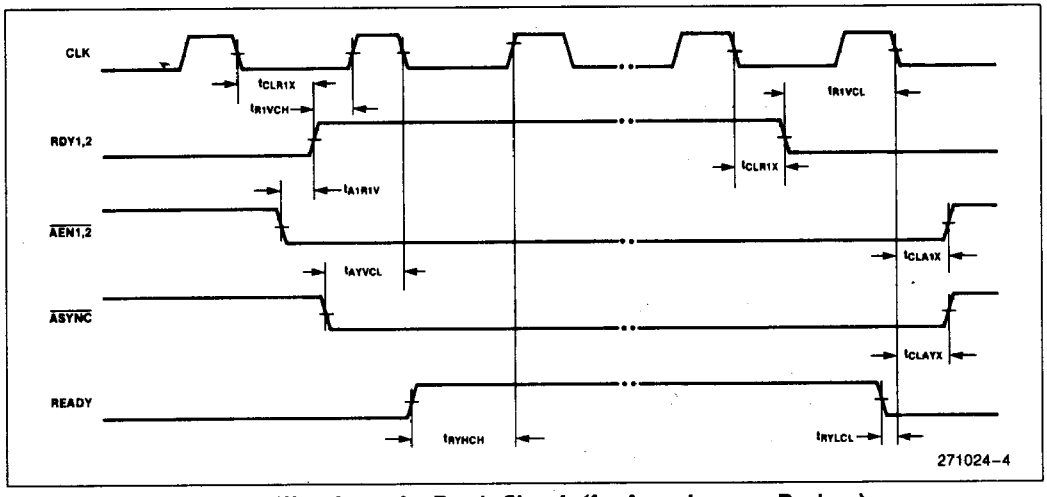


Figure 4. Waveforms for Ready Signals (for Asynchronous Devices)

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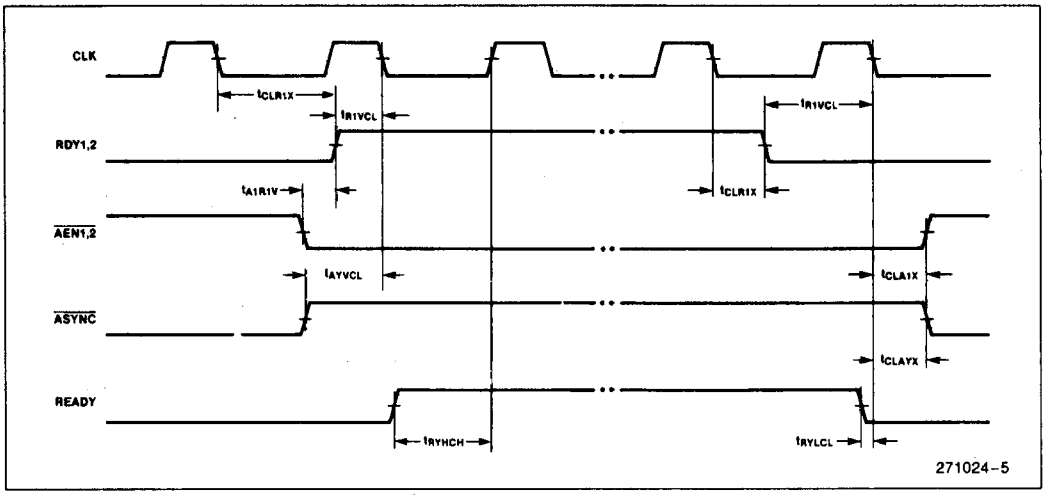


Figure 5. Waveforms for Ready Signals (for Synchronous Devices)

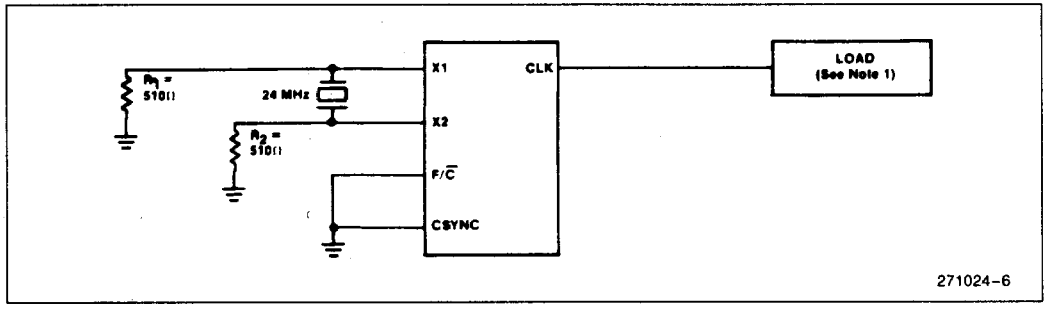


Figure 6. Clock High and Low Time (Using X1, X2)

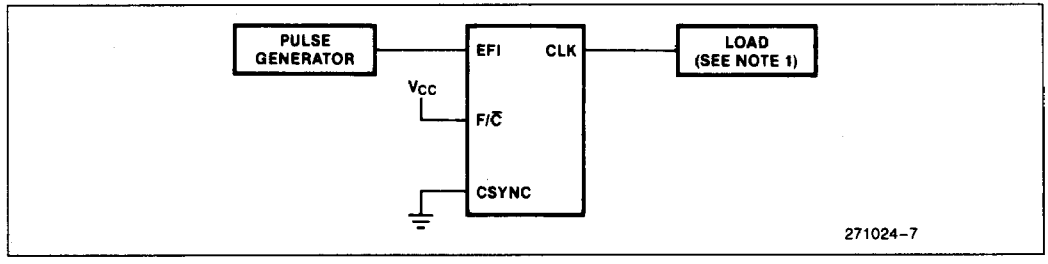


Figure 7. Clock High and Low Time (Using EFI)

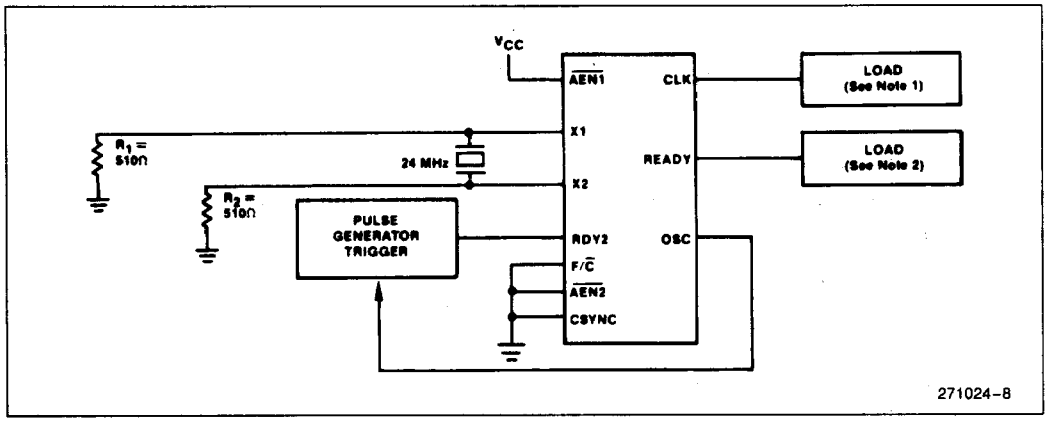


Figure 8. Ready to Clock (Using X1, X2)

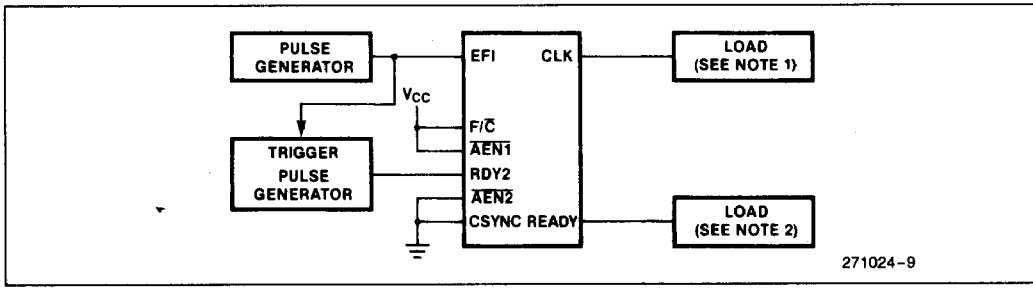


Figure 9. Ready to Clock (Using EFI)

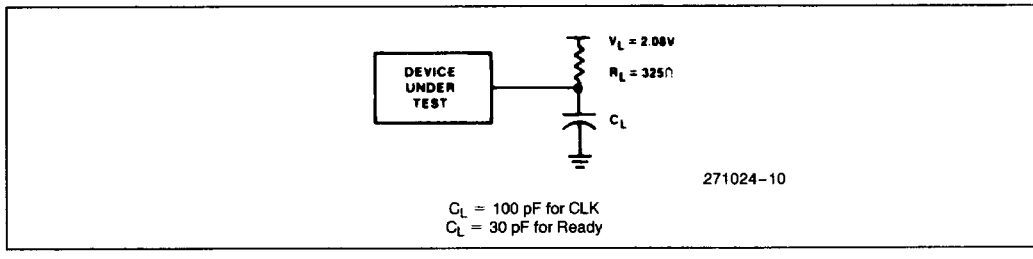
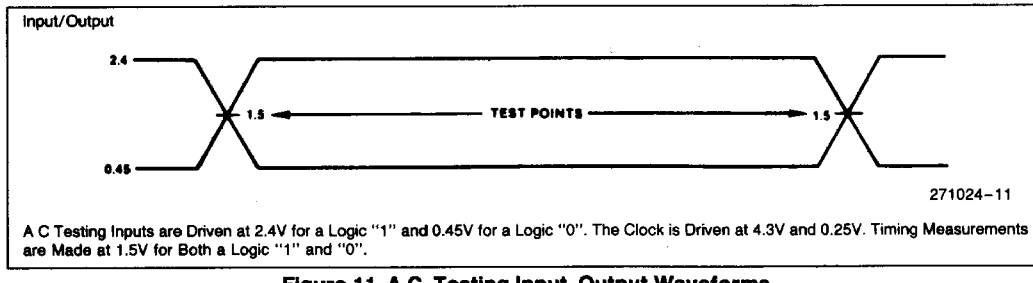


Figure 10. Test Load Measurement Condition

NOTES:
1. C_L = 100 pF
2. C_L = 30 pF



A C Testing Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". The Clock is Driven at 4.3V and 0.25V. Timing Measurements are Made at 1.5V for Both a Logic "1" and "0".

Figure 11. A.C. Testing Input, Output Waveforms

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