SLG46585

GreenPAK Programmable Mixed-Signal Matrix with Asynchronous State Machine, LDOs, and DC/DC Converter

General Description

The SLG46585 is a small, low power component commonly used to integrate Mixed-Signal functions under control of an asynchronous state machine. The user creates the circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, and the macrocells of the SLG46585. In addition, the device contains one 1 A DC/DC buck converter operating from 1 MHz to 2 MHz and four 150 mA configurable LDOs. This highly versatile device allows a wide variety of functions and control logic to be designed within a very small, low power monolithic integrated circuit.

Key Features

- Four Analog Comparators
- Voltage Reference for Analog Comparators
- Analog Temperature Sensor
- Fifteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - Six Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter, or 3-bit LUT
  - Five 8-bit Delays/Counters or 3-bit LUTs
- Combinatorial Logic
  - One 4-bit LUT with Two Outputs
- Programmable Asynchronous State Machine
  - Eight States
  - Flexible Input Logic from State Transitions
- Real Time Clock Binary Counter
- Four Tri-Mode 150 mA LDO Regulators
  - High Power Mode (HP Mode): 150 mA Output
  - Low Power Mode (LP Mode): 100 µA Output
  - Power Switch Mode: Acts like a Load Switch
- 1 A Synchronous Constant-on-Time DC/DC Step Down Converter
- Serial Communications
  - I^2C Slave Protocol Interface
- Programmable Delay with Edge Detector Output
- Additional Logic Functions
  - 2 Deglitch Filters with Edge Detectors
- Two Oscillators
  - Configurable 25 kHz/2 MHz
  - 1.73 kHz Low Power Oscillator
- Eight Byte RAM + OTP User Memory
  - RAM with I^2C interface
  - User Defined Initial Values Transferred from OTP
- Power-On Reset
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 2.5 V to 5.5 V Supply
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- 29-pin MSTQFN: 3 mm x 3 mm x 0.55 mm, 0.4 mm pitch

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Smartphones and Fitness Bands
- Notebook and Tablet PCs
- Power Management Switches
- Power Sequencing with Complex Analog Control
- Power Plane Component Size Reduction Project
- LED Driver
- Haptic Motor Driver

Contents

Figures

Tables

1 Block Diagram

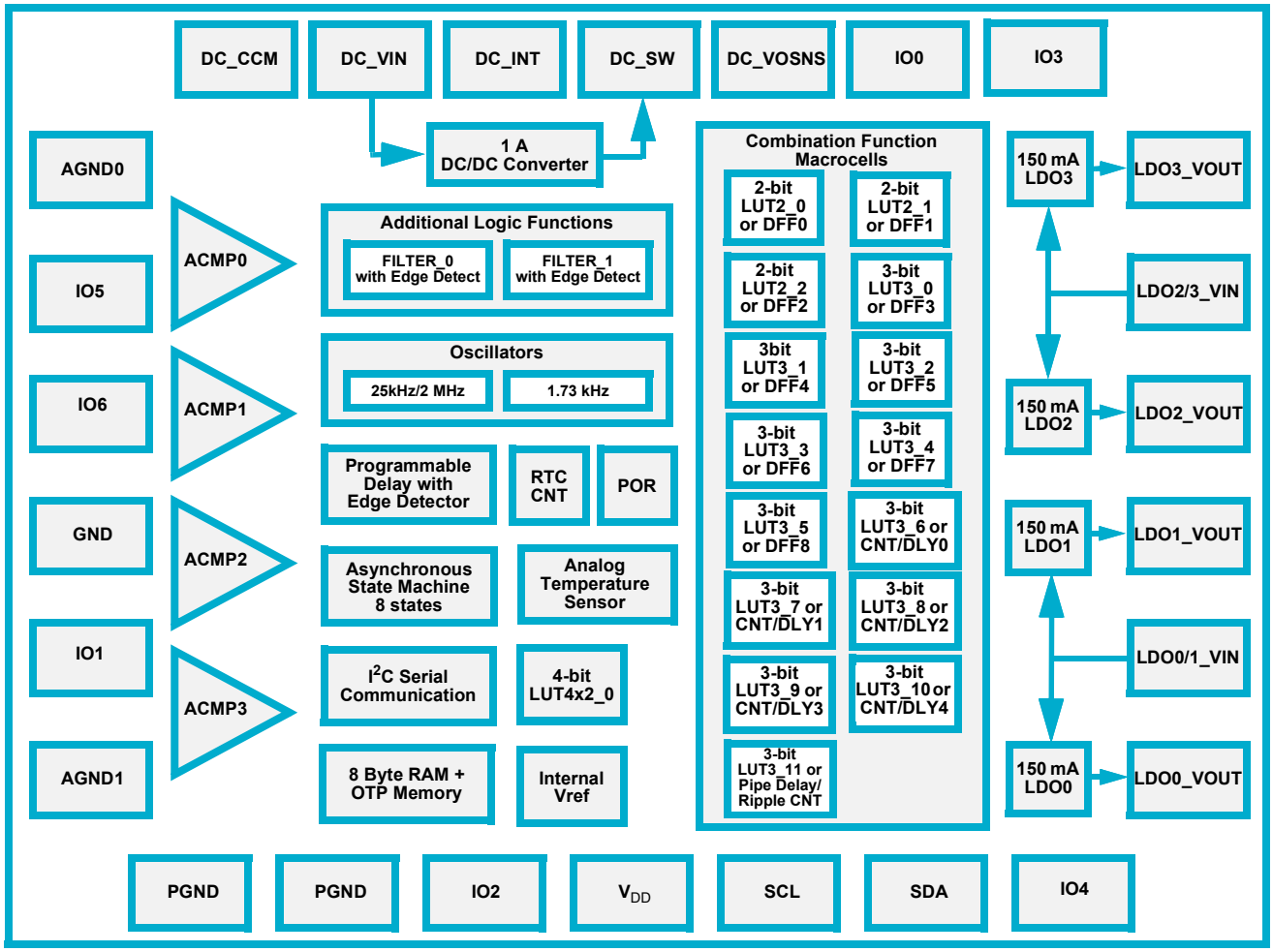
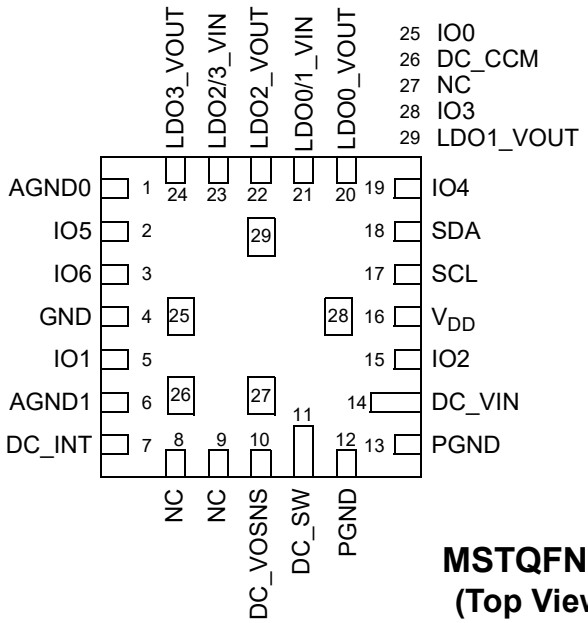


Figure 1: Block Diagram

2 Pinout

2.1 PIN CONFIGURATION - MSTQFN- 29L



MSTQFN-29
(Top View)

Pin #	Signal Name	Pin Functions
1	AGND0 **(Note 3)**	Analog Ground for LDOs
2	IO5	GPIO/ACMP2+
3	IO6	GPIO with OE **(Note 1)**/ACMP3+
4	GND **(Note 3)**	Ground
5	IO1	GPIO/ACMP0+
6	AGND1 **(Note 3)**	Analog Ground for DC/DC Converter
7	DC_INT	Interrupt Output
8	NC **(Note 2)**	No Connect
9	NC **(Note 2)**	No Connect
10	DC_VOSNS	Input Sense Pin
11	DC_SW	Switch Output
12	PGND **(Note 3)**	DC/DC Power Ground
13	PGND **(Note 3)**	DC/DC Power Ground
14	DC_VIN **(Note 4)**	Power Supply Input for DC/DC Converter
15	IO2	GPIO with OE **(Note 1)**/ACMP1+
16	V_{DD} **(Note 4)**	Power Supply
17	SCL	I^2C_SCL
18	SDA	I^2C_SDA
19	IO4	GPIO with OE **(Note 1)**/EXT_Vref
20	LDO0_VOUT	LDO0 Output Voltage
21	LDO0/1_VIN	LDO0/LDO1 Input Voltage
22	LDO2_VOUT	LDO2 Output Voltage
23	LDO2/3_VIN	LDO2/LDO3 Input Voltage
24	LDO3_VOUT	LDO3 Output Voltage
25	IO0	GPIO with OE **(Note 1)**/EXT_CLK
26	DC_CCM	CCM Output Indicator
27	NC **(Note 2)**	No Connect
28	IO3	GPI
29	LDO1_VOUT	LDO1 Output Voltage

Note 1 General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.
Note 2 Manufacture test pin, do not connect.
Note 3 All GND, AGND0, AGND1, and PGND pins must be connected together externally.
Note 4 DC_VIN and V_{DD} pins must be connected together externally.

Table 1: Functional Pin Description

STQFN 29L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	AGND0	Analog ground for LDO. All GND, AGND0, AGND1, and PGND pins must be connected together externally.			
2	IO5	IO5	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
		ACMP2+	Analog Comparator 2 Positive Input	Analog	--

Table 1: Functional Pin Description (Continued)

STQFN 29L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
3	IO6	IO6	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
4	GND	Logic Ground. All GND, AGND0, AGND1, and PGND pins must be connected together externally.			
5	IO1	IO1	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
6	AGND1	Analog ground for internal control circuit. Connect this pin to Power GND plane on PCB. All GND, AGND0, AGND1, and PGND pins must be connected together externally			
7	DC_INT	DC/DC Converter Interrupt Output. INT is an Open-Drain, asserted logic high digital output that becomes asserted within T_{INT}(HIGH) when an over-current condition has been detected at the output. INT becomes deasserted within $T_{INT(LOW)}$ when the over-current condition no longer persists.			
8	NC	Manufacture test pin, do not connect			
9	NC	Manufacture test pin, do not connect			
10	DC_VOSNS	DC/DC Converter Input sense pin for output voltage			
11	DC_SW	DC/DC Converter Switch Output. Connect this pin to an external, low DCR inductor – see Applications Information for additional details			
12	PGND	DC/DC Converter Power ground. Connect this pin to Power GND plane. All GND, AGND0, AGND1, and PGND pins must be connected together externally			
13	PGND	DC/DC Converter Power ground. Connect this pin to Power GND plane. All GND, AGND0, AGND1, and PGND pins must be connected together externally			
14	DC_VIN	DC/DC Converter Supply input. Connect a 10 µF (or larger) low ESR capacitor from this pin to Power GND plane. Capacitors used at VIN should be rated at 10 V or higher. DC_VIN and V_{DD} pins must be connected together externally.			
15	IO2	IO2	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--

Table 1: Functional Pin Description (Continued)

STQFN 29L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
16	V_{DD}	V_{DD}	Power Supply	--	--
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
		ACMP0-	Analog Comparator 0 Negative Input	Analog	--
		ACMP1-	Analog Comparator 1 Negative Input	Analog	--
		ACMP2-	Analog Comparator 2 Negative Input	Analog	--
		ACMP3-	Analog Comparator 3 Negative Input	Analog	--
17	SCL	SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
		SCL	I^2C Serial Clock	Digital Input with Schmitt Trigger	--
		SCL	I^2C Serial Clock	Low Voltage Digital Input	--
18	SDA	SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	Open-Drain NMOS
		SDA	I^2C Serial Data	Digital Input with Schmitt Trigger	--
		SDA	I^2C Serial Data	Low Voltage Digital Input	--
19	IO4	IO4	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		EXT_Vref	All Analog Comparators Negative Input	Analog	--
20	LDO0_VOUT	LDO0_VOUT	LDO0 Output Voltage	--	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
21	LDO0/1_VIN	LDO0/1_VIN	LDO0/LDO1 Input Voltage	--	--
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
22	LDO2_VOUT	LDO2_VOUT	LDO2 Output Voltage	--	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
23	LDO2/3_VIN	LDO2/3_VIN	LDO2/LDO3 Input Voltage	--	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
24	LDO3_VOUT	LDO3_VOUT	LDO3 Output Voltage	--	--

Table 1: Functional Pin Description (Continued)

STQFN 29L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
25	IO0	IO0	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
			EXT_CLK	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
26	DC_CCM	DC/DC Converter Continuous Conduction Mode Indicator Output. CCM is an Open-Drain digital output that becomes Low within $T_{CCM(Low)}$ when the loading conditions on the output of the converter switches into continuous conduction mode(ccm). The CCM output continues to toggle when the converter is in non-ccm mode.			
27	NC	Manufacture test pin, do not connect			
28	IO3	IO3	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
29	LDO1_VOUT	LDO1_VOUT	LDO1 Output Voltage	--	--

Note 1 General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.

Table 2: Pin Type Definitions

Pin Type	Description
AGND0	Analog Ground for LDO
AGND1	Analog Ground for DC/DC Converter
IO	Input/Output
GND	Ground
NC	No Connect
DC_INT	DC/DC Converter Interrupt Output
DC_VOSNS	DC/DC Converter Input Sense Pin for Output Voltage
DC_SW	DC/DC Converter Switch Output
DC_VIN	DC/DC Converter Supply Input
DC_CCM	DC/DC Converter Continuous Conduction Mode Indicator Output
PGND	DC/DC Converter Power Ground
V_{DD}	Power Supply
SCL	I^2C Serial Clock
SDA	I^2C Serial Data
LDO_VIN	LDO Input Voltage
LDO_VOUT	LDO Output Voltage

3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Condition	Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.3	7	V
DC Input Voltage		GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum Average or DC Current Through V_{DD} Pin (Per chip side) **(Note 1)**	T_J = 85 °C	--	73	mA
	T_J = 110 °C	--	35	mA
Maximum Average or DC Current Through GND Pin (Per chip side) **(Note 1)**	T_J = 85 °C	--	152	mA
	T_J = 110 °C	--	72	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitivity Level		1		

Note 1 The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, and 5 are connected to one side, IO 6, SCL, and SDA to another.

3.2 ELECTROSTATIC DISCHARGE RATINGS

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V

3.3 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions for SLG46585

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		2.5	5.5	V
Operating Temperature		-40	85	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}+ 0.3	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Voltage HIGH-Level	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.4 ELECTRICAL CHARACTERISTICS

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage **(Note 1)**		2.5	3.3	5.5	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{AIR}	Analog Input Common Mode Range	Negative ACMP Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input **(Note 2)**	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input **(Note 2)**	1.25	--	V_{DD}+ 0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input **(Note 2)**	GND- 0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger	GND- 0.3	--	0.2x V_{DD}	V
		Low-Level Logic Input **(Note 2)**	GND- 0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	V_{DD} = 2.5 V +/- 8%	0.4	0.6	0.8	V
		V_{DD} = 3.3 V +/- 10%	0.5	0.7	0.9	V
		V_{DD} = 5 V +/- 10%	0.7	1.0	1.2	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V **(Note 3)**	2.39	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V **(Note 3)**	2.60	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3 V **(Note 3)**	2.72	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V **(Note 3)**	3.04	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V **(Note 3)**	3.36	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V **(Note 3)**	4.16	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5 V **(Note 3)**	4.69	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V **(Note 3)**	5.20	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V **(Note 3)**	2.44	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V **(Note 3)**	2.65	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3 V **(Note 3)**	2.86	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V **(Note 3)**	3.17	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V **(Note 3)**	3.48	--	--	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V **(Note 3)**	4.32	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5 V **(Note 3)**	4.83	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V **(Note 3)**	5.34	--	--	V
		PMOS OD, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V **(Note 3)**	2.39	--	--	V
		PMOS OD, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V **(Note 3)**	2.60	--	--	V
		PMOS OD, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3 V **(Note 3)**	2.72	--	--	V
		PMOS OD, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V **(Note 3)**	3.05	--	--	V
		PMOS OD, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V **(Note 3)**	3.36	--	--	V
		PMOS OD, 1x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V **(Note 3)**	4.16	--	--	V
		PMOS OD, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5 V м	4.69	--	--	V
		PMOS OD, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V **(Note 3)**	5.21	--	--	V
		PMOS OD, 2x Drive, I_{OH}=1 mA, V_{DD} = 2.5 V **(Note 3)**	2.44	--	--	V
		PMOS OD, 2x Drive, I_{OH}=1 mA, V_{DD} = 2.7 V **(Note 3)**	2.65	--	--	V
		PMOS OD, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3 V **(Note 3)**	2.86	--	--	V
		PMOS OD, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V **(Note 3)**	3.17	--	--	V
		PMOS OD, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V **(Note 3)**	3.48	--	--	V
		PMOS OD, 2x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V **(Note 3)**	4.32	--	--	V
		PMOS OD, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5 V **(Note 3)**	4.83	--	--	V
		PMOS OD, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V **(Note 3)**	5.34	--	--	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull, 1x Drive, I_{OL} =1 mA, V_{DD} = 2.5 V **(Note 3)**	--	--	0.10	V
		Push-Pull, 1x Drive, I_{OL} =1 mA, V_{DD} = 2.7 V **(Note 3)**	--	--	0.09	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3 V **(Note 3)**	--	--	0.26	V
		Push-Pull, 1x Drive, I_{OL} =3 mA, V_{DD} = 3.3 V **(Note 3)**	--	--	0.24	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V **(Note 3)**	--	--	0.22	V
		Push-Pull, 1x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V **(Note 3)**	--	--	0.33	V
		Push-Pull, 1x Drive, I_{OL} = 5 mA, V_{DD} = 5 V **(Note 3)**	--	--	0.31	V
		Push-Pull, 1x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V **(Note 3)**	--	--	0.29	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V **(Note 3)**	--	--	0.05	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V **(Note 3)**	--	--	0.05	V
		Push-Pull, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3 V **(Note 3)**	--	--	0.13	V
		Push-Pull, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V **(Note 3)**	--	--	0.12	V
		Push-Pull, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V **(Note 3)**	--	--	0.11	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V **(Note 3)**	--	--	0.16	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5 V **(Note 3)**	--	--	0.15	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V **(Note 3)**	--	--	0.15	V
		NMOS OD, 1x Drive, I_{OL}=1 mA, V_{DD} = 2.5 V **(Note 3)**	--	--	0.05	V
		NMOS OD, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.7 V **(Note 3)**	--	--	0.05	V
		NMOS OD, 1x Drive, I_{OL}= 3 mA, V_{DD} = 3 V **(Note 3)**	--	--	0.13	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	NMOS OD, 1x Drive, I_{OL}= 3 mA, V_{DD} = 3.3 V **(Note 3)**	--	--	0.12	V
		NMOS OD, 1x Drive, I_{OL}=3 mA, V_{DD} = 3.6 V **(Note 3)**	--	--	0.11	V
		NMOS OD, 1x Drive, I_{OL}= 5 mA, V_{DD} = 4.5 V **(Note 3)**	--	--	0.17	V
		NMOS OD, 1x Drive, I_{OL}=5 mA, V_{DD} = 5 V **(Note 3)**	--	--	0.16	V
		NMOS OD, 1x Drive, I_{OL}=5 mA, V_{DD} = 5.5 V **(Note 3)**	--	--	0.16	V
		NMOS OD, 2x Drive, I_{OL}=1 mA, V_{DD} = 2.5 V **(Note 3)**	--	--	0.03	V
		NMOS OD, 2x Drive, I_{OL}=1 mA, V_{DD} = 2.7 V **(Note 3)**	--	--	0.03	V
		NMOS OD, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3 V **(Note 3)**	--	--	0.08	V
		NMOS OD, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.3 V **(Note 3)**	--	--	0.07	V
		NMOS OD, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.6 V **(Note 3)**	--	--	0.07	V
		NMOS OD, 2x Drive, I_{OL}= 5 mA, V_{DD} = 4.5 V **(Note 3)**	--	--	0.12	V
		NMOS OD, 2x Drive, I_{OL}= 5 mA, V_{DD} = 5 V **(Note 3)**	--	--	0.12	V
		NMOS OD, 2x Drive, I_{OL}= 5 mA, V_{DD} = 5.5 V **(Note 3)**	--	--	0.11	V
I_{OH}	HIGH-Level Output Current	Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V **(Note 3)**	1.81	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V **(Note 3)**	1.97	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V **(Note 3)**	5.78	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V **(Note 3)**	8.76	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V **(Note 3)**	11.75	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V **(Note 3)**	20.77	--	--	mA

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	HIGH-Level Output Current	Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5 V **(Note 3)**	25.45	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4V, V_{DD} = 5.5 V **(Note 3)**	29.65	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V **(Note 3)**	3.48	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V **(Note 3)**	3.77	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V **(Note 3)**	11.05	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V **(Note 3)**	16.74	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V **(Note 3)**	22.44	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V **(Note 3)**	39.54	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5 V **(Note 3)**	48.25	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V **(Note 3)**	55.92	--	--	mA
		PMOS OD, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V **(Note 3)**	1.81	--	--	mA
		PMOS OD, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V **(Note 3)**	1.97	--	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V **(Note 3)**	5.79	--	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V **(Note 3)**	8.76	--	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V **(Note 3)**	11.76	--	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5V **(Note 3)**	20.78	--	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5V **(Note 3)**	25.45	--	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V **(Note 3)**	29.65	--	--	mA

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	HIGH-Level Output Current	PMOS OD, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V **(Note 3)**	3.47	--	--	mA
		PMOS OD, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V **(Note 3)**	3.76	--	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4V, V_{DD} = 3 V **(Note 3)**	11.05	--	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V **(Note 3)**	16.73	--	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V **(Note 3)**	22.46	--	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V **(Note 3)**	39.54	--	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5 V **(Note 3)**	48.25	--	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V **(Note 3)**	55.92	--	--	mA
I_{OL}	LOW-Level Output Current	Push-Pull, 1x Drive, V_{OL} = 0.15 V V_{DD} = 2.5 V **(Note 3)**	1.52	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V V_{DD} = 2.7 V **(Note 3)**	1.63	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3 V **(Note 3)**	4.45	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V **(Note 3)**	4.82	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V **(Note 3)**	5.16	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 4.5 V **(Note 3)**	6.02	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 5 V **(Note 3)**	6.40	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 5.5 V **(Note 3)**	6.74	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V V_{DD} = 2.5 V **(Note 3)**	3.05	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V V_{DD} = 2.7 V **(Note 3)**	3.26	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3 V **(Note 3)**	8.87	--	--	mA

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Current	Push-Pull, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V **(Note 3)**	9.58	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V **(Note 3)**	10.23	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V V_{DD} = 4.5 V **(Note 3)**	11.82	--	--	mA
		Push-Pull, 2x Drive, V_{OL}= 0.4 V V_{DD} = 5 V **(Note 3)**	12.52	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V V_{DD} = 5.5 V **(Note 3)**	13.11	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V V_{DD} = 2.5 V **(Note 3)**	3.03	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V V_{DD} = 2.7 V **(Note 3)**	3.24	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3 V **(Note 3)**	8.83	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V **(Note 3)**	9.54	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V **(Note 3)**	10.17	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 4.5 V **(Note 3)**	11.75	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 5 V **(Note 3)**	12.38	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 5.5 V **(Note 3)**	12.82	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V V_{DD} = 2.5 V **(Note 3)**	5.59	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V V_{DD} = 2.7 V **(Note 3)**	5.76	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3 V **(Note 3)**	16.1	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V **(Note 3)**	16.6	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V **(Note 3)**	16.95	--	--	mA

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Current	NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 4.5 V **(Note 3)**	17.64	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 5 V **(Note 3)**	17.34	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 5.5 V **(Note 3)**	18.36	--	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.3	--	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.34	1.55	1.74	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.05	1.25	1.45	V
R_{PUP}	Pull-up Resistance	1 M Pull-up	--	1	--	MΩ
		100 k Pull-up	--	100	--	kΩ
		10 k Pull-up	--	10	--	kΩ
R_{PDWN}	Pull-down Resistance	1 M Pull-down	--	1	--	MΩ
		100 k Pull-down	--	100	--	kΩ
		10 k Pull-down	--	10	--	kΩ
C_{IN}	Input Capacitance		--	4	--	pF
T_{PW_RTC}	RTC Clock Pulse Width	Minimum Pulse Width for the RTC's Clock Input	1	--	--	µs

Note 1 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2 No hysteresis.
Note 3 The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, and 5 are connected to one side, IO 6, SCL, and SDA to another.

Table 7: EC of the I^2C Pins at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	0.3xV_{DD}	-0.5	0.3xV_{DD}	V
V_{IH}	HIGH-level Input Voltage		0.7xV_{DD}	5.5	0.7xV_{DD}	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	0.05xV_{DD}	--	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain or open collector) at 3mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain or open collector) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	0	0.2xV_{DD}	V

Table 7: EC of the I²C Pins at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
I_{OL}	LOW-Level Output Current **(Note 1)**	V_{OL} = 0.4 V, V_{DD} = 2.5 V	3	--	12.6	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	16.1	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	17.6	--	mA
		V_{OL} = 0.6 V	6	--	--	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5 V)	250	10x (V_{DD}/5.5 V)	120	ns
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		0	50	0	50	ns
I_i	Input Current each IO Pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	-10	+10	µs
C_i	Capacitance for each IO Pin		--	10	--	10	pF

Note 1 Does not meet standard I²C specifications: t_{of} = 20x(V_{DD}/5.5 V) (min); For Fast-mode Plus I_{OL} = 20 mA (min) at V_{OL} = 0.4 V.
Note 2 For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see Table 34.

Table 8: I²C Pins Timing Characteristics at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.5 V	--	95	--	168	ns
		V_{DD} = 3.3 V	--	95	--	157	
		V_{DD} = 5.0 V	--	111	--	156	
t_{AA}	Clock Low to Data Out Valid		--	900	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Rise Time		--	300	--	120	ns
t_F	Inputs Fall Time		--	300	--	120	ns
t_{SU_STD}	Stop Set-up Time		600	--	260	--	ns
t_{DH}	Data Out Hold Time		50	--	50	--	ns

Note 1 Timing diagram can be found in the Figure 88.

Table 9: Asynchronous State Machine EC at T = 25 °C

Parameter	Description	Condition	Min	Typ	Max	Unit
$t_{st\_out\_delay}$	Asynchronous State Machine Output Delay Time	V_{DD} = 2.5 V	82	--	108	ns
		V_{DD} = 3.3 V	57	--	74	
		V_{DD} = 5.0 V	40	--	49	
t_{st_out}	Asynchronous State Machine Output Transition Time	V_{DD} = 2.5 V	--	--	89	ns
		V_{DD} = 3.3 V	--	--	61	
		V_{DD} = 5.0 V	--	--	39	
t_{st_pulse}	Asynchronous State Machine Input Pulse Acceptance Time	V_{DD} = 2.5 V	12	--	--	ns
		V_{DD} = 3.3 V	9	--	--	
		V_{DD} = 5.0 V	6	--	--	
t_{st_comp}	Asynchronous State Machine Input Compete Time	V_{DD} = 2.5 V	--	--	13	ns
		V_{DD} = 3.3 V	--	--	9	
		V_{DD} = 5.0 V	--	--	6	

Table 10: Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent (POR, BG auto Power-On)	0.06	0.08	0.13	µA
		BG Force On	12.85	14.07	17.15	µA
		LP OSC (1.73 kHz)	0.28	0.35	0.61	µA
		Configurable OSC (25 kHz), pre-divider = 1	5.12	5.32	6.14	µA
		Configurable OSC (25 kHz), pre-divider = 8	4.98	5.13	5.83	µA
		Configurable OSC (2 MHz), pre-divider = 1	34.66	42.18	61.05	µA
		Configurable OSC (2 MHz), pre-divider = 8	22.23	25.26	34.01	µA
		Real Time Clock (RTC), RTC Clocked by Counter Divider Clock (see Note)	0.18	0.24	0.40	µA
		1st ACMP used with LB enabled	53.22	46.60	56.37	µA
		1st ACMP used (includes Vref)	56.50	49.89	59.65	µA
		Each additional ACMP add	3.35	3.35	3.35	µA
		ACMP0 or ACMP1 used with Input Buffer	66.93	60.47	70.59	µA
		ACMP1 used with 100 µA enabled	71.99	65.37	75.13	µA
		ACMP2 used with Temp Sensor	62.94	56.38	66.26	µA
		Push-Pull 1x + 4 pF @ 2 MHz	40	47	106	µA
		Push-Pull 1x + 4 pF @ 25 kHz	4.5	5	16	µA

Note 1 The RTC current measurements were taken with an external 32.768 kHz clock with the GPIO current consumption extracted.

3.5 TIMING CHARACTERISTICS

Table 11: Typical Delay Estimated for Each Macrocell at T = 25 °C

Parameter	Description	Condition	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input to PP 1x	26	28	19	20	14	14	ns
tpd	Delay	Digital Input to PP 2x	25	27	18	19	13	14	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1x	25	27	18	20	13	14	ns
tpd	Delay	Low Voltage Digital Input to PP 1x	33	307	25	207	19	131	ns
tpd	Delay	Digital input to NMOS 1x	--	46	--	31	--	20	ns
tpd	Delay	Digital input to NMOS 2x	--	42	--	28	--	18	ns
tpd	Delay	Digital input to PMOS 1x	26	--	19	--	14	--	ns
tpd	Delay	Digital input to PMOS 2x	25	--	18	--	13	--	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	28	--	20	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	--	27	--	20	--	14	ns
tpd	Delay	1x3 State Hi-Z to 1	28	--	20	--	15	--	ns
tpd	Delay	1x3 State Hi-Z to 0	--	27	--	20	--	14	ns
tpd	Delay	2x3 State Hi-Z to 1	27	--	20	--	14	--	ns
tpd	Delay	2x3 State Hi-Z to 0	--	26	--	19	--	14	ns
tpd	Delay	CNT/DLY Counter Mode	54	54	38	38	27	27	ns
tpd	Delay	CNT/DLY Freq. Detect	39	39	28	28	20	20	ns
tpd	Delay	CNT/DLY One Shot	38	38	27	27	19	19	ns
tpd	Delay	CNT/DLY Delay Mode	36	38	26	27	18	19	ns
tpd	Delay	CNT/DLY Edge Detect	36	36	26	25	18	18	ns
tpd	Delay	CNT/DLY High Level Reset	40	--	28	--	20	--	ns
tpd	Delay	LATCH Q	19	20	14	14	10	9	ns
tpd	Delay	LATCH nQ	20	20	14	14	10	10	ns
tpd	Delay	LATCH nRESET Q	20	21	15	15	11	10	ns
tpd	Delay	LATCH nRESET nQ	21	21	15	15	11	11	ns
tpd	Delay	LATCH nSET Q	21	22	15	15	10	11	ns
tpd	Delay	LATCH nSET nQ	22	22	16	15	11	10	ns
tpd	Delay	LUT2bit	17	17	13	12	9	8	ns
tpd	Delay	LUT3bit	20	20	14	14	10	9	ns
tpd	Delay	LUT4bit	18	18	13	12	9	8	ns
tpd	Delay	EDGE DETECT	27	27	19	19	13	13	ns
tpd	Delay	EDGE DETECT Delayed	214	212	158	156	117	115	ns
tpd	Width	EDGE DETECT	182	182	136	136	101	101	ns
tpd	Delay	Ripple CLK DOWN CNT Q0	21	20	15	14	11	10	ns
tpd	Delay	Ripple CLK DOWN CNT Q1	29	25	21	18	15	13	ns
tpd	Delay	Ripple CLK DOWN CNT Q2	29	31	21	22	15	16	ns
tpd	Delay	Ripple CLK UP CNT Q0	21	20	15	15	11	10	ns
tpd	Delay	Ripple CLK UP CNT Q1	26	26	19	19	13	13	ns
tpd	Delay	Ripple CLK UP CNT Q2	31	26	23	19	16	14	ns
tpd	Delay	Ripple nRESET DOWN CNT Q0	25	48	18	34	13	25	ns
tpd	Delay	Ripple nRESET DOWN CNT Q1	24	54	17	39	12	28	ns

Table 11: Typical Delay Estimated for Each Macrocell at T = 25 °C(Continued)

Parameter	Description	Condition	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Ripple nRESET DOWN CNT Q2	24	54	17	39	13	28	ns
tpd	Delay	Ripple nRESET UP CNT Q0	25	48	18	34	13	25	ns
tpd	Delay	Ripple nRESET UP CNT Q1	24	52	17	38	12	27	ns
tpd	Delay	Ripple nRESET UP CNT Q2	25	57	18	41	13	30	ns
tpd	Delay	DFF Q	19	20	13	14	10	10	ns
tpd	Delay	DFF nQ	20	19	14	14	10	10	ns
tpd	Delay	DFF nRESET Q	--	21	--	15	--	10	ns
tpd	Delay	DFF nRESET nQ	21	--	15	--	11	--	ns
tpd	Delay	DFF nSET Q	21	--	15	--	11	--	ns
tpd	Delay	DFF nSET nQ	--	22	--	15	--	10	ns
tpd	Delay	Pipe Delay Out	24	23	17	17	13	12	ns
tpd	Delay	Pipe Delay nRESET Out	25	26	18	19	13	13	ns
tpd	Delay	Filter	111	112	77	77	50	50	ns
tpd	Delay	ACMP (100 mV overdrive, low bandwidth disabled, input gain = 1, IN- = 600 mV)	0.49	0.45	0.42	0.38	0.40	0.36	µs
tpd	Delay	ACMP (10 mV overdrive, low bandwidth disabled, input gain = 1, IN- = 600 mV)	1.26	1.16	1.17	1.08	1.14	1.06	µs
tpd	Delay	ACMP (100 mV overdrive, low bandwidth enabled, input gain = 1, IN- = 600 mV)	3.89	3.55	3.82	3.48	3.78	3.44	µs
tpd	Delay	ACMP (10 mV overdrive, low bandwidth enabled, input gain = 1, IN- = 600 mV)	10.04	10.82	9.88	10.76	9.77	10.68	µs
tw	Width	filter (min transmitted)	79	78	55	55	35	35	ns

Table 12: Typical Propagations Delays and Pulse Widths at T = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
tw	Pulse Width, 1 cell	mode: (any)edge detect, edge detect output	185	137	101	ns
tw	Pulse Width, 2 cell	mode: (any)edge detect, edge detect output	373	277	205	ns
tw	Pulse Width, 3 cell	mode: (any)edge detect, edge detect output	561	417	308	ns
tw	Pulse Width, 4 cell	mode: (any)edge detect, edge detect output	748	556	411	ns
time1	Delay, 1 cell	mode: (any)edge detect, edge detect output	28	20	15	ns
time1	Delay, 2 cell	mode: (any)edge detect, edge detect output	28	20	15	ns
time1	Delay, 3 cell	mode: (any)edge detect, edge detect output	28	20	15	ns
time1	Delay, 4 cell	mode: (any)edge detect, edge detect output	28	20	15	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	218	161	119	ns

Table 12: Typical Propagations Delays and Pulse Widths at T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
time2	Delay, 2 cell	mode: both edge delay, edge detect output	405	300	222	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	593	440	325	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	780	579	427	ns

Table 13: Typical Filter Rejection Pulse Width at T = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 75	< 55	< 35	ns

Table 14: Typical Counter/Delay Offset Measurements at T = 25 °C

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
offset	25 kHz	auto	16	2.5	2.5	µs
offset	2 MHz	auto	1	0.6	0.4	µs
offset	1.73 kHz	auto	247	232	198	µs
frequency settling time	25 kHz	auto	16	14	12	µs
frequency settling time	2 MHz	auto	14	14	14	µs
frequency settling time	1.73 kHz	auto	250	200	150	µs
variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
variable (CLK period)	1.73 kHz	forced	0-0.5	0-0.5	0-0.5	ms
tpd (non-delayed edge)	25kHz/2MHz	either	25	14	10	ns

3.6 OSC CHARACTERISTICS

Table 15: 25 kHz RC OSC0 Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
2.5 V ±8%	24.705	25.342	23.724	25.932	23.357	26.888
3.3 V ±10%	24.710	25.289	23.690	25.932	23.334	26.836
5 V ±10%	24.650	25.801	23.661	26.249	23.376	26.987
2.5 V to 4.5 V	24.650	25.334	23.659	25.932	23.334	26.879
2.5 V to 5.5 V	24.650	25.801	23.659	26.249	23.335	26.987

Table 16: 25 kHz RC OSC0 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8%	-1.18%	1.37%	-5.10%	3.73%	-6.57%	7.55%
3.3 V ±10%	-1.16%	1.16%	-5.24%	3.73%	-6.66%	7.34%
5 V ±10%	-1.40%	3.20%	-5.36%	5.00%	-6.50%	7.95%
2.5 V to 4.5 V	-1.40%	1.34%	-5.36%	3.73%	-6.66%	7.52%
2.5 V to 5.5 V	-1.40%	3.20%	-5.36%	5.00%	-6.66%	7.95%

Table 17: 2 MHz RC OSC0 Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±8%	1.916	2.082	1.859	2.128	1.859	2.128
3.3 V ±10%	1.967	2.032	1.908	2.082	1.828	2.125
5 V ±10%	1.947	2.262	1.897	2.268	1.820	2.268
2.5 V to 4.5 V	1.935	2.066	1.873	2.117	1.814	2.125
2.5 V to 5.5 V	1.935	2.262	1.873	2.268	1.814	2.268

Table 18: 2 MHz RC OSC0 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8%	-4.22%	4.09%	-7.06%	6.40%	-7.06%	6.40%

Table 18: 2 MHz RC OSC0 Frequency Error (Error Calculated Relative to Nominal Value)(Continued)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
3.3 V ±10%	-1.64%	1.60%	-4.62%	4.10%	-8.62%	6.24%
5 V ±10%	-2.67%	13.09%	-5.14%	13.39%	-9.01%	13.39%
2.5 V to 4.5 V	-3.26%	3.31%	-6.37%	5.84%	-9.31%	6.24%
2.5 V to 5.5 V	-3.26%	13.09%	-6.37%	13.39%	-9.31%	13.39%

Table 19: 1.73 kHz RC OSC1 Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±8%	1.390	2.017	1.330	2.020	1.180	2.022
3.3 V ±10%	1.339	2.011	1.276	2.017	1.125	2.021
5 V ±10%	1.318	2.034	1.255	2.037	1.099	2.037
2.5 V to 4.5 V	1.318	2.016	1.255	2.019	1.099	2.022
2.5 to 5.5 V	1.318	2.034	1.255	2.037	1.099	2.037

Table 20: 1.73 kHz RC OSC1 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8%	-19.65%	16.58%	-23.12%	16.77%	-31.75%	16.85%
3.3 V ±10%	-22.57%	16.23%	-26.21%	16.58%	-34.93%	16.85%
5 V ±10%	-23.79%	17.54%	-27.44%	17.73%	-36.47%	17.73%
2.5 V to 4.5 V	-23.79%	16.51%	-27.44%	16.73%	-36.47%	16.85%
2.5 V to 5.5 V	-23.79%	17.54%	-27.44%	17.73%	-36.47%	17.73%

3.6.1 OSC Power-On Delay

Note: DLY/CNT Counter Data = 100, RC OSC Power Setting: "Auto Power-On", RC OSC Clock to Matrix Input: "Enable"

Table 21: Oscillators Power-On Delay at T = 25 °C

Power Supply Range (V_{DD}) V	RC OSC0 2 MHz		RC OSC0 25 kHz		RC OSC1 1.73 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs
2.50	619	905	14.35	17.57	222.53	296.85
2.70	563	813	13.76	16.98	217.52	293.04
3.00	500	709	12.94	16.61	210.43	287.82
3.30	454	638	9.67	36.51	203.51	283.89
3.60	419	582	1.82	19.46	196.79	280.17
4.20	370	510	1.79	2.70	183.73	272.25
4.50	352	484	1.89	2.94	177.64	267.27
5.00	328	454	2.09	3.28	169.40	258.96
5.50	309	428	2.21	3.45	165.60	248.45

Table 22: OSC Power-On Delay, at T = 25 °C, Fast Start-up Time Mode

Power Supply Range (V_{DD}) V	RC OSC0 2 MHz		RC OSC1 25 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs
2.50	216	313	20.61	22.61
2.70	197	286	20.58	22.47
3.00	178	254	20.52	22.43
3.30	166	234	20.49	22.28
3.60	158	222	20.46	22.42
4.20	150	209	20.39	22.20
4.50	147	207	20.32	22.12
5.00	142	201	20.20	21.83
5.50	138	194	19.97	21.33

3.7 ANALOG COMPARATOR CHARACTERISTICS

Table 23: Analog Comparator EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input set to GPIO or V_{DD}		0	--	V_{DD}	V
		Positive Input set to LDO VIN		0	--	V_{DD} - 0.4	V
		Negative Input		0	--	1.2	V

Table 23: Analog Comparator EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = 50 mV to 1200 mV	T = 25 °C	-9.0	--	9.4	mV
				-12.3	--	12.8	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = 50 mV to 1200 mV	T = 25 °C	-12.6	--	8.0	mV
				-9.2	--	9.9	mV
t_{start}	ACMP Start Time	ACMP Power-On delay, Minimal required wake time for the “Wake and Sleep function”	T = 25 °C	--	140	667	µs
				--	143	1369	µs
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = 25 °C	3.48	--	38.4	mV
			LB - Disabled, T = 25 °C	14.6	--	36.7	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25 °C	43.9	--	57.1	mV
			LB - Disabled, T = 25 °C	44.1	--	53.7	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25 °C	194.0	--	206.8	mV
			LB - Disabled, T = 25 °C	194.4	--	203.3	mV
		V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled	0.0	--	41.1	mV
			LB - Disabled	2.4	--	41.4	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled	37.7	--	64.9	mV
			LB - Disabled	43.6	--	55.4	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled	187.5	--	214.0	mV
			LB - Disabled	192.4	--	205.1	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ

Table 23: Analog Comparator EC at T = -40 °C to +85 °C, V_{DD} = 2.5 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time for ACMP0 to ACMP3	Low Bandwidth - Enable, Gain = 1, Overdrive =10 mV	Low to High	--	11.2	51.9	µs
			High to Low	--	12.2	58	µs
		Low Bandwidth - Disable, Gain = 1, Overdrive =10 mV	Low to High	--	1.0	4.2	µs
			High to Low	--	1.0	3.7	µs
		Low Bandwidth - Enable, Gain = 1, Overdrive =100 mV	Low to High	--	4.8	22.8	µs
			High to Low	--	4.4	22.4	µs
		Low Bandwidth - Disable, Gain = 1, Overdrive =100 mV	Low to High	--	0.4	2.2	µs
			High to Low	--	0.4	0.7	µs
G	Gain error (including threshold and internal Vref error)	G = 1		--	1	--	
		G = 0.5		-0.81%	--	0.76%	
		G = 0.33		-1.33%	--	1.4%	
		G = 0.25		-1.43%	--	1.63%	

3.8 LOW DROP OUT "LDO" REGULATOR ELECTRICAL CHARACTERISTICS

All four LDO regulators within SLG46585 have the same electrical specification. Some circuits are common to all LDOs and so the current consumption varies depending on the number of Active LDOs. Each LDO has three modes – HP MODE is a typical 150 mA LDO regulator mode, and LP MODE is an ultra-low current regulator mode. The LDO also has an LDO Power Switch Mode when the LDO MOSFET simply turns into a load switch passing VIN to VOUT.

Table 24: LDO Current Consumption at T = 25 °C

Parameter	Description	Condition	Min	Typ	Max	Unit
I_Q	Quiescent Current	One LDO Regulator in HP Mode	--	32	--	µA
		Two LDO Regulators in HP Mode	--	48	--	µA
		Three LDO Regulators in HP Mode	--	64	--	µA
		Four LDO Regulators in HP Mode	--	80	--	µA
I_Q	Quiescent Current	One LDO Regulator in LP Mode	--	2	--	µA
		Two LDO Regulators in LP Mode	--	3	--	µA
		Three LDO Regulators in LP Mode	--	4	--	µA
		Four LDO Regulators in LP Mode	--	5	--	µA
Note 1 Typ means under V_{DD} = VIN = 3.3 V, VOUT = 2.0 V, no load.						

Table 25: LDO Regulator Thermal Limitations

Parameter	Description	Condition	Min	Typ	Max	Unit
IC_{TL}	Thermal Limitation	T_C = 85 °C	--	--	0.6	W
		T_C = 70 °C	--	--	0.8	W
		Max Watt per LDO **(Note 1)**	--	--	0.5	W
Shutdown	Thermal Shutdown **(Note 2)**		115	125	135	°C
	Thermal Shutdown Recovery		90	100	110	°C
Note 1 Max Watt LDO multiplied by number of LDOs can easily exceed the Max Watt for the total IC package. **Note 2** Lower Thermal shutdown levels may be achieved by using the temperature sensor and comparator.						

Table 26: LDO HP MODE EC at T = 25 °C

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OUT}	Output Current Rating	per LDO	--	--	150	mA
V_{IN}	Voltage Input		2.5	--	V_{DD}	V
V_{DO}	Voltage Dropout		--	250	300	mV
ΔV_{OUT}	Output Voltage Accuracy (Note 1)	over PVT of V_{OUT} > 1.5 V	-3	--	+3	%
		over PVT of V_{OUT} ≤ 1.5 V	-60	--	+60	mV
e_N	Noise Voltage (rms)	10 Hz to 100 kHz	--	75	--	µV
PSRR	Power Supply Rejection Ratio (Note 2)	100 Hz to 100 kHz	--	50	--	dB
CTRR	Crosstalk Rejection Ratio	LDO0 to LDO1 regulation perturbation, and LDO2 to LDO3 perturbation at 0 to 150 mA at 1 kHz at 1.8 V V_{OUT}	--	50	--	dB
ΔV_{LINE}	Line Regulation	V_{OUT} + 0.5 V < V_{IN} ≤ 5.5 V	-1%	--	+1%	%/V
ΔV_{LOAD}	Load Regulation	1 mA < I_{OUT} < 150 mA	--	--	0.3	mV/mA
ΔV_{TC}	V_{OUT} Temp Coefficient		--	100	--	ppm/C
C_{IN}	External Input Capacitance (Note 2)	per LDO	2	--	--	µF
C_{OUT}	External Output Capacitance (Note 2)	per LDO	2	--	--	µF
SS0	SS Slew Rate 0	V_{OUT} = 5% to 95%	--	10	--	V/ms
SS1	SS Slew Rate 1	V_{OUT} = 5% to 95%	--	20	--	V/ms
SS2	SS Slew Rate 2	V_{OUT} = 5% to 95%	--	1.25	--	V/ms
SS3	SS Slew Rate 3	V_{OUT} = 5% to 95%	--	2.50	--	V/ms
SC	Short Circuit Protection		--	189	--	mA
t_{WAIT}	Wait Time	Time from EN = 1 to V_{OUT} start rise	--	500	--	µs
R_D	Output Discharge Pull-down Resistance	Enable = 1, Disable = 0	--	300	--	Ω

Note 1 Accuracy specifies all the effects of line regulation (ΔV_{LINE}), load regulation (ΔV_{LOAD}), and temperature coefficient (ΔV_{TC}).
Note 2 X7R-type and X5R-type capacitors are recommended.

Table 27: LDO LP MODE EC at T = 25 °C

Parameter	Description (Note 2)	Condition	Min	Typ	Max	Unit
I_{OUT}	Output Current Rating	per LDO	--	--	100	µA
V_{IN}	Voltage Input		2.5	--	V_{DD}	V
V_{DO}	Voltage Dropout		--	500	750	mV
ΔV_{OUT}	Output Voltage Accuracy	over PVT	-10	--	+10	%
C_{IN}	External Input Capacitance (Note 1)	per LDO	2	--	--	µF
C_{OUT}	External Output Capacitance (Note 1)	per LDO	2	--	--	µF
R_D	Output Discharge Pull-down Resistance	Enable = 1, Disable = 0	--	300	--	Ω

Table 27: LDO LP MODE EC at T = 25 °C(Continued)

Parameter	Description (Note 2)	Condition	Min	Typ	Max	Unit
Note 1 X7R-type and X5R-type capacitors are recommended. **Note 2** Soft Start and Short Circuit protection circuits are not available in LDO LP MODE.						

Table 28: LDO Power Switch Mode EC at T = 25 °C

Parameter	Description (Note 1)	Condition	Min	Typ	Max	Unit
I_{OUT}	Output Current Rating	per LDO	--	--	150	mA
V_{IN}	Voltage Input		2.5	--	V_{DD}	V
RDS_{ON}	MOSFET ON resistance	P-Channel with V_{IN} at 2.5, per LDO	--	1	--	Ω
I_Q	Quiescent Current	No load, per LDO	--	--	1	µA
Note 1 Soft Start and Short Circuit protection circuits are not available in LDO Power Switch Mode.						

3.9 DC/DC CONVERTER ELECTRICAL CHARACTERISTICS

Table 29: DC/DC Converter EC

Parameter	Description	Condition	Min	Typ	Max	Unit
Typical values are at T_A = 25 °C						
V_{IN}	Operating Input Voltage		2.5	--	5.5	V
I_{DD}	Power Supply Current	when OFF	--	0.17	--	µA
		when ON, No load	--	79	--	µA
V_{OUT}	Output Voltage	sel_vo [2:0] = 000; V_{IN} = 2.7 to 5.5 V, f_{SW} = 1.5 MHz	1.16	1.20	1.24	V
		sel_vo [2:0] = 001; V_{IN} = 2.7 to 5.5 V, f_{SW} = 1.5 MHz	1.46	1.50	1.55	V
		sel_vo [2:0] = 010; V_{IN} = 2.7 to 5.5 V, f_{SW} = 1.5 MHz	1.75	1.80	1.85	V
		sel_vo [2:0] = 011; V_{IN} = 3.125 to 5.5 V, f_{SW} = 1.5 MHz	2.41	2.50	2.58	V
		sel_vo [2:0] = 100; V_{IN} = 3.75 to 5.5 V, f_{SW} = 1.5 MHz	2.89	3.00	3.105	V
		sel_vo [2:0] = 101; V_{IN} = 4.125 to 5.5 V, f_{SW} = 1.5 MHz	3.20	3.30	3.40	V
V_{RIPPLE}	Output Voltage Ripple	V_{IN} = 3.3 V; V_{OUT} = 1.2 V; in CCM Mode	--	10	--	mV
RDS_{ON_P}	HS Switch ON Resistance		--	90	--	mΩ
RDS_{ON_N}	LS Switch ON Resistance		--	51	--	mΩ
I_{LIMIT}	Current Limit Threshold	Default sel_ocp[1:0] = 00	--	2.5	--	A
η_{EF}	Efficiency	V_{IN} = 5 V, V_{OUT} = 1.2 V; I_{LOAD} = 0.5 A; Temp = 27˚C, f_{SW} = 1.5 MHz; Inductor DCR =10 mΩ	--	88	--	%
f_{SW}	Switching Frequency	Default sel_fsw[1:0] = 00	--	1.5	--	MHz
		Default sel_fsw[1:0] = 01	--	2	--	MHz
T_{Total_ON}	Total Turn-on Time from Enable to DC_VOUT		--	0.6	--	ms
T_{SS}	Soft Start Time		--	0.5	--	ms

Table 29: DC/DC Converter EC(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
DC_{MAX}	Maximum Duty Cycle	V_{OUT} = 3.3 V, f_{SW} = 1.5 MHz	--	80	--	%
		V_{OUT} = 3.3 V, f_{SW} = 2.0 MHz	--	75	--	%
DC_{MIN}	Minimum Duty Cycle		--	20	--	%
$I_{SW(LKG)}$	SW Leakage Current	Set on/off = 0, V_{IN} = 5.5 V, V_{SW} = 0 V and 5.5 V	--	0	--	µA
$T_{INT(Low)}$	INT De-assertion Time	V_{IN} = 3.3 V, Temp = 27˚C	--	60	--	ns
$T_{INT(High)}$	INT Assertion Time	V_{IN} = 3.3 V, Temp = 27˚C	--	2	--	µs
$THERM_{ON}$	Thermal Protection Restart Threshold		--	125	--	˚C
$THERM_{OFF}$	Thermal Protection Shutdown Threshold		--	100	--	˚C

Note 1 INT Interrupt is an Open-Drain output. Logic high level becomes asserted within $T_{INT(HIGH)}$ when an over-current condition has been detected. After the over-current event no longer persist the INT becomes de-asserted after $T_{INT(LOW)}$.

Note 2 CCM - Continuous Conduction Mode Indicator Output. CCM is an Open-Drain digital output that becomes Low when the load is high and the converter switches to the continuous conduction mode (CCM). The CCM output continues to toggle when the converter is in non-CCM mode. Customers might use LP filter to convert the toggling signal to a DC signal, and based on DC level to identify the converter operation mode.

4 User Programmability

The SLG46585 is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

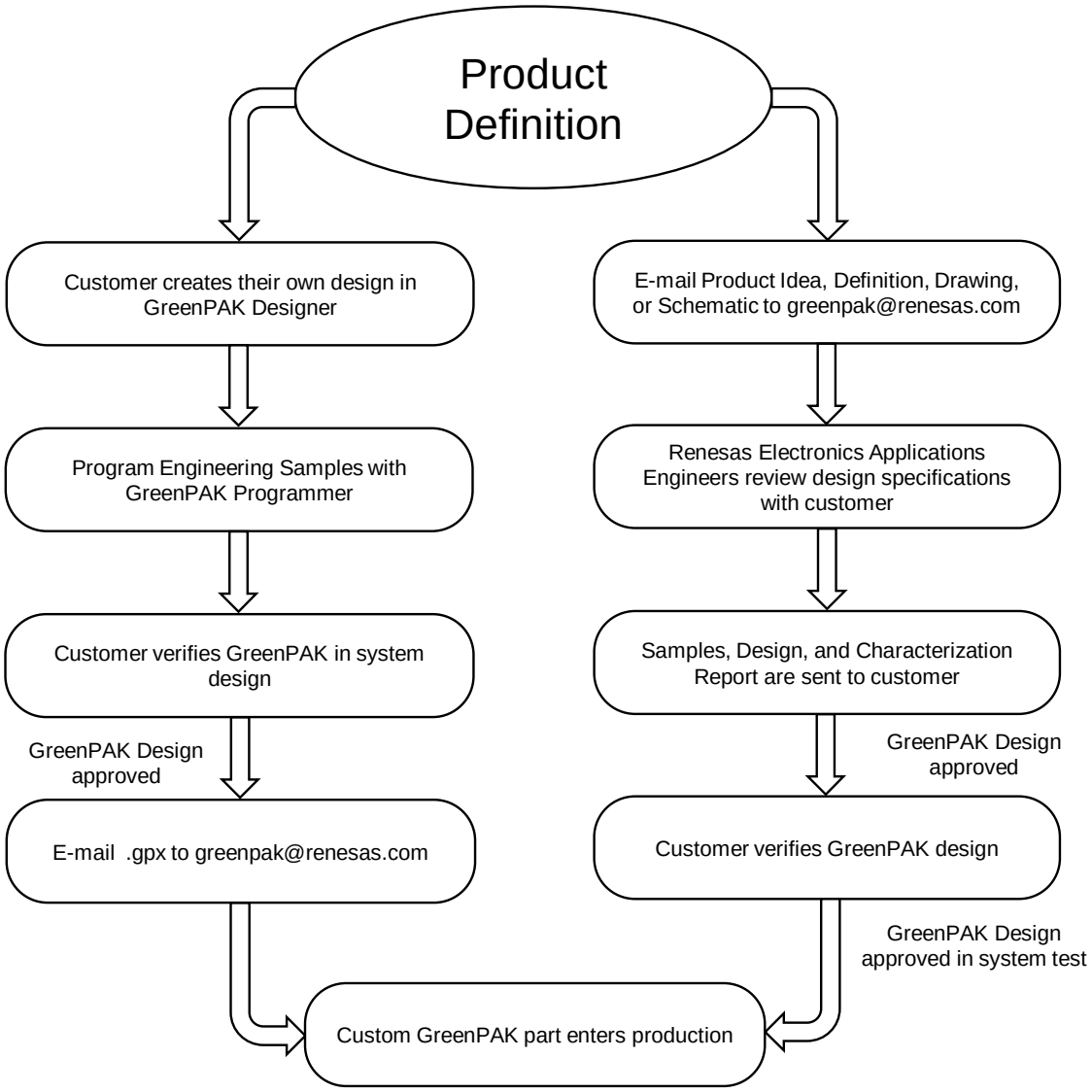


Figure 2: Steps to Create a Custom GreenPAK Device

5 IO Pins

The SLG46585 has a total of 9 multi-function IO pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non-Volatile Memory (NVM).

Refer to Section 2 for normal and programming mode pin definitions.

Normal Mode pin definitions are as follows:

- IO0: General Purpose Input or Output with OE
- IO1 General Purpose Input or Output or Analog Comparator 0(+)
- IO2: General Purpose Input or Output with OE or Analog Comparator 1(+)
- IO3: General Purpose Input
- V_{DD}: V_{DD} Power supply
- SCL: I^2C_SCL
- SDA: I^2C_SDA
- IO4: General Purpose Input or Output with OE or Analog Comparator (-)
- LDO Pins:
  - LDO0 VOUT: LDO0 Output or Analog Comparator 3(+)
  - LDO0/1 VIN: LDO0 & LDO1 Input or Analog Comparator 0(+)
  - LDO1 VOUT: LDO1 Output
  - LDO2 VOUT: LDO2 Output or Analog Comparator 3(+)
  - LDO2/3 VIN: LDO2 & LDO3 Input or Analog Comparator 1(+)
  - LDO3 VOUT: LDO3 Output
- AGND: LDO Ground
- IO5: General Purpose Input or Output or Analog Comparator 2(+)
- IO6: General Purpose Input or Output with OE or Analog Comparator 3(+)
- GND: Ground

Programming Mode pin definitions are as follows:

- IO3: V_{PP} Programming voltage
- V_{DD}: V_{DD} Power supply
- SCL: Programming SCL
- SDA: Programming SDA
- IO5: Programming Mode Control
- GND: Ground

Of the 9 user defined IO pins on the SLG46585, all but one of the pins (IO3) can serve as both digital input and digital output. IO3 can only serve as a digital input pin with RESET function, which has settings as follows:

- Level polarity:
  - Non-inverted
  - Inverted
- Reset mode:
  - Level sensitive
  - Edge triggered
- Edge detection:
  - Rising edge
  - Falling edge

5.1 INPUT MODES

Each IO pin can be configured as a digital input pin with/without Schmitt Trigger and low voltage input. IO1, IO2, IO5, and IO6 can also be configured to serve as analog inputs to the on-chip comparators. IO4 can also be configured as ACMP reference voltage input.

5.2 OUTPUT MODES

Pins IO0, IO1, IO2, IO4, IO5, and IO6 can all be configured as digital output pins.

5.3 PULL-UP/DOWN RESISTORS

All IO pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. In the case of IO3, the resistors are fixed to a Pull-down configuration. In the case of all other IO pins, the internal resistors can be configured as either Pull-up or Pull-downs.

5.4 IO REGISTER SETTINGS

Table 30: IO0 Register Settings

Signal Function	Register Bit Address	Register Definition
IO0 Pull-up/down Resistor Selection	[1025]	0: Pull-down Resistor 1: Pull-up Resistor
IO0 Pull-up/down Resistor Value Selection	[1027:1026]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO0 Mode Control (sig_io0_oe = 0)	[1029:1028]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
IO0 Mode Control (sig_io0_oe = 1)	[1031:1030]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

Table 31: IO1 Register Settings

Signal Function	Register Bit Address	Register Definition
IO1 Driver Strength Selection	[1033]	0: 1x 1: 2x
IO1 Pull-up/down Resistor Selection	[1034]	0: Pull-down Resistor 1: Pull-up Resistor
IO1 Pull-down Resistor Value Selection	[1036:1035]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO1 Mode Control	[1039:1037]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input and Open-Drain

Table 32: IO2 Register Settings

Signal Function	Register Bit Address	Register Definition
IO2 Pull-up/down Resistor Selection	[1057]	0: Pull-down Resistor 1: Pull-up Resistor

Table 32: IO2 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
IO2 Pull-up/down Resistor Value Selection	[1059:1058]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO2 Mode Control (sig_IO2_oe = 0)	[1061:1060]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO2 Mode Control (sig_IO2_oe = 1)	[1063:1062]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

Table 33: IO3 Register Settings

Signal Function	Register Bit Address	Register Definition
IO3 Pull-down Resistor Value Selection	[1069:1068]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO3 Mode Control	[1071:1070]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
IO3 reset level polarity selection	[1304]	0: Non-inverted 1: Inverted
IO3 reset bypass selection	[1305]	0: Edge selection 1: Level selection
IO3 reset edge selection	[1306]	0: Rising edge 1: Falling edge
IO3 reset enable	[1307]	0: Disable 1: Enable

Table 34: SCL Register Settings

Signal Function	Register Bit Address	Register Definition
SCL Mode Control	[1078:1077]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved

Table 35: SDA Register Settings

Signal Function	Register Bit Address	Register Definition
SDA Driver Strength Selection	[1081]	0: 1x 1: 2x

Table 35: SDA Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
SDA Mode Control	[1086:1085]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved

Table 36: IO4 Register Settings

Signal Function	Register Bit Address	Register Definition
IO4 Pull-up/down Resistor Selection	[1089]	0: Pull-down Resistor 1: Pull-up Resistor
IO4 Pull-up/down Resistor Value Selection	[1091:1090]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO4 Mode Control (sig_IO4_oe = 0)	[1093:1092]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO4 Mode Control (sig_IO4_oe = 1)	[1095:1094]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

Table 37: IO5 Register Settings

Signal Function	Register Bit Address	Register Definition
IO5 Driver Strength Selection	[1097]	0: 1x 1: 2x
IO5 Pull-up/down Resistor Selection	[1098]	0: Pull-down Resistor 1: Pull-up Resistor
IO5 Pull-up/down Resistor Value Selection	[1100:1099]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO5 Mode Control	[1103:1101]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input and Open-Drain

Table 38: IO6 Register Settings

Signal Function	Register Bit Address	Register Definition
IO6 Pull-up/down Resistor Selection	[1105]	0: Pull-down Resistor 1: Pull-up Resistor

Table 38: IO6 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
IO6 Pull-up/down Resistor Value Selection	[1107:1106]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO6 Mode Control (sig_IO6_oe = 0)	[1109:1108]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO6 Mode Control (sig_IO6_oe = 1)	[1111:1110]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

5.5 GPI STRUCTURE

5.5.1 GPI Structure (for IO3)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1, OE=0
01: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
10: Low Voltage Digital In mode, lv_en = 1, OE = 0
11: Reserved

Note 1: OE cannot be selected by user
Note 2: OE is Matrix output, Digital In is Matrix input

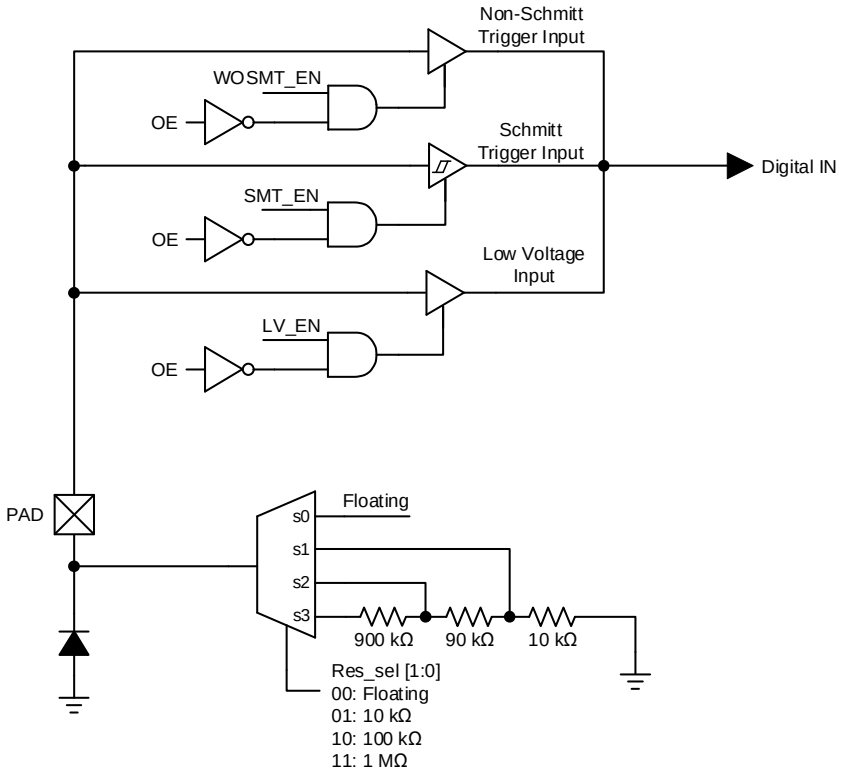


Figure 3: IO3 GPI Structure Diagram

5.6 MATRIX OE IO STRUCTURE

5.6.1 Matrix OE IO Structure (for IO0, IO2, IO4, IO6)

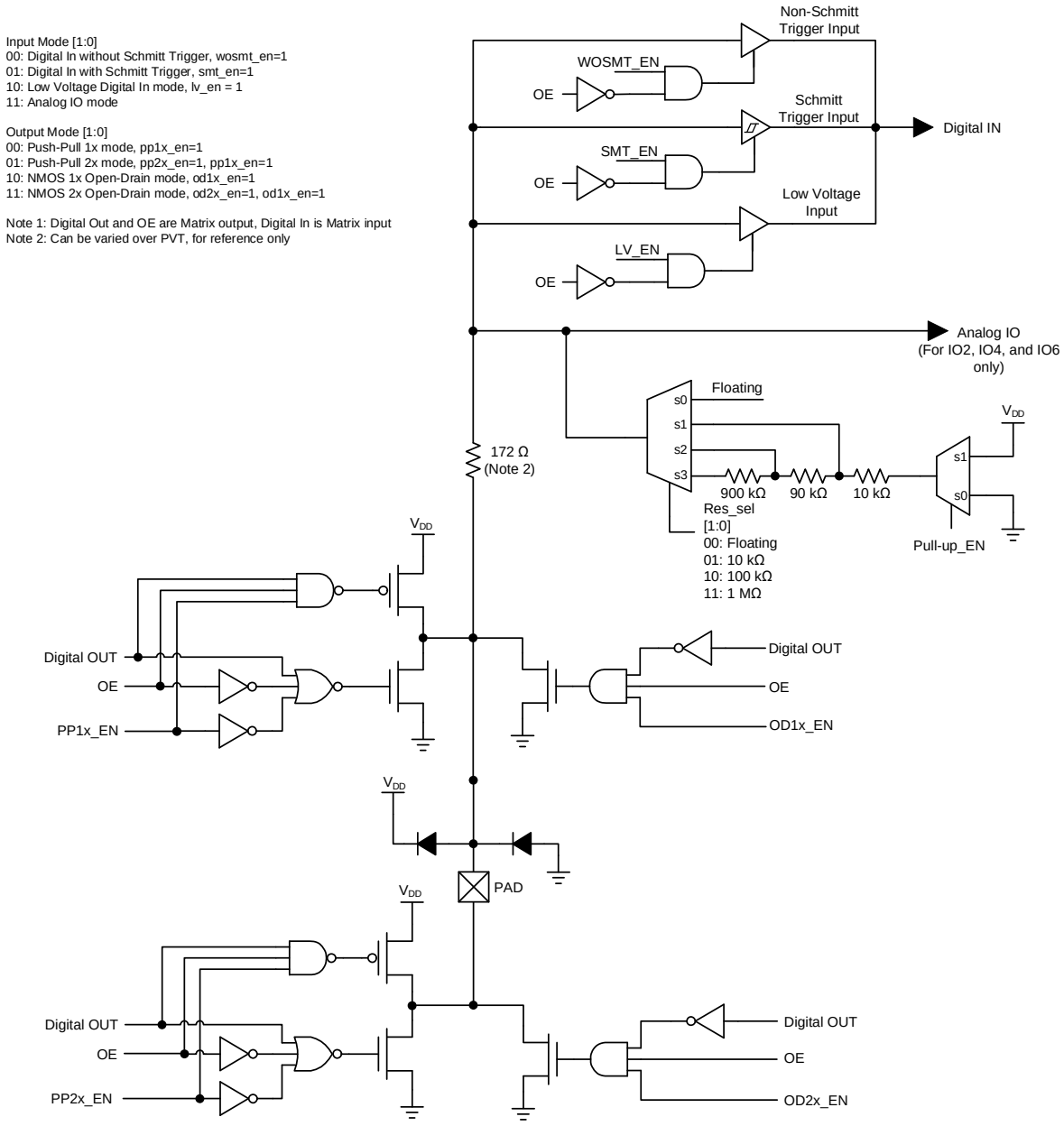


Figure 4: Matrix OE IO Structure Diagram

5.6.2 Matrix OE IO Structure (for SCL and SDA)

SCL, SDA Mode[1:0]
00: Digital Input without Schmitt Trigger, wosmt_en=1
01: Digital Input with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital Input, lv_en = 1
11: Reserved

Note 1: Digital Out and OE are Matrix output, Digital In is Matrix input
Note 2: Output mode is fixed as OD for SDA only

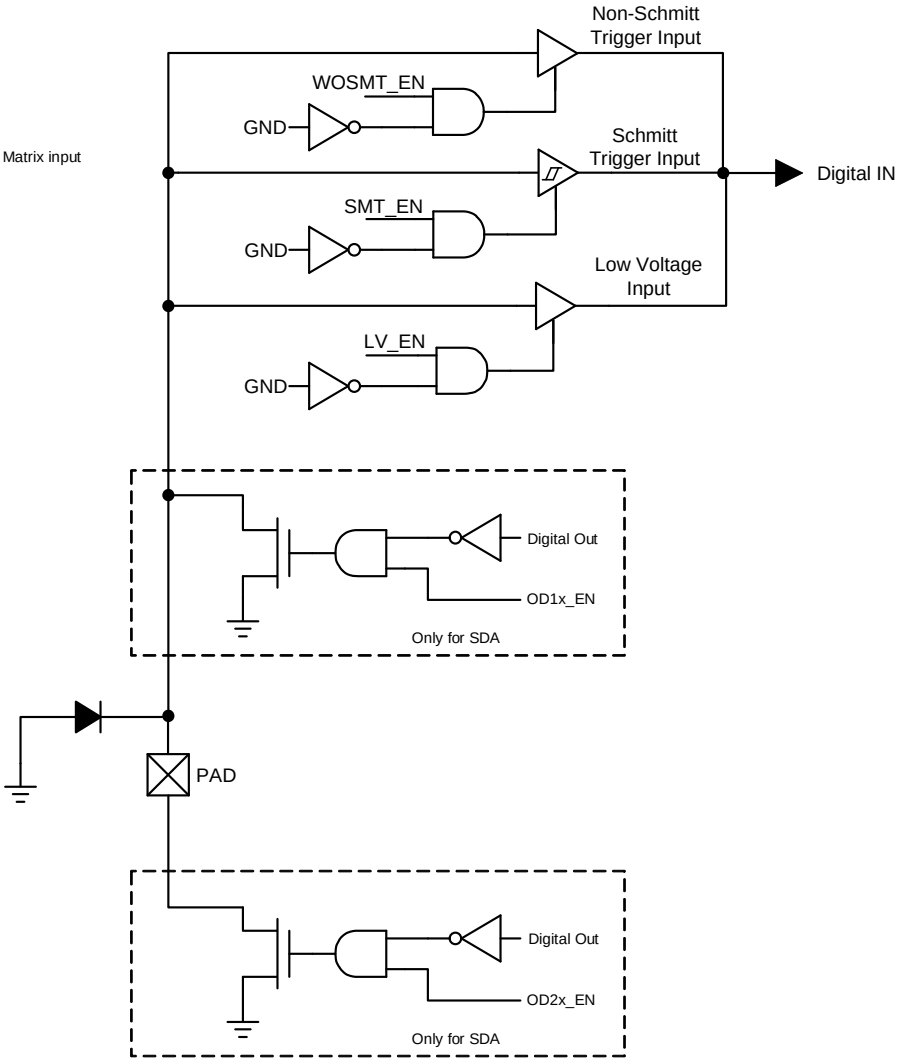


Figure 5: Matrix OE IO Structure Diagram

5.7 IO STRUCTURE

5.7.1 IO Structure (for IO1 and IO5)

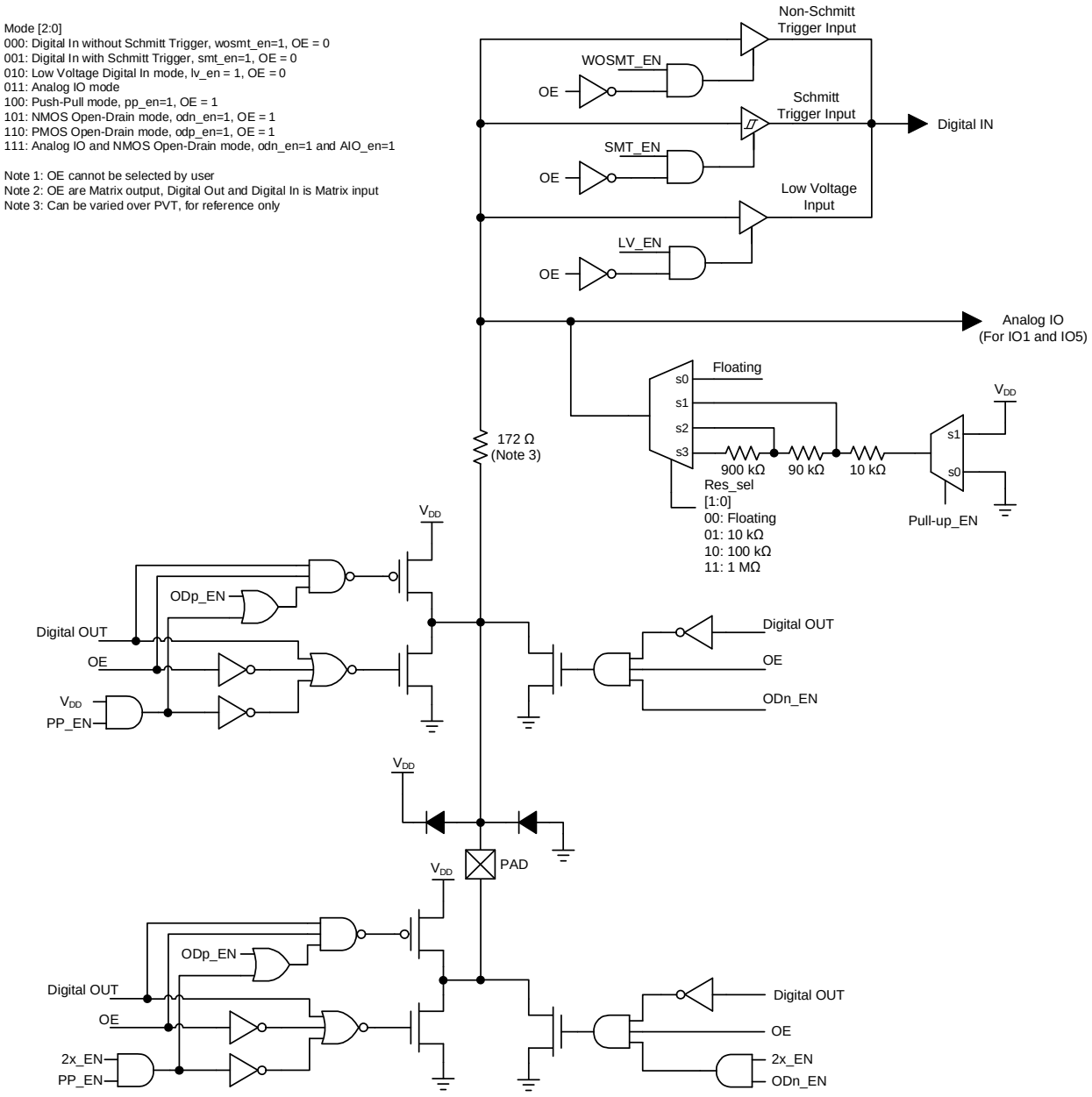


Figure 6: IO Structure Diagram

6 Connection Matrix

The Connection Matrix in the SLG46585 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46585 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low”, based on the design that is created. Once the 2048 register bits within the SLG46585 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 104 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46585’s register table, see Section 22.

Matrix Input Signal Functions	N
GND	0
IO0 Digital In	1
IO1 Digital In	2
IO2 Digital In	3
⋮	⋮
nRST_core (POR)	62
V_{DD}	63

Matrix Inputs / Matrix Outputs	N	0	1	2	…	104
	Registers	[5:0]	[13:8]	[21:16]	…	[839:832]
	Function	Matrix OUT: ASM-state0-EN0	Matrix OUT: ASM-state0-EN1	Matrix OUT: ASM-state0-EN2	…	Reserved

Figure 7: Connection Matrix

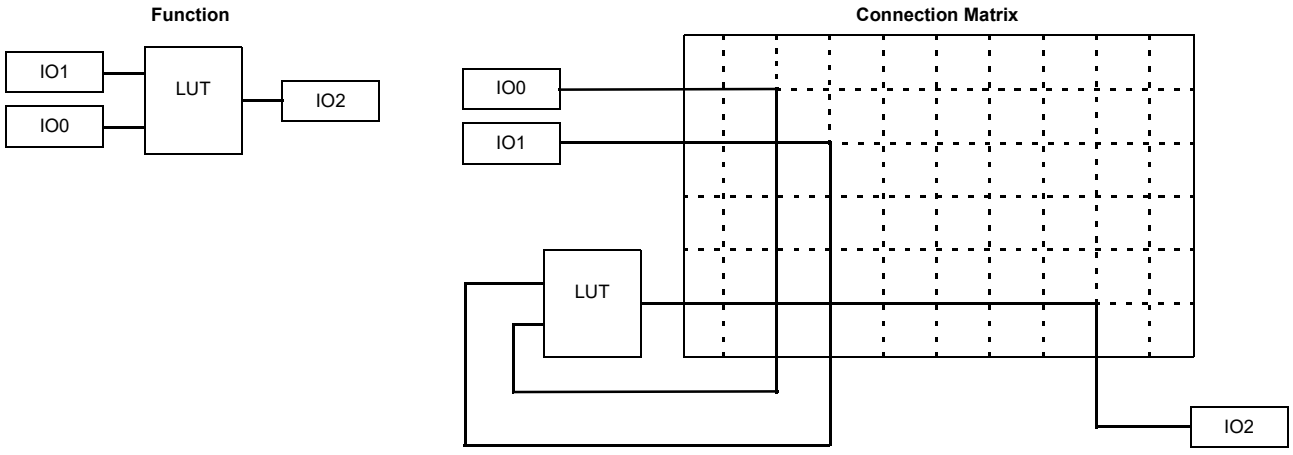


Figure 8: Connection Matrix Example

6.1 MATRIX INPUT TABLE

Table 39: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	IO0 Digital Input	0	0	0	0	0	1
2	IO1 Digital Input	0	0	0	0	1	0
3	Synchronous DC/DC Step Down Converter Fault	0	0	0	0	1	1
4	GND	0	0	0	1	0	0
5	IO2 Digital Input	0	0	0	1	0	1
6	LUT2_0/DFF0 Output	0	0	0	1	1	0
7	LUT2_1/DFF1 Output	0	0	0	1	1	1
8	LUT2_2/DFF2 Output	0	0	1	0	0	0
9	LUT3_0/DFF3 Output	0	0	1	0	0	1
10	LUT3_1/DFF4 Output	0	0	1	0	1	0
11	LUT3_2/DFF5 Output	0	0	1	0	1	1
12	LUT3_3/DFF6 Output	0	0	1	1	0	0
13	LUT3_4/DFF7 Output	0	0	1	1	0	1
14	LUT3_6/CNT_DLY0(8bit) Output	0	0	1	1	1	0
15	LUT3_7/CNT_DLY1(8bit) Output	0	0	1	1	1	1
16	LUT3_8/CNT_DLY2(8bit) Output	0	1	0	0	0	0
17	LUT3_9/CNT_DLY3(8bit) Output	0	1	0	0	0	1
18	LUT3_10/CNT_DLY4(8bit) Output	0	1	0	0	1	0
19	LUT3_11/Pipe Delay (1st stage) Output/Ripple CNT Output0	0	1	0	0	1	1
20	LUT3_5/DFF8 Output	0	1	0	1	0	0
21	LUT4X2_0 Output0	0	1	0	1	0	1
22	LUT4X2_0 Output1	0	1	0	1	1	0
23	RTC CNT 1 second Output	0	1	0	1	1	1
24	RTC DCOMP Output	0	1	1	0	0	0
25	Pipe Delay Output0/Ripple CNT Output1	0	1	1	0	0	1
26	Pipe Delay Output1/Ripple CNT Output2	0	1	1	0	1	0
27	Internal OSC Post-Divided by 1/2/3/4/8/12/24/64 Output (25KHz/ 2MHz)	0	1	1	0	1	1
28	Internal OSC Post-Divided by 1/2/3/4/8/12/24/64 Output (25KHz/ 2MHz)	0	1	1	1	0	0
29	LPOSC Output	0	1	1	1	0	1
30	Filter0/Edge Detect0 Output	0	1	1	1	1	0
31	Filter1/Edge Detect1 Output	0	1	1	1	1	1
32	I^2C_virtual_0 Input	1	0	0	0	0	0
33	I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0

Table 39: Matrix Input Table(Continued)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1
38	I^2C_virtual_6 Input	1	0	0	1	1	0
39	I^2C_virtual_7 Input	1	0	0	1	1	1
40	ASM-stateX-dout0	1	0	1	0	0	0
41	ASM-stateX-dout1	1	0	1	0	0	1
42	ASM-stateX-dout2	1	0	1	0	1	0
43	ASM-stateX-dout3	1	0	1	0	1	1
44	ASM-stateX-dout4	1	0	1	1	0	0
45	ASM-stateX-dout5	1	0	1	1	0	1
46	ASM-stateX-dout6	1	0	1	1	1	0
47	ASM-stateX-dout7	1	0	1	1	1	1
48	BG_OK Output	1	1	0	0	0	0
49	LDO0 nFault	1	1	0	0	0	1
50	LDO1 nFault	1	1	0	0	1	0
51	LDO2 nFault	1	1	0	0	1	1
52	LDO3 nFault	1	1	0	1	0	0
53	IO3 Digital Input (GPI)	1	1	0	1	0	1
54	IO4 Digital Input	1	1	0	1	1	0
55	IO5 Digital Input	1	1	0	1	1	1
56	IO6 Digital Input	1	1	1	0	0	0
57	ACMP_0 Output	1	1	1	0	0	1
58	ACMP_1 Output	1	1	1	0	1	0
59	ACMP_2 Output	1	1	1	0	1	1
60	ACMP_3 Output	1	1	1	1	0	0
61	Programmable Delay with Edge Detector Output	1	1	1	1	0	1
62	nRST_core (POR) as matrix input	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 MATRIX OUTPUT TABLE

Table 40: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
7:0	Matrix OUT: ASM-state0-EN0	0
15:8	Matrix OUT: ASM-state0-EN1	1
23:16	Matrix OUT: ASM-state0-EN2	2
31:24	Matrix OUT: ASM-state1-EN0	3
39:32	Matrix OUT: ASM-state1-EN1	4
47:40	Matrix OUT: ASM-state1-EN2	5
55:48	Matrix OUT: ASM-state2-EN0	6
63:56	Matrix OUT: ASM-state2-EN1	7
71:64	Matrix OUT: ASM-state2-EN2	8
79:72	Matrix OUT: ASM-state3-EN0	9
87:80	Matrix OUT: ASM-state3-EN1	10
95:88	Matrix OUT: ASM-state3-EN2	11
103:96	Matrix OUT: ASM-state4-EN0	12
111:104	Matrix OUT: ASM-state4-EN1	13
119:112	Matrix OUT: ASM-state4-EN2	14
127:120	Matrix OUT: ASM-state5-EN0	15
135:128	Matrix OUT: ASM-state5-EN1	16
143:136	Matrix OUT: ASM-state5-EN2	17
151:144	Matrix OUT: ASM-state6-EN0	18
159:152	Matrix OUT: ASM-state6-EN1	19
167:160	Matrix OUT: ASM-state6-EN2	20
175:168	Matrix OUT: ASM-state7-EN0	21
183:176	Matrix OUT: ASM-state7-EN1	22
191:184	Matrix OUT: ASM-state7-EN2	23
199:192	Matrix OUT: ASM-state-nRST	24
207:200	Matrix OUT: IN0 of LUT3_6 or Delay0 Input (or Counter0 RST Input)	25
215:208	Matrix OUT: IN1 of LUT3_6 or External Clock Input of Delay0 (or Counter0)	26
223:216	Matrix OUT: IN2 of LUT3_6	27
231:224	Matrix OUT: IN0 of LUT3_7 or Delay1 Input (or Counter1 RST Input)	28
239:232	Matrix OUT: IN1 of LUT3_7 or External Clock Input of Delay1 (or Counter1)	29
247:240	Matrix OUT: IN2 of LUT3_7	30
255:248	Matrix OUT: IN0 of LUT3_8 or Delay2 Input (or Counter2 RST Input)	31
263:256	Matrix OUT: IN1 of LUT3_8 or External Clock Input of Delay2 (or Counter2)	32
271:264	Matrix OUT: IN2 of LUT3_8	33
279:272	Matrix OUT: IN0 of LUT3_9 or Delay3 Input (or Counter3 RST Input)	34
287:280	Matrix OUT: IN1 of LUT3_9 or External Clock Input of Delay3 (or Counter3)	35
295:288	Matrix OUT: IN2 of LUT3_9	36
303:296	Matrix OUT: IN0 of LUT3_10 or Delay4 Input (or Counter4 RST Input)	37

Table 40: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
311:304	Matrix OUT: IN1 of LUT3_10 or External Clock Input of Delay4 (or Counter4)	38
319:312	Matrix OUT: IN2 of LUT3_10	39
327:320	Matrix OUT: IO0 Digital Output Source	40
335:328	Matrix OUT: IO0 Output Enable	41
343:336	Matrix OUT: IO1 Digital Output Source	42
351:344	Reserved	43
359:352	Reserved	44
367:360	Matrix OUT: IO2 Digital Output Source	45
375:368	Matrix OUT: IO2 Output Enable	46
383:376	Matrix OUT: IO4 Digital Output Source	47
391:384	Matrix OUT: IO4 Output Enable	48
399:392	Matrix OUT: IO5 Digital Output Source	49
407:400	Matrix OUT: IO6 Digital Output Source	50
415:408	Matrix OUT: IO6 Output Enable	51
423:416	Matrix OUT: ACMP0 PWR UP	52
431:424	Matrix OUT: ACMP1 PWR UP	53
439:432	Matrix OUT: ACMP2 PWR UP	54
447:440	Matrix OUT: ACMP3 PWR UP	55
455:448	Matrix OUT: Input of Filter_0 with fixed time edge detector	56
463:456	Matrix OUT: Input of Filter_1 with fixed time edge detector	57
471:464	Matrix OUT: Input of Programmable Delay & Edge Detector	58
479:472	Matrix OUT: OSC 25KHz/2MHz PD (Power-Down)	59
487:480	Matrix OUT: LPOSC PD (Power-Down)	60
495:488	Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0	61
503:496	Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0	62
511:504	Matrix OUT: IN0 of LUT2_1 or Clock Input of DFF1	63
519:512	Matrix OUT: IN1 of LUT2_1 or Data Input of DFF1	64
527:520	Matrix OUT: IN0 of LUT2_2 or Clock Input of DFF2	65
535:528	Matrix OUT: IN1 of LUT2_2 or Data Input of DFF2	66
543:536	Matrix OUT: IN0 of LUT3_0 or Clock Input of DFF3	67
551:544	Matrix OUT: IN1 of LUT3_0 or Data Input of DFF3	68
559:552	Matrix OUT: IN2 of LUT3_0 or nRST (nSET) of DFF3	69
567:560	Matrix OUT: IN0 of LUT3_1 or Clock Input of DFF4	70
575:568	Matrix OUT: IN1 of LUT3_1 or Data Input of DFF4	71
583:576	Matrix OUT: IN2 of LUT3_1 or nRST (nSET) of DFF4	72
591:584	Matrix OUT: IN0 of LUT3_2 or Clock Input of DFF5	73
599:592	Matrix OUT: IN1 of LUT3_2 or Data Input of DFF5	74
607:600	Matrix OUT: IN2 of LUT3_2 or nRST (nSET) of DFF5	75
615:608	Matrix OUT: IN0 of LUT3_3 or Clock Input of DFF6	76

Table 40: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
623:616	Matrix OUT: IN1 of LUT3_3 or Data Input of DFF6	77
631:624	Matrix OUT: IN2 of LUT3_3 or nRST (nSET) of DFF6	78
639:632	Matrix OUT: IN0 of LUT3_4 or Clock Input of DFF7	79
647:640	Matrix OUT: IN1 of LUT3_4 or Data Input of DFF7	80
655:648	Matrix OUT: IN2 of LUT3_4 or nRST (nSET) of DFF7	81
663:656	Matrix OUT: IN0 of LUT3_11 or Input of Pipe Delay or Up/Down selection of Ripple Counter	82
671:664	Matrix OUT: IN1 of LUT3_11 or nRST of Pipe Delay or nRST of Ripple Counter	83
679:672	Matrix OUT: IN2 of LUT3_11 or Clock of Pipe Delay or Clock of Ripple Counter	84
687:680	Matrix OUT: IN0 of LUT3_5 or Clock Input of DFF8	85
695:688	Matrix OUT: IN1 of LUT3_5 or Data Input of DFF8	86
703:696	Matrix OUT: IN2 of LUT3_5 or nRST (nSET) of DFF8	87
711:704	Matrix OUT: IN0 of LUT4X2_0	88
719:712	Matrix OUT: IN1 of LUT4X2_0	89
727:720	Matrix OUT: IN2 of LUT4X2_0	90
735:728	Matrix OUT: IN3 of LUT4X2_0	91
743:736	Matrix OUT: LDO LP Mode Enable for LDO0/1/2/3	92
751:744	Matrix OUT: LDO0_EN	93
759:752	Matrix OUT: LDO1_EN	94
767:760	Matrix OUT: LDO2_EN	95
775:768	Matrix OUT: LDO3_EN	96
783:776	Matrix OUT: LDO0 2nd VOUT Selection Enable	97
791:784	Matrix OUT: LDO1 2nd VOUT Selection Enable	98
799:792	Matrix OUT: LDO2 2nd VOUT Selection Enable	99
807:800	Matrix OUT: LDO3 2nd VOUT Selection Enable	100
815:808	Matrix OUT: RTC Clock	101
823:816	Matrix OUT: RTC Trigger signal to read/write RTC CNT values	102
831:824	Matrix OUT: ON/OFF command for Synchronous DC/DC Step Down Converter	103
839:832	Reserved	104
Note 1 For each Address, the two most significant bits are unused.		

6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0xF4 (0244).

Eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

See Table 41 for Connection Matrix Virtual Inputs.

Table 41: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[1952]
33	I^2C_virtual_1 Input	[1953]
34	I^2C_virtual_2 Input	[1954]
35	I^2C_virtual_3 Input	[1955]
36	I^2C_virtual_4 Input	[1956]
37	I^2C_virtual_5 Input	[1957]
38	I^2C_virtual_6 Input	[1958]
39	I^2C_virtual_7 Input	[1959]

6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are 0x70 (0112) to 0x71 (0113). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at 0xF4 (0244)).

7 Combination Function Macrocells

The SLG46585 has 15 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUTs or as D Flip-Flops
- Six macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay or as a Ripple Counter
- Five macrocells that can serve as either 3-bit LUTs or as 8-Bit Counter/Delays

Inputs/Outputs for the 15 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP-FLOP MACROCELLS

There are three macrocells that can serve as either 2-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change
- LATCH: if CLK = 0, then Q = D

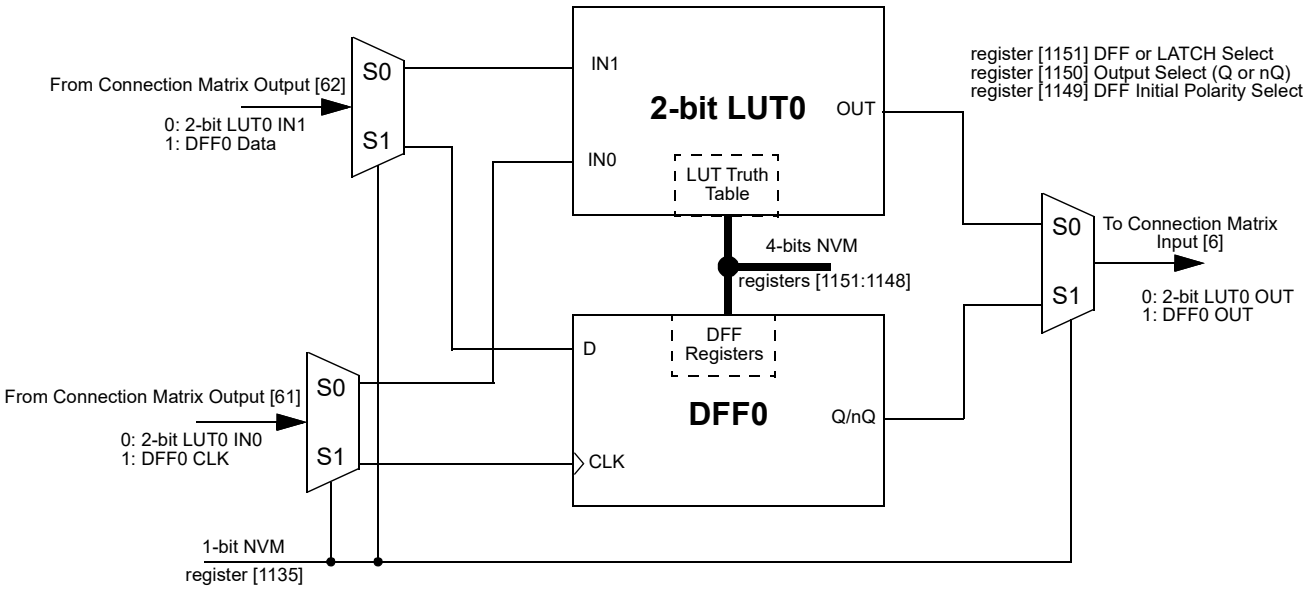


Figure 9: 2-bit LUT0 or DFF0

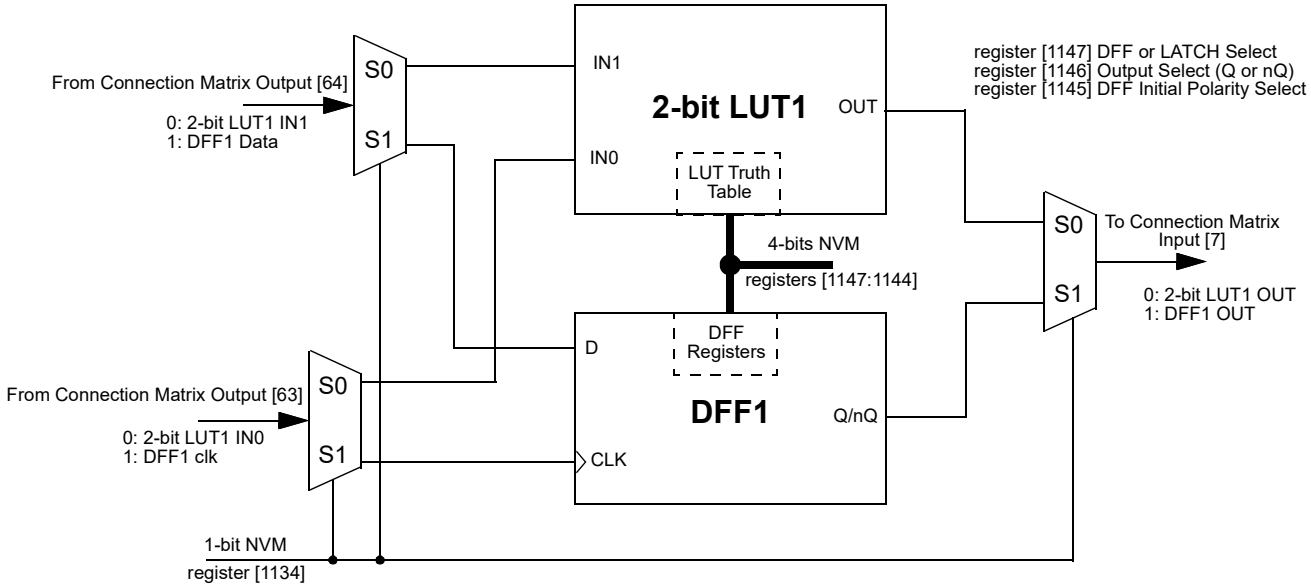


Figure 10: 2-bit LUT1 or DFF1

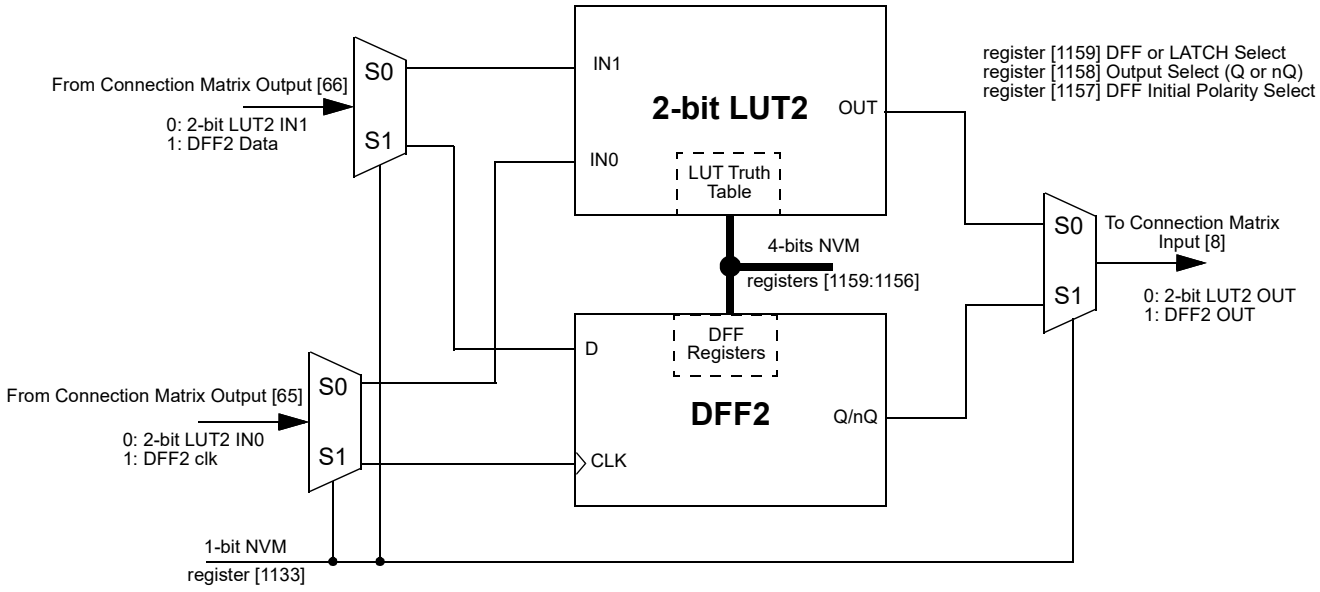


Figure 11: 2-bit LUT2 or DFF2

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 42: 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1148]	LSB
0	1	register [1149]	
1	0	register [1150]	
1	1	register [1151]	MSB

Table 43: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1144]	LSB
0	1	register [1145]	
1	0	register [1146]	
1	1	register [1147]	MSB

Table 44: 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1156]	LSB
0	1	register [1157]	
1	0	register [1158]	
1	1	register [1159]	MSB

Each macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by registers [1151:1148]

2-Bit LUT1 is defined by registers [1147:1144]

2-Bit LUT2 is defined by registers [1159:1156]

Table 45 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the three 2-bit LUT logic cells.

Table 45: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 2-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 46: DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_0 or DFF0 Select	[1135]	0: LUT2_0 1: DFF0
DFF0 Initial Polarity Select	[1149]	0: Low 1: High
DFF0 Output Select	[1150]	0: Q output 1: nQ output
DFF0 or LATCH Select	[1151]	0: DFF function 1: LATCH function

Table 47: DFF1 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_1 or DFF1 Select	[1134]	0: LUT2_1 1: DFF1
DFF1 Initial Polarity Select	[1145]	0: Low 1: High
DFF1 Output Select	[1146]	0: Q output 1: nQ output
DFF1 or LATCH Select	[1147]	0: DFF function 1: LATCH function

Table 48: DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_2 or DFF2 Select	[1133]	0: LUT2_2 1: DFF2
DFF2 Initial Polarity Select	[1157]	0: Low 1: High
DFF2 Output Select	[1158]	0: Q output 1: nQ output
DFF2 or LATCH Select	[1159]	0: DFF function 1: LATCH function

7.1.3 Initial Polarity Operations

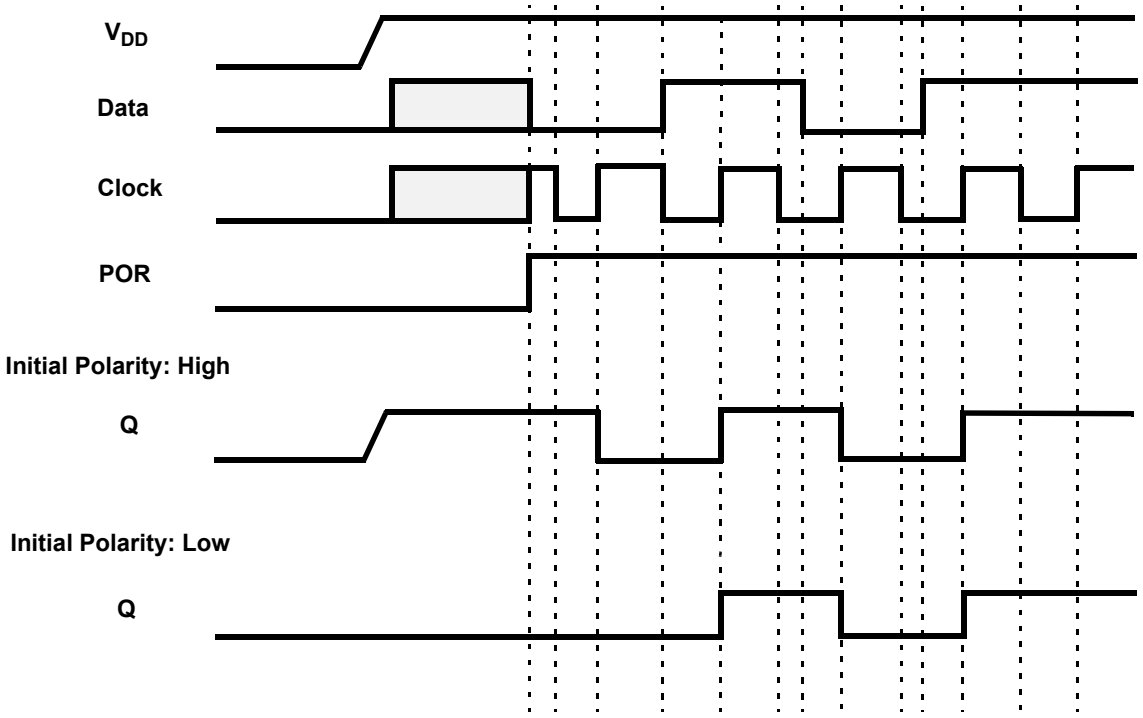


Figure 12: DFF Polarity Operations

7.2 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS

There are six macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

DFF3 has a user selectable option to allow the macrocell output to either come from the Q/nQ output of one D Flip-Flop, or two D Flip-Flops in series, with the first D Flip-Flop triggering on the rising clock edge, and the second D Flip-Flop triggering on the falling clock edge.

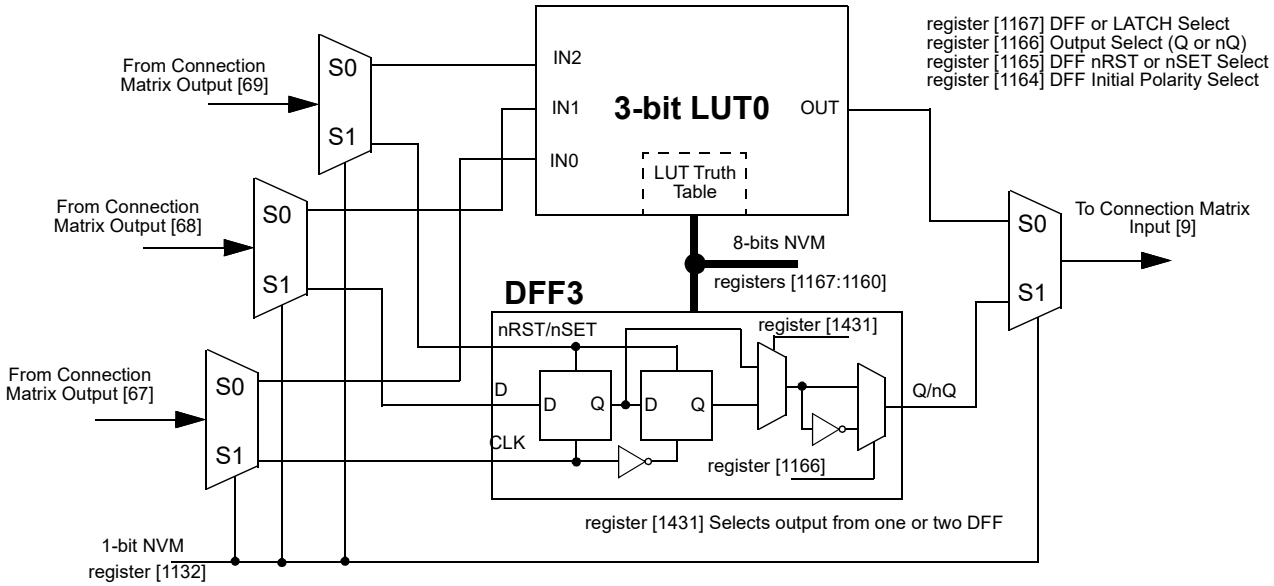


Figure 13: 3-bit LUT0 or DFF3

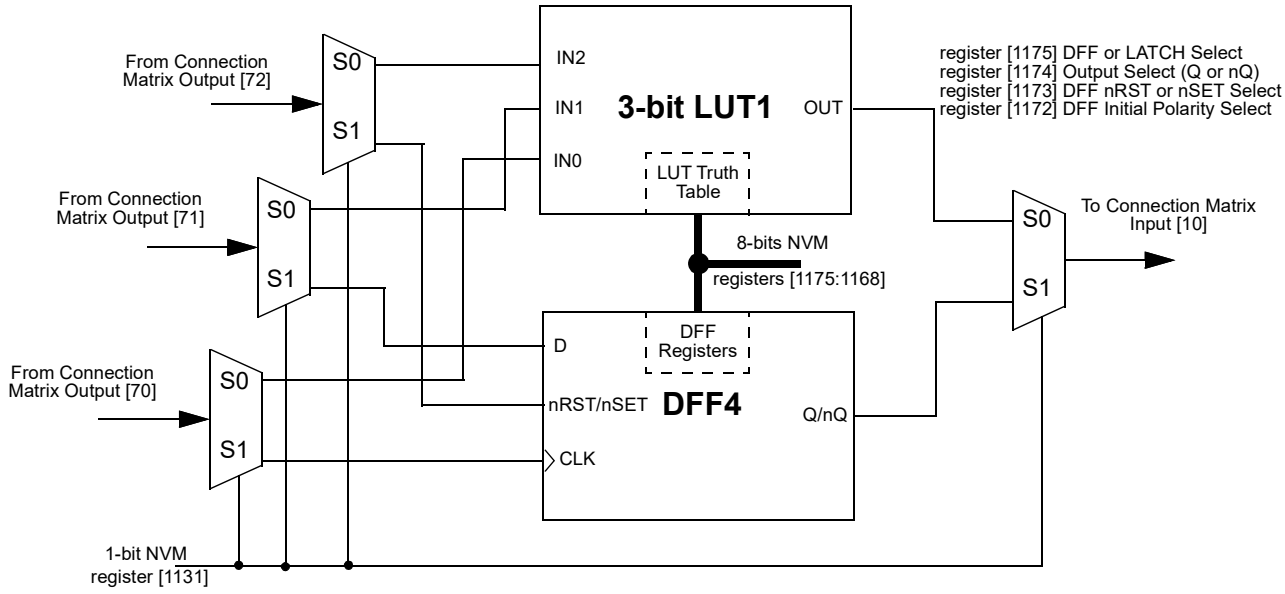


Figure 14: 3-bit LUT1 or DFF4

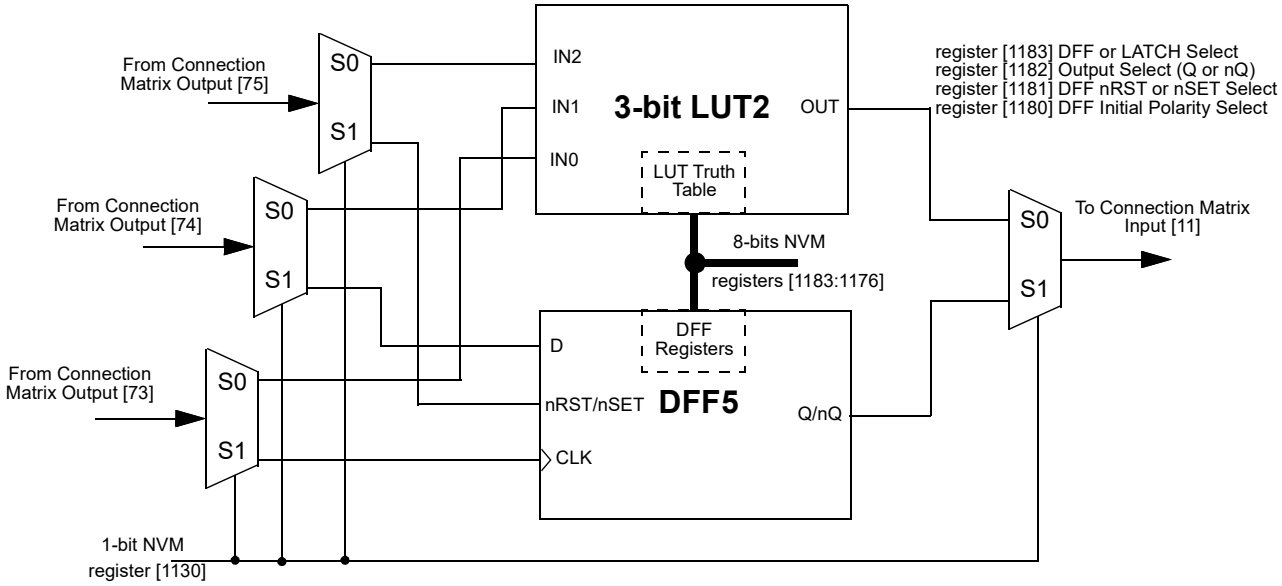


Figure 15: 3-bit LUT2 or DFF5

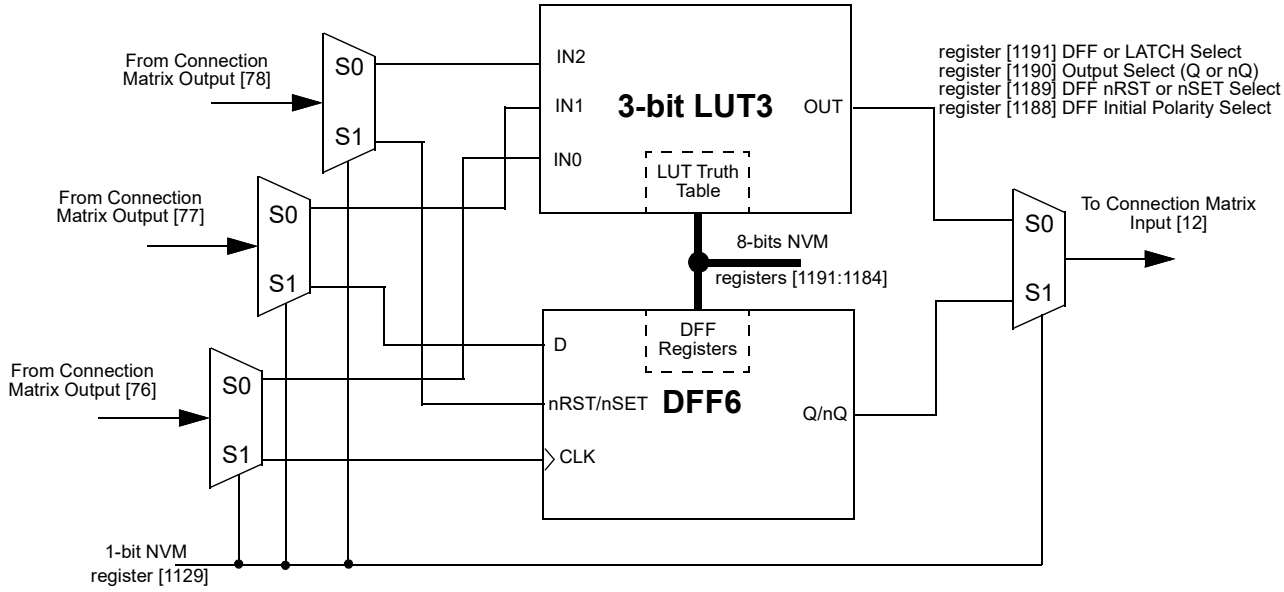


Figure 16: 3-bit LUT3 or DFF6

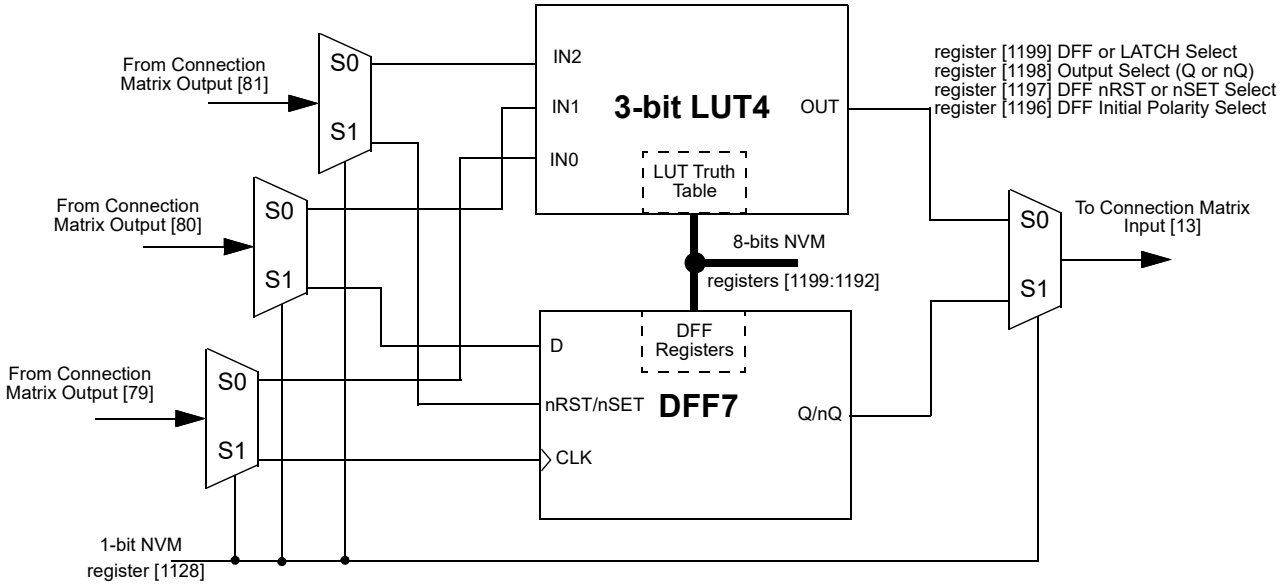


Figure 17: 3-bit LUT4 or DFF7

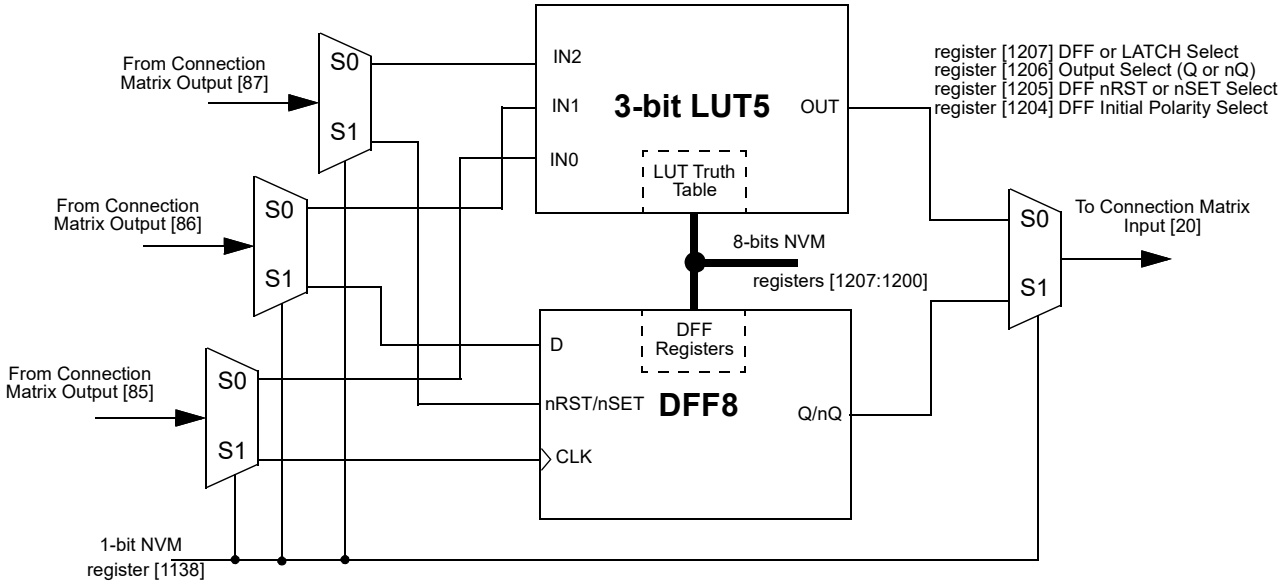


Figure 18: 3-bit LUT5 or DFF8

7.2.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUT

Table 49: 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1160]	LSB
0	0	1	register [1161]	
0	1	0	register [1162]	
0	1	1	register [1163]	
1	0	0	register [1164]	
1	0	1	register [1165]	
1	1	0	register [1166]	
1	1	1	register [1167]	MSB

Table 50: 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1168]	LSB
0	0	1	register [1169]	
0	1	0	register [1170]	
0	1	1	register [1171]	
1	0	0	register [1172]	
1	0	1	register [1173]	
1	1	0	register [1174]	
1	1	1	register [1175]	MSB

Table 51: 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1176]	LSB
0	0	1	register [1177]	
0	1	0	register [1178]	
0	1	1	register [1179]	
1	0	0	register [1180]	
1	0	1	register [1181]	
1	1	0	register [1182]	
1	1	1	register [1183]	MSB

Table 52: 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1184]	LSB
0	0	1	register [1185]	
0	1	0	register [1186]	
0	1	1	register [1187]	
1	0	0	register [1188]	
1	0	1	register [1189]	
1	1	0	register [1190]	
1	1	1	register [1191]	MSB

Table 53: 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1192]	LSB
0	0	1	register [1193]	
0	1	0	register [1194]	
0	1	1	register [1195]	
1	0	0	register [1196]	
1	0	1	register [1197]	
1	1	0	register [1198]	
1	1	1	register [1199]	MSB

Table 54: 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1200]	LSB
0	0	1	register [1201]	
0	1	0	register [1202]	
0	1	1	register [1203]	
1	0	0	register [1204]	
1	0	1	register [1205]	
1	1	0	register [1206]	
1	1	1	register [1207]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT0 is defined by registers [1167:1160]

3-Bit LUT1 is defined by registers [1175:1168]

3-Bit LUT2 is defined by registers [1183:1176]

3-Bit LUT3 is defined by registers [1191:1184]

3-Bit LUT4 is defined by registers [1199:1192]

3-Bit LUT5 is defined by registers [1207:1200]

Table 55 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

Table 55: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.2.2 3-BIT LUT OR D FLIP-FLOP MACROCELLS USED AS D FLIP-FLOP REGISTER SETTINGS

Table 56: DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_0 or DFF3 Select	[1132]	0: LUT3_0 1: DFF3
DFF3 Initial Polarity Select	[1164]	0: Low 1: High
DFF3 nRST/nSET Select	[1165]	0: nRST from matrix out 1: nSET from matrix out
DFF3 Output Select	[1166]	0: Q output 1: nQ output
DFF3 or LATCH Select	[1167]	0: DFF function 1: LATCH function

Table 57: DFF4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_1 or DFF4 Select	[1131]	0: LUT3_1 1: DFF4
DFF4 Initial Polarity Select	[1172]	0: Low 1: High
DFF4 nRST/nSET Select	[1173]	0: nRST from matrix out 1: nSET from matrix out
DFF4 Output Select	[1174]	0: Q output 1: nQ output
DFF4 or LATCH Select	[1175]	0: DFF function 1: LATCH function

Table 58: DFF5 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_2 or DFF5 Select	[1130]	0: LUT3_2 1: DFF5
DFF5 Initial Polarity Select	[1180]	0: Low 1: High
DFF5 nRST/nSET Select	[1181]	0: nRST from matrix out 1: nSET from matrix out
DFF5 Output Select	[1182]	0: Q output 1: nQ output
DFF5 or LATCH Select	[1183]	0: DFF function 1: LATCH function

Table 59: DFF6 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_3 or DFF6 Select	[1129]	0: LUT3_3 1: DFF6
DFF6 Initial Polarity Select	[1188]	0: Low 1: High
DFF6 nRST/nSET Select	[1189]	0: nRST from matrix out 1: nSET from matrix out
DFF6 Output Select	[1190]	0: Q output 1: nQ output
DFF6 or LATCH Select	[1191]	0: DFF function 1: LATCH function

Table 60: DFF7 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_4 or DFF7 Select	[1128]	0: LUT3_4 1: DFF7
DFF7 Initial Polarity Select	[1196]	0: Low 1: High
DFF7 nRST/nSET Select	[1197]	0: nRST from matrix out 1: nSET from matrix out
DFF7 Output Select	[1198]	0: Q output 1: nQ output
DFF7 or LATCH Select	[1199]	0: DFF function 1: LATCH function

Table 61: DFF8 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_5 or DFF8 Select	[1138]	0: LUT3_5 1: DFF8
DFF8 Initial Polarity Select	[1204]	0: Low 1: High

Table 61: DFF8 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
DFF8 nRST/nSET Select	[1205]	0: nRST from matrix out 1: nSET from matrix out
DFF8 Output Select	[1206]	0: Q output 1: nQ output
DFF8 or LATCH Select	[1207]	0: DFF function 1: LATCH function

7.2.3 Initial Polarity Operations

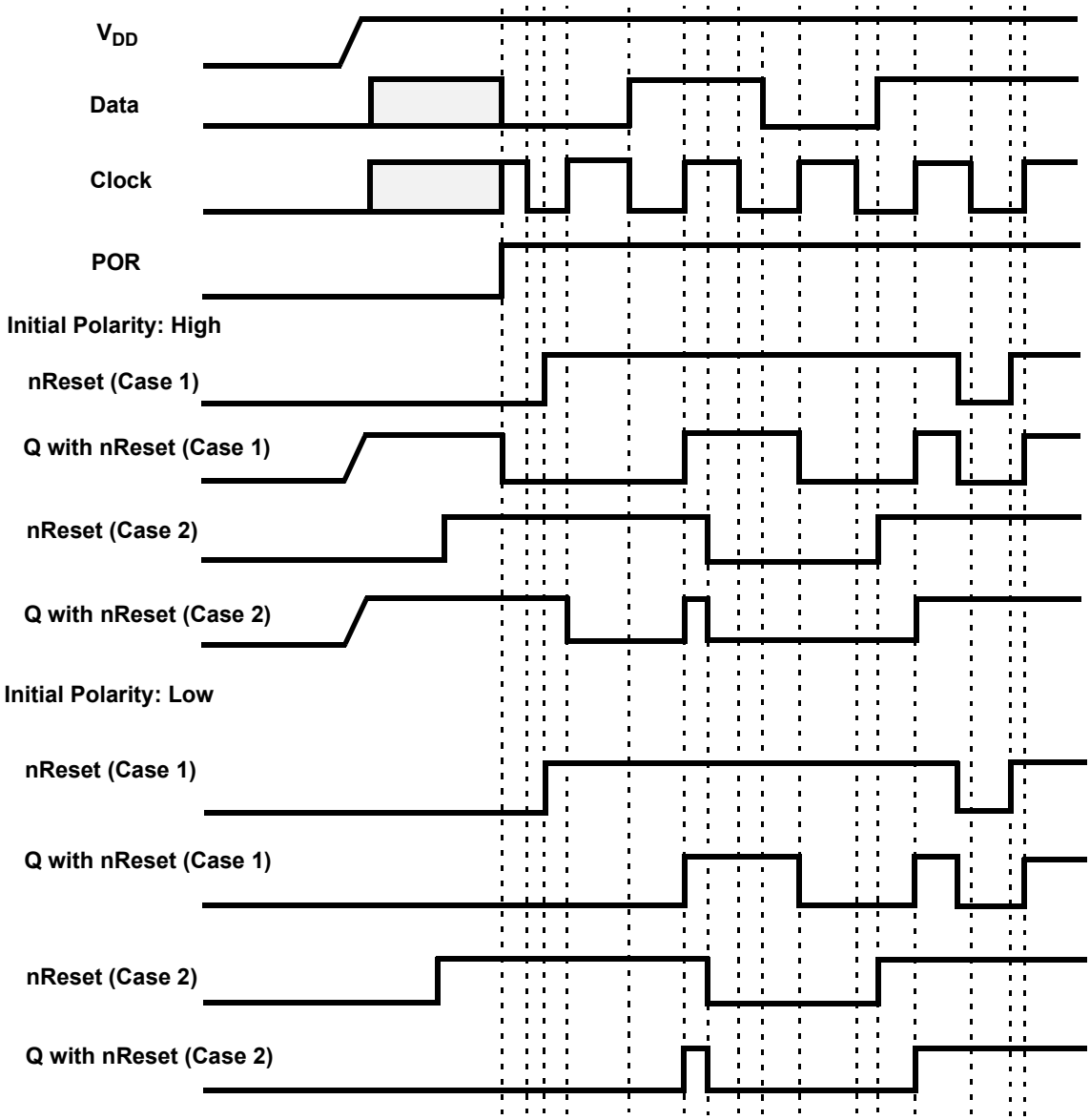


Figure 19: DFF Polarity Operations with nReset

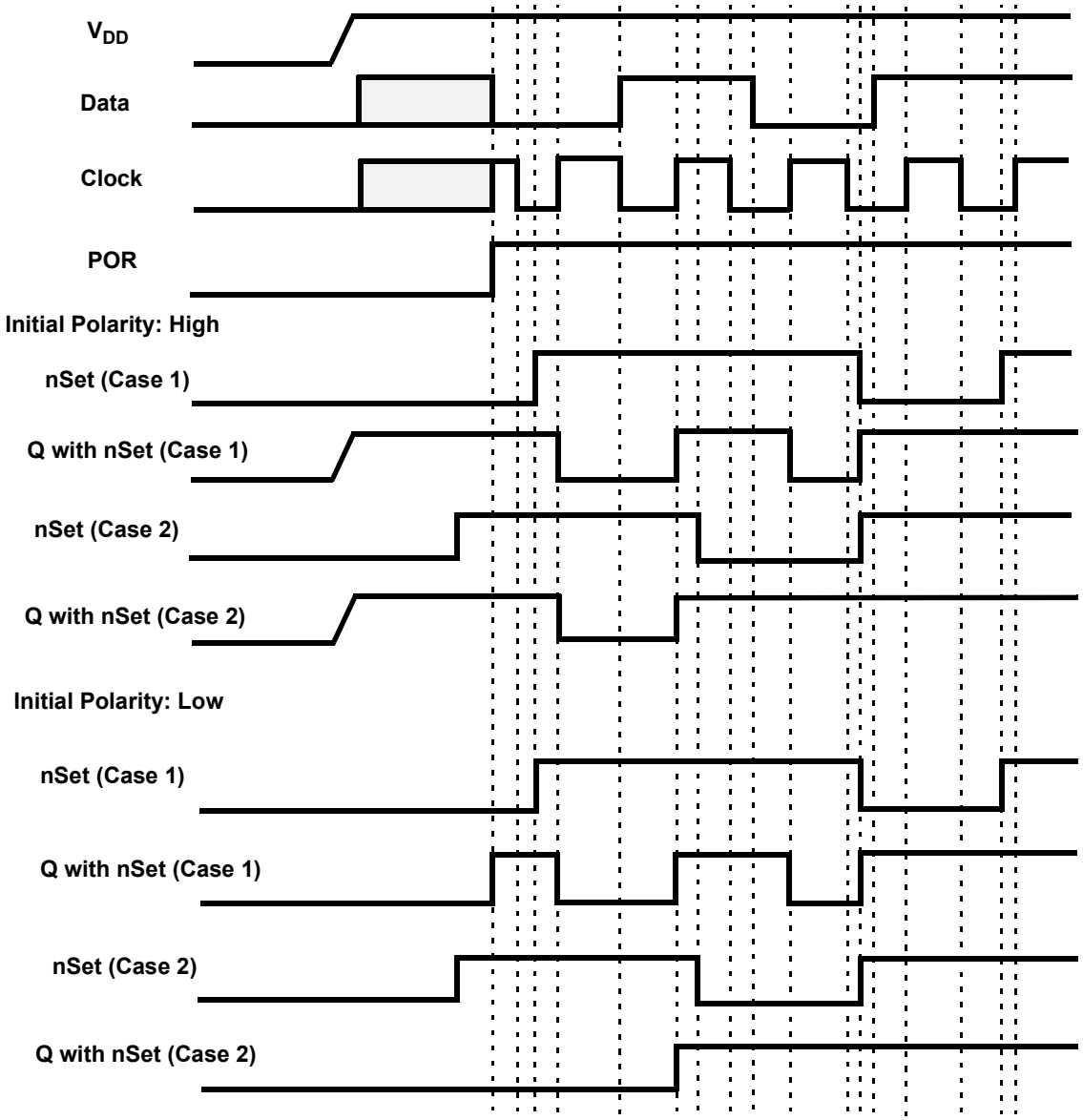


Figure 20: DFF Polarity Operations with nSet

7.3 3-BIT LUT OR PIPE DELAY/RIPPLE COUNTER MACROCELL

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (RST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 16-input MUX that is controlled by registers [1227:1224] for OUT0 and registers [1231:1228] for OUT1. The 16-input MUX is used to select the amount of delay.

The overall time of the delay is based on the clock used in the SLG46585 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46585). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [1239]).

In the Ripple Counter mode there are 3 options for setting, which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. It is a value, which will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting outputs code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

We can select one of the functionality modes by the register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV and others. (if SV is smaller than EV) or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV and others.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0 etc.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV etc. Please see Ripple counter functionality example in Figure 22.

Every step is executed by the rising edge on CLK input.

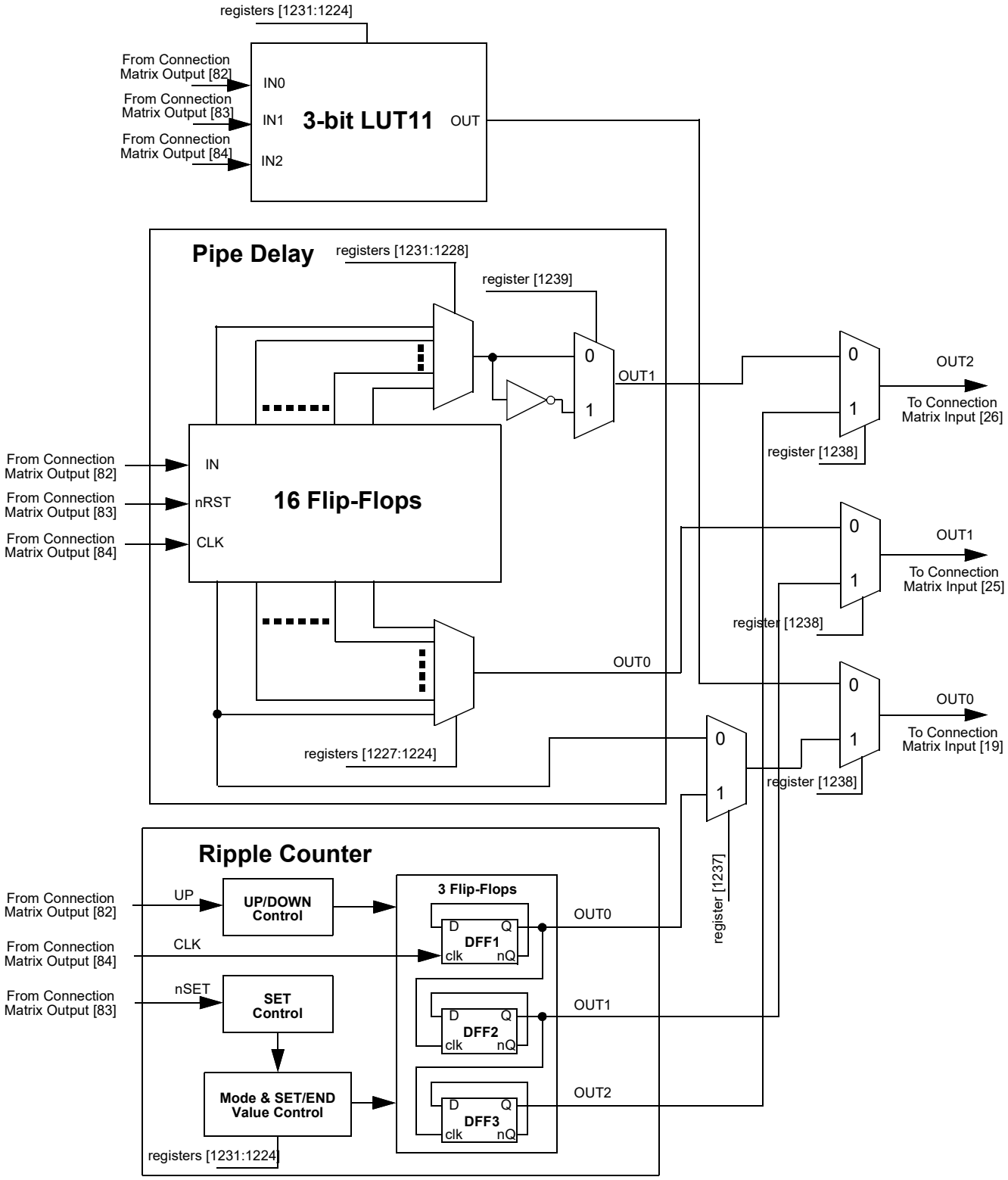


Figure 21: 3-bit LUT11/Pipe Delay/Ripple Counter

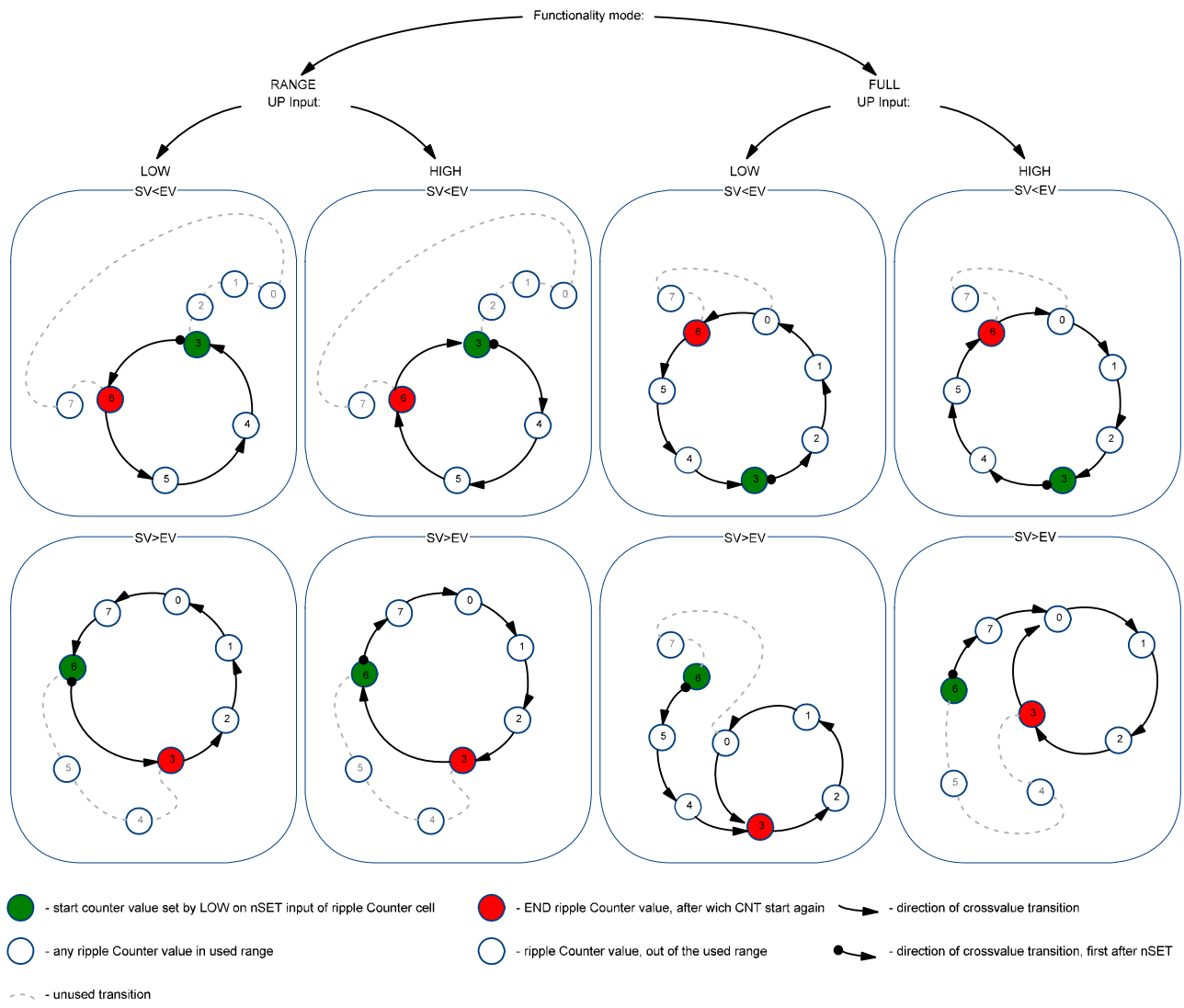


Figure 22: Example: Ripple Counter Functionality

7.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 62: 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1224]
0	0	1	register [1225]
0	1	0	register [1226]
0	1	1	register [1227]
1	0	0	register [1228]
1	0	1	register [1229]
1	1	0	register [1230]
1	1	1	register [1231]

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT11 is defined by registers [1231:1224]

7.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 63: Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 select	[1227:1224]	
OUT1 select	[1231:1228]	
Pipe Delay or Ripple Counter select	[1237]	0: Pipe Delay 1: Ripple Counter
LUT3_11 or Pipe Delay Output select	[1238]	0: LUT3_11 1: Pipe Delay/Ripple Counter by register [1237]
Pipe delay OUT1 Polarity Select Bit	[1239]	0: Non-inverted 1: Inverted

7.4 3-BIT LUT OR 8-BIT COUNTER/DELAY MACROCELLS

There are five macrocells that can serve as either 3-bit LUTs or as Counter/Delays. When used to implement LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter/Delay function, two of the three input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the counter/delay, with the output going back to the connection matrix.

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection or edge detection mode.

Two of the five macrocells can have their active count value read via I^2C (CNT2 and CNT4). See Section 19.5.2 for further details.

7.4.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

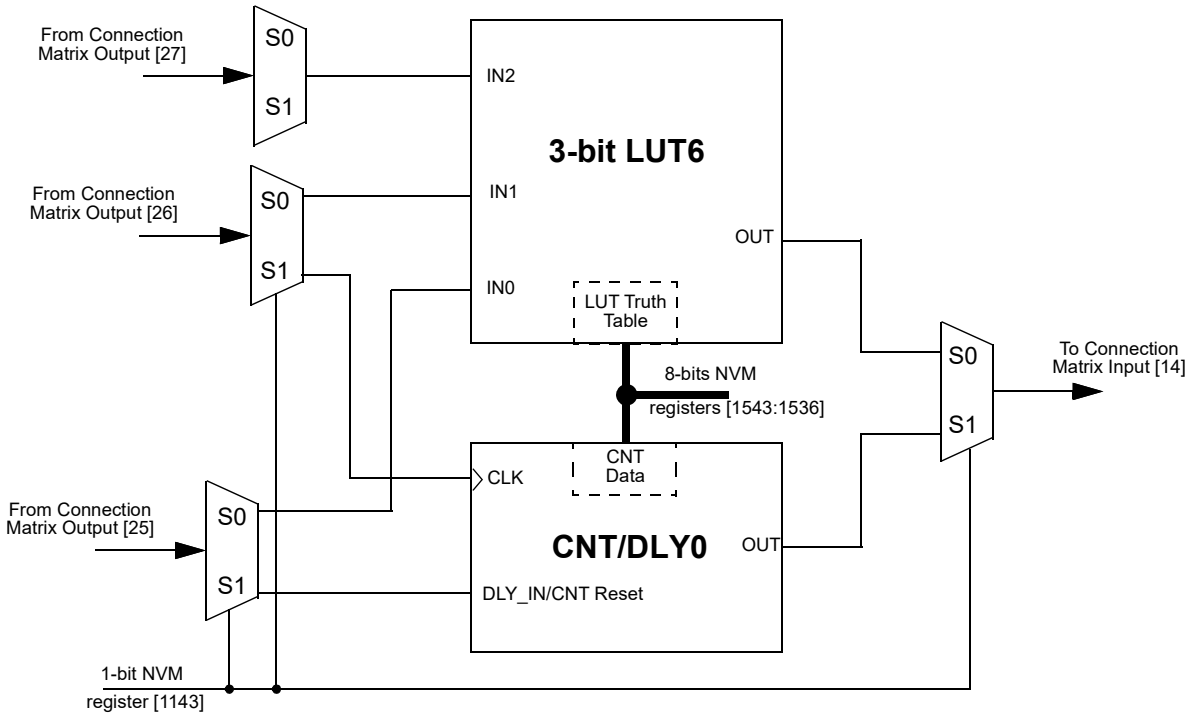


Figure 23: 3-bit LUT6 or CNT/DLY0

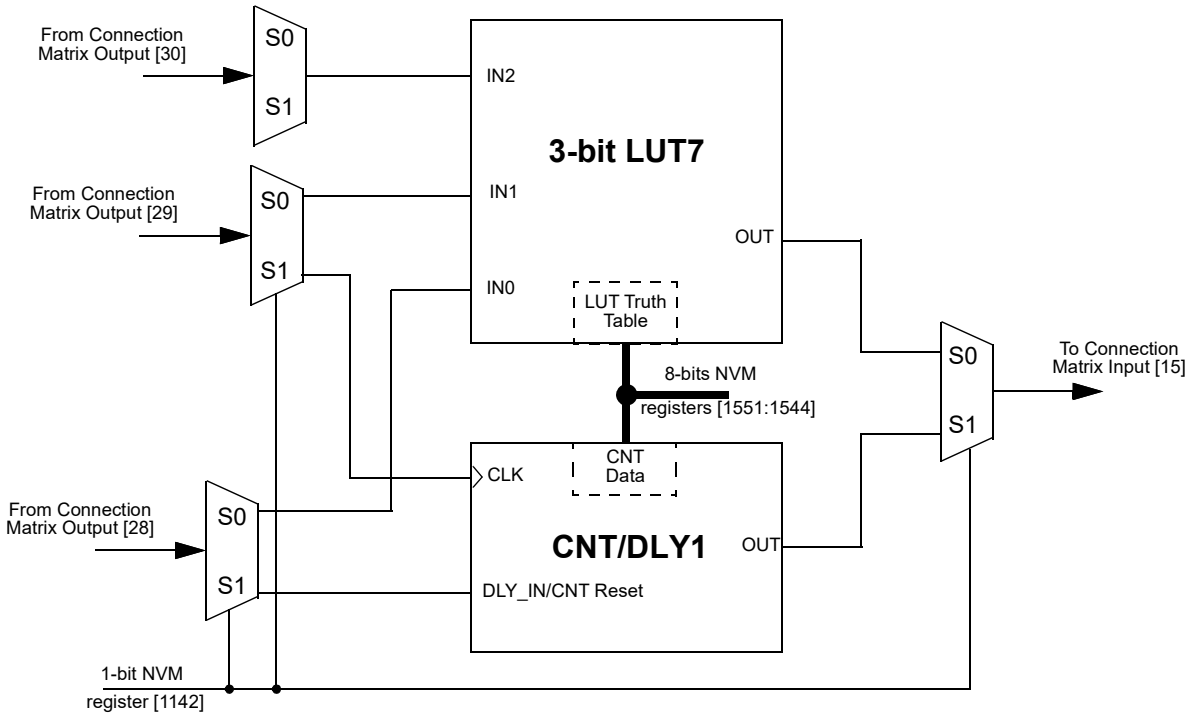


Figure 24: 3-bit LUT7 or CNT/DLY1

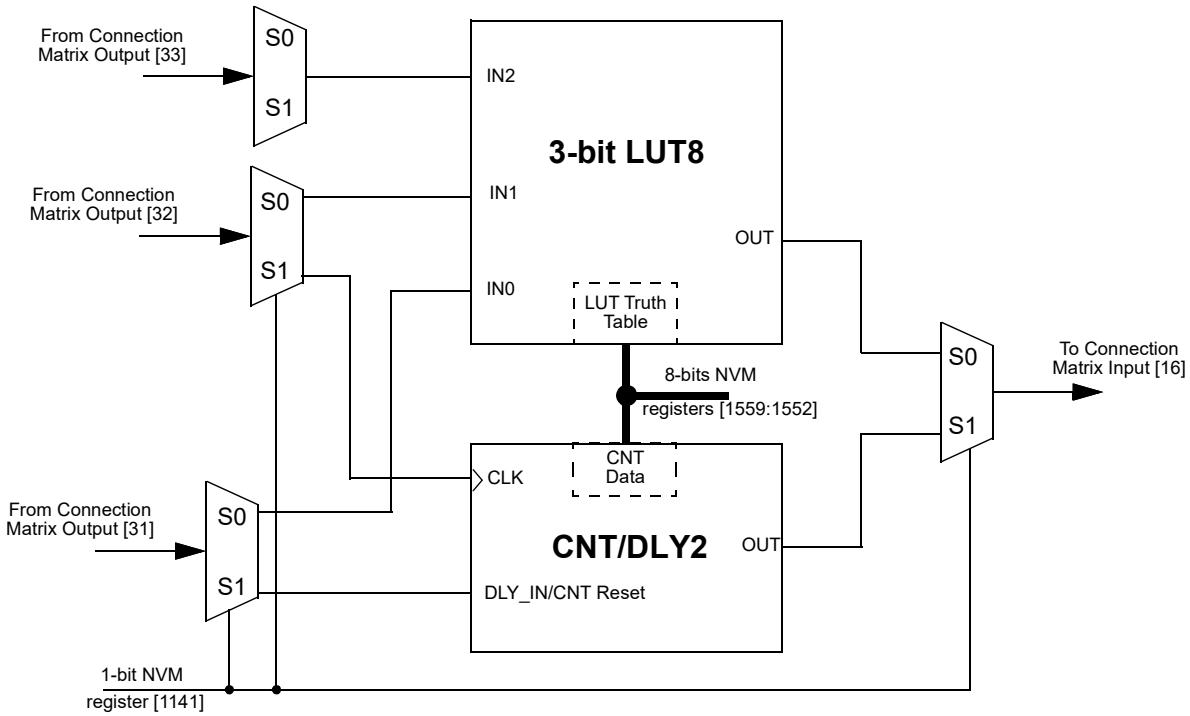


Figure 25: 3-bit LUT8 or CNT/DLY2

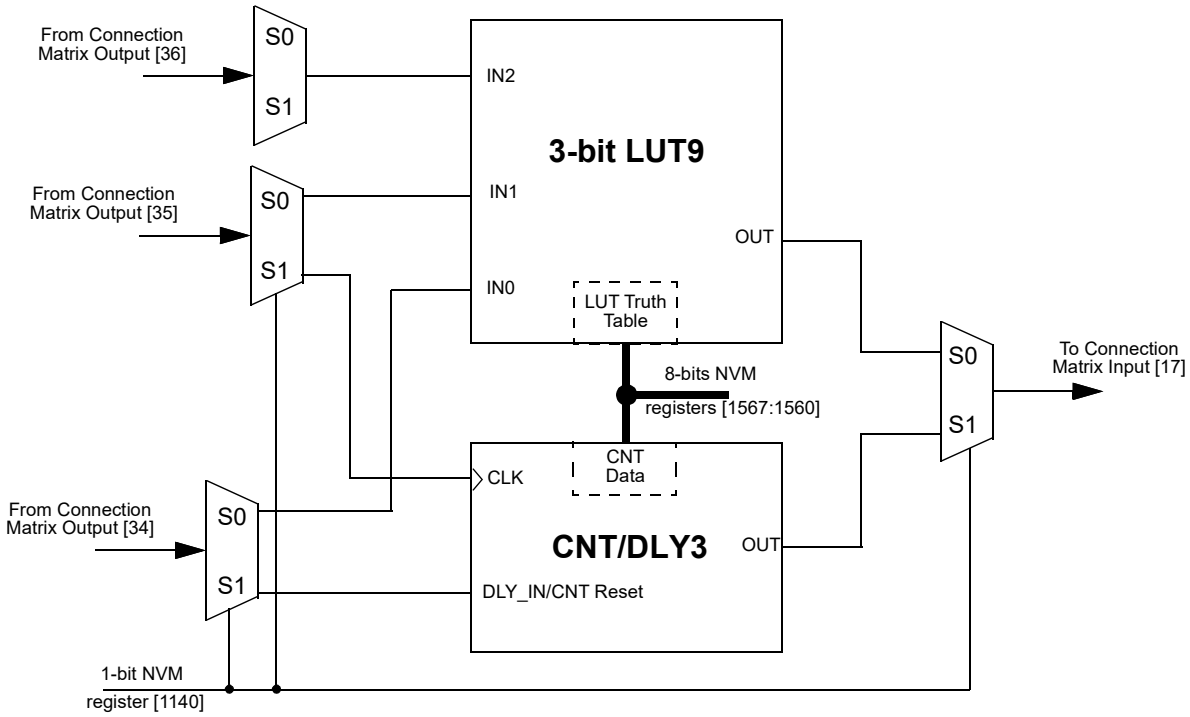


Figure 26: 3-bit LUT9 or CNT/DLY3

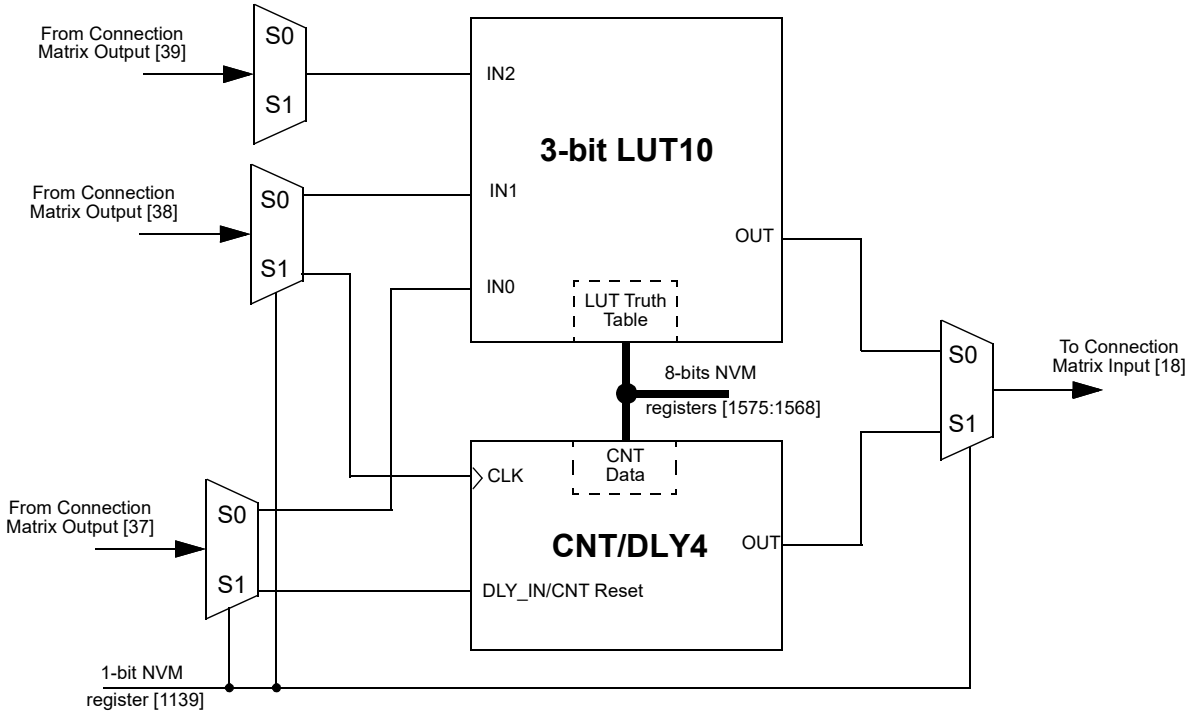


Figure 27: 3-bit LUT10 or CNT/DLY4

7.4.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 64: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1536]
0	0	1	register [1537]
0	1	0	register [1538]
0	1	1	register [1539]
1	0	0	register [1540]
1	0	1	register [1541]
1	1	0	register [1542]
1	1	1	register [1543]

Table 65: 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1544]
0	0	1	register [1545]
0	1	0	register [1546]
0	1	1	register [1547]
1	0	0	register [1548]
1	0	1	register [1549]
1	1	0	register [1550]
1	1	1	register [1551]

Table 66: 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1552]
0	0	1	register [1553]
0	1	0	register [1554]
0	1	1	register [1555]
1	0	0	register [1556]
1	0	1	register [1557]
1	1	0	register [1558]
1	1	1	register [1559]

Table 67: 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1560]
0	0	1	register [1561]
0	1	0	register [1562]
0	1	1	register [1563]
1	0	0	register [1564]
1	0	1	register [1565]
1	1	0	register [1566]
1	1	1	register [1567]

Table 68: 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1568]
0	0	1	register [1569]
0	1	0	register [1570]
0	1	1	register [1571]
1	0	0	register [1572]
1	0	1	register [1573]
1	1	0	register [1574]
1	1	1	register [1575]

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT6 is defined by registers [1543:1536]

3-Bit LUT7 is defined by registers [1551:1544]

3-Bit LUT8 is defined by registers [1559:1552]

3-Bit LUT9 is defined by registers [1567:1560]

3-Bit LUT10 is defined by registers [1575:1568]

Table 69 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

Table 69: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.4.3 3-Bit LUT or 8-Bit Counter/Delay Macrocells Used as 8-Bit Counter/Delay Register Settings

Table 70: CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_6 or Counter0 Select	[1143]	0: LUT3_6 1: Counter0
Delay0 Mode Select or asynchronous counter reset	[1241:1240]	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges/high level reset
Counter/delay0 Clock Source Select	[1244:1242]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter4 Overflow
CNT0‘s Q are Set to data or Reset to 0s Selection (8 bits)	[1245]	0: Reset to 0s 1: Set to data (Register [1543:1536])
Counter/delay0 Mode Selection	[1247:1246]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay0 Control Data	[1543:1536]	1 – 256 (delay time = (counter control data +1)/freq)

Table 71: CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_7 or Counter1 Select	[1142]	0: LUT3_7 1: Counter1
Delay1 Mode Select or asynchronous counter reset	[1249:1248]	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges/high level reset

Table 71: CNT/DLY1 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
Counter/delay1 Clock Source Select	[1252:1250]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter0 Overflow
Counter/delay1 Output Selection for Counter mode	[1253]	0: Default Output 1: Edge Detector Output
Counter/delay1 Delayed Edge Output Selection	[1236]	0: Default Output from register [1253] 1: Delayed Edge Detect
Counter/delay1 Mode Selection	[1255:1254]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay1 Control Data	[1551:1544]	1 – 256 (delay time = (counter control data +1)/freq)

Table 72: CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_8 or Counter2 Select	[1141]	0: LUT3_8 1: Counter2
Delay2 Mode Select or asynchronous counter reset	[1257:1256]	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges/high level reset
Counter/delay2 Clock Source Select	[1260:1258]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter1 Overflow
Counter/delay2 Output Selection for Counter mode	[1261]	0: Default Output 1: Edge Detector Output
Counter/delay2 Delayed Edge Output Selection	[1235]	0: Default Output from register [1261] 1: Delayed Edge Detect
Counter/delay2 Mode Selection	[1263:1262]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay2 Control Data	[1559:1552]	1 – 256 (delay time = (counter control data +1)/freq)

Table 73: CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_9 or Counter3 Select	[1140]	0: LUT3_9 1: Counter3
Delay3 Mode Select or asynchronous counter reset	[1265:1264]	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges/high level reset
Counter/delay3 Clock Source Select	[1268:1266]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter2 Overflow
Counter/delay3 Output Selection for Counter mode	[1269]	0: Default Output 1: Edge Detector Output
Counter/delay3 Delayed Edge Output Selection	[1234]	0: Default Output from register [1269] 1: Delayed Edge Detect
Counter/delay3 Mode Selection	[1271:1270]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay3 Control Data	[1567:1560]	1 – 256 (delay time = (counter control data +1)/freq)

Table 74: CNT/DLY4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_10 or Counter4 Select	[1139]	0: LUT3_10 1: Counter4
Delay4 Mode Select or asynchronous counter reset	[1273:1272]	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges/high level reset
Counter/delay4 Clock Source Select	[1276:1274]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter1 Overflow
Counter/delay4 Output Selection for Counter mode	[1277]	0: Default Output 1: Edge Detector Output
Counter/delay4 Delayed Edge Output Selection	[1233]	0: Default Output from register [1277] 1: Delayed Edge Detect

Table 74: CNT/DLY4 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
Counter/delay4 Mode Selection	[1279:1278]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay4 Control Data	[1575:1568]	1 – 256 (delay time = (counter control data +1)/freq)

Table 75: DLY/CNT Polarity Select

Signal Function	Register Bit Address	Register Definition
Select the polarity of DLY/CNT0's output	[1287]	0: Default Output 1: Inverted Output
Select the polarity of DLY/CNT1's output	[1286]	0: Default Output 1: Inverted Output
Select the polarity of DLY/CNT2's output	[1285]	0: Default Output 1: Inverted Output
Select the polarity of DLY/CNT3's output	[1284]	0: Default Output 1: Inverted Output
Select the polarity of DLY/CNT4's output	[1283]	0: Default Output 1: Inverted Output

7.5 CNT/DLY TIMING DIAGRAMS

7.5.1 Delay Mode

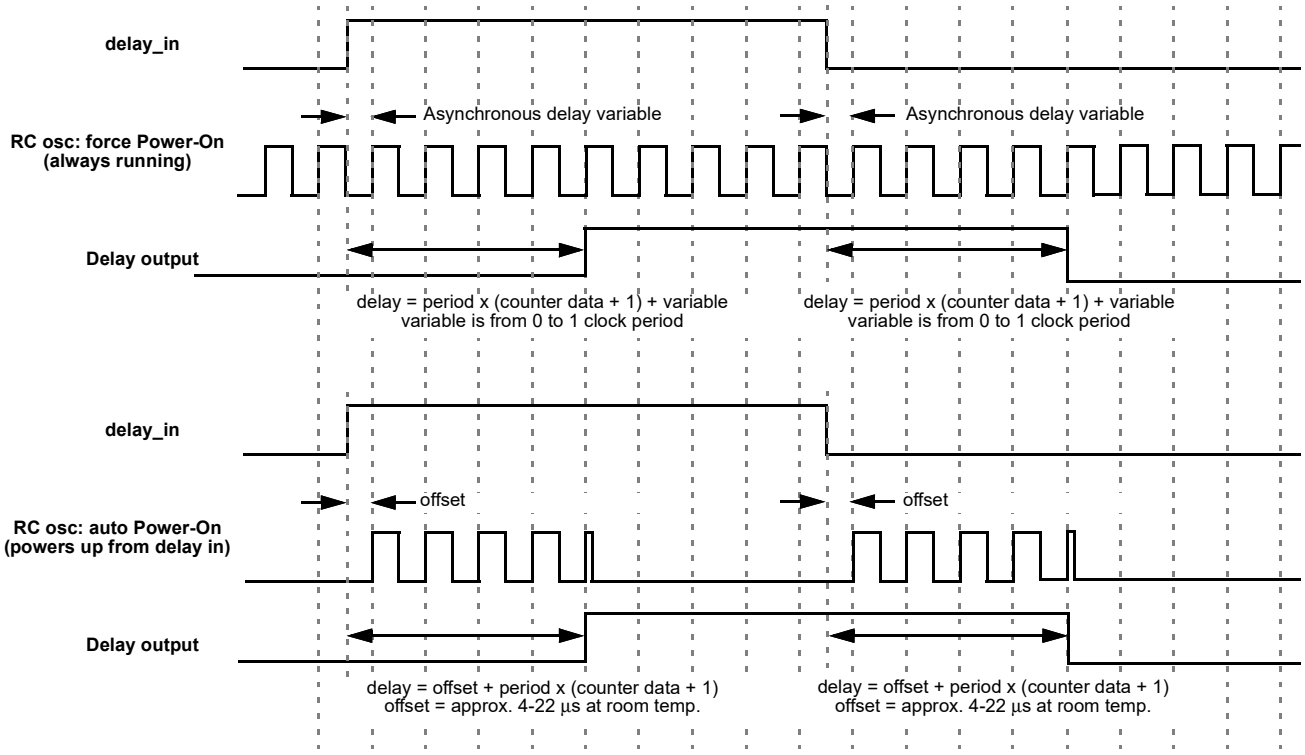


Figure 28: Delay Mode Timing Diagram, Edge Select: Both, Counter Data:3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

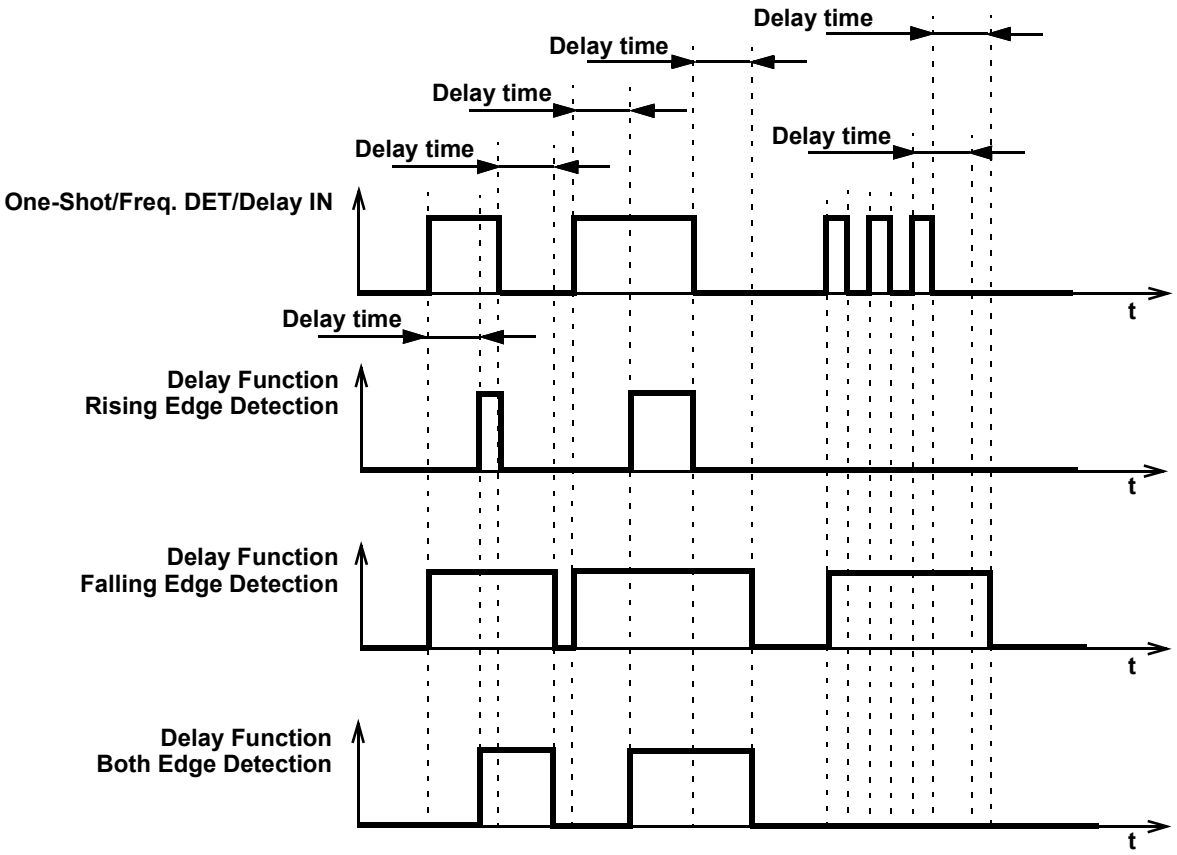


Figure 29: Delay Mode Timing Diagram for Different Edge Select Modes

7.5.2 Count Mode (Count Data:3), Counter Reset (Rising Edge Detect Reset by Reset_In Input)

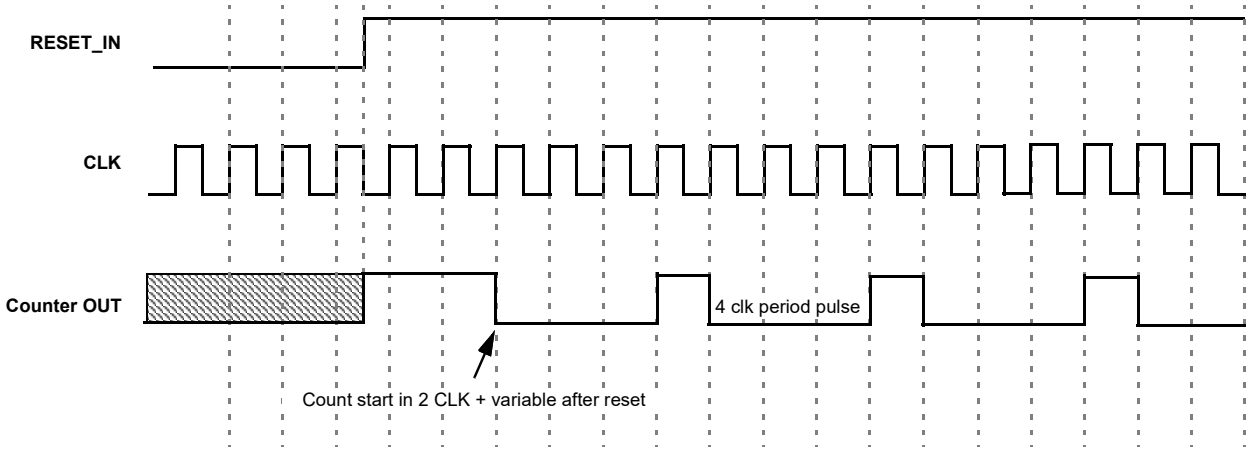


Figure 30: Counter Mode Timing Diagram with Reset Signal

7.5.3 Count Mode (Count Data:3), Counter Set (Rising Edge Detect Set by Set_In Input)

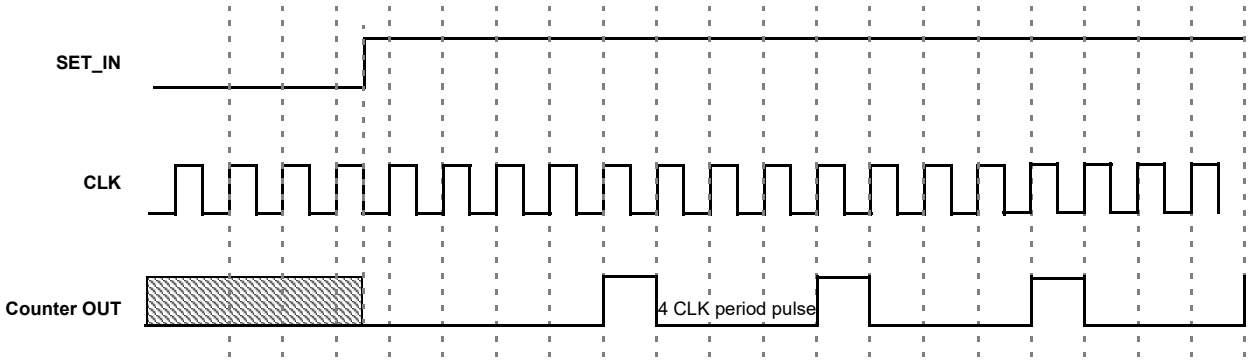


Figure 31: Counter Mode Timing Diagram with SET Signal (only for DLY/CNT0)

7.5.4 One-Shot Mode

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. There is also an option to ignore or detect selected edge during pulse is outputting. The following diagram is showing one-shot function for non-inverted output.

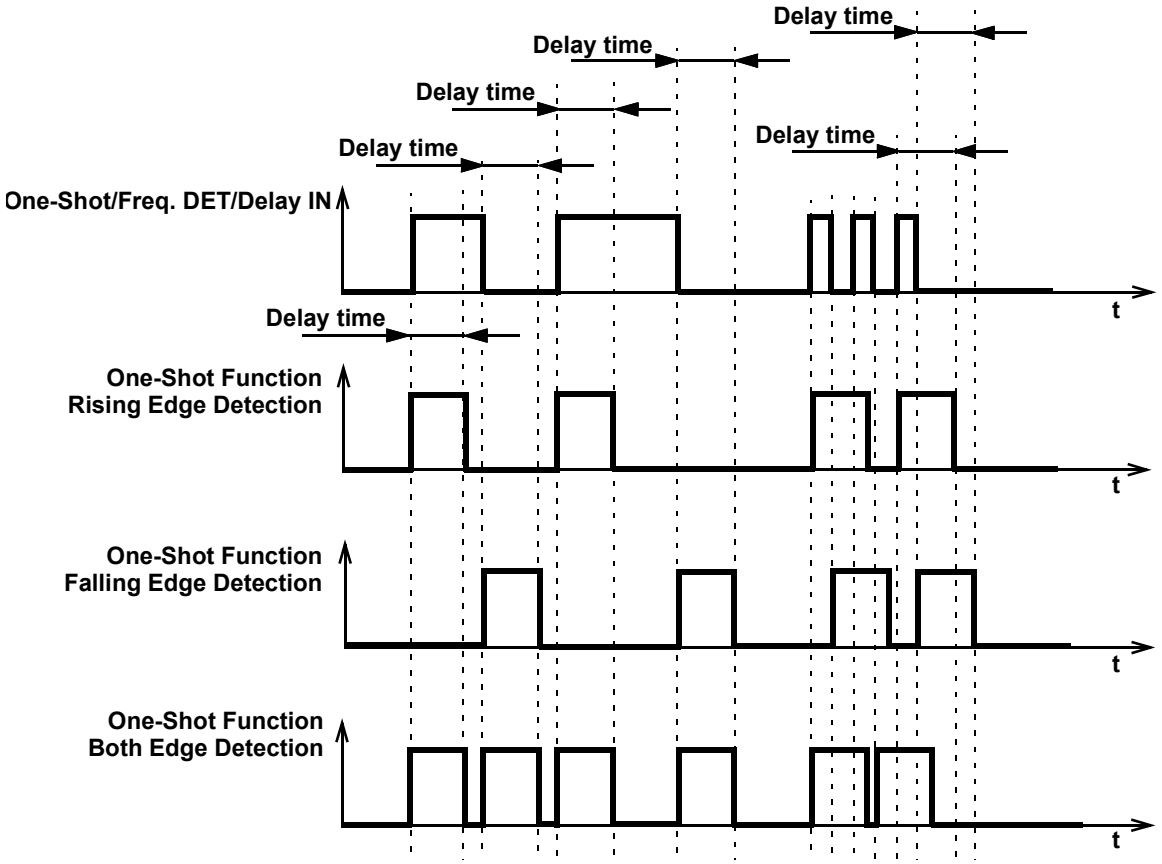


Figure 32: One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data and clock selection properties) when detecting the respective edge. It does not restart while pulse is high.

7.5.5 Frequency Detection Mode

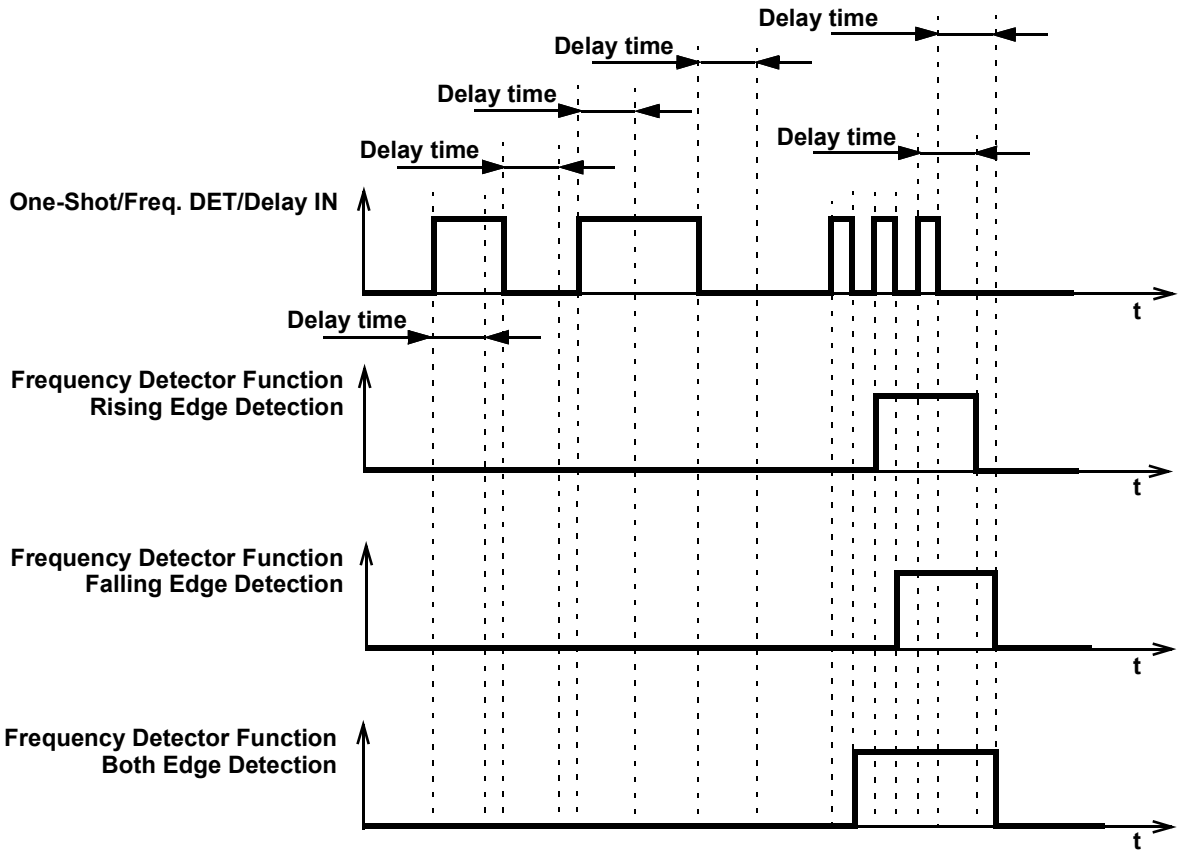


Figure 33: Frequency Detection Mode Timing Diagram

Rising Edge: The output goes high if the time between two successive rising edges is less than the set time. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two successive falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

7.5.6 Edge Detection Mode

The macrocell generates high level short pulse when detecting the respective edge. See Table 12.

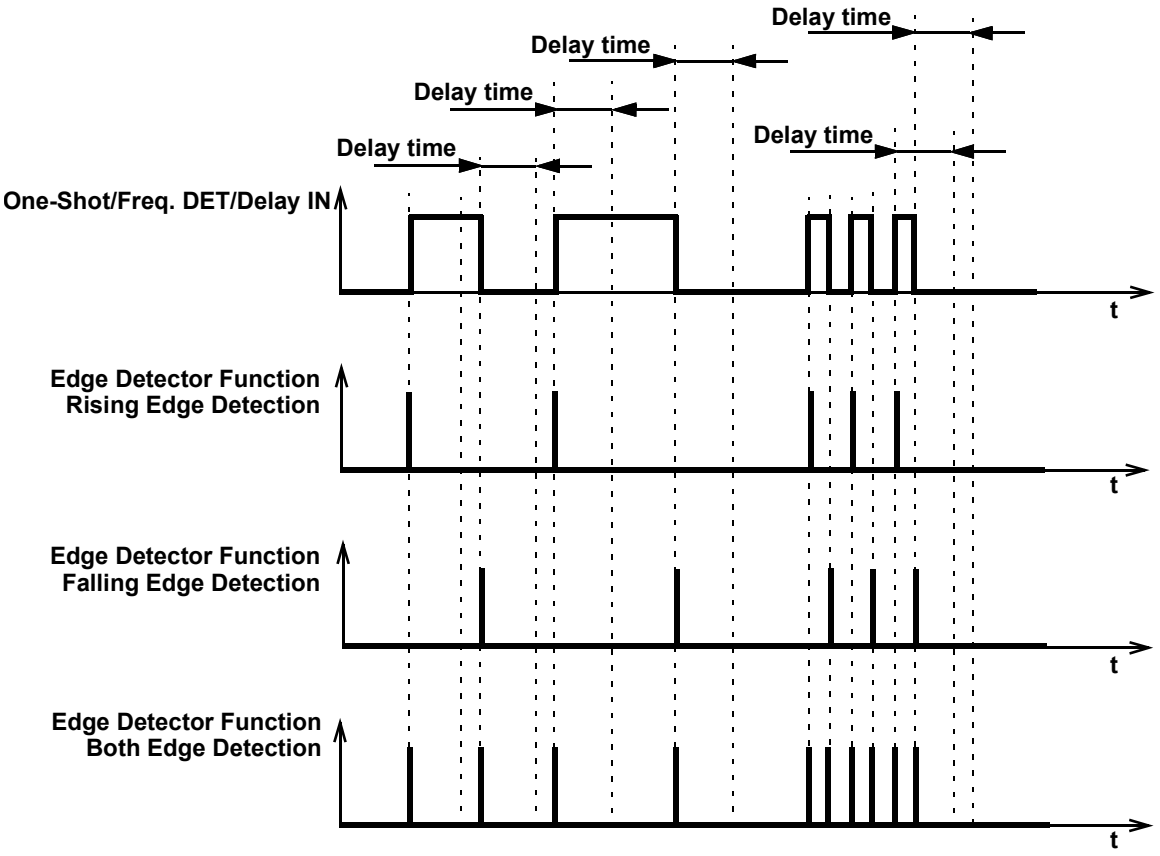


Figure 34: Edge Detection Mode Timing Diagram (Except DLY/CNT0)

7.5.7 Delayed Edge Detection Mode

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 35.

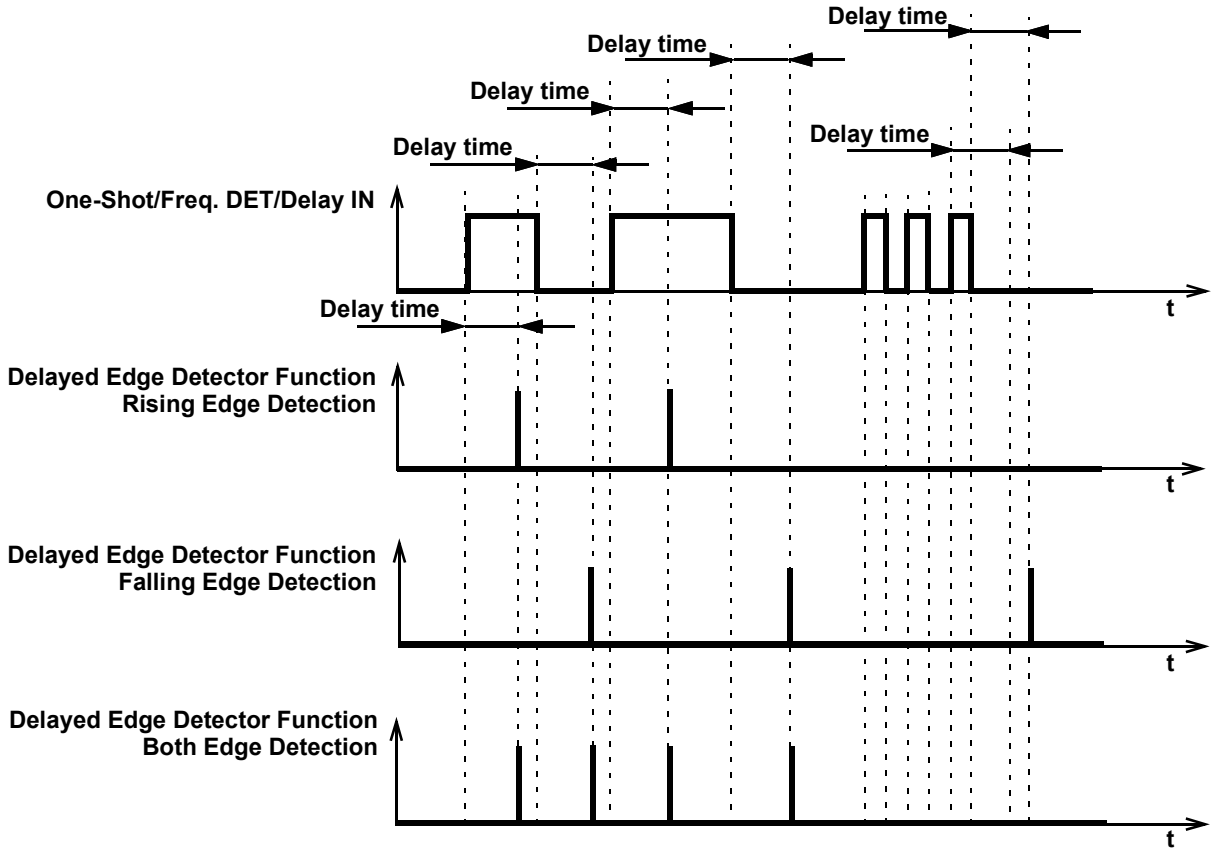


Figure 35: Delayed Edge Detection Mode Timing Diagram (Except DLY/CNT0)

7.6 WAKE AND SLEEP CONTROLLER

The SLG46585 has a Wake and Sleep function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1247:1246] = 11 and register [1447] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 8-bit counter.

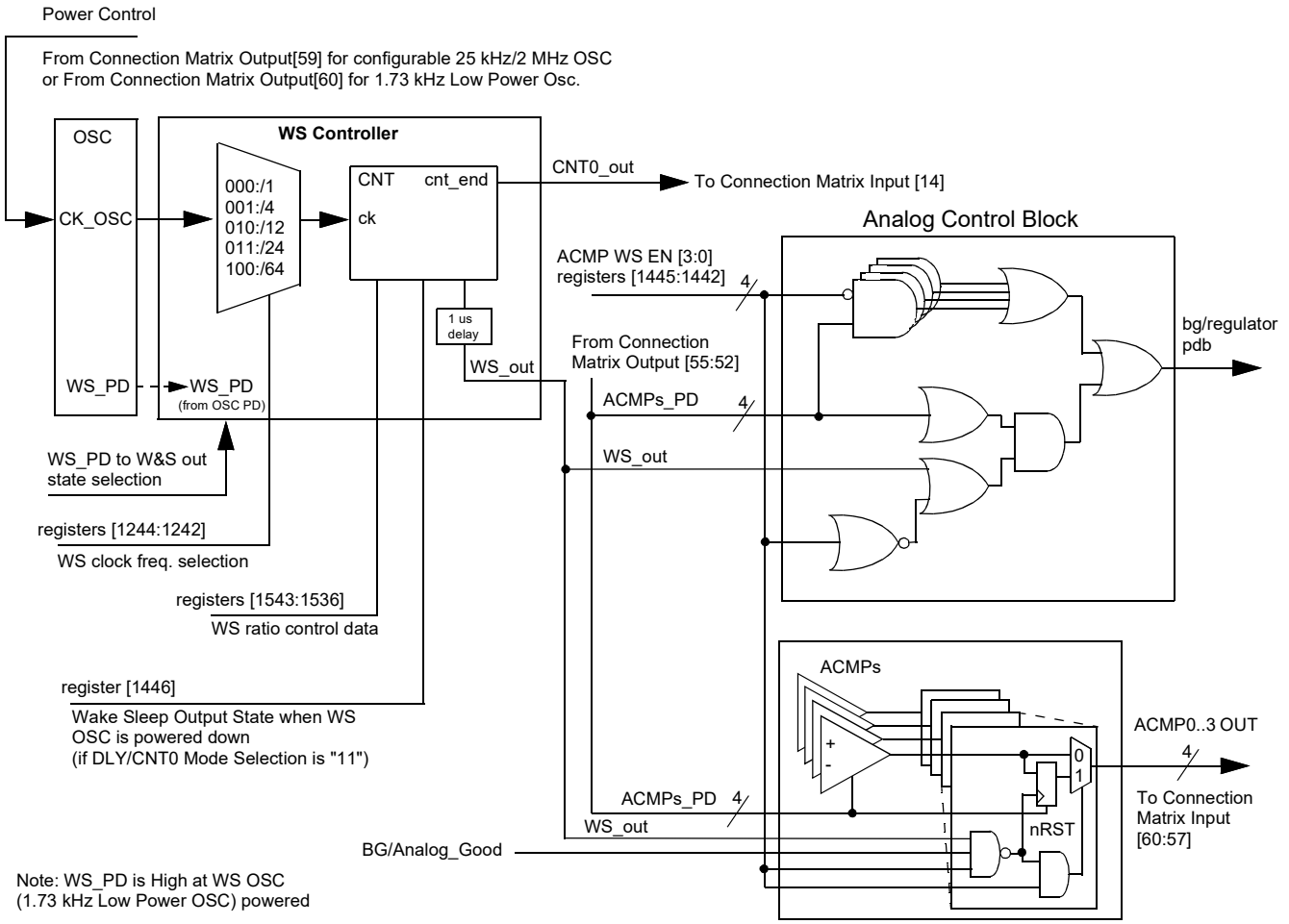


Figure 36: Wake/Sleep Controller

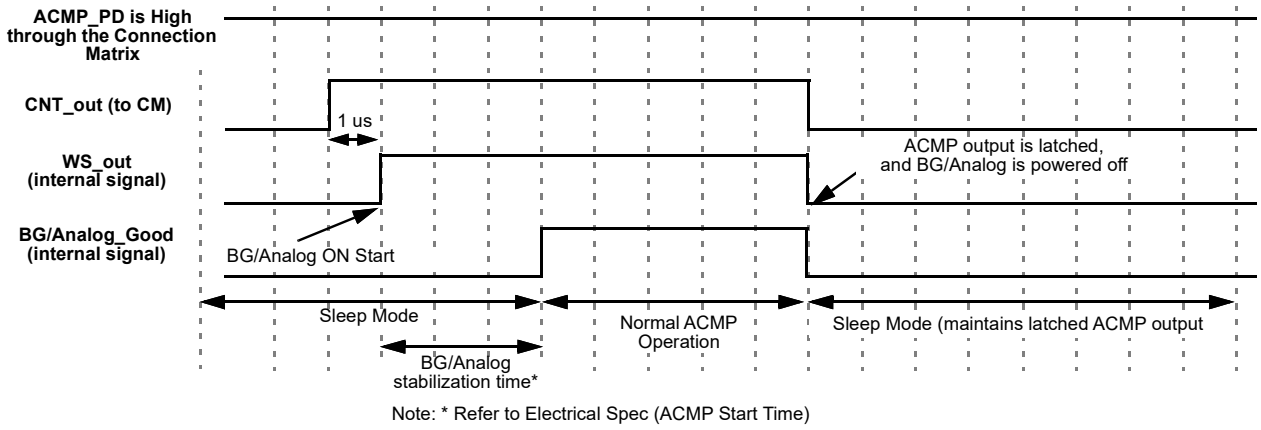


Figure 37: Wake/Sleep Timing Diagram

To use any ACMP under WS controller the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately).
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs).
- Register WS => enable (for each ACMP separately).
- CNT/DLY0 set/reset input = 0 (for all ACMPs).

For the OSC, any oscillator with any pre-divider can be used. The user can select a period of time while the ACMPs are sleeping in a range of 1 - 255 clock cycles. Before they are sent to sleep their outputs are latched so the ACMPs remain their state (High or Low) while sleeping. When the WS signal is High, it takes a BG time (refer to electrical spec) to turn the ACMPs on. The wake time must be longer than BG/Analog Power-On time.

Note: If 25 kHz/2 MHz Oscillator is used for WS, the 1.73 kHz Low Power OSC must be set to Force Power-On.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power-Down option is selected; Power-Down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on
  If OSC is powered off (Power-Down option is selected; Power-Down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off
  Both cases WS function is turned off

- Counter Data (Range: 1 to 255)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears

  Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn the ACMPs on. When Reset signal goes out, the WS counter will go Low and turn the ACMPs off until the counter counts up to the end

  Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn the ACMPs off. When Set signal goes out, the WS counter will go on counting and High level signal will turn the ACMPs on while counter is counting up to the end.

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High.

Note: Q mode operates only in case of "High Level Set/Reset".

8 Combinatorial Logic

8.1 4-BIT LUT WITH TWO OUTPUTS

There is one 4-bit LUT with two outputs. The device also includes fifteen Combination Function Macrocells that can be used as LUTs. For more details please see Section 8.

Inputs/Outputs for the nine LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

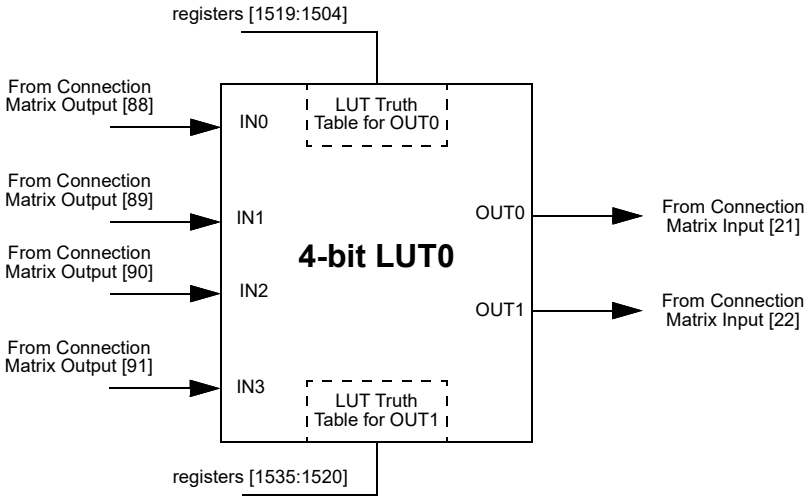


Figure 38: 4-bit LUT0 with Two Outputs

Table 76: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT0	OUT1	
0	0	0	0	register [1504]	register [1520]	LSB
0	0	0	1	register [1505]	register [1521]	
0	0	1	0	register [1506]	register [1522]	
0	0	1	1	register [1507]	register [1523]	
0	1	0	0	register [1508]	register [1524]	
0	1	0	1	register [1509]	register [1525]	
0	1	1	0	register [1510]	register [1526]	
0	1	1	1	register [1511]	register [1527]	
1	0	0	0	register [1512]	register [1528]	
1	0	0	1	register [1513]	register [1529]	
1	0	1	0	register [1514]	register [1530]	
1	0	1	1	register [1515]	register [1531]	
1	1	0	0	register [1516]	register [1532]	
1	1	0	1	register [1517]	register [1533]	
1	1	1	0	register [1518]	register [1534]	
1	1	1	1	register [1519]	register [1535]	MSB

This macrocell uses a 16-bit register to define their output function. Table 77 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within the 4-bit LUT logic cell.

4-Bit LUT0 OUT0 is defined by registers [1519:1504]

4-Bit LUT0 OUT1 is defined by registers [1535:1520]

Table 77: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

9 Analog Comparators

There are four Analog Comparator (ACMP) macrocells in the SLG46585. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0 PWR UP, ACMP1 PWR UP, ACMP2 PWR UP, and ACMP3 PWR UP) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is LOW.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal Vref or provided by way of the external sources.

PWR UP = 1 => ACMP is powered up.
PWR UP = 0 => ACMP is powered down.

During power-up, the ACMP output will remain low, and then become valid 2 ms (max) after ACMP power up signal goes HIGH. If V_{DD} is greater than 2.7 V, then power up time will decrease.

Vref accuracy is optimized near 1000 mV selection.
Input bias current < 1 nA (typ). The Gain divider is unbuffered and consists of 1 MΩ resistors. IN- voltage range: 0 to 1.2 V. Can use Vref selection $V_{DD}/4$ and $V_{DD}/3$ to maintain this input range.

Table 78: Gain Divider Input Resistance

Gain	x1	x0.5	x0.33	x0.25
Input Resistance	100 MΩ	1 MΩ	0.75 MΩ	1 MΩ

To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the V_{DD} signal.

Each of the ACMP cells has a selection for the bandwidth of the input signal, which can be used to save power when low bandwidth signals are input into the analog comparator.

Note that power supply control options have influence on Analog macrocells operation.

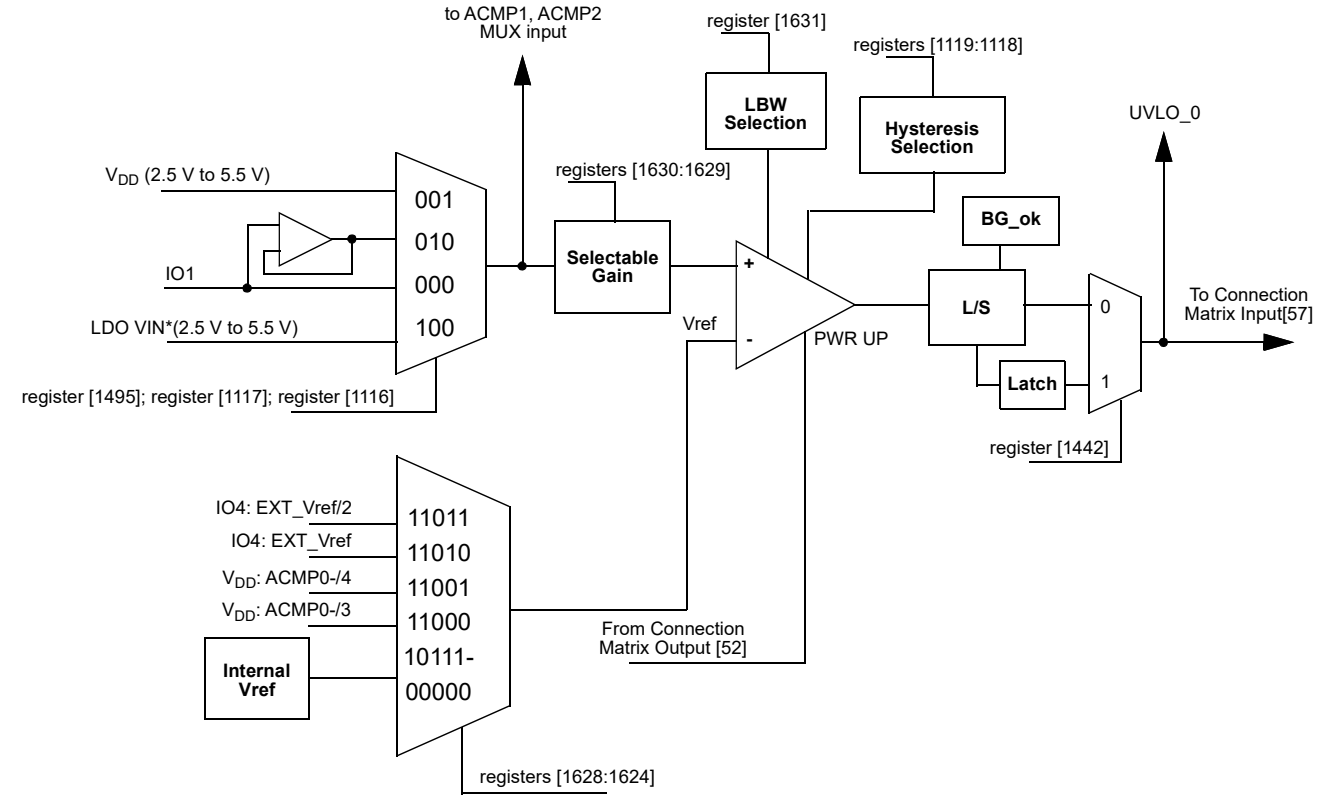
Note: Any ACMP powered ON enables the BandGap circuit as well, and an analog voltage will appear on Vref (even when Force BandGap is disabled).

Each cell also has a hysteresis selection, to offer hysteresis of (0, 25, 50, 200) mV. ACMP2 and ACMP3 has additional hysteresis options for 100 mV and 150 mV.

Note: the 25 mV hysteresis option works with either internal or external Vref, while all other options work with internal Vref only. The (50, 100, 150, 200) mV hysteresis options are one way hysteresis. This means that actual thresholds will be Vref (high threshold) and Vref - hysteresis (low threshold). The ACMP output will retain its output value if the input voltage is within the threshold window (between Vref and Vref - hysteresis). The 25 mV hysteresis option threshold levels will be Vref + hysteresis/2 (high threshold) and Vref - hysteresis/2 (low threshold).

Hysteresis: Input signal hysteresis options are disable, 25 mV, 50 mV, 200 mV (and additionally 100 mV and 150 mV for ACMP2 and ACMP3).
ACMP0 IN+ options are IO1, buffered IO1, V_{DD}, LDO0/1 VIN.
ACMP1 IN+ options are IO2, buffered IO2, ACMP0 IN+, LDO2/3 VIN.
ACMP2 IN+ options are IO5, ACMP0 IN+, Temp. Sensor.
ACMP3 IN+ options are IO6, ACMP2 IN+, LDO0 VOUT and LDO2 VOUT.

9.1 ACMP0 BLOCK DIAGRAM AND REGISTER SETTINGS



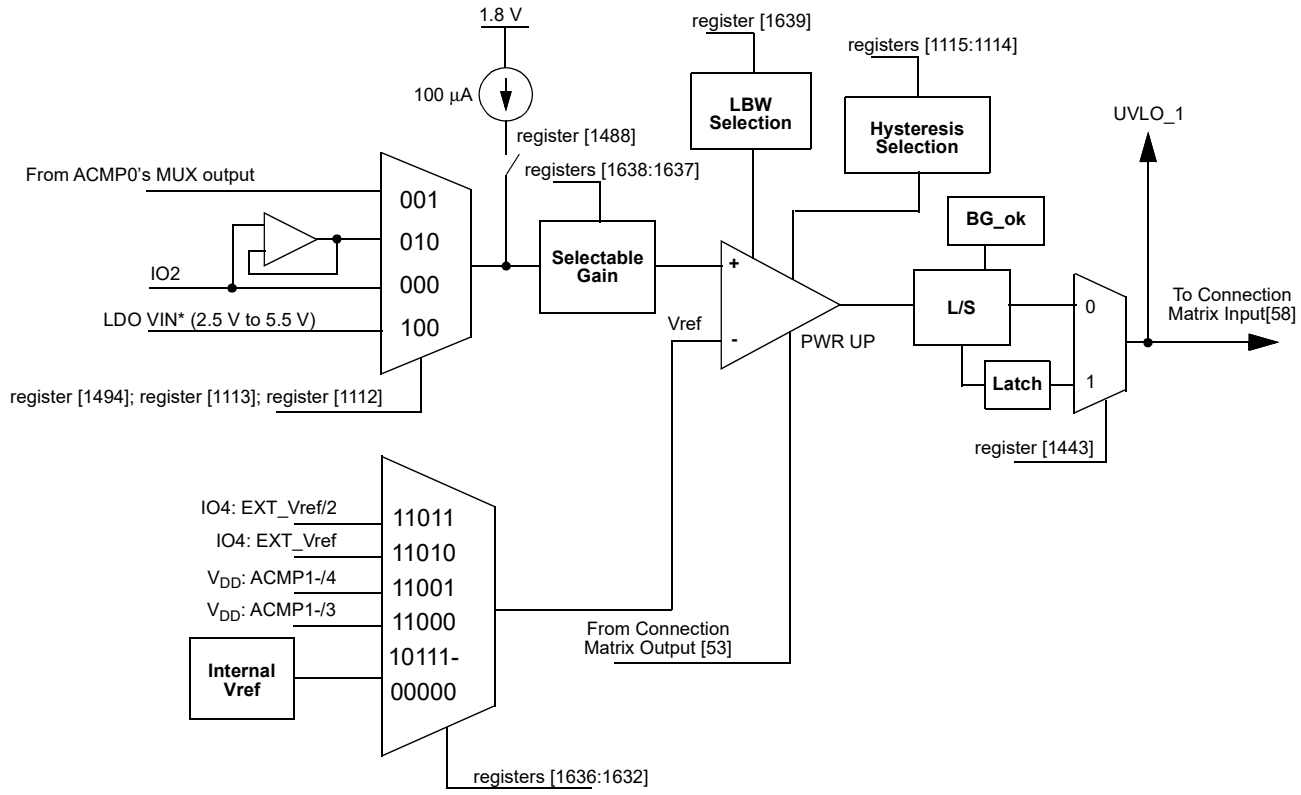
Note*: See Sections 2.2 to 2.4.

Figure 39: ACMP0 Block Diagram

Table 79: ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 Positive Input Source Select V_{DD}	[1116]	0: Disable 1: Enable
Analog Buffer at ACMP0 Enable (Max. BW 1 MHz)	[1117]	0: Disable analog buffer 1: Enable analog buffer
ACMP0 Hysteresis Enable	[1119:1118]	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV) (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50 mV & 200 mV hysteresis.)
ACMP0 Wake & Sleep function Enable	[1442]	0: Disable 1: Enable
LDO0/1 VIN connection enable to ACMP0	[1495]	0: Default ACMP function 1: Enable UVLO0 function
ACMP0 In Voltage Select	[1628:1624]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}: ACMP0-/3 11001: V_{DD}: ACMP0-/4 11010: IO4: EXT_Vref 11011: IO4: EXT_Vref/2
ACMP0 Positive Input Divider	[1630:1629]	00: 1.00x 01: 0.50x 10: 0.33x 11: 0.25x
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	[1631]	0: Off 1: On

9.2 ACMP1 BLOCK DIAGRAM AND REGISTER SETTINGS



Note*: See Sections 2.2 to 2.4.

Figure 40: ACMP1 Block Diagram

Table 80: ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 Positive Input Source Select - ACMP0 IN+ Source	[1112]	0: Disable 1: Enable
Analog Buffer at ACMP1 Enable (Max. BW 1 MHz)	[1113]	0: Disable analog buffer 1: Enable analog buffer
ACMP1 Hysteresis Enable	[1115:1114]	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV) (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50 mV & 200 mV hysteresis.)
ACMP1 Wake & Sleep function Enable	[1443]	0: Disable 1: Enable
ACMP1 100 uA Current Source Enable	[1488]	0: Disable 1: Enable
LDO2/3 VIN connection enable to ACMP1	[1494]	0: Default ACMP function 1: Enable UVLO1 function
ACMP1 In Voltage Select	[1636:1632]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}: ACMP1-/3 11001: V_{DD}: ACMP1-/4 11010: IO4: EXT_Vref 11011: IO4: EXT_Vref/2
ACMP1 Positive Input Divider	[1638:1637]	00: 1.00x 01: 0.50x 10: 0.33x 11: 0.25x
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	[1639]	0: Off 1: On

9.3 ACMP2 BLOCK DIAGRAM AND REGISTER SETTINGS

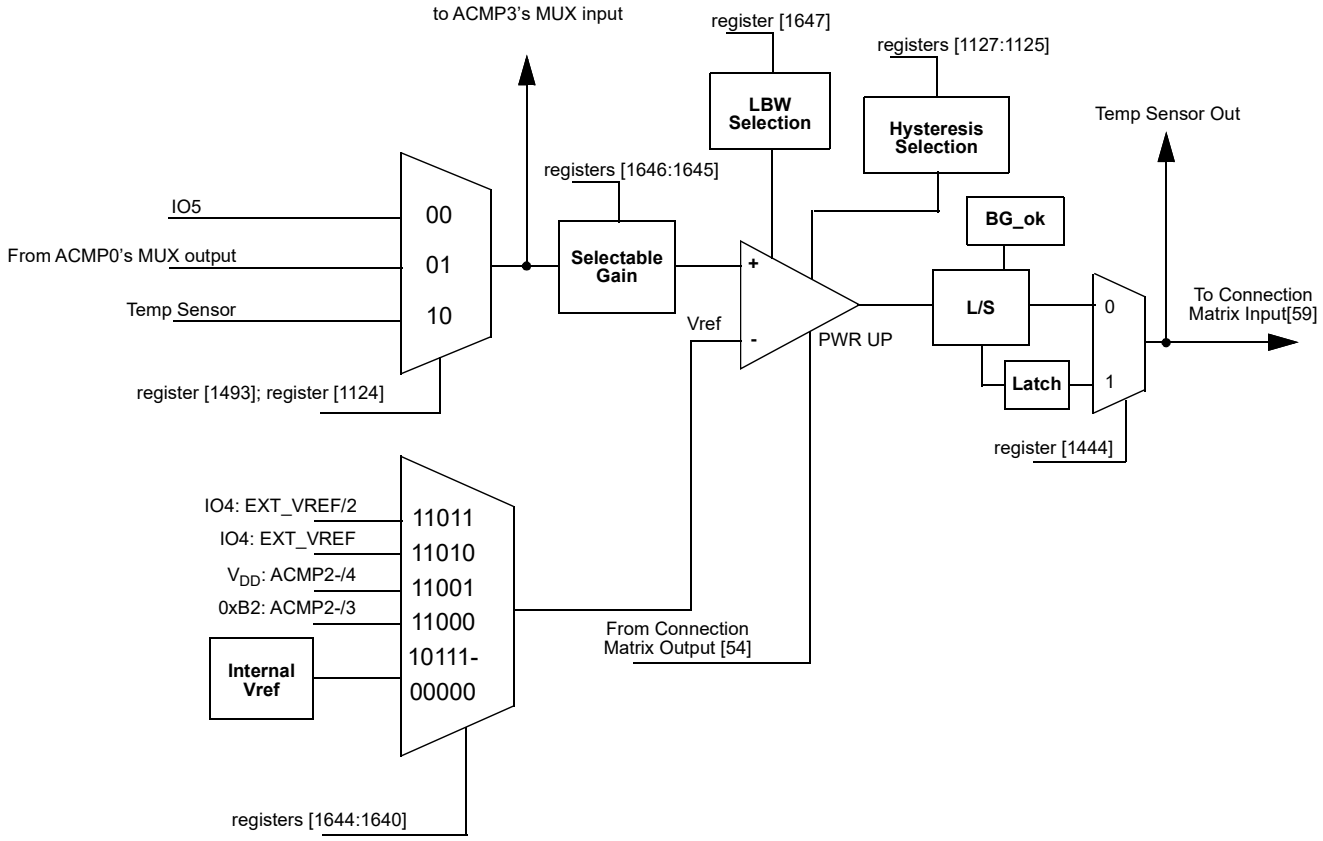
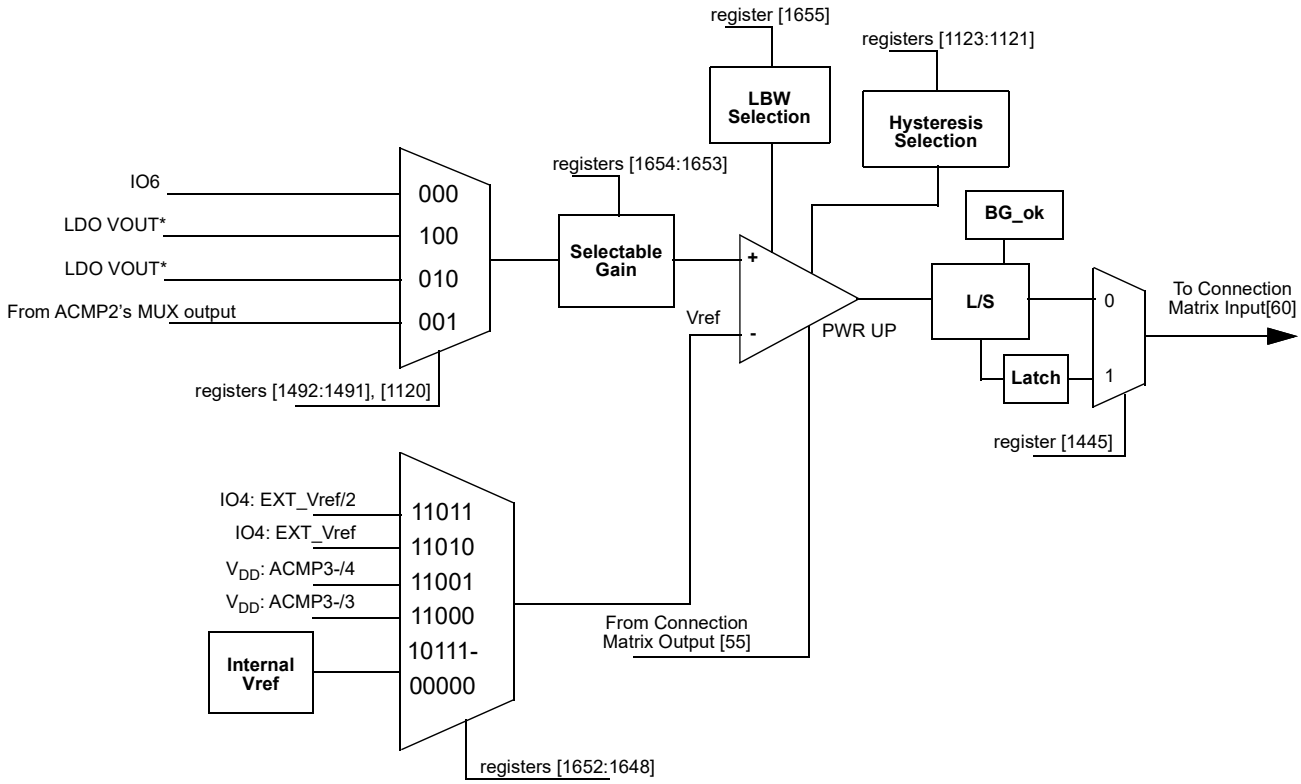


Figure 41: ACMP2 Block Diagram

Table 81: ACMP2 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP2 Positive Input Source Select - ACMP0 IN+ Source	[1124]	0: Disable 1: Enable
ACMP2 Hysteresis Enable	[1127:1125]	000: 0 mV 001: 25 mV 010: 50 mV 011: 200 mV 100: Reserved 101: Reserved 110: 100 mV 111: 150 mV (001: for both external & internal Vref, 010 & 011 & 110 & 111: for only internal Vref, External Vref will not have (50, 100, 150, 200) mV hysteresis.)
ACMP2 Wake & Sleep function Enable	[1444]	0: Disable 1: Enable
TS output connection enable to ACMP2	[1493]	0: Default ACMP function 1: Enable TS function
ACMP2 In Voltage Select	[1644:1640]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}: ACMP2-/3 11001: V_{DD}: ACMP2-/4 11010: IO4: EXT_Vref 11011: IO4: EXT_Vref/2
ACMP2 Positive Input Divider	[1646:1645]	00: 1.00x 01: 0.50x 10: 0.33x 11: 0.25x
ACMP2 Low Bandwidth (Max: 1 MHz) Enable	[1647]	0: Off 1: On

9.4 ACMP3 BLOCK DIAGRAM AND REGISTER SETTINGS



Note*: See Sections 2.2 to 2.4.

Figure 42: ACMP3 Block Diagram

Table 82: ACMP3 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP3 Positive Input Source Select - ACMP2 IN+ Source	[1120]	0: Disable 1: Enable
ACMP3 Hysteresis Enable	[1123:1121]	000: 0 mV 001: 25 mV 010: 50 mV 011: 200 mV 100: Reserved 101: Reserved 110: 100 mV 111: 150 mV (001: for both external & internal Vref, 010 & 011 & 110 & 111: for only internal Vref, External Vref will not have (50, 100, 150, 200) mV hysteresis.)
ACMP3 Wake & Sleep function Enable	[1445]	0: Disable 1: Enable
LDO2 VOUT output connection enable to ACMP3	[1491]	0: Default ACMP function 1: Enable LDO2 VOUT function

Table 82: ACMP3 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
LDO0 VOUT output connection enable to ACMP3	[1492]	0: Default ACMP function 1: Enable LDO0 VOUT function
ACMP3 In Voltage Select	[1652:1648]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}: ACMP3-/3 11001: V_{DD}: ACMP3-/4 11010: IO4: EXT_Vref 11011: IO4: EXT_Vref/2
ACMP3 Positive Input Divider	[1654:1653]	00: 1.00x 01: 0.50x 10: 0.33x 11: 0.25x
ACMP3 Low Bandwidth (Max: 1 MHz) Enable	[1655]	0: Off 1: On

9.5 ACMPS TYPICAL PERFORMANCE

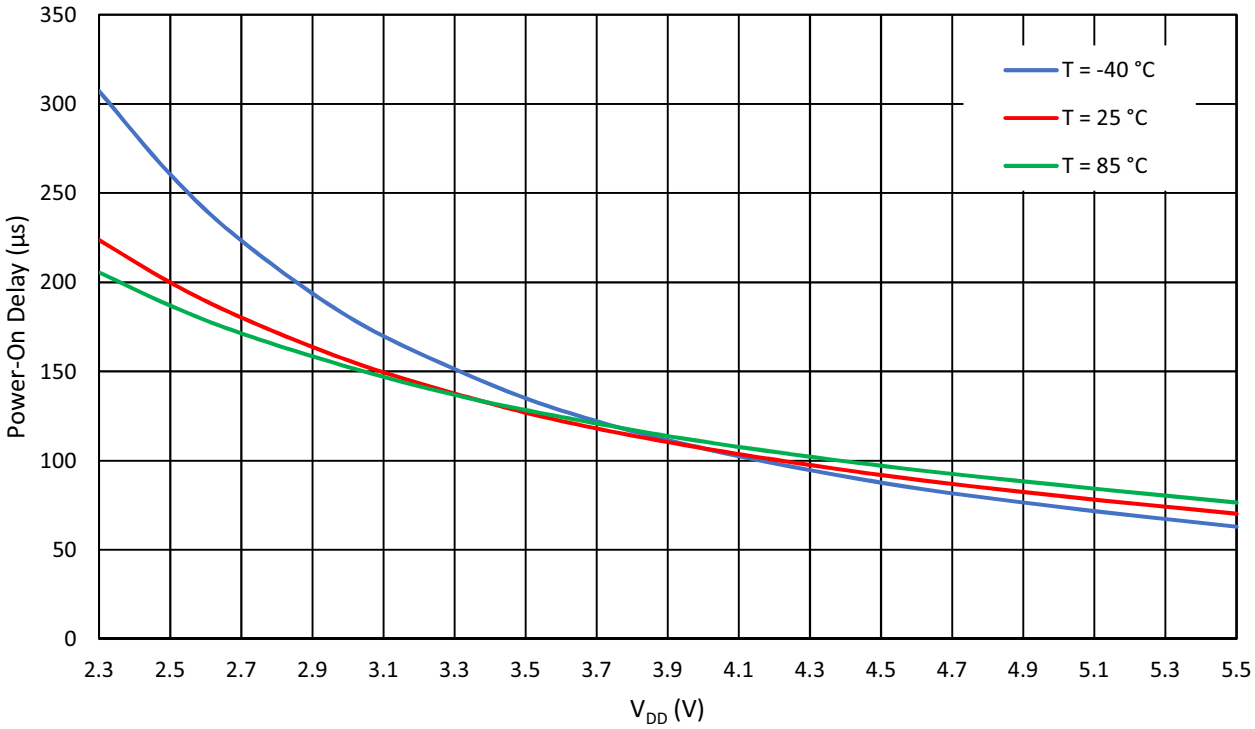


Figure 43: ACMPs Power-On Delay vs. V_{DD}

10 Pipe Delay

The SLG46585 has a pipe delay logic cell that is shared with the 3-bit LUT11 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. Please see Section 7.3.1 for the description of this Combination Function macrocell.

11 Programmable Delay/Edge Detector

The SLG46585 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See Figure 44 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

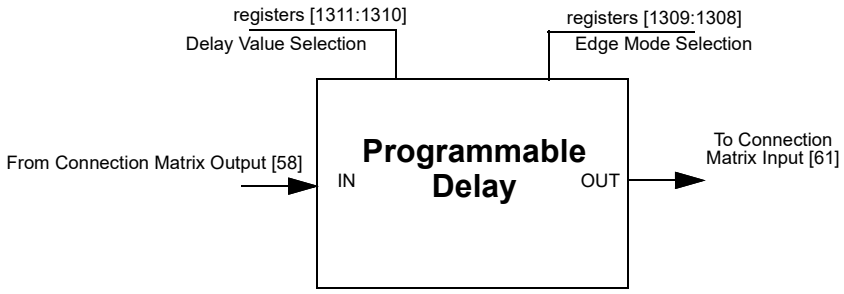


Figure 44: Programmable Delay

11.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

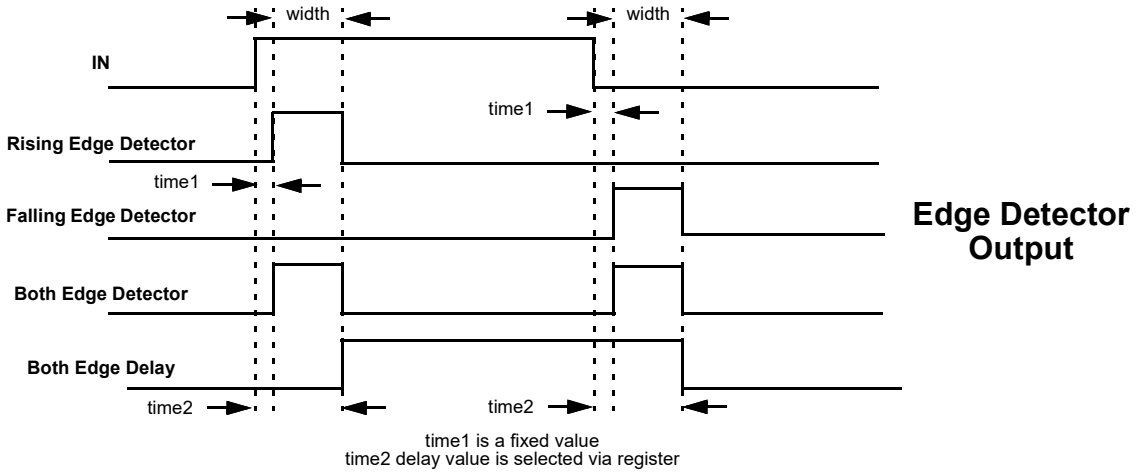


Figure 45: Edge Detector Output

Please refer to Table 12.

Table 83: Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Select the edge mode of programmable delay & edge detector	[1309:1308]	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value select for programmable delay & edge detector (V_{DD} = 3.3 V, typical condition)	[1311:1310]	00: 165 ns 01: 300 ns 10: 440 ns 11: 575 ns

12 Additional Logic Functions

The SLG46585 has two additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two deglitch filters, each with edge detector functions.

12.1 DEGLITCH FILTER/EDGE DETECTOR

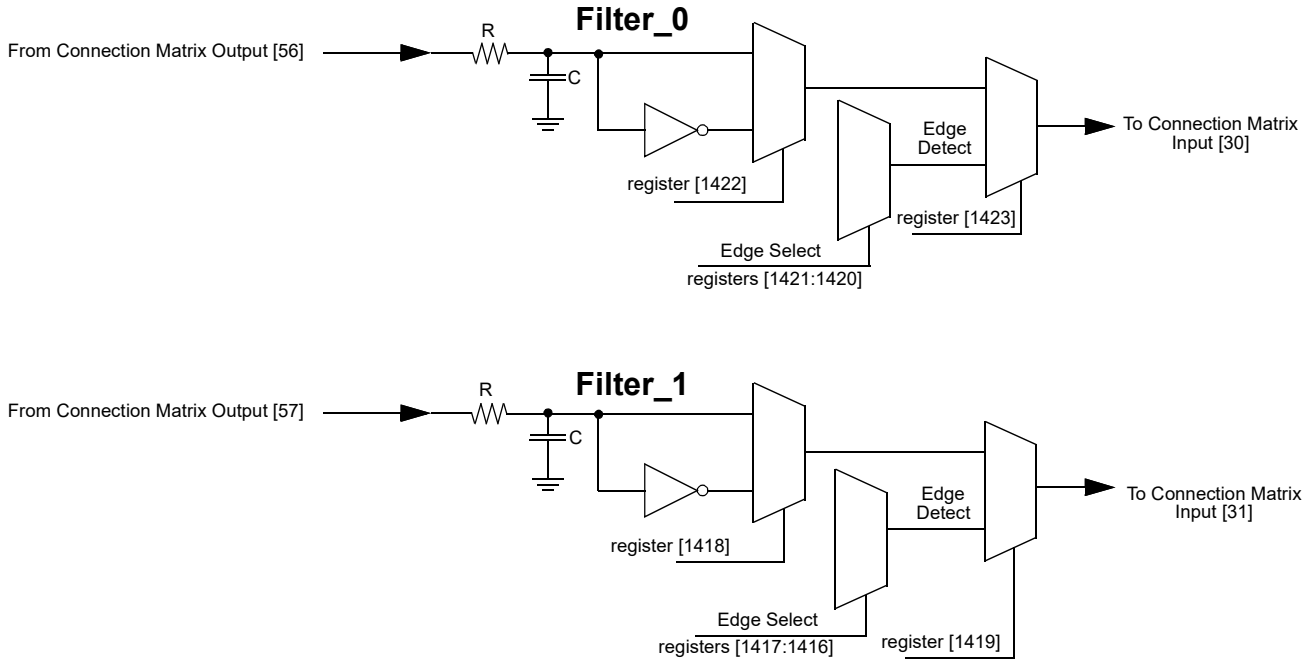


Figure 46: Deglitch Filter/Edge Detector

Table 84: Deglitch Filter Register Settings

Signal Function	Register Bit Address	Register Definition
Filter_1/Edge Detector_1 Edge Select	[1417:1416]	00: Rising Edge Detector 01: Fall Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Filter_1/Edge Detector_1 output Polarity Select	[1418]	0: Filter_1 output 1: Filter_1 output inverted
Filter_1 or Edge Detector_1 Select (Typ. 50 nS @V_{DD}=3.3 V)	[1419]	0: Filter_1 1: Edge Detector_1
Filter_0/Edge Detector_0 Edge Select	[1421:1420]	00: Rising Edge Detector 01: Fall Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Filter_0/Edge Detector_0 output Polarity Select	[1422]	0: Filter_0 output 1: Filter_0 output inverted

Table 84: Deglitch Filter Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
Filter_0 or Edge Detector_0 Select (Typ. 70 nS @V_{DD}=3.3 V)	[1423]	0: Filter_0 1: Edge Detector_0

13 RTC Binary Counter

The SLG46585 includes a 47-bit binary Real Time Counter (RTC) designed to continuously count time. This counter consists of three components and can be programmed serially through an I^2C serial interface.

The first component is a 15-bit Counter Divider used to divide the external clock, which generates a high level pulse (with width equal to the RTC clock period) to Connection Matrix Input [23] when the counter reaches the end of the count. Since the RTC counter is used for time keeping, the most common expected use case is to connect this 15-bit counter divider to a 32.768 kHz clock source, in which case the output will be a pulse at 1 second intervals, with high time of ~30.5 µs.

The second component is the 32-bit Time Counter, which takes its clock input from either the output of the 15-bit counter divider, or directly from Connection Matrix Output [101]. If the input clock comes from the 15-bit counter divider, and this counter divider is used to count time in seconds (most common use case), then the count value in this 32-bit time counter will be the number of seconds elapsed since it was loaded. The contents are read/write accessible via the address range 0x75 to 0x7A. When the counter is read, the current time is latched into a shadow buffer register, which is output on the serial data line while the counter continues to increment.

The third component is a 32-bit Alarm Digital Comparator (DCMP). This generates an alarm signal to Connection Matrix Input [24] when the time counter value matches the DCMP alarm value, which is set via I^2C serial interface. An I^2C bus Master is used to write to the 32-bit Alarm DCMP register bits in order to define the next wake up time. The 32-bit Alarm DCMP loads its initial value from registers [1023:992] at POR, and can be changed at any time by I^2C. The Alarm DCMP output is high for one clock period of the 32-bit Time Counter.

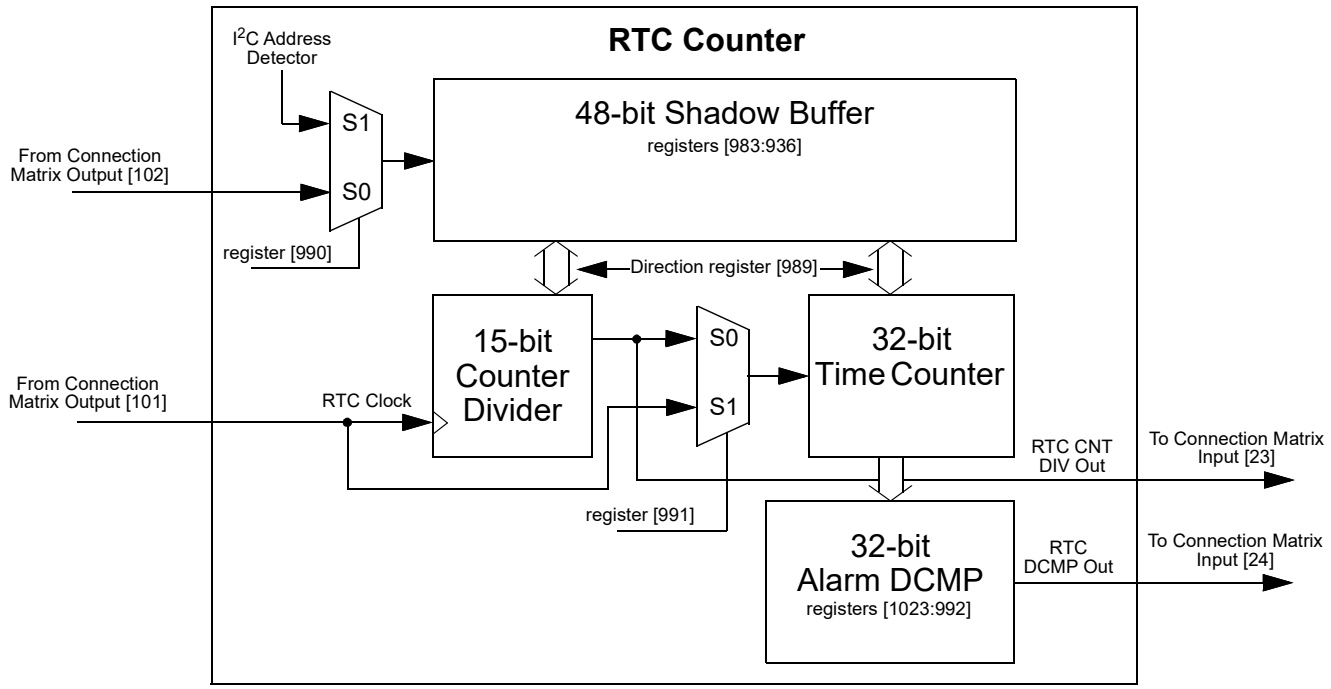


Figure 47: RTC Counter Macrocell

13.1 RTC BINARY COUNTER SHADOW BUFFER

All reading or writing of data to this macrocell goes through the 48-bit Shadow Buffer. In order to read the current RTC counter value through the I^2C, the RTC counter value must first be copied to the shadow buffer. The RTC Counter's value can be copied to the 48-bit shadow buffer by either rising edge trigger signal through the Connection Matrix Output [102] or by a trigger signal generated by reading the I^2C address at 0x75 to 0x7A. The same trigger signals are used to transfer data in the opposite direction (from the shadow buffer to RTC counter).

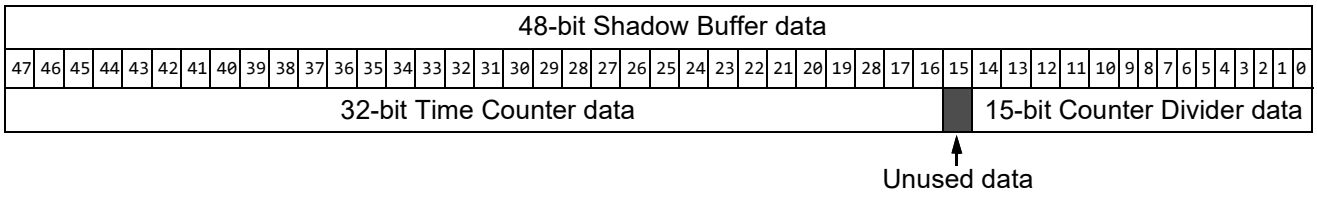


Figure 48: RTC Counter Shadow Buffer Bits

- Register [990] defines the source of the trigger signal for the copy to shadow buffer, either from the Connection Matrix or from the designated I^2C address read. The trigger source can be changed though an I^2C write command to change this bit setting.
- Register [989] defines the direction of whether RTC Counter data will be copied to 48-bit shadow buffer or the 48-bit shadow buffer data will be copied to the RTC Counter. The direction can be changed though an I^2C write command to change this bit setting.

13.1.1 RTC Binary Counter Shadow Buffer Operating Modes

The combined values in register [990] and register [989] provide four modes of operation for the shadow buffer, allowing the user to latch the shadow buffer data into the RTC counter, or to latch data the RTC counter data into the shadow buffer, and to choose the signal that will latch the data.

Table 85: Shadow Buffer Register Settings

Register [989]	Register [990]	Shadow Buffer Operating Modes
0	0	RTC data will be latched in the shadow buffer by rising edge on Connection Matrix Output [102].
0	1	RTC data will be latched in the shadow buffer by reading any I^2C address in the range 0x75 – 0x7A. The LATCH signal is activated when the I^2C address comparison circuit indicates a matching address in an incoming command. All bytes of one RTC data sample can be read using Sequential Read Command.
1	0	Shadow buffer data will be latched in the RTC by rising edge on Connection Matrix Output [102].
1	1	Shadow buffer data will be latched in the RTC at the completion of a write command to I^2C address in the range 0x75 to 0x7A. All bytes of one shadow buffer data sample can be written using Sequential Write Command.

14 Voltage Reference

14.1 VOLTAGE REFERENCE OVERVIEW

The SLG46585 has a Voltage Reference Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from IO4. See Table 86 for the available selections for each analog comparator.

14.2 VREF SELECTION TABLE

Table 86: Vref Selection Table

SEL[4:0]	ACMP0_VREF	ACMP1_VREF	ACMP2_VREF	ACMP3_VREF
11011	IO4: EXT_VREF/2	IO4: EXT_VREF/2	IO4: EXT_VREF/2	IO4: EXT_VREF/2
11010	IO4: EXT_VREF	IO4: EXT_VREF	IO4: EXT_VREF	IO4: EXT_VREF
11001	V_{DD}: ACMP0-/4	V_{DD}: ACMP1-/4	V_{DD}: ACMP2-/4	V_{DD}: ACMP3-/4
11000	V_{DD}: ACMP0-/3	V_{DD}: ACMP1-/3	V_{DD}: ACMP2-/3	V_{DD}: ACMP3-/3
10111	1.20	1.20	1.20	1.20
10110	1.15	1.15	1.15	1.15
10101	1.10	1.10	1.10	1.10
10100	1.05	1.05	1.05	1.05
10011	1.00	1.00	1.00	1.00
10010	0.95	0.95	0.95	0.95
10001	0.90	0.90	0.90	0.90
10000	0.85	0.85	0.85	0.85
01111	0.80	0.80	0.80	0.80
01110	0.75	0.75	0.75	0.75
01101	0.70	0.70	0.70	0.70
01100	0.65	0.65	0.65	0.65
01011	0.60	0.60	0.60	0.60
01010	0.55	0.55	0.55	0.55
01001	0.50	0.50	0.50	0.50
01000	0.45	0.45	0.45	0.45
00111	0.40	0.40	0.40	0.40
00110	0.35	0.35	0.35	0.35
00101	0.30	0.30	0.30	0.30
00100	0.25	0.25	0.25	0.25
00011	0.20	0.20	0.20	0.20
00010	0.15	0.15	0.15	0.15
00001	0.10	0.10	0.10	0.10
00000	0.05	0.05	0.05	0.05

Note: the ACMP external reference voltage (IN-) is limited by 1.2 V for full power supply range.

15 Analog Temperature Sensor

The SLG46585 has an analog temperature sensor (TS) with an output voltage linearly-proportional to Centigrade temperature. This feature was designed with a range from 50 °C to 150 °C as a tool to protect the chip from overheating. The TS's operates based on the temperature coefficient of a Silicon diode (~-2.1 mV/°C). As the chip temperature increases, the TS's analog output voltage decreases.

If the junction temperature exceeds the thresholds of ACMP2 or ACMP3, the ACMP outputs toggle and can shut down both internal and external circuitry. Since most of the GreenPAK's self-heating originates within the LDO regulation circuitry, ACMP2's output can lower the chip's junction temperature by disabling the LDOs.

The equation below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input. It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_{TS} = -4.935 \times T + 1467.03$$

where:

V_{TS} (mV) - TS Output Voltage

T (°C) - Temperature

Temperature hysteresis can be setup by enabling the GreenPAK's internal ACMP hysteresis. Many of the applicable ACMP reference voltages are listed in Table 87, but for those that are not, use the previous equation to approximate the temperature level.

Table 87: Temperature Sensor Voltage for V_{DD} = 2.5 V to 5.5 V

Vref, mV	T_{IL} - Typ, °C	T_{IH} - Typ, °C
700	154.84	155.06
750	144.82	145.47
800	134.87	135.61
850	124.87	125.65
900	114.89	115.63
950	104.85	105.56
1000	94.75	95.42
1050	84.64	85.22
1100	74.45	74.98
1150	64.26	64.73
1200	54.01	54.22

To enable the TS, set the TS enable register high in the "Temp Sensor" macrocell or the "ACMP2" macrocell's IN+ source settings. In addition, the PWR UP matrix connection of ACMP2 or ACMP3 must be set high. See Figure 49 for the TS block diagram when used with ACMP2 and ACMP3.

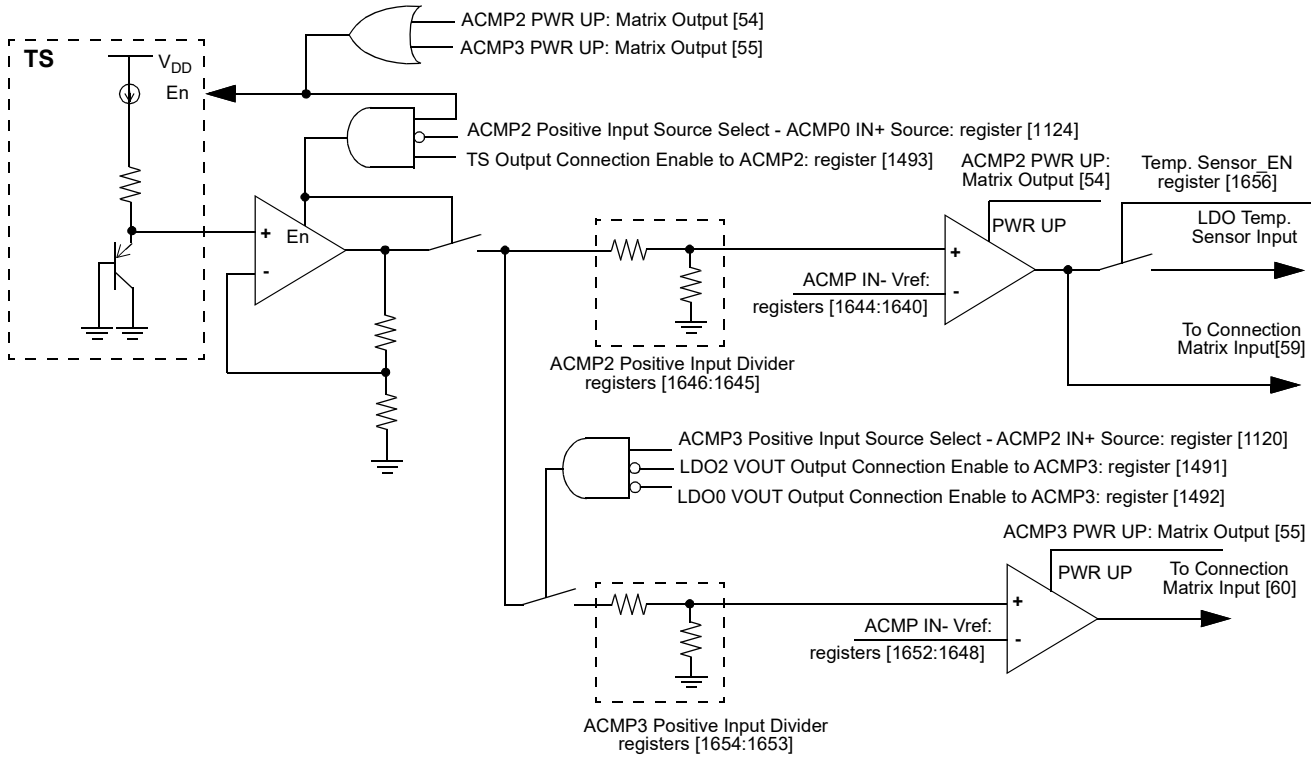


Figure 49: Analog Temperature Sensor Structure Diagram

Note: If ACMP2 or/and ACMP3 is/are used for TS function, IO5 or/and IO6 should not be used as “Analog IO”.

16 Clocking

16.1 OSC GENERAL DESCRIPTION

The SLG46585 has two internal oscillators to support a variety of applications:

- Low Power Oscillator (1.73 kHz)
- Configurable Oscillator (25 kHz or 2 MHz)

There are two divider stages that give the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The pre-divider (first stage) for Configurable Oscillator allows the selection of /1, /2, /4 or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines [27] and [28]. The second stage divider is available to the configurable OSC (25 kHz or 2 MHz) only while the Low Power OSC is connected to Connection Matrix Input [29] directly after the pre-divider /1, /2, /4 or /16 for LP OSC.

The Matrix Power-Down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power-Down/Force On (Connection Matrix Output [59] and [60) signal has the highest priority.The OSC operates according to the Table 88.

Table 88: Oscillator Operation Mode Configuration Settings

Power-Down/Force ON matrix control selection registers [1658], [1657]	From Connection Matrix Output [59], [60]	OSC POWER MODE selection registers [1295], [1290]	OSC operation mode
0	0	0	Auto Power-On **(Note 1)**
0	0	1	ON
0	1	0	OFF
0	1	1	OFF
1	0	0	Auto Power-On **(Note 1)**
1	0	1	ON
1	1	0	ON
1	1	1	ON
Note 1 The OSC will run only when any macrocell that uses OSC is powered on.			

The SLG46585 has a 25 kHz/2 MHz OSC Fast Start-up option up function controlled by register [1293] (1: Enabled; 0: Disabled). It allows the OSC to have faster start up time, less than one OSC cycle when this option is enabled).

Note: The quiescent current consumption will increase when the OSC Fast Start-up option is enabled.

16.2 LOW POWER OSC (1.73 kHz)

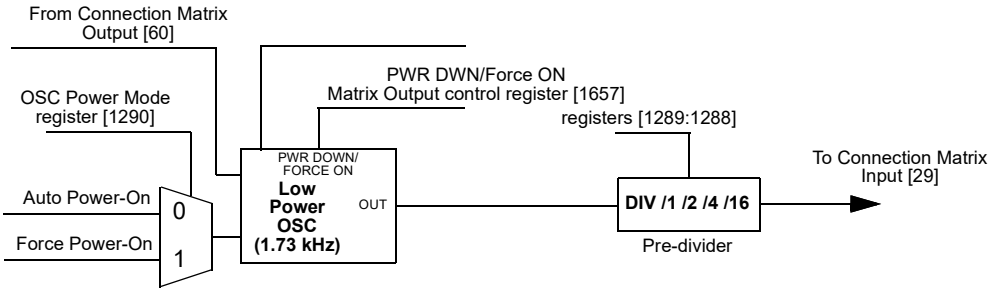


Figure 50: Low Power Oscillator Block Diagram

16.3 CONFIGURABLE OSC(25 KHZ/2MHZ)

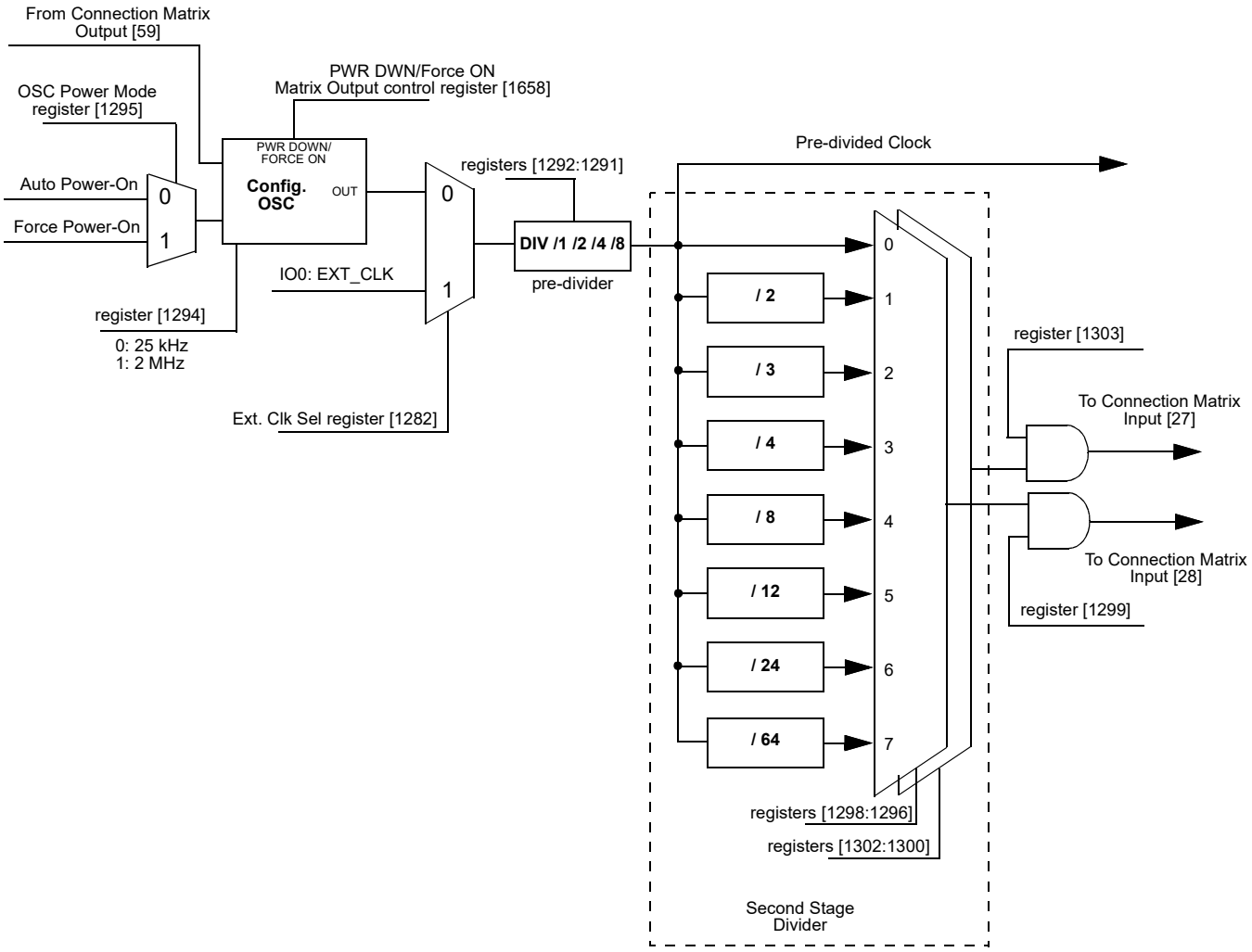


Figure 51: Configurable OSC Block Diagram

16.4 OSCILLATOR POWER-ON DELAY

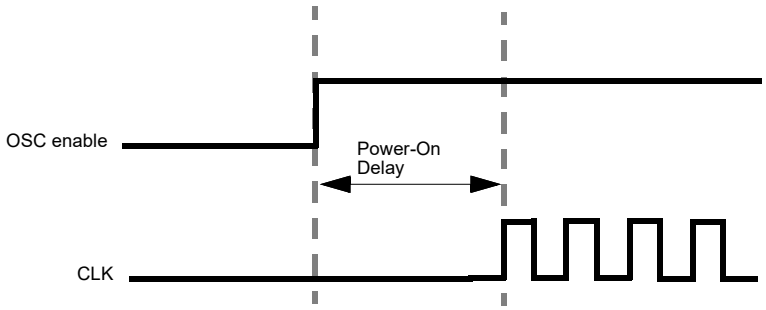


Figure 52: Oscillator Startup Diagram

Note 1 OSC power mode: "Auto Power-On".

Note 2 'OSC enable' signal appears when any macrocell that uses OSC is powered on.

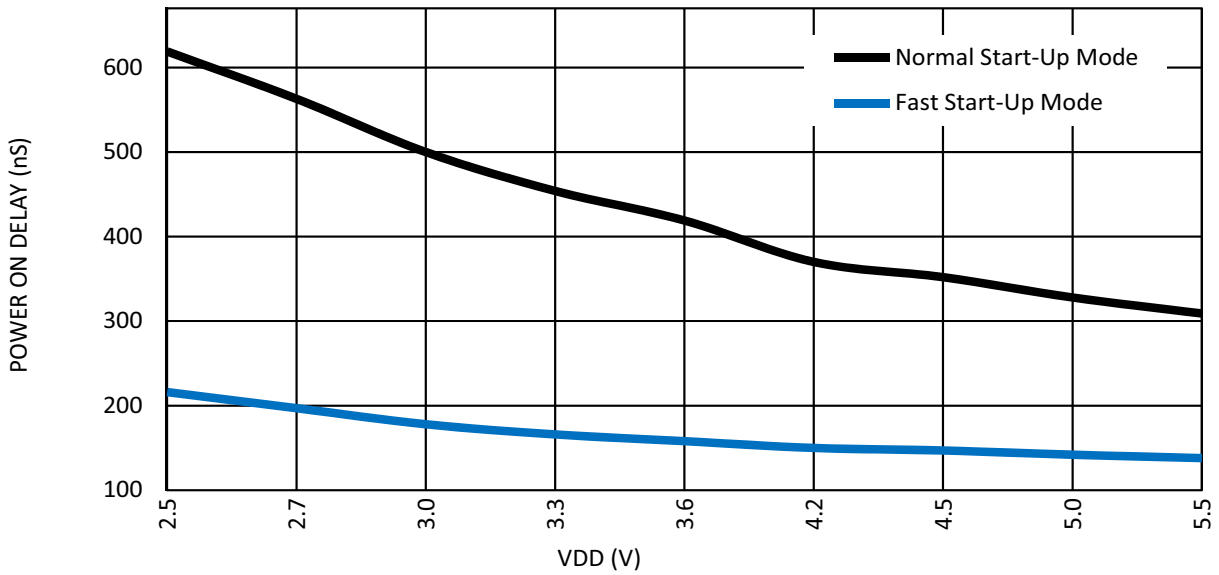


Figure 53: Oscillator Maximum Power-On Delay vs. V_{DD}, T = +25 °C, OSC0 = 2 MHz

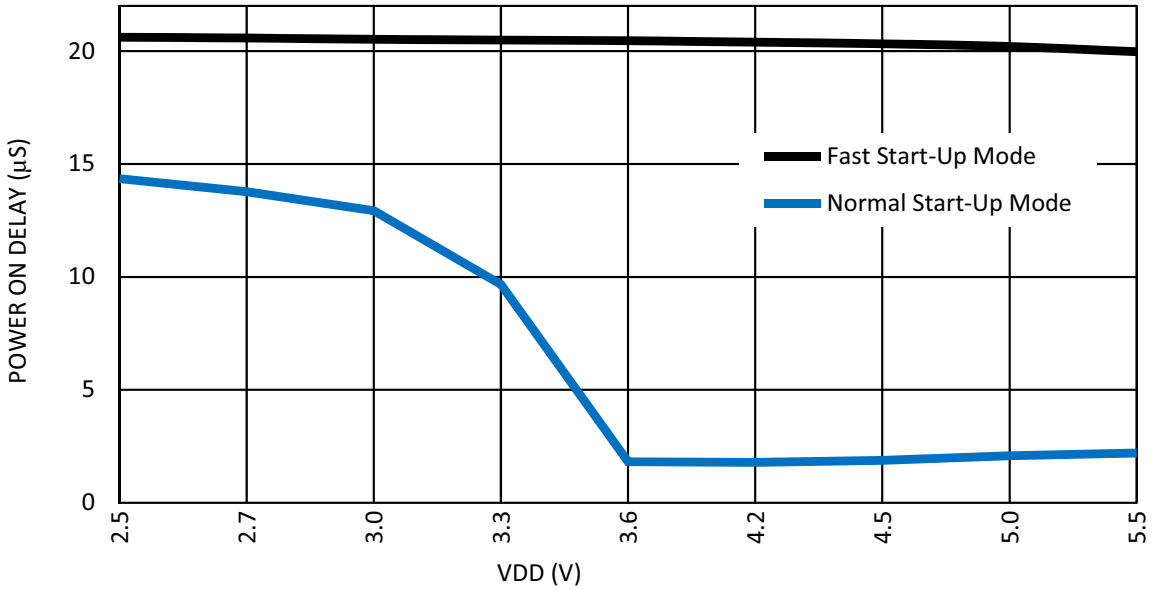


Figure 54: Oscillator Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC0 = 25 kHz

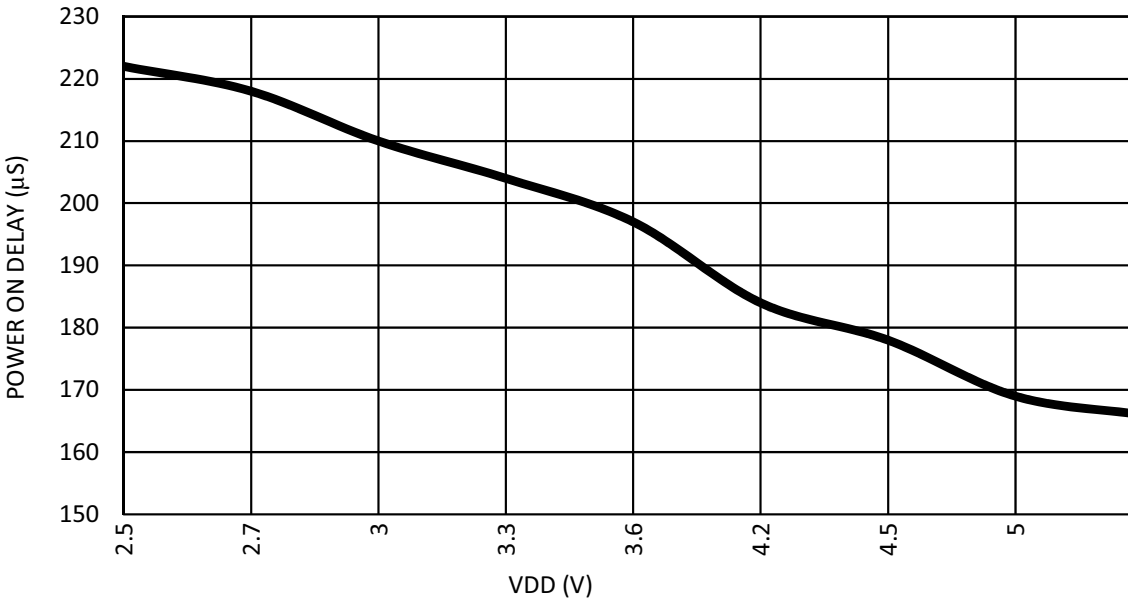


Figure 55: Oscillator Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC1 = 1.73 kHz

16.5 OSCILLATOR ACCURACY

Note 1 OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

Note 2 For more information see Section 3.6.

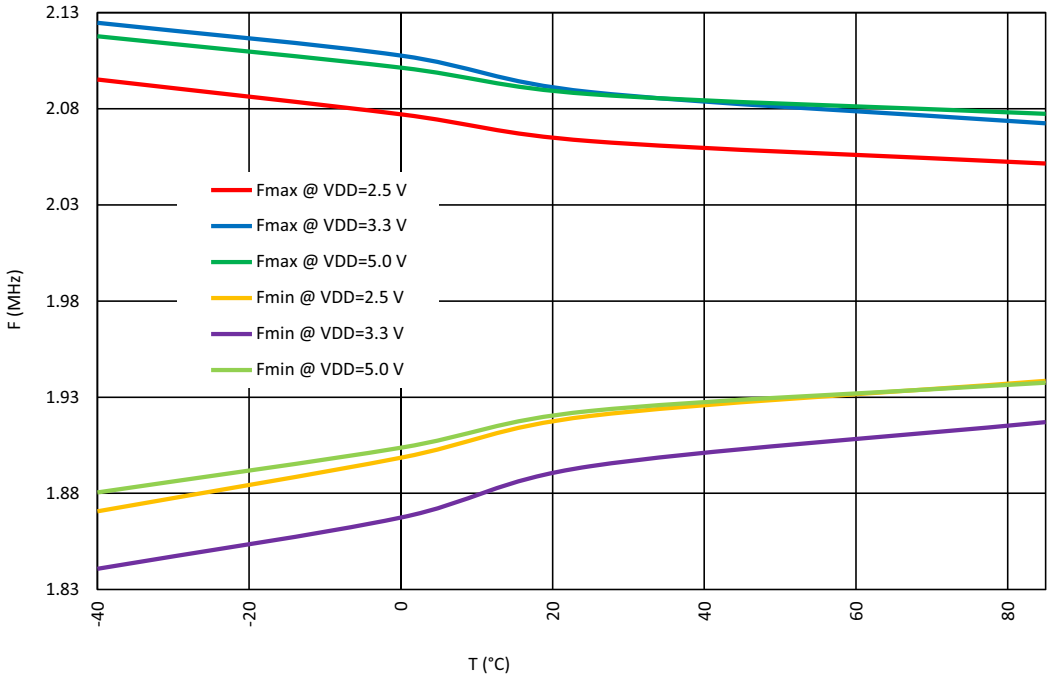


Figure 56: Oscillator Frequency vs. Temperature, OSC0 = 2 MHz

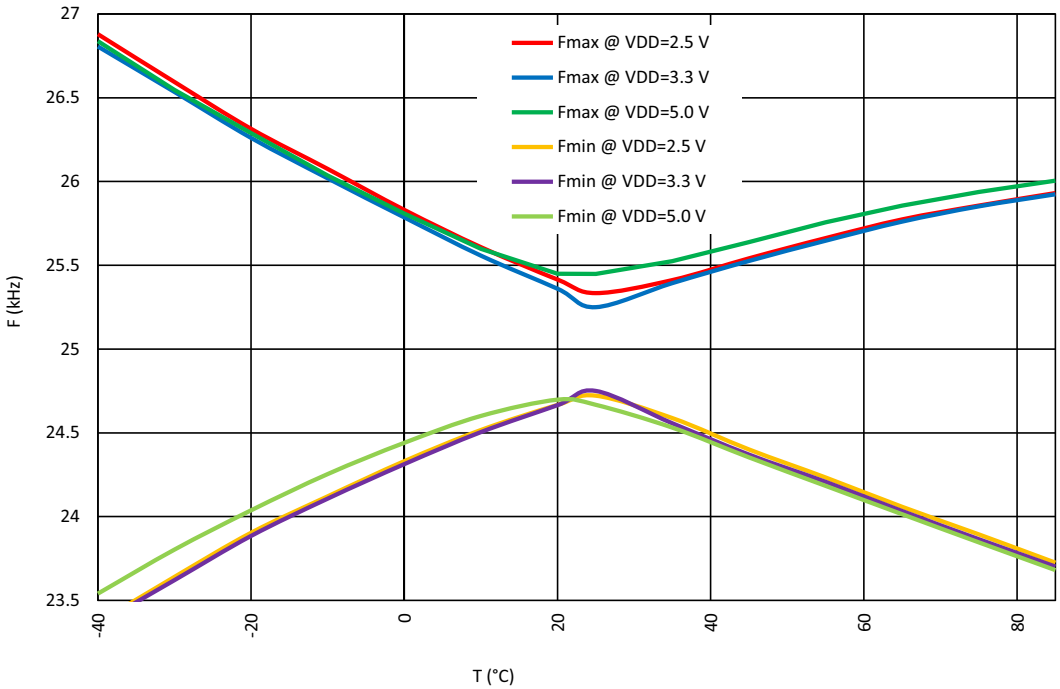


Figure 57: Oscillator Frequency vs. Temperature, OSC0 = 25 kHz

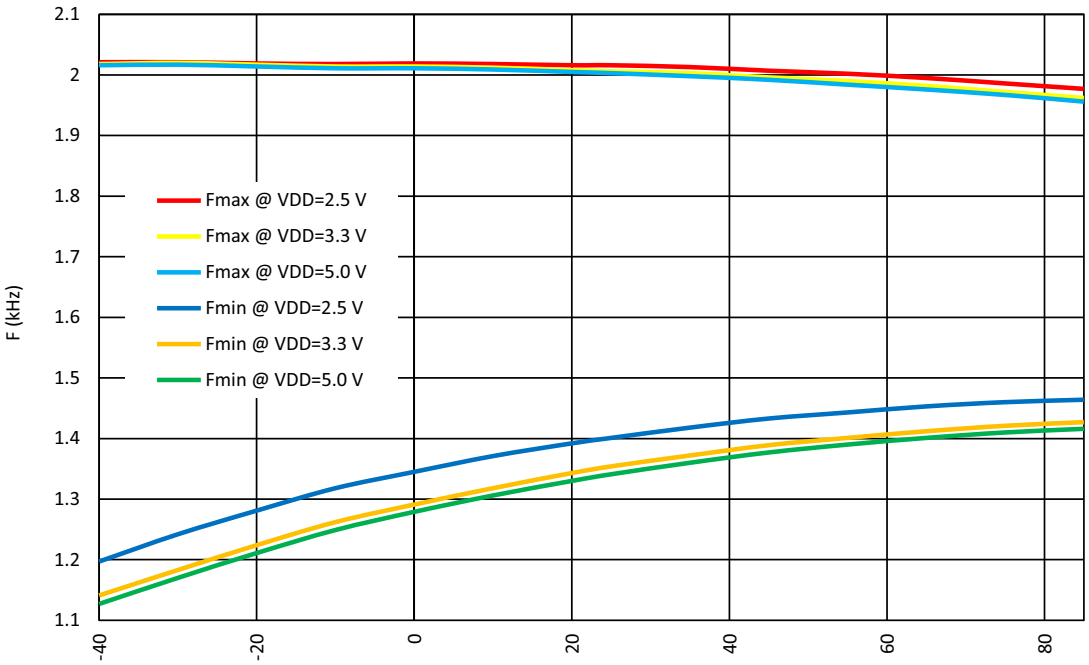


Figure 58: Oscillator Frequency vs. Temperature, OSC1 = 1.73 kHz

17 Power-On Reset

The SLG46585 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during Power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

17.1 GENERAL OPERATION

The SLG46585 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on V_{DD} pin) is less than Power-Off Threshold (see Section 3.4), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (see Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46585, the voltage applied on the V_{DD} should be higher than the Power-On threshold (Note). The full operational V_{DD} range for the SLG46585 is 2.5 V – 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence has started, the SLG46585 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note: The Power_ON threshold is defined in Table 6.

Note: LDOs begin to operate when $V_{DD} \geq 2.5$ V.

To power-down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down, it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before, the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

17.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 59.

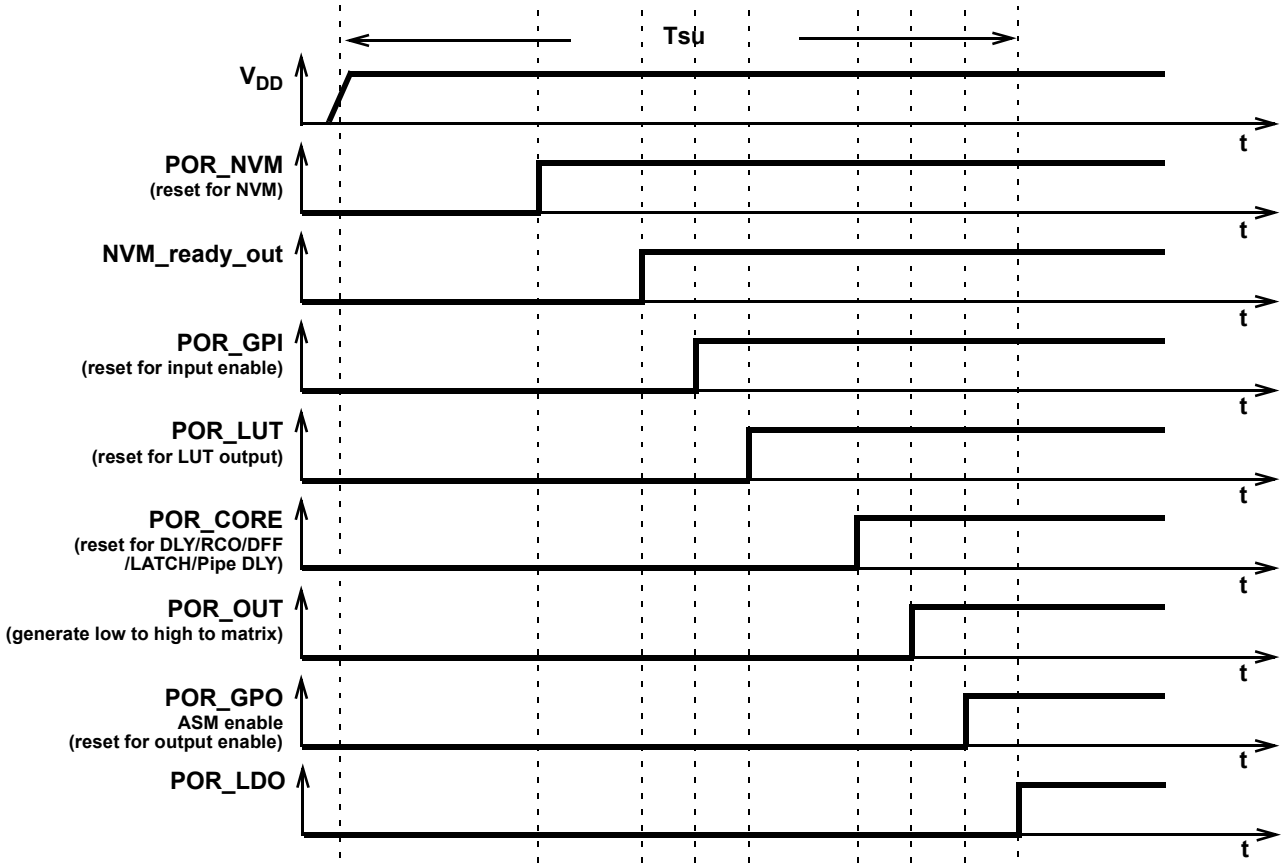


Figure 59: POR Sequence

As can be seen from Figure 59 after the V_{DD} has started ramping up and crossed the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to a CMOS LATCH that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, RC OSC, DFFs, Latches, and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH (POR_OUT in Figure 59). The last portion of the device to be initialized is the output pins, which transition from high impedance to active at this point. LDOs begin to operate in 500 μs after PINs become active.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

17.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46585 operation during powering and POR sequence, review the overview of macrocell output states during the POR sequence (Figure 60 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

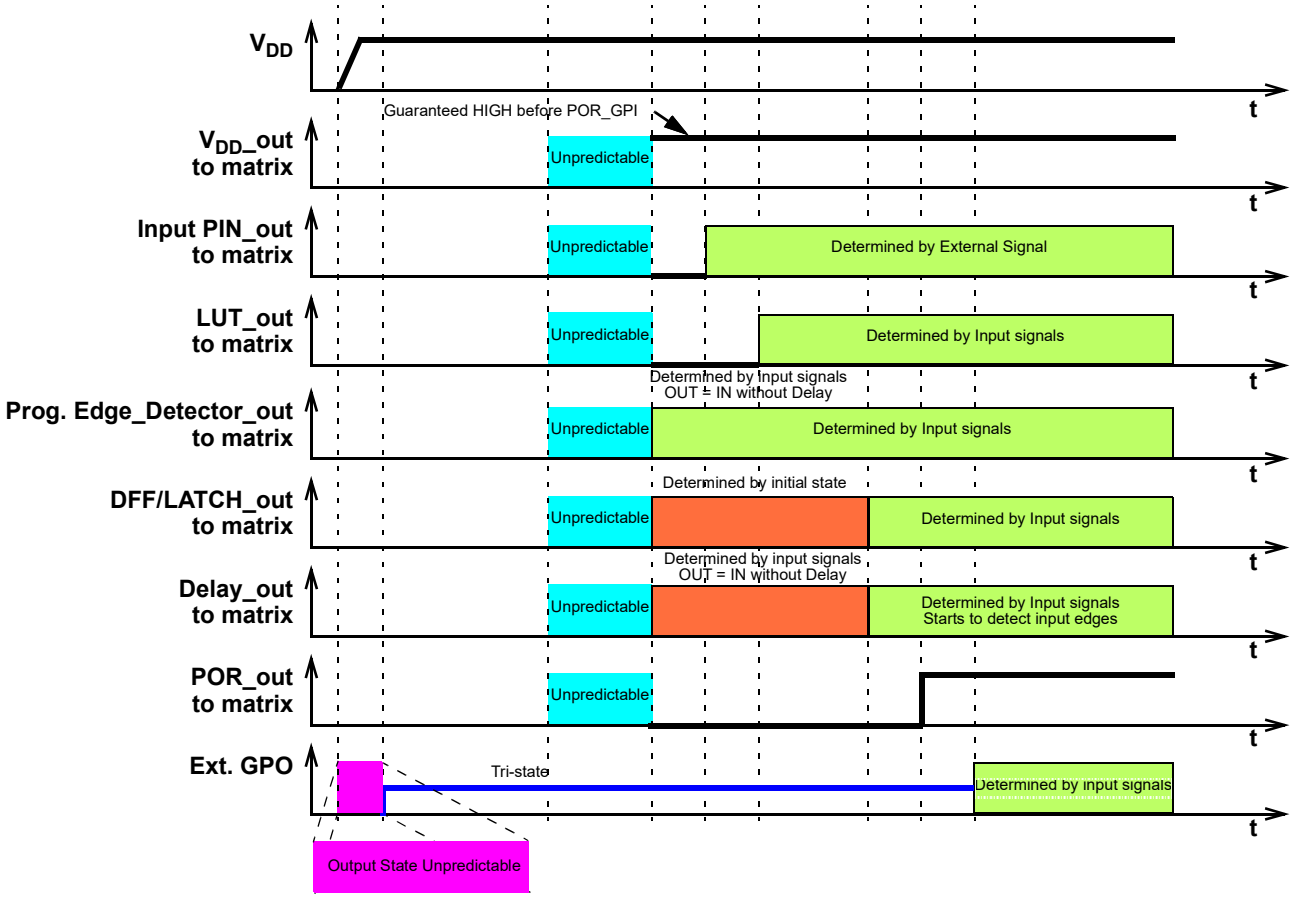


Figure 60: Internal Macrocell States during POR Sequence

17.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.15 V - 1.6 V, macrocells are powered on while forced to the reset state, All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input PINs, ACMP, Pull-up/down.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay.
4. POR output to matrix.
5. Output PIN corresponds to the internal logic.
6. LDOs.

Note: LDOs begin to operate above 2.5 V.

Note: The maximum voltage applied to any PIN should not be higher than the V_{DD} level. There are ESD Diodes between PIN → V_{DD} and PIN → GND on each PIN. So, if the input signal applied to PIN is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input PIN, and V_{DD} will be pulled up, following the voltage on the input PIN.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

17.3.2 Power-Down

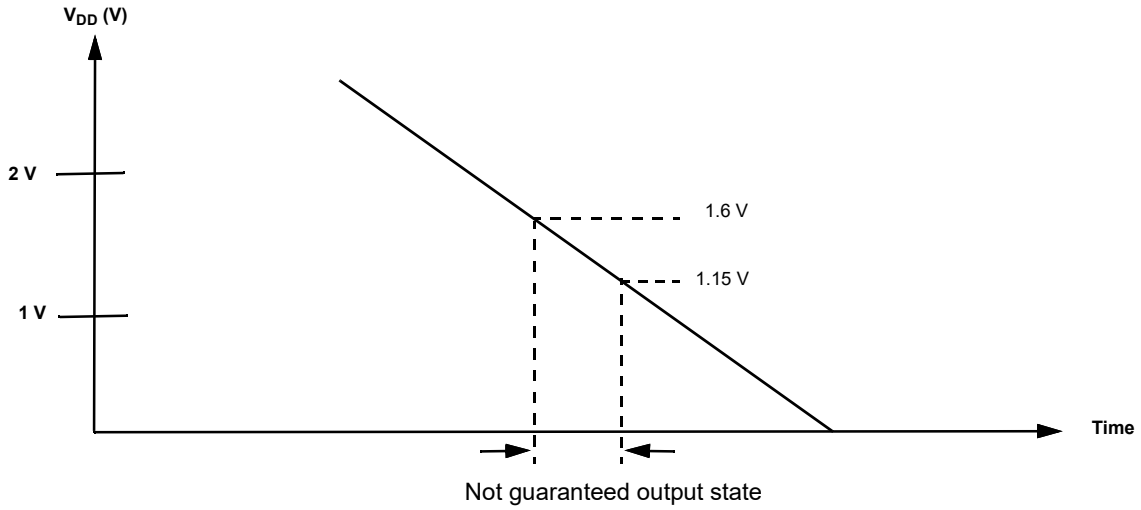


Figure 61: Power-Down

During power down, macrocells in SLG46585 are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state.

17.4 EXTERNAL RESET

The SLG46585 has an optional External Reset function on IO3. It allows to reset the chip while powered on.
IO3 must be configured as Digital Input registers [1071:1070] and function Reset must be enabled also, register [1307]: 0 - disabled, 1 - enabled. Unlike POR, External Reset affects only GPI, LUTs, DLY, RC OSC, DFFs, Latches, Pipe Delay, Matrix, and GPO. While NVM remains its previous state, see Figure 62 to Figure 64.

Note that during External Reset the output pin's status will depend on the OE control circuits and current consumption is determined by the design.

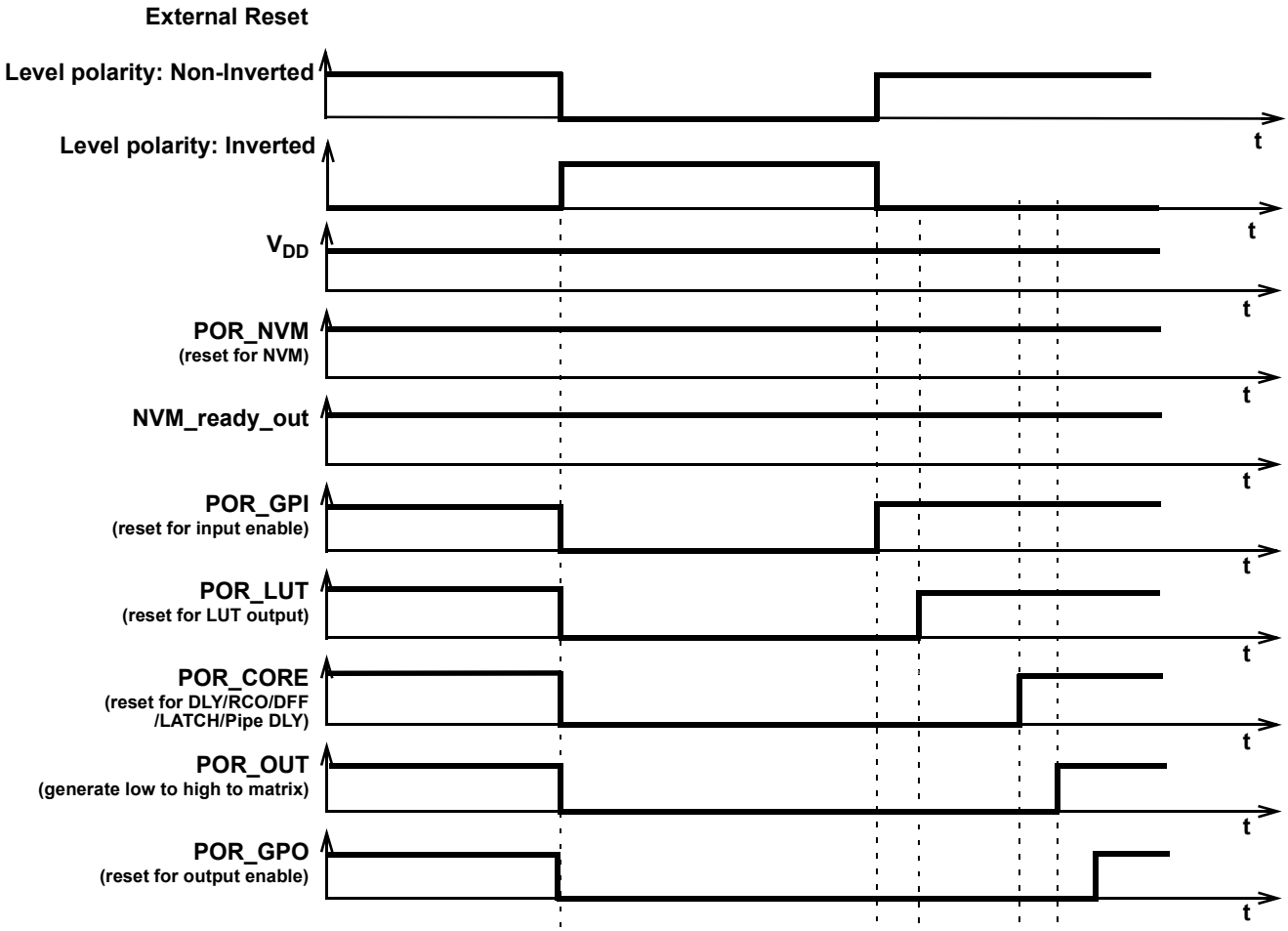


Figure 62: External Reset Sequence (Level Sensitive)

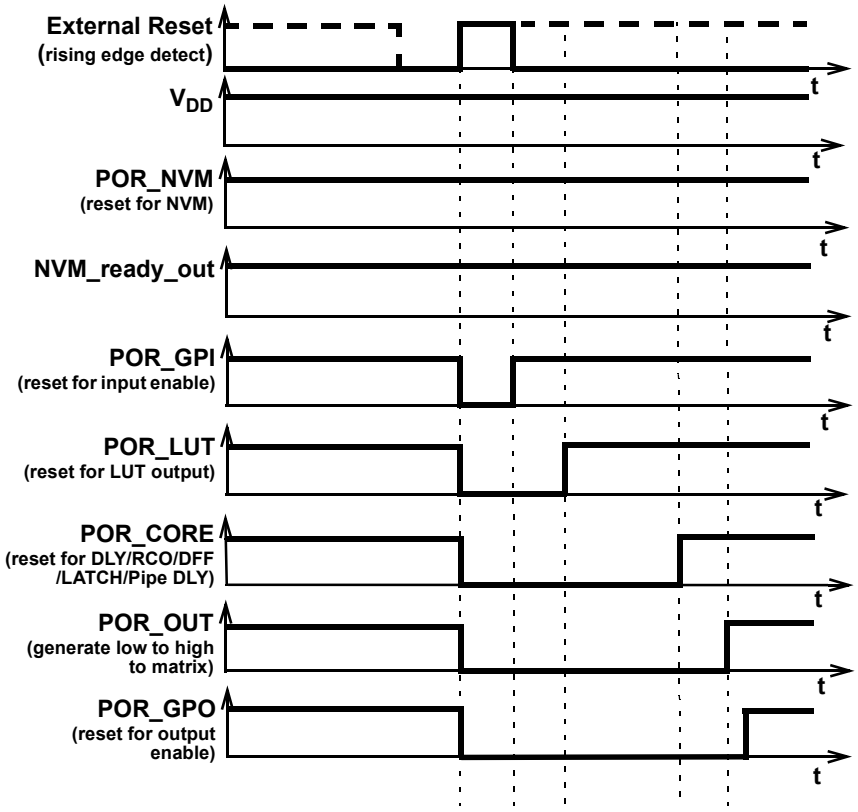


Figure 63: External Reset Sequence (Rising Edge Detect)

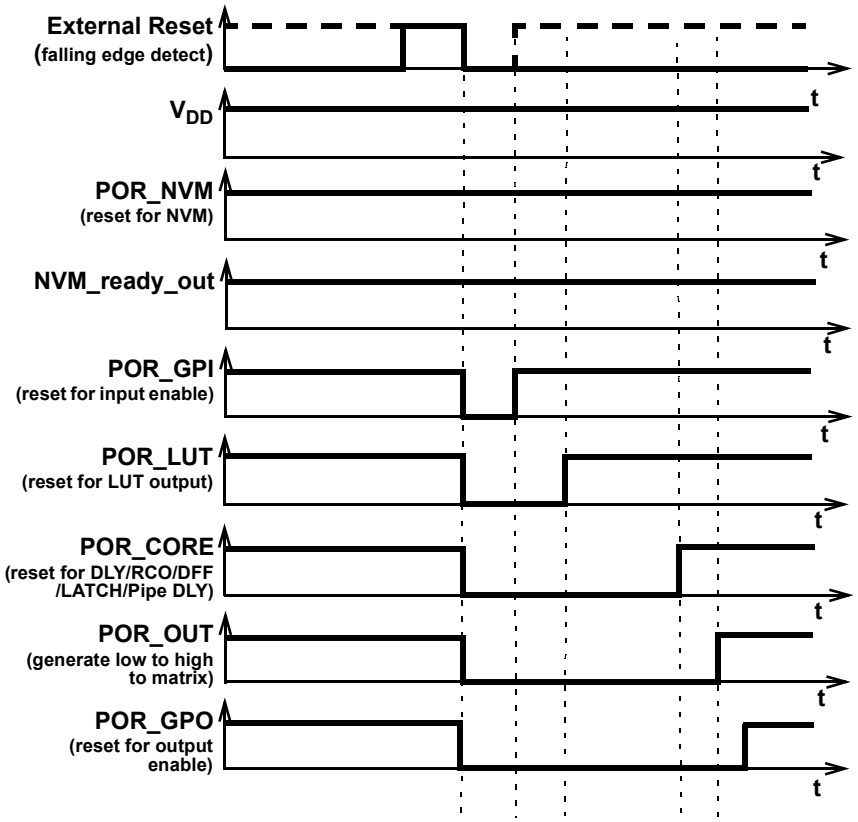


Figure 64: External Reset Sequence (Falling Edge Detect)

Table 89: External Reset Register Settings

Signal Function	Register Bit Address	Register Definition
IO3 Reset level polarity selection	[1304]	0: Non-inverted 1: Inverted
IO3 edge reset enable	[1305]	0: Edge reset enable (controlled by register [1306]) 1: High level reset
IO3 rising/falling edge reset	[1306]	0: Rising 1: Falling
IO3 reset function	[1307]	0: Disable 1: Enable

18 Asynchronous State Machine Macrocell

18.1 ASM MACROCELL OVERVIEW

The Asynchronous State Machine (ASM) macrocell is designed to allow the user to create state machines with between 2 to 8 states. The user has flexibility to define the available states, the available state transitions, and the input signals (a, b, c …) that will cause transitions from one state to another state, as shown in Figure 65.

This macrocell has a total of 25 inputs, as shown in Figure 66, which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial/Reset state. Each of the 24 inputs is level sensitive and active high, meaning that a high level input will drive the user selected transition from one state to another. Additionally, 8 out of the 24 inputs (one per state) has an option to select whether the input is rising edge sensitive, meaning that a rising level input signal will drive the user selected transition from one state to another. The fact that there are 24 inputs puts the upper bound of 24 possible state transitions total in the user defined state machine design. There is a nReset input which will drive an immediate state transition to the user-defined Initial/Reset state when active, shown in red, in Figure 65.

There are a total of 8 outputs, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states. This information is held in the Connection Matrix Output RAM.

In using this macrocell, the user must take into consideration the critical timing required on all input and output signals. The timing waveforms and timing specifications for this macrocell are all measured relative to the input signals (which come into the macrocell on the Connection Matrix outputs) and on the outputs from the macrocell (which are direct connections to Connection Matrix inputs). The user must consider any delays from other logic and internal chip connections, including IO delays, to ensure that signals are properly processed, and state transitions are deterministic.

The GPAK Designer development tools support user designs for the ASM macrocell at both the physical level and logic level. Figure 65 is a representation of the user design at the logical level, and Figure 66 shows the physical resources inside the macrocell. To best utilize this macrocell, the user must develop a logical representation of their desired state machine, as well as a physical mapping of the input and outputs required for the desired functionality.

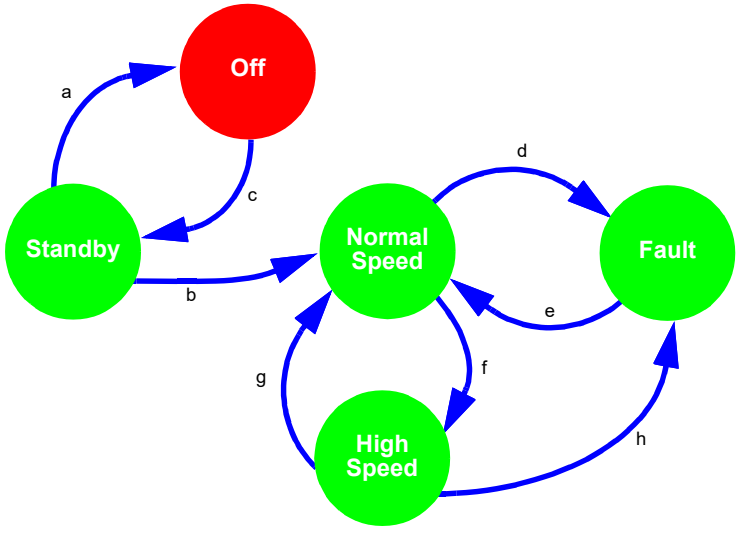


Figure 65: Asynchronous State Machine State Transitions

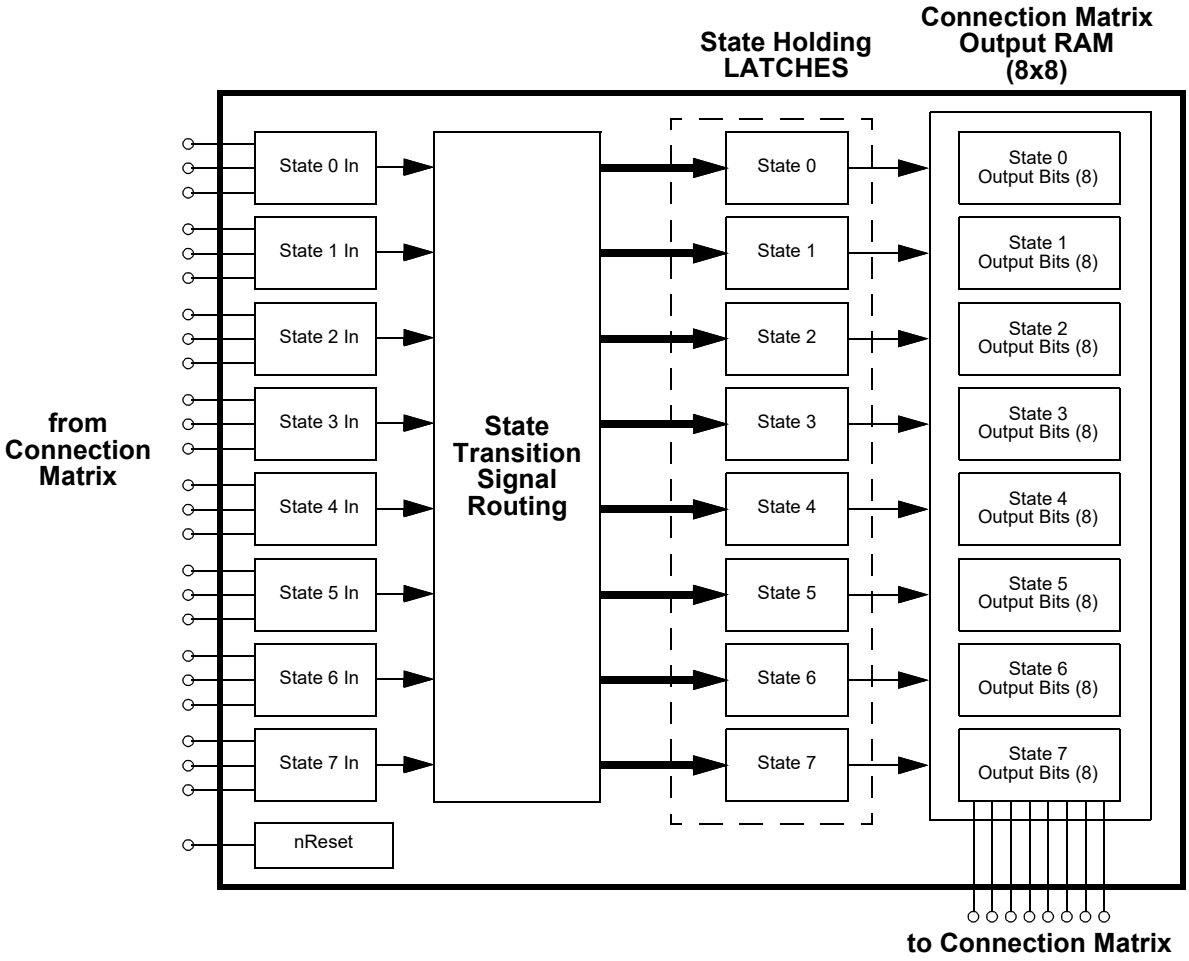


Figure 66: Asynchronous State Machine

18.2 ASM INPUTS

The ASM macrocell has a total of 25 inputs which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial/Reset state.

There are a total of 24 inputs to the ASM macrocell for general state transitions, highlighted in red in Figure 67. Each of these inputs is level sensitive, and active high. A high level input will trigger a state transition. Additionally, 8 out of the 24 inputs (one per state) has an option to select whether the input is rising edge sensitive, meaning that a rising level input signal will drive the user selected transition from one state to another, shown in Figure 68.

These inputs are grouped so that each set of 3 inputs can drive a state transition **going into** a particular state. As an example, there are three inputs that can drive a state transition to State 1. This sets an upper bound on the number of transitions that the user can select going into a particular state to be 3, shown in Figure 69.

There is no limitation on the number of transitions that can be supported coming out of a particular state, the user can select to have transitions going from a state to all other states, shown in Figure 70.

The ASM macrocell also has a nReset input highlighted in blue in Figure 67. This input is level sensitive and active low. An active signal on this input will drive an immediate state transition to the user-defined Initial/Reset state. The user can choose which state within the ASM Editor inside GPAK Designer is the initial state.

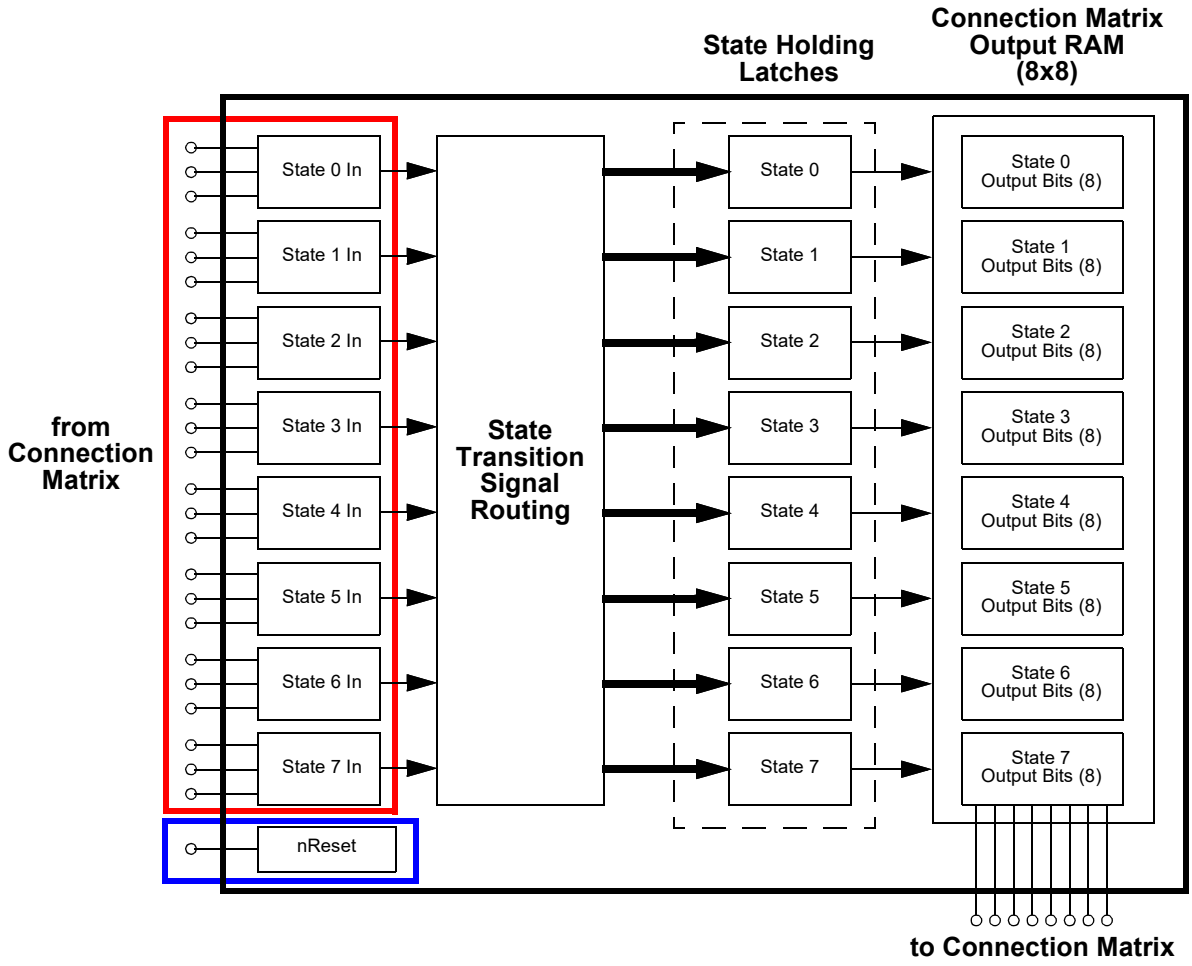


Figure 67: Asynchronous State Machine Inputs

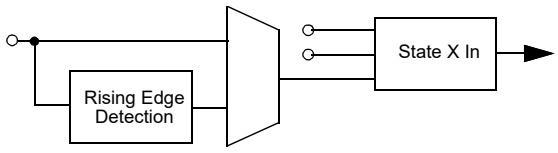


Figure 68: Rising Edge State Transition Selection (for Each State X)

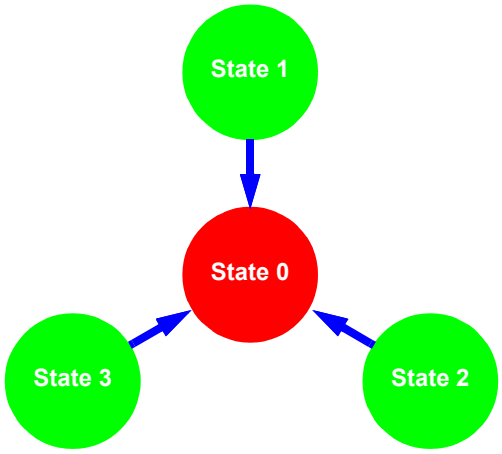


Figure 69: Maximum 3 State Transitions into Given State

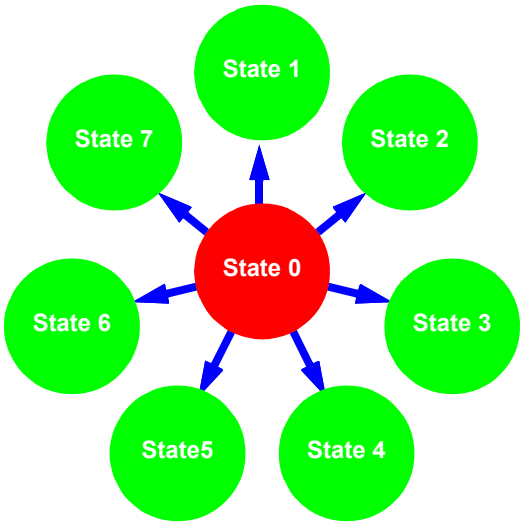


Figure 70: Maximum 7 State Transitions out of a Given State

18.3 ASM OUTPUTS

There are a total of 8 outputs from the ASM macrocell, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states, this information is held in the Connection Matrix Output RAM, shown in Figure 71. The Connection Matrix Output RAM has a total of 64 bits, arranged as 8 bits per state. The values loaded in each of the 8 bits define the signal level on each of the 8 ASM macrocell outputs.

The ASM Editor inside the GPAK Designer software allows the user to make their selections for the value of each bit in the Connection Matrix Output RAM, which selects the level of the macrocell outputs based on the current state of the ASM macrocell, as shown in Figure 66.

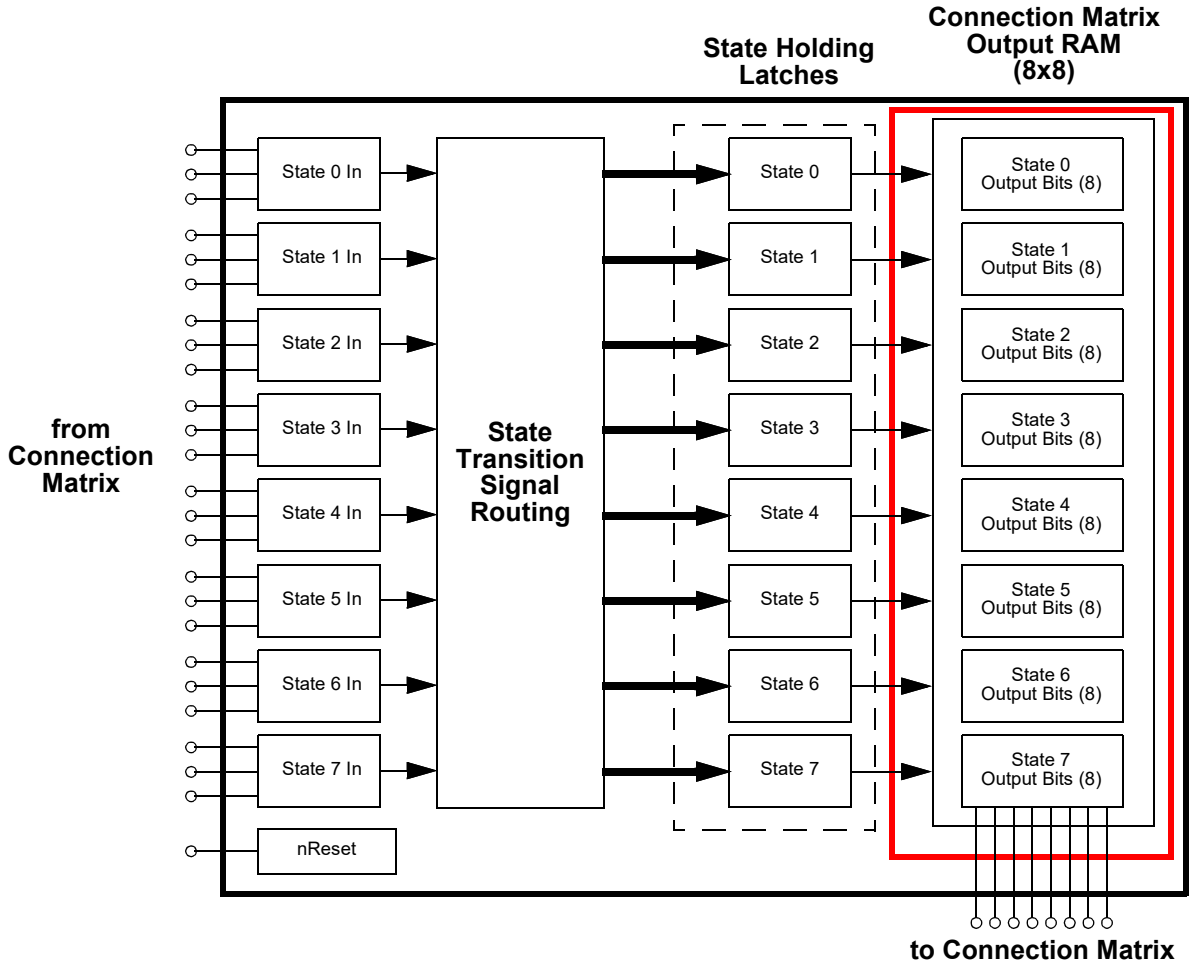


Figure 71: Connection Matrix Output RAM

Table 90: ASM Editor - Connection Matrix Output RAM

RAM								
State name	**Connection Matrix Output RAM**							
	OUT7	**OUT6**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**
State 0	0	0	0	0	0	0	0	1
State 1	0	0	0	0	0	0	1	0
State 2	0	0	0	0	0	1	0	0
State 3	0	0	0	0	1	0	0	0
State 4	0	0	0	1	0	0	0	0
State 5	0	0	1	0	0	0	0	0
State 6	0	1	0	0	0	0	0	0
State 7	1	0	0	0	0	0	0	0

18.4 BASIC ASM TIMING

The basic state transition timing from input on Matrix Connection output to output on Matrix Connection input is shown in Figure 72 and Figure 73. The time from a valid input signal to the time that there is a valid change of state and valid signals being available on the state outputs is State Machine Output Delay Time ($T_{st\_out\_delay}$). The minimum and maximum values of $T_{st\_out\_delay}$ define the differential timing between the shortest state transition (input on matrix output and output on matrix input) and the longest state transition (input on matrix output and output on matrix input).

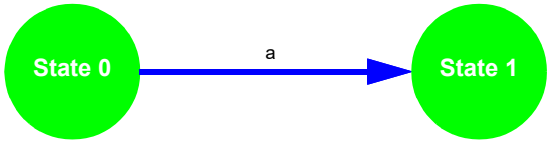


Figure 72: State Transition

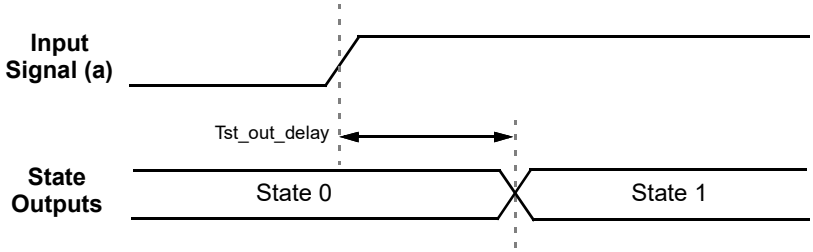


Figure 73: State Transition Timing

18.5 ASYNCHRONOUS STATE MACHINES VS. SYNCHRONOUS STATE MACHINES

It is important to note that this macrocell is designed for asynchronous operation, which means the following:

1. No clock source is needed, it reacts only to input signals.
2. The input signals do not have to be synchronized to each other, the macrocell will react to the earliest valid signal for state transition.
3. This macrocell does not have traditional set-up and hold time specifications which are related to incoming clock, as this macrocell has no clock source.
4. The macrocell only consumes power while in state transition.

18.6 ASM POWER CONSIDERATION

A benefit of the asynchronous nature of this macrocell is that it will consume power only during state transitions. Shown in Figure 72 and Figure 74, the current consumption of the macrocell will be a fraction of a µA between state transitions, and will rise only during state transitions. See Section 3.4 to find average current during state transitions.

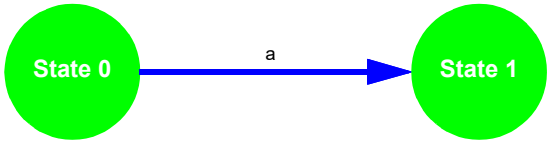


Figure 74: State Transition

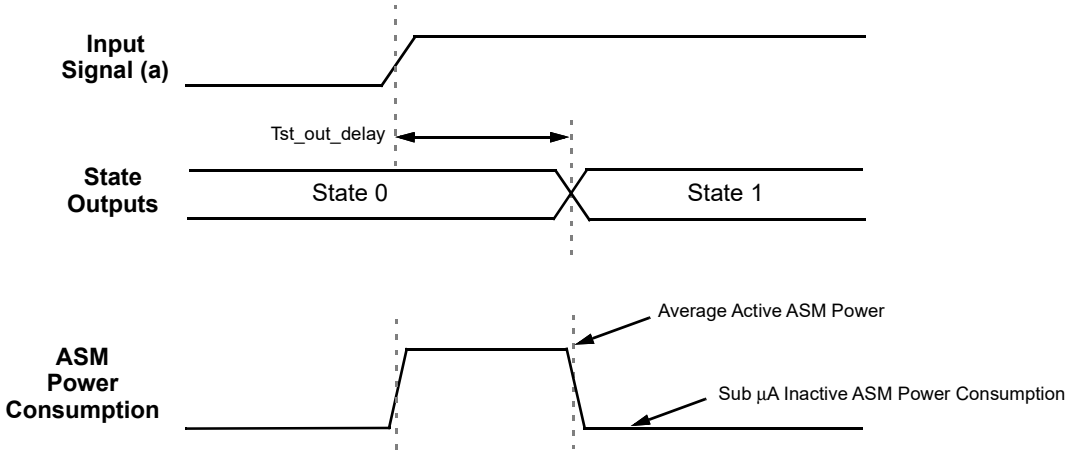


Figure 75: State Transition Timing and Power Consumption

18.7 ASM LOGICAL VS. PHYSICAL DESIGN

A successful design with the ASM macrocell must include both the logic level design as well as the physical level design. The GPAK Designer development software support user designs for the ASM macrocell at both the logic level and physical level. The logic level design of the user defined state machine takes place inside the ASM Editor. In the ASM Editor, the user can select and name states, define and name allowed state transitions, define the Initial/Reset state, and define the output values for the 8 outputs in the Output RAM Matrix. The physical level design takes place in the general GPAK Designer window, and here the user makes connections for the sources for ASM input signals, as well as making connections for destinations for ASM output signals.

18.8 ASM SPECIAL CASE TIMING CONSIDERATIONS

18.8.1 State Transition Pulse Input Timing

All inputs to the ASM macrocell are level sensitive. If the input to the state machine macrocell for a state transition is a pulse, there is a minimum pulse width on the input to the state machine macrocell (as measured at the matrix input to the macrocell) which is guaranteed to result in a state transition shown in Figure 76 and Figure 77. This pulse width is defined by the State Machine Input Pulse Acceptance Time (T_{st_pulse}). If a pulse width that is shorter than T_{st_pulse} is input to the state machine macrocell, it is indeterminate whether the state transition will happen or not. If a pulse that is rejected (invalid due to the pulse width being narrower than the guaranteed minimum of T_{st_pulse}), this will not stop a valid pulse on another state transition input that does meet minimum pulse width.

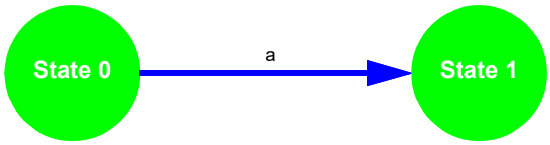


Figure 76: State Transition

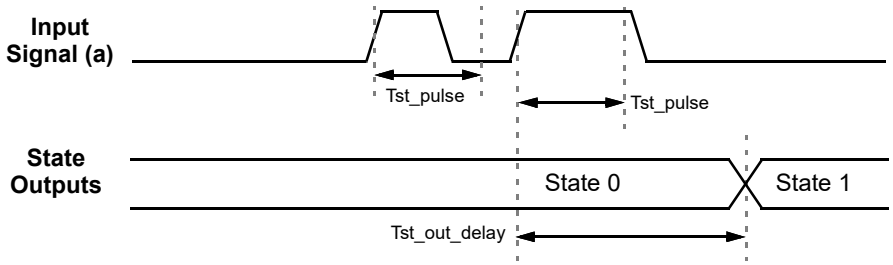


Figure 77: State Transition Pulse Input Timing

18.8.2 ASM State Transition Competing Input Timing

There will be situations where two input signals can be valid inputs that will drive two different state transitions from a given state. In that sense, the two signals are “competing” (signals a and b in Figure 78), and the signal that arrives sooner should drive the state transition that will “win”, or drive the state transition. If one signal arrives T_{st_comp} before the other one, it is guaranteed to win, and the state transition that it codes for will be taken, as shown in Figure 79. If the two signals arrive within T_{st_comp} of each other, it will be indeterminate which state transition will win, but one of the transitions will take place as long as the winning signal satisfies the pulse width criteria described in the paragraph above, as shown in Figure 80.

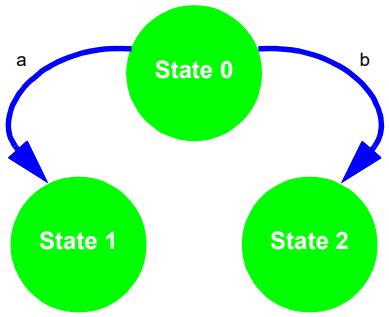


Figure 78: State Transition - Competing Inputs

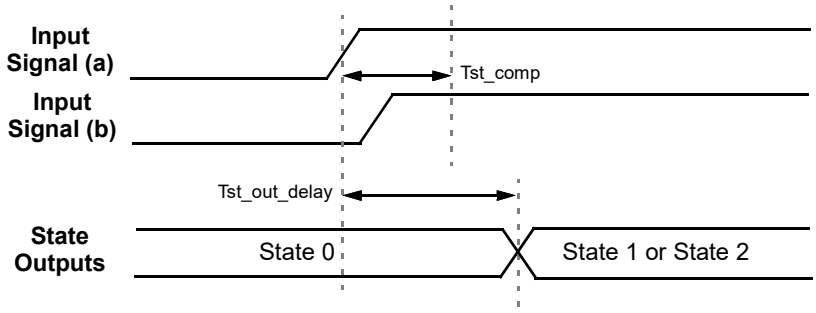


Figure 79: State Transition Timing - Competing Inputs Indeterminate

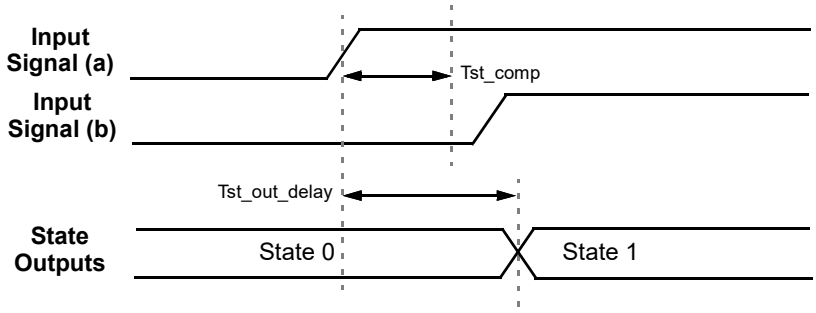


Figure 80: State Transition Timing - Competing Inputs Determinable

18.8.3 ASM State Transition Sequential Timing

It is possible to have a valid input signal for a transition out from a particular state be active before the state is active. If this is the case, the macrocell will only stay in that particular state for $T_{st\_sequential\_delay}$ time before making the transition to the next state. An example of this sequential behavior is shown in Figure 81 and the associated timing is shown in Figure 82.

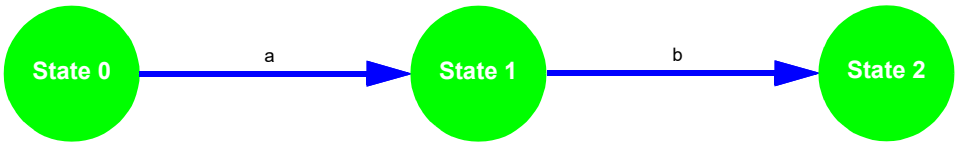


Figure 81: State Transition - Sequential

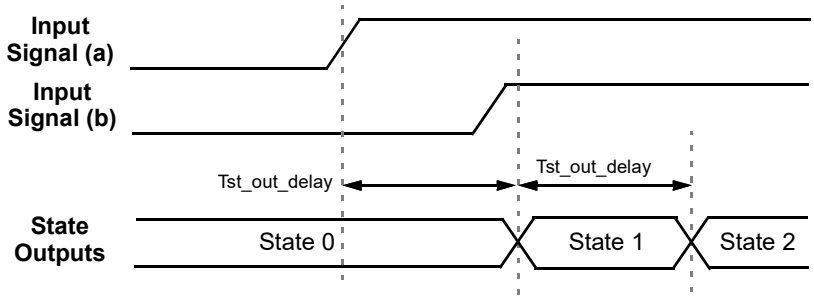


Figure 82: State Transition - Sequential Timing

18.8.4 State Transition Closed Cycling

It is possible to have a closed cycle of state transitions that will run continuously if there if there are valid inputs that are active at the same time. The rate at which the state transitions will take place is determined by $T_{st\_out\_delay}$. The example shown in Figure 83 involves cycling between two states, but any number of two to eight states can be included in state transition closed cycling of this nature. Figure 84 shows the associated timing for closed cycling.

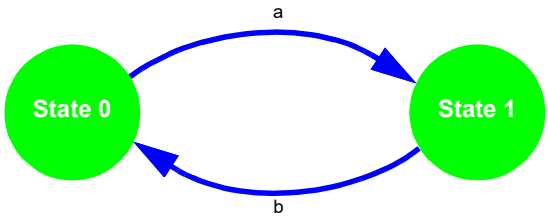


Figure 83: State Transition - Closed Cycling

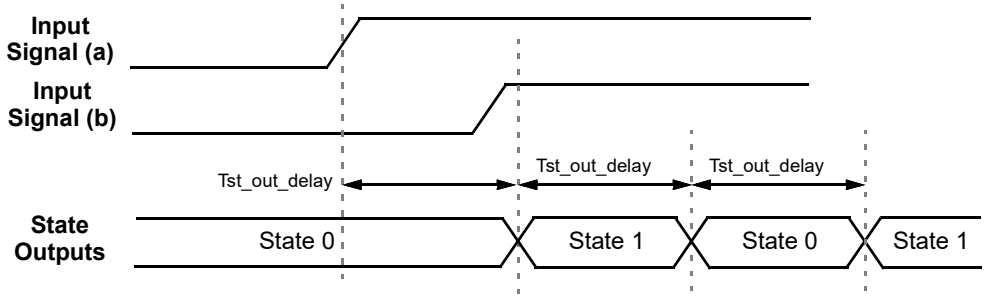


Figure 84: State Transition - Closed Cycling Timing

18.8.5 ASM State Transition Using Edge Detector Option

It is possible to use a rising edge detector option for state transitions. In this case, state transition happens on low to high signal transition as shown in Figure 85 and Figure 86.

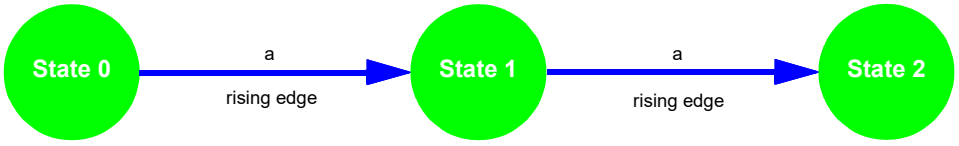


Figure 85: State Transition - Rising Edge Transition

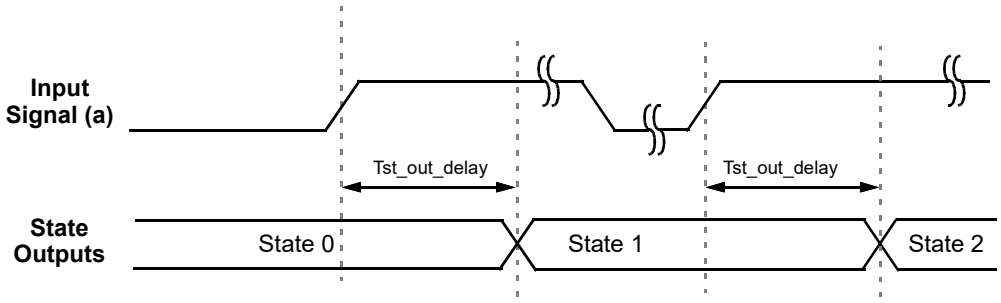


Figure 86: State Transition - Rising Edge Transition Timing

19 I²C Serial Communications Macrocell

19.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM). This information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The SLG46585 supports both 400 kHz (Fast-mode I²C bus) and 1 MHz (Fast-mode Plus I²C bus) I²C bus interfaces, which is selected by register [1868].

The user has the flexibility to control read access and write access via registers bits register [1832] and register [1871]. See Section for more details on I²C read/write memory protection.

Note: GreenPAK I²C is fully compatible with standard I²C protocol.

19.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 87. After the Start bit, the first four bits are a control code, which can be set by the user in registers [1867:1864]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10,A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/$\overline{W}$ bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46585 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46585.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 87 shows this basic command structure.

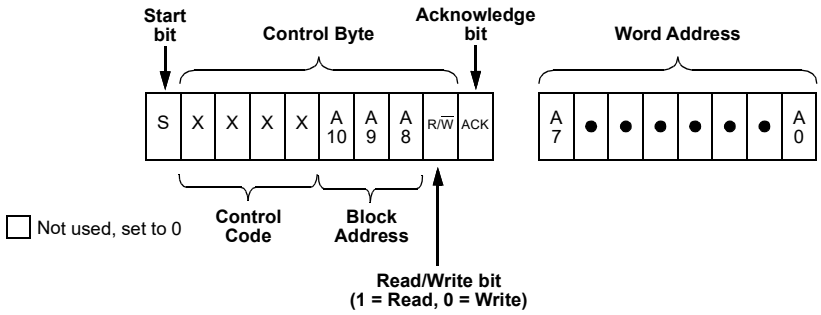


Figure 87: Basic Command Structure

19.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 88. Timing specifications can be found in Section 3.4.

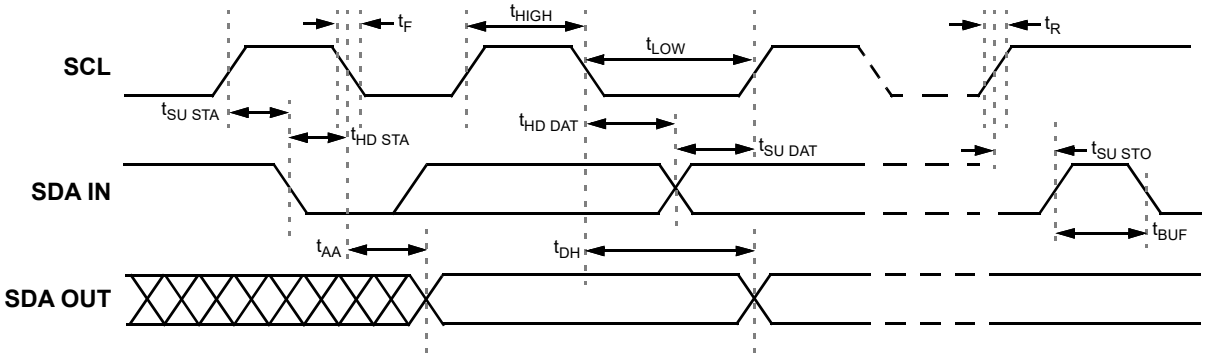


Figure 88: I²C General Timing Characteristics

19.4 I²C SERIAL COMMUNICATIONS COMMANDS

19.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/$\overline{W}$ bit (set to “0”), are placed onto the I²C bus by the Master. After the SLG46585 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46585, where the data byte is to be written. After the SLG46585 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46585 again

provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46585 generates the Acknowledge bit.

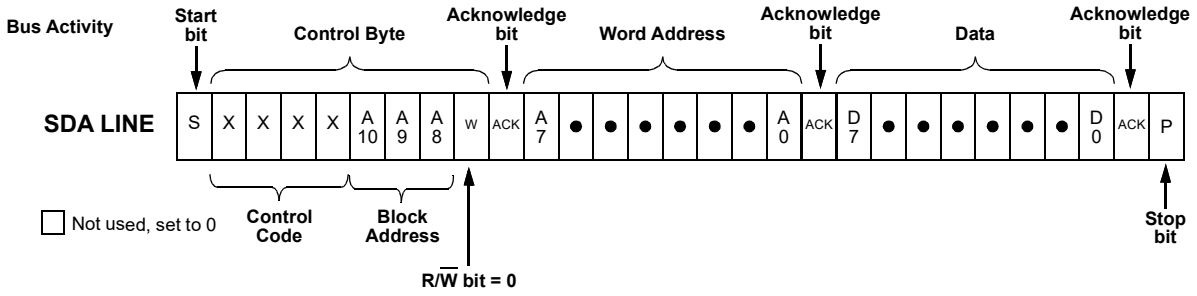


Figure 89: Byte Write Command, R/$\overline{W}$ = 0

19.4.2 Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG46585 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Master continues to transmit data bytes to the SLG46585. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46585 generates the Acknowledge bit.

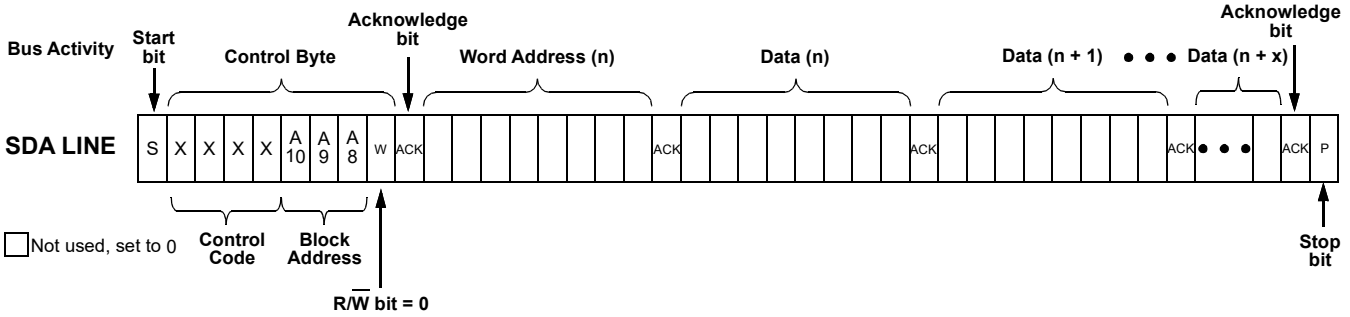


Figure 90: Sequential Write Command, R/$\overline{W}$ = 0

19.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Write or Random Read (which contains a write control byte) writes or reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently,

a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = “1”. The SLG46585 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

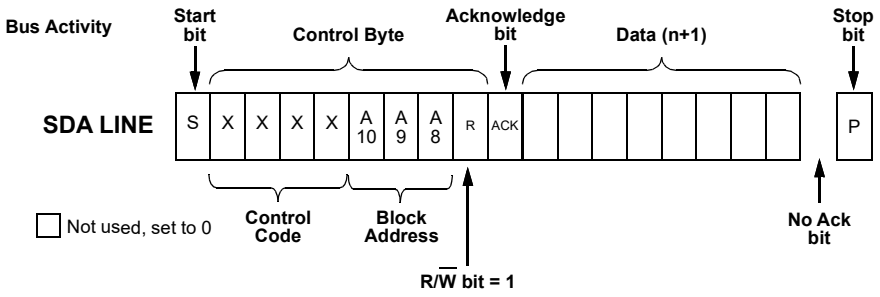


Figure 91: Current Address Read Command, R/$\overline{W}$ = 1

19.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG46585 issues an Acknowledge bit, followed by the requested eight data bits.

.

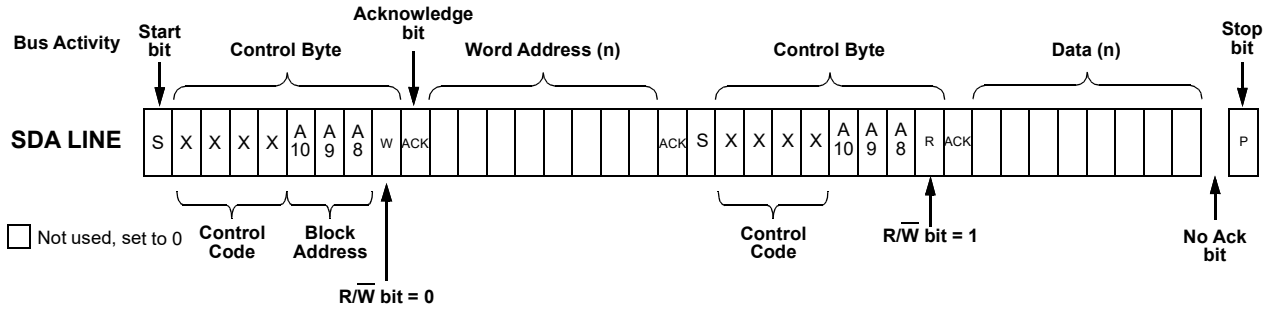


Figure 92: Random Read Command

19.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Current Address Read or Random Read command, except that once the SLG46585 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

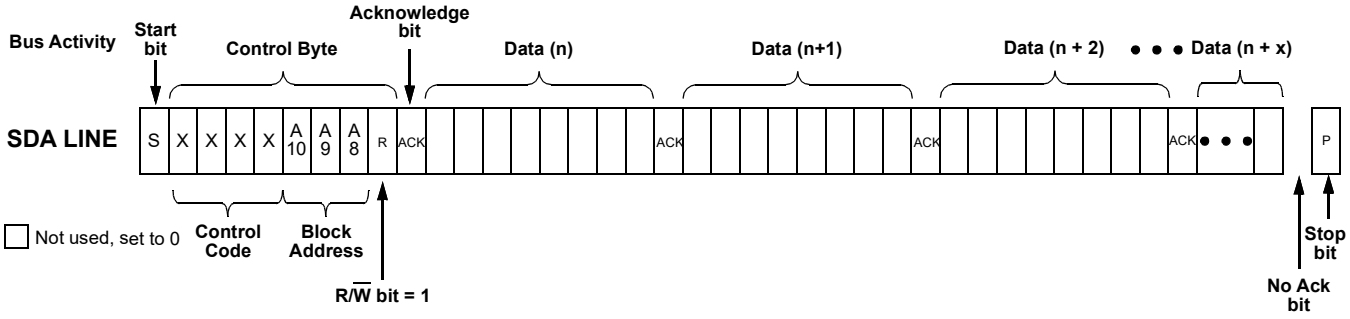


Figure 93: Sequential Read Command

19.4.6 I²C Serial Command Address Space

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46585 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46585.

19.5 I²C SERIAL COMMAND REGISTER MAP

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 91 for details.

Table 91: Read/Write Protection Options

Configurations	Protection Modes Configuration						Data Output From	Register Address (HEX)
	Unlocked	Locked for read bits	Locked for write bits	Locked for write all bits	Locked for read and write bits	Locked for read bits and write all bits		
	Register [1832]=0 Register [1871]=0 Register [1870]=0	Register [1832]=1 Register [1871]=0 Register [1870]=0	Register [1832]=0 Register [1871]=1 Register [1870]=0	Register [1832]=0 Register [1871]=x Register [1870]=1	Register [1832]=1 Register [1871]=1 Register [1870]=0	Register [1832]=1 Register [1871]=x Register [1870]=1		
I²C Serial Reset Command	R/W	R/W	R/W	R	R/W	R	Memory	CF,b'6
Outputs Latching During I²C Write	R	R	R	R	R	R	Memory	CF,b'7
Connection Matrix Virtual Inputs	R/W	R/W	R/W	R	R/W	R	Macrocell	F4
Configuration Bits for All Macrocells (IO Pins, Combination Function Macrocells, ASM, etc.)	R/W	W	R	R	-	-	Memory	80-BF
Macrocells Inputs Configuration (Connection Matrix Outputs)	R/W	W	R	R	-	-	Memory	00-67
LDO settings, RAM, ACMP settings, DLY/ CNT control data, RTC settings	R/W	R/W	R/W	R	R/W	R		6E, D0-E3; CF,b'0-b'2; C6-CE; C0-C4; 75-7F
Macrocells Output Values (Connection Matrix Inputs)	R	R	R	R	R	R	Macrocell	F0-F3; F5-F7
Counter Current Value	R	R	R	R	R	R	Macrocell	70-71
ASM Current State	R	R	R	R	R	R	Macrocell	EF
Silicon Identification Service Bits	R	R	R	R	R	R	Memory	E8
Pattern ID0/1	R/W	R/W	R/W	R	R/W	R	Memory	E6, E4
I²C Control Code	R	R	R	R	R	R	Memory	E9,b'0-b3;
Protection Read Configuration (Register [1832])	R	R	R	R	R	R	Memory	E5,b'0
Protection Write Configuration (Register [1870], Register [1871)	R	R	R	R	R	R	Memory	E9,b'6-b'7

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as counter current value, ASM current state, connection matrix, and connection matrix virtual inputs. The I^2C write does not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allow identifying silicon family, its revision, and others.

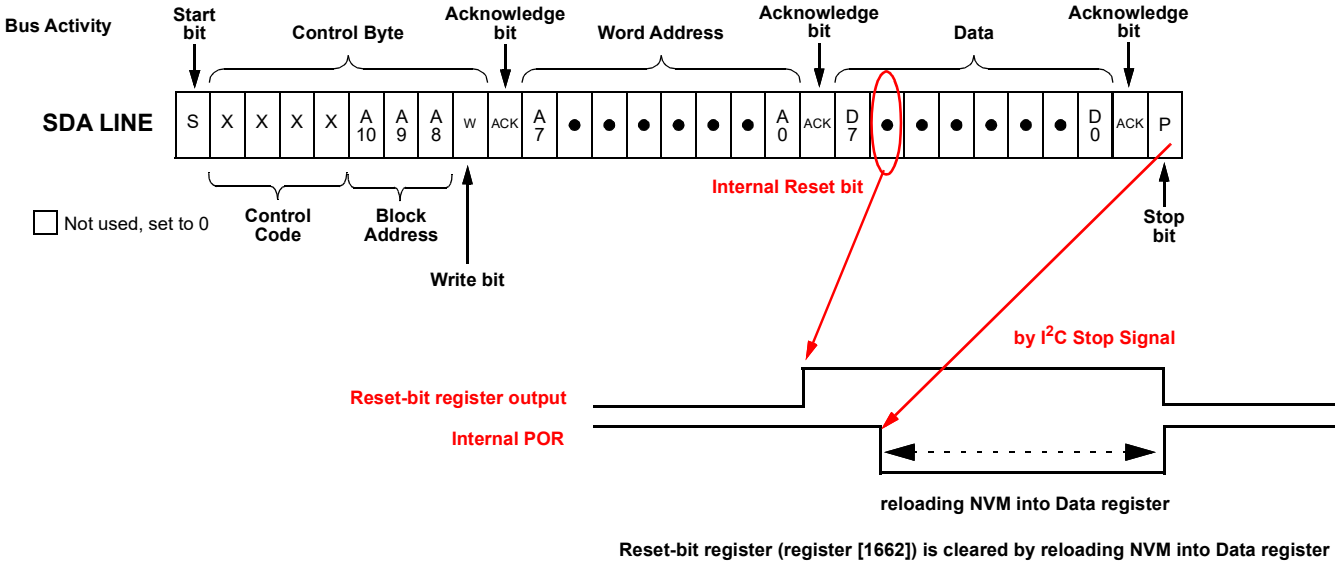
Note: If register [1663] = 1, all outputs are latched while inputs and internal macrocells retain their status during I^2C write.

Note: Any write commands that come to the device via I^2C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See Section 22 for detailed information on all registers.

19.5.1 I^2C Serial Reset Command

If I^2C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1662] I^2C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1662] will be set to “0” automatically. The timing diagram shown in Figure 94 illustrates the sequence of events for this reset function.



1) I²C write with register [1662] = 1 (I²C reset bit with reloading NVM into Data register)
2) POR go to LOW and reloading NVM into Data register start after "STOP" of I²C
3) POR go to HIGH after reloading NVM into Data register

Figure 94: Reset Command Timing

19.5.2 Reading Counter Data via I²C

The current count value in the RTC counter and two counters in the device can be read via I²C. The counters that have this additional functionality are 8-bit counters CNT2 and CNT4.

19.5.3 User RAM and OTP Memory Array

There are eight bytes of RAM memory that can be read and written remotely by I²C commands. The initial contents of this memory space can be selected by the user, and this information will be transferred from OTP memory to the RAM memory space during the power-up sequence. The lowest order byte in this array (User Configurable RAM/OTP Byte 0) is located at I²C address 0xD8, and the highest order byte in this array is located at I²C address 0xDF.

Table 92: RAM Array Table

I²C Address (hex)	Highest Bit Address	Lowest Bit Address	Memory Byte
D8	1735	1728	User Configurable RAM/OTP Byte 0
D9	1743	1736	User Configurable RAM/OTP Byte 1
DA	1751	1744	User Configurable RAM/OTP Byte 2
DB	1759	1752	User Configurable RAM/OTP Byte 3
DC	1767	1760	User Configurable RAM/OTP Byte 4
DD	1775	1768	User Configurable RAM/OTP Byte 5
DE	1783	1776	User Configurable RAM/OTP Byte 6
DF	1791	1784	User Configurable RAM/OTP Byte 7

20 Low Dropout Regulators

20.1 LDO REGULATOR DESCRIPTION

The SLG46585 comes with four low dropout regulators each rated at 150 mA. Each LDO regulator has 3 modes which are: HP MODE is the standard active mode supporting full 150 mA output; LP MODE is a low power mode with maximum 100 µA; and finally Power Switch Mode in which the LDO regulator ceases to regulate and the Regulator MOSFET is turned on as a power switch, passing the voltage applied to VIN directly to VOUT.

The LDO regulators are paired together with LDO0 and LDO1 sharing the same V_{IN} called LDO0/1 VIN, likewise LDO2 and LDO3 share the same V_{IN} called LDO2/3 VIN.

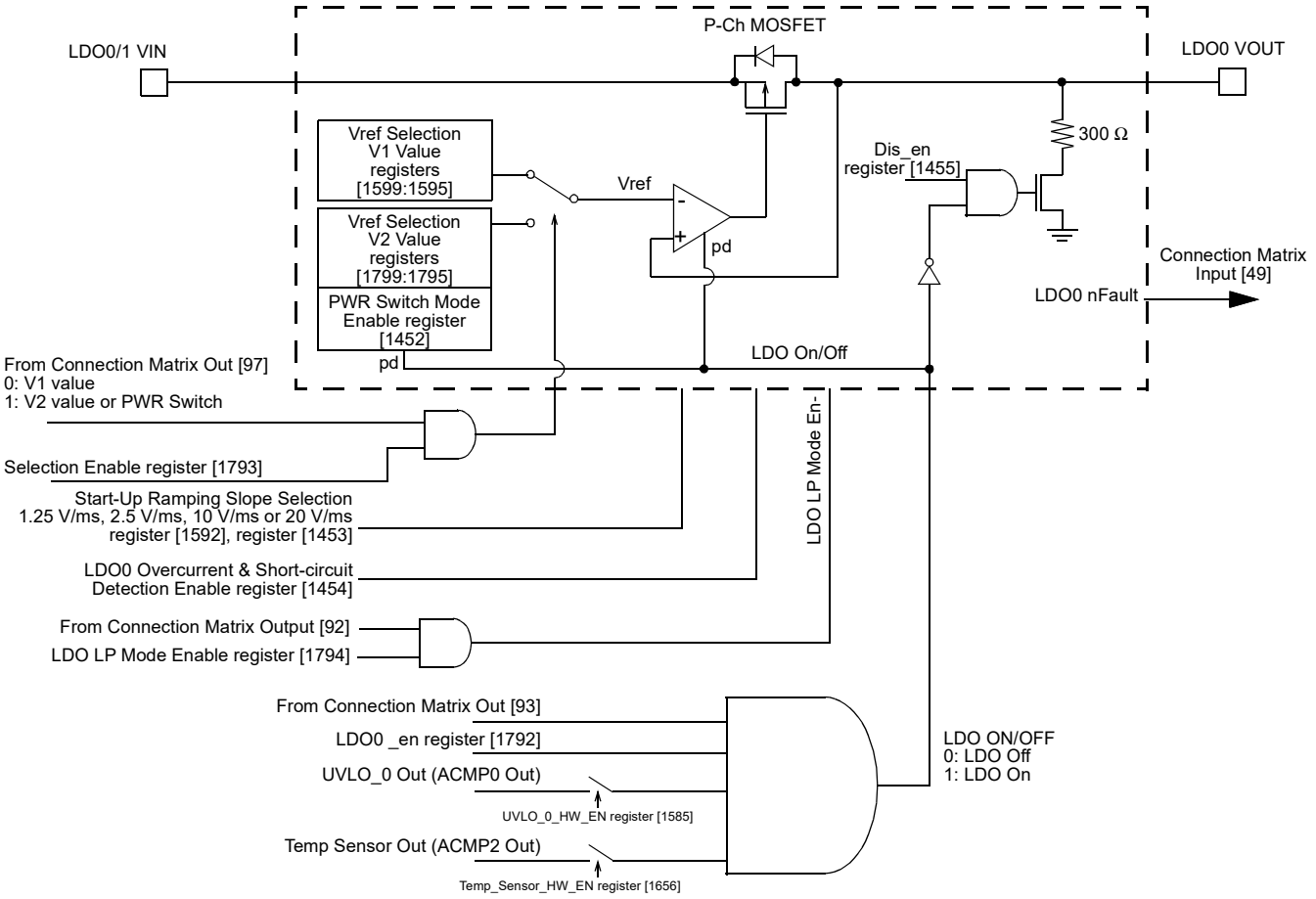


Figure 95: LDO0 Regulator Block Diagram

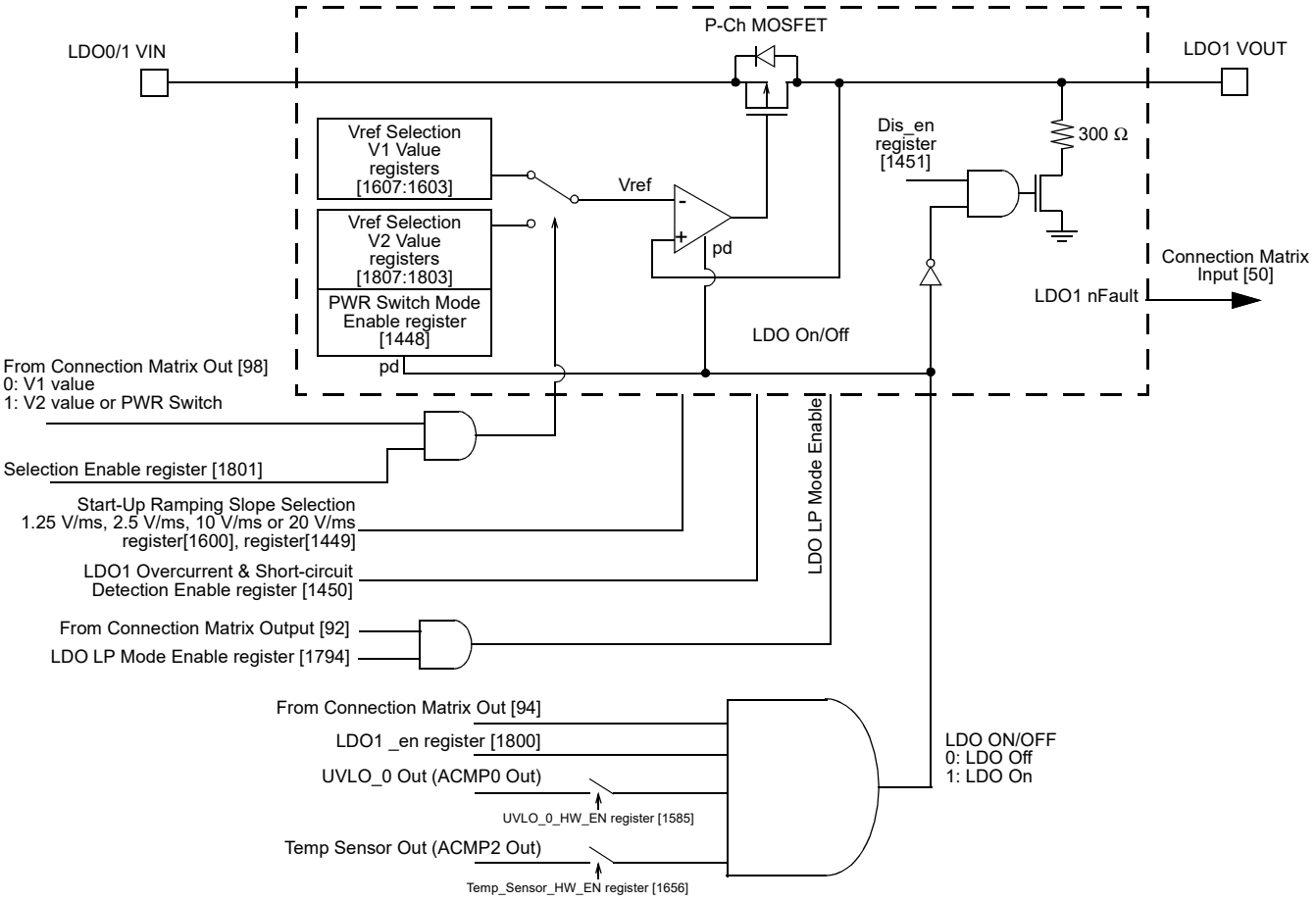


Figure 96: LDO1 Regulator Block Diagram

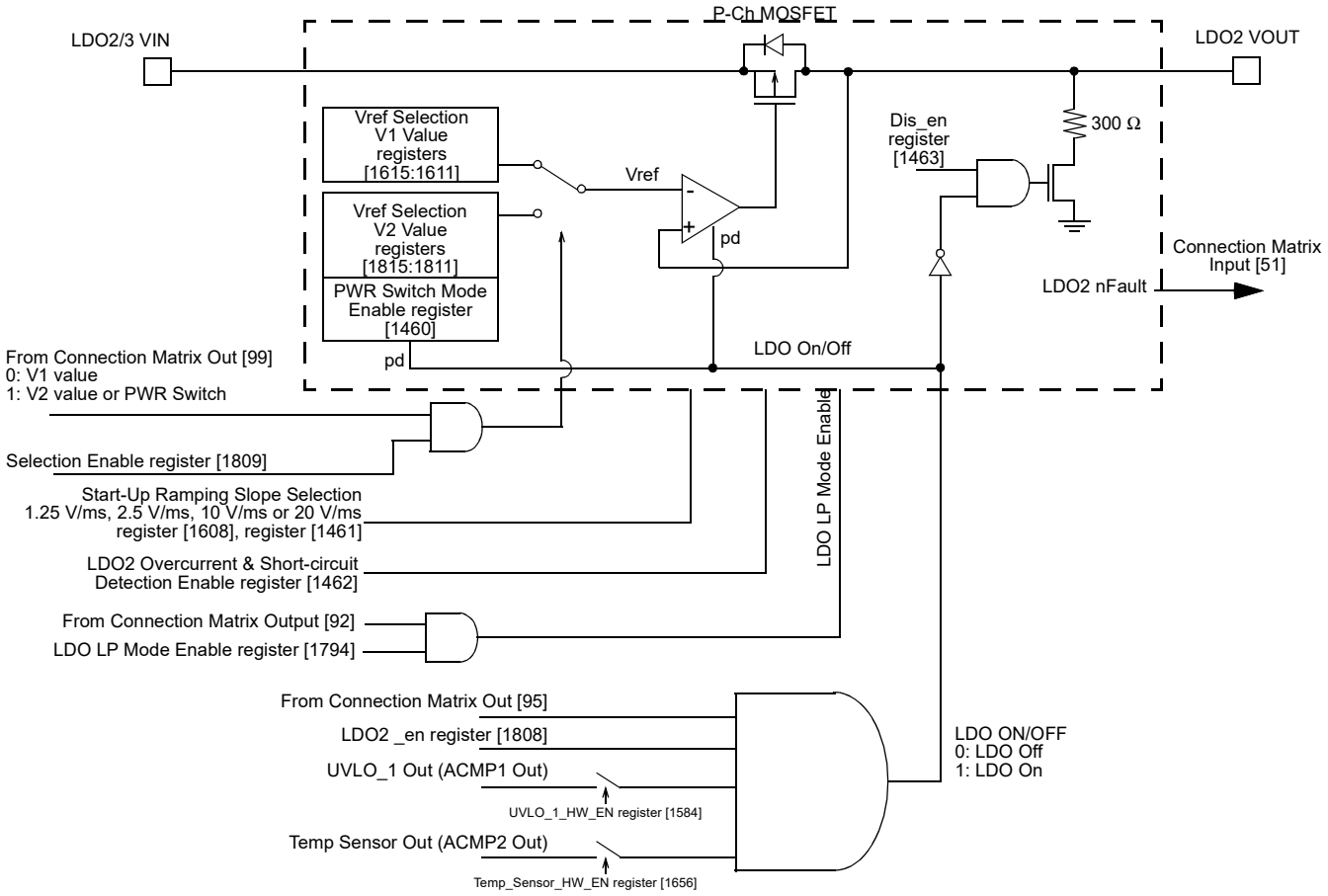


Figure 97: LDO2 Regulator Block Diagram

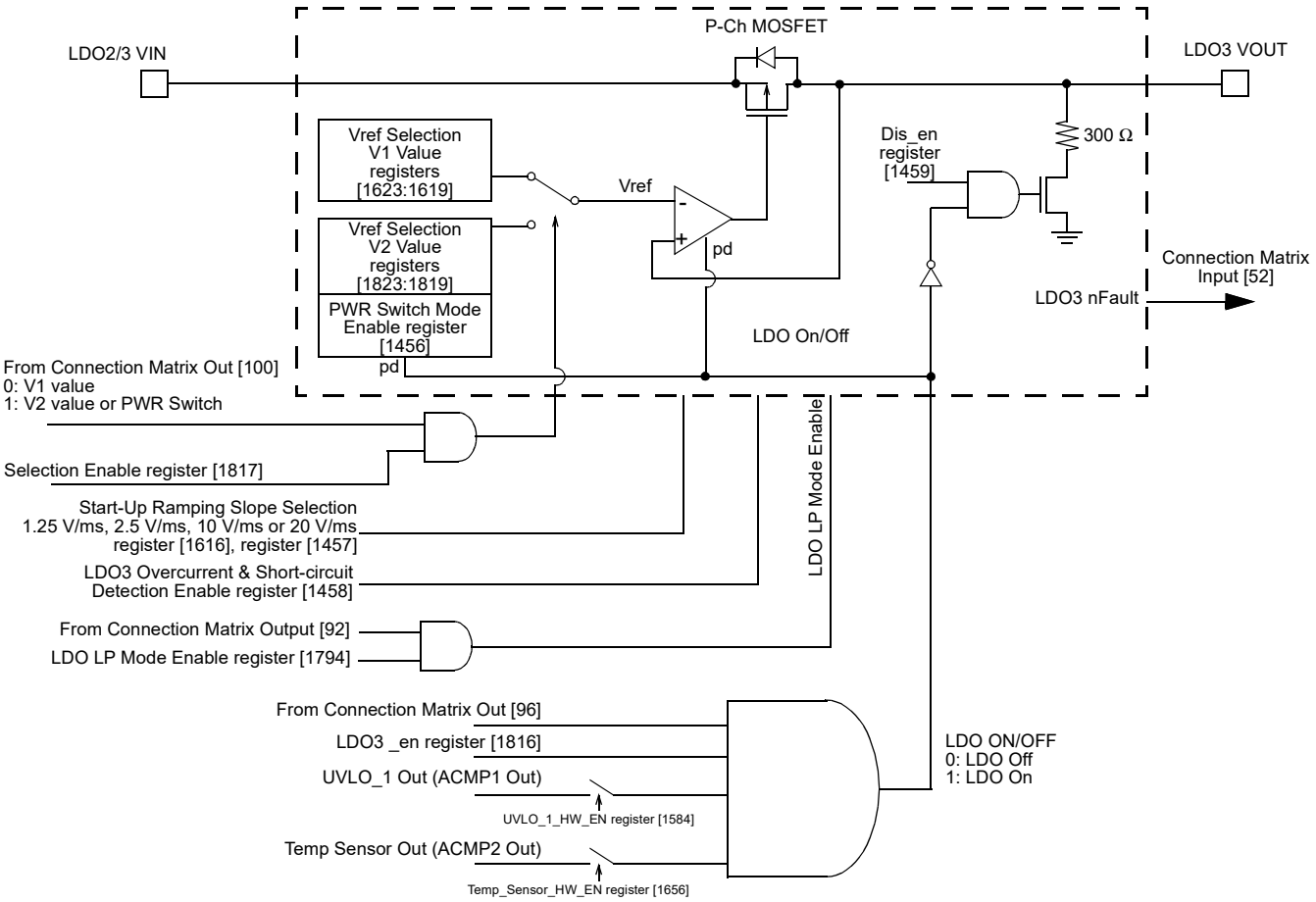


Figure 98: LDO3 Regulator Block Diagram

20.1.1 Voltage Selection

Each LDO has access to 32 voltage levels derived from a bandgap voltage reference.

It is possible to select two different output voltage levels (V1 and V2) per LDO. The voltage levels can be changed through the Connection Matrix, after V1/V2 selection is enabled through the register bit. It is also possible to change the LDO output voltage level through the I^2C by writing the corresponding LDO output voltage selection number according to Table 93.

Table 93: LDO Output Voltage Selection

Selection #	LDO VOUT (V)	LDO Min VIN (V)	Min V_{DD} (V)	PW SEL
0	0.90	2.50	2.50	000
1	1.00	2.50	2.50	000
2	1.05	2.50	2.50	000
3	1.10	2.50	2.50	000
4	1.20	2.50	2.50	000
5	1.25	2.50	2.50	000

Table 93: LDO Output Voltage Selection (Continued)

Selection #	LDO VOUT (V)	LDO Min VIN (V)	Min V_{DD} (V)	PW SEL
6	1.35	2.50	2.50	000
7	1.50	2.50	2.50	000
8	1.67	2.50	2.50	000
9	1.80	2.50	2.50	000
10	1.90	2.50	2.50	000
11	2.00	2.50	2.50	000
12	2.10	2.50	2.80	001
13	2.20	2.50	2.80	001
14	2.30	2.60	2.80	001
15	2.40	2.70	2.80	001
16	2.50	2.80	2.80	001
17	2.60	2.90	3.00	010
18	2.70	3.00	3.00	010
19	2.80	3.10	3.30	011
20	2.85	3.15	3.30	011
21	2.90	3.20	3.30	011
22	3.00	3.30	3.30	011
23	3.10	3.40	3.60	100
24	3.20	3.50	3.60	100
25	3.30	3.60	3.60	100
26	3.40	3.70	3.90	101
27	3.50	3.80	3.90	101
28	3.60	3.90	3.90	101
29	4.00	4.30	4.40	110
30	4.10	4.40	4.50	111
31	4.20	4.50	4.50	111

Note 1 The combination of VIN, $V_{DD,}$ and VOUT must satisfy the rule: $V_{DD} \geq VIN \geq VOUT + 0.3$ V.
Note 2 VIN and V_{DD} should not exceed 5.5 V.

20.1.2 LDO HP Mode Operation

HP Mode is the standard active LDO mode with a 150 mA per LDO output loading capability. $V_{DD} \geq 2.5$ V.

A high level signal should be applied to Connection Matrix Outputs [93], [94], [95], and [96] together with the register enable bits [1792], [1800], [1808], and [1816] to enable LDO0, LDO1, LDO2, and LDO3, respectively. The LDO requires a wait time to enable analog circuitry before the LDO output starts to rise with the desired ramping slope selected through the register bits.

20.1.3 LDO LP Mode Operation

It is possible to enable ultra-low power LP Mode in which max output loading is 100 µA and quiescent current consumption is ~2 µA per LDO (without load). LP Mode can be enabled through Connection Matrix Output [92] together with the register enable bit <1794> and have an impact for all LDOs enabled in the SLG46585 chip.

20.1.4 Power Switch Mode Operation

Each LDO has an additional option to operate in power switch mode. In this case, all LDO related circuitry will be disabled. The quiescent current consumption is ~1 µA in power switch mode.

The power switch option is available in each LDO and can be used instead of the VOUT2 output voltage level selected by the following register bits: register [1452] for LDO0, register [1448] for LDO1, register [1460] for LDO2, and register [1456] for LDO3.

The Power Switch Mode can be selected by applying a high-level signal to the Connection Matrix Output [97], [98], [99], and [100] for LDO0, LDO1, LDO2, and LDO3 respectively.

20.2 OVER-CURRENT LIMIT AND SHORT-CIRCUIT DETECTION

Each LDO has an option to enable OCL (Over-Current Limit, if the output current rises above 210 mA) and SCD (Short-Circuit Detection, if output voltage drops below 0.5 V with the current limited by 20 mA).

These options are available for the LDO in HP Mode only. The nFAULT signal per LDO will generate a low-level signal to the connection matrix input when the short-circuit is detected.

20.3 LDO EFFICIENCY

The efficiency of LDO regulators is limited by the quiescent current and input/output voltages as follows:

$$\eta_{EF} = \frac{I_{OUT} \times V_{OUT}}{(I_{OUT} + I_Q) \times V_{IN}} \times 100$$

where:

η_{EF} = LDO efficiency, in percents (%)
I_{OUT} = Output current, in Amps (A)
V_{OUT} = Output voltage, in Volts (V)
I_Q = Quiescent current, in Amps (A)
V_{IN} = Input voltage, in Volts (V)

To have a high efficiency, drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and output must be minimized, since the power dissipation of LDO regulators accounts for efficiency:

$$PD = V_{DO} \times I_{OUT}$$

where:

PD = Power Dissipation, in Watts (W)
V_{DO} = Drop out voltage, in Volts (V)
I_{OUT} = Output current, in Amps (A)

The Input/Output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load conditions.

20.4 LDO THERMAL CONSIDERATIONS

The thermal limitations must be taken into consideration during regulator design. The SLG46585 is rated at 0.6 W of power dissipation at 85 °C ambient and 0.8 W of power dissipation at 70 °C ambient. If a regulator is connected to 5.0 V and then is programmed to output 1.8 V, the power dissipation at 150 mA is 0.48 W or almost the entire thermal budget of the SLG46585. In this case we recommend putting an external resistor between the application's power source (battery or wall power) and the SLG46585's LDO VIN to help distribute the thermal load. A 10 Ω, ¼ watt resistor would cut the IC thermal dissipation about in half without impacting overall performance. However, because the LDO VIN voltage is shared between two LDOs the resistor should be properly selected for the higher of the desired LDO output voltages.

If it is possible to use the temperature sensor together with ACMP2 to automatically shut down all LDOs if the die temperature rises to a predetermined threshold level. The LDOs will automatically restart when the chip has cooled down within the hysteresis range for ACMP2. Other temperature shut off levels may be achieved by incorporating the temperature sensor into ACMP3's input.

20.5 SOFT START FUNCTION (SS)

Table 94 to Table 97 show the bit settings and slew rate selection options for each LDO.

Table 94: LDO0 Ramp Rate Selection Table

Parameter	Description	Typical Value	register [1453]	register [1592]
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

Table 95: LDO1 Ramp Rate Selection Table

Parameter	Description	Typical Value	register [1449]	register [1600]
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

Table 96: LDO2 Ramp Rate Selection Table

Parameter	Description	Typical Value	register [1461]	register [1608]
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

Table 97: LDO3 Ramp Rate Selection Table

Parameter	Description	Typical Value	register [1457]	register [1616]
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

20.6 ACMPS: UNDER VOLTAGE LOCKOUT CAPABILITY, POWER GOOD

LDO0/1 VIN and LDO2/3 VIN are sensed by ACMP0 and ACMP1 respectively as one of their input options. The sense line can be divided by 2, 3, or 4 for the common mode voltage input limitation of ACMP0 and ACMP1. ACMP0 and ACMP1 can be set to the customers desired under voltage lockout (UVLO) level. The undervoltage lockout can be set by either hardware connection to control the LDO or through the Connection Matrix. The UVLO_0 hardware connection to the LDO can be enabled by register [1585] for LDO0 and LDO1, and UVLO_1 by register [1584] for LDO2 and LDO3.

Note: ACMP0 needs to be properly configured to use UVLO_0 for LDO0 and LDO1. ACMP1 needs to be properly configured to use UVLO_1 for LDO2 and LDO3.

A lockout level below 2.5 V is not useful as the lowest acceptable power supply voltage is 2.5 V.

ACMP3 has a selectable input from the output of LDO0 or 2 for the purpose of a power good.

The ACMPs connection to V_{DD} may be reused for the purpose stated above.

20.7 REGULATOR STABILITY CONSIDERATIONS

The regulators are only stable in HP MODE when a 2 µF (min) capacitor or greater is attached to each LDOs V_{OUT}. The recommended capacitor is a 2 µF (min) X5R capacitor rated for 6 V or greater. The X5R capacitor varies with temperature, DC bias voltage, and process; however the SLG46585 LDOs have taken this variance into consideration when recommending the 2 µF (min) X5R from -40 °C to +85 °C.

20.8 LDO REGULATOR COLD START UP

When the SLG46585 V_{DD} goes high, then the fastest that an LDO regulator can begin to power up under the control of the SLG46585 is ~2 ms typical, and 3 ms max.

During this cold start period the P Channel MOSFET gate is 0 V so the MOSFET is automatically turning on if LDO VIN is also coming up.

20.9 LDO REGULATOR HOT START UP

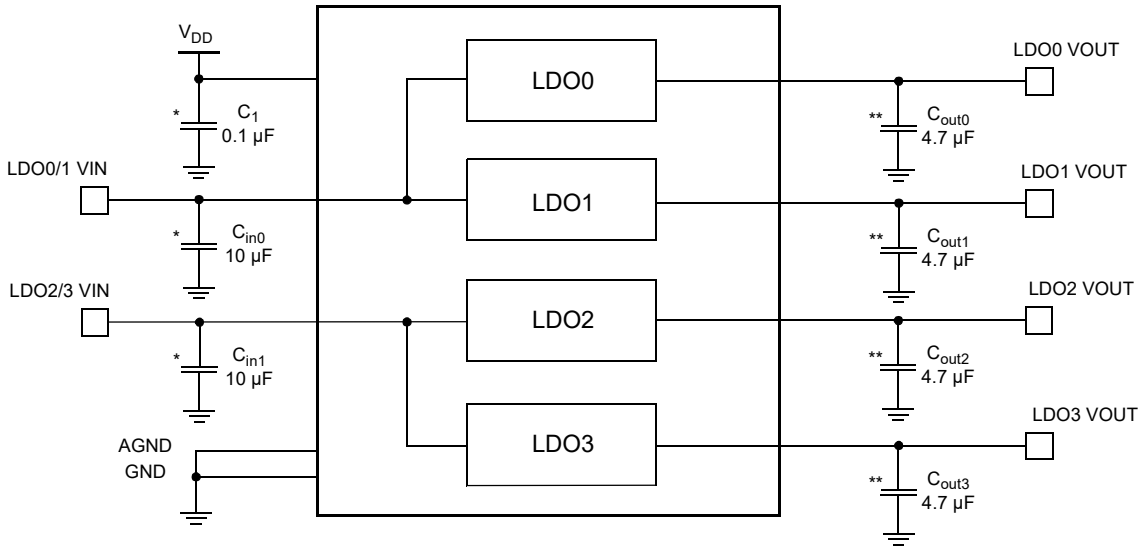
When the SLG46585 V_{DD} is already high, then the fastest than an LDO regulator can begin to power up is around 500 µs + soft start ramping.

20.10 DISCHARGE RESISTORS

Each LDO comes with a program selectable 300 Ω discharge resistor. For applications that desire a power rail to be brought to near zero during shutdown, then the 300 Ω discharge resistor is useful. For applications that desire to keep remaining charge on a V_{OUT} capacitor the discharge resistor should not be selected.

The discharge resistor is set by register [1455] for LDO0, register [1451] for LDO1, register [1463] for LDO2, and register [1459] for LDO3.

20.11 TYPICAL APPLICATION CIRCUIT



Note: All internal connections shown inside the SLG46585 are hardwired connections that cannot be changed.
Note: Keep decoupling capacitors close to the SLG46585.*
*Note**: Keep output capacitors close to the SLG46585. Long distances negatively impact LDO stability.*

Figure 99: LDO Typical Application Circuit

20.12 TYPICAL APPLICATION PERFORMANCE

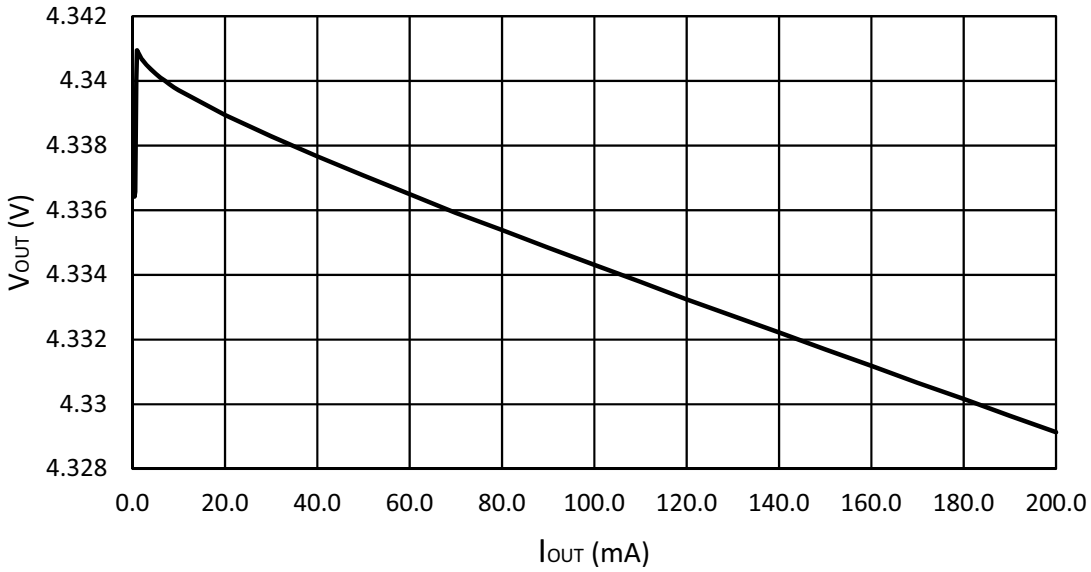


Figure 100: LDO Load Regulation, HIGH POWER Mode, T = 25 °C, V_{DD} = 5 V, VOUT = 4.35 V

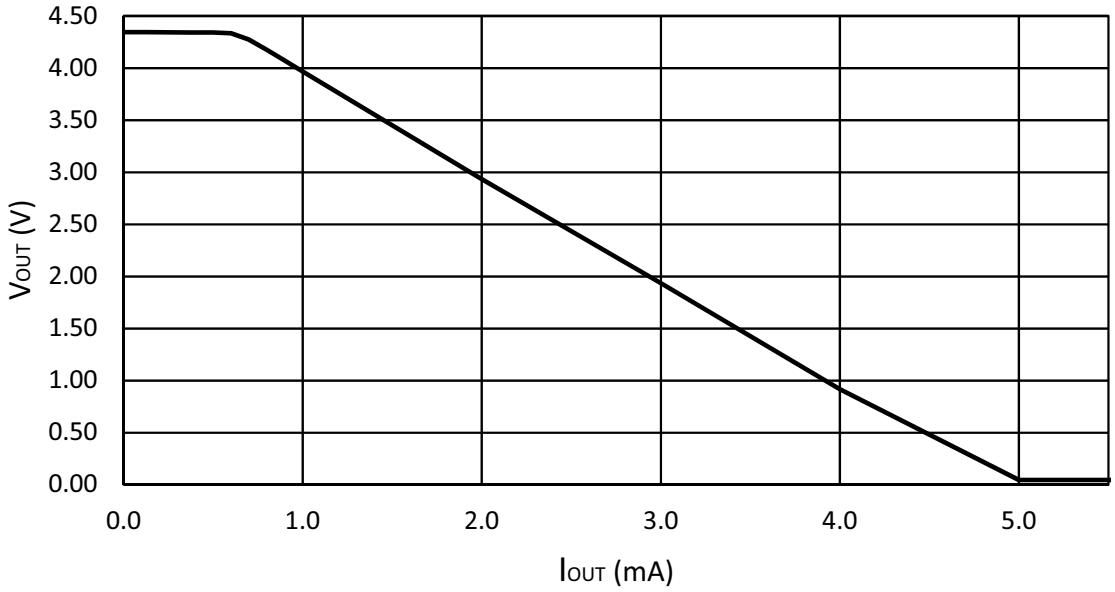


Figure 101: LDO Load Regulation, LOW POWER Mode, T = 25 °C, V_{DD} = 5 V, VOUT = 4.35 V

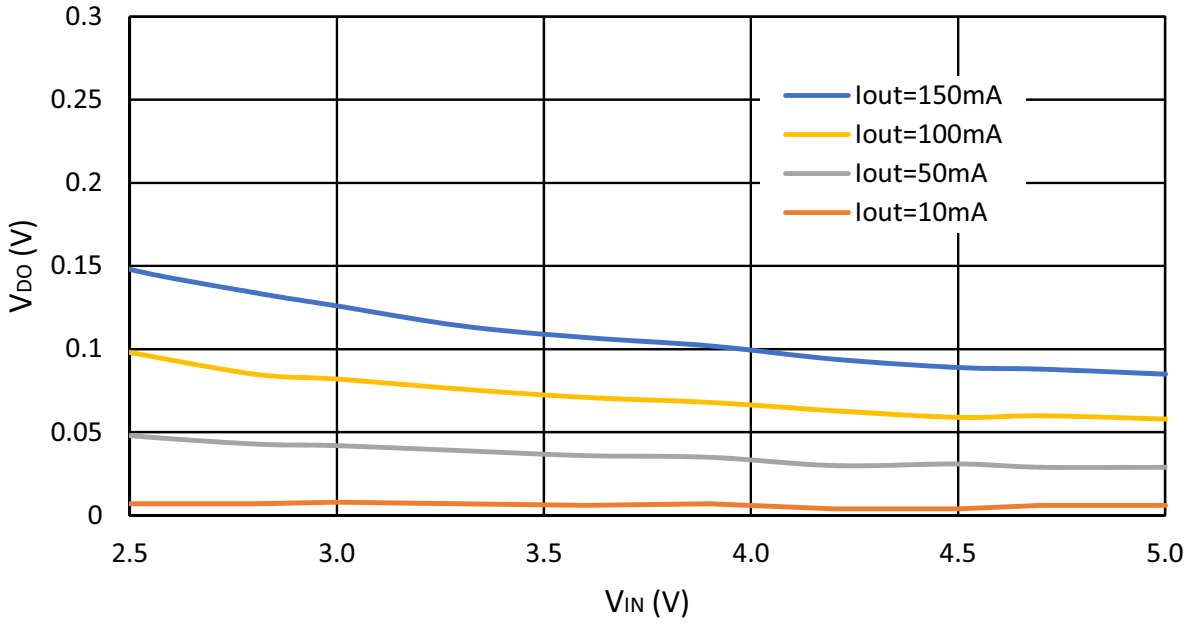


Figure 102: LDO Dropout Voltage vs. VIN

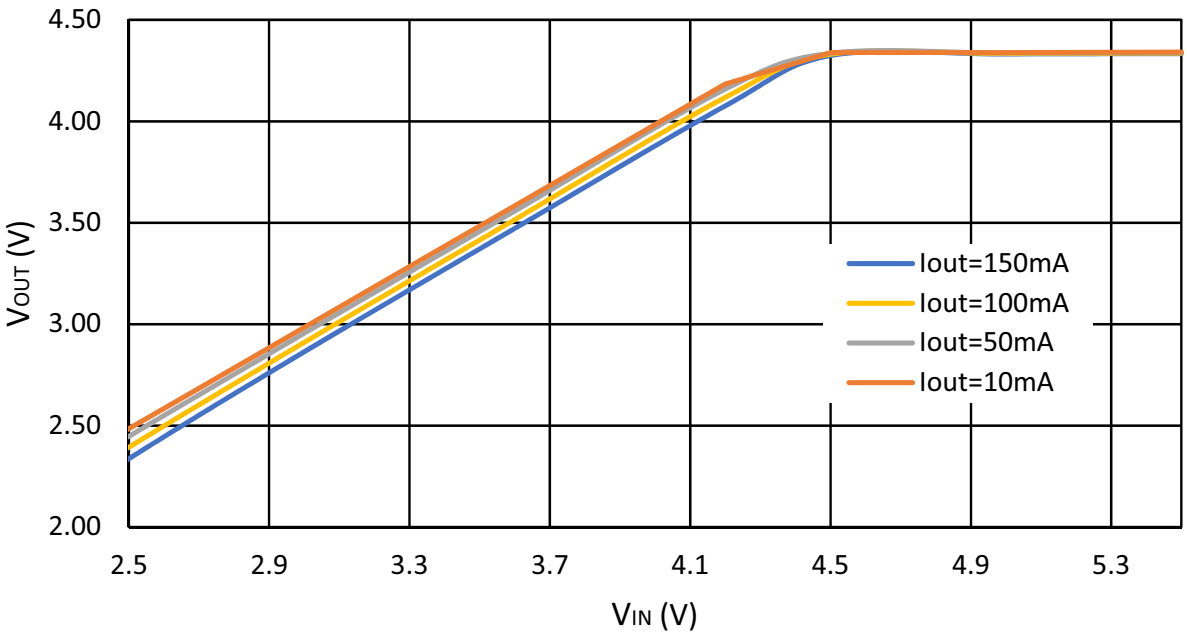


Figure 103: LDO High Power Mode VOUT vs. VIN, T = 25 °C, V_{DD} = 5 V

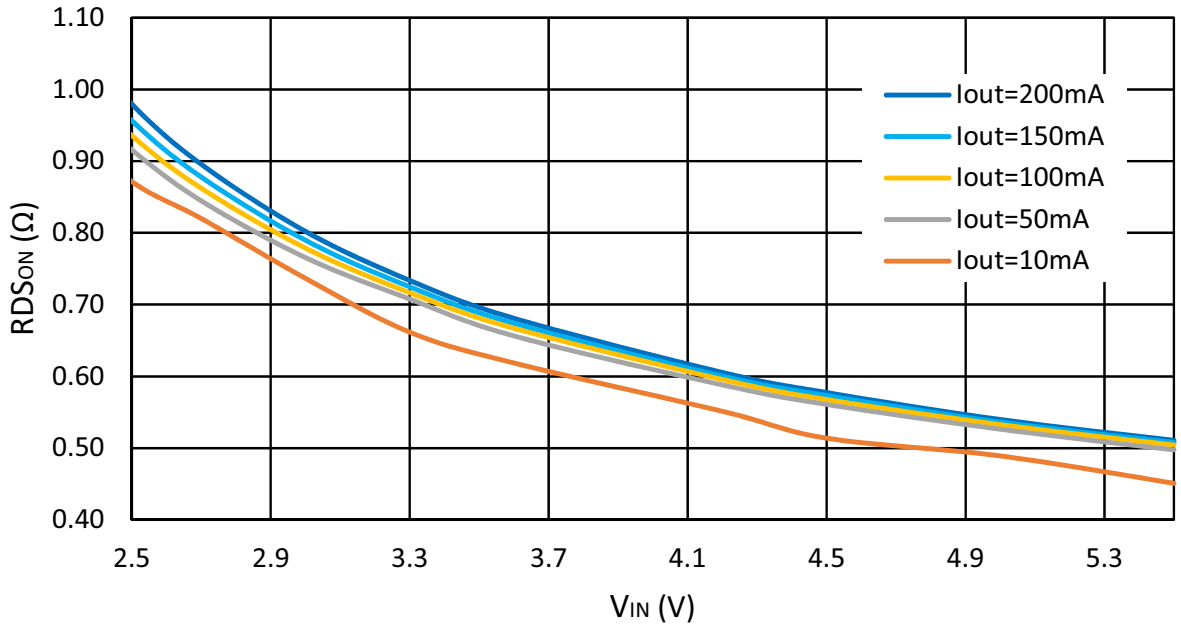


Figure 104: LDO P-Channel ON Resistance RDSon vs. VIN, Power Switch Mode, T = 25 °C

21 1 A Synchronous DC/DC Step Down Converter

21.1 DC/DC BUCK CONVERTER DESCRIPTION

The SLG46585 has a Synchronous DC/DC Step Down Converter macrocell. The DC/DC is rated for 1 A of current for an input voltage range 2.5 V to 5.5 V and has one output voltage that can be regulated at six user selectable steps from 1.2 V to 3.3 V.

The DC/DC Step Down Converter is classified as a synchronous driver circuit that uses constant-on-time and constant frequency pulse modulation technique. The device features DCM and CCM mode with automatic mode switching, and uses an integrated internal resistive feedback divider.

Protection features include Over Current Protection, Thermal Shutdown, Under Voltage Lockout.

21.2 SYNCHRONOUS DC/DC STEP DOWN CONVERTER BLOCK DIAGRAM

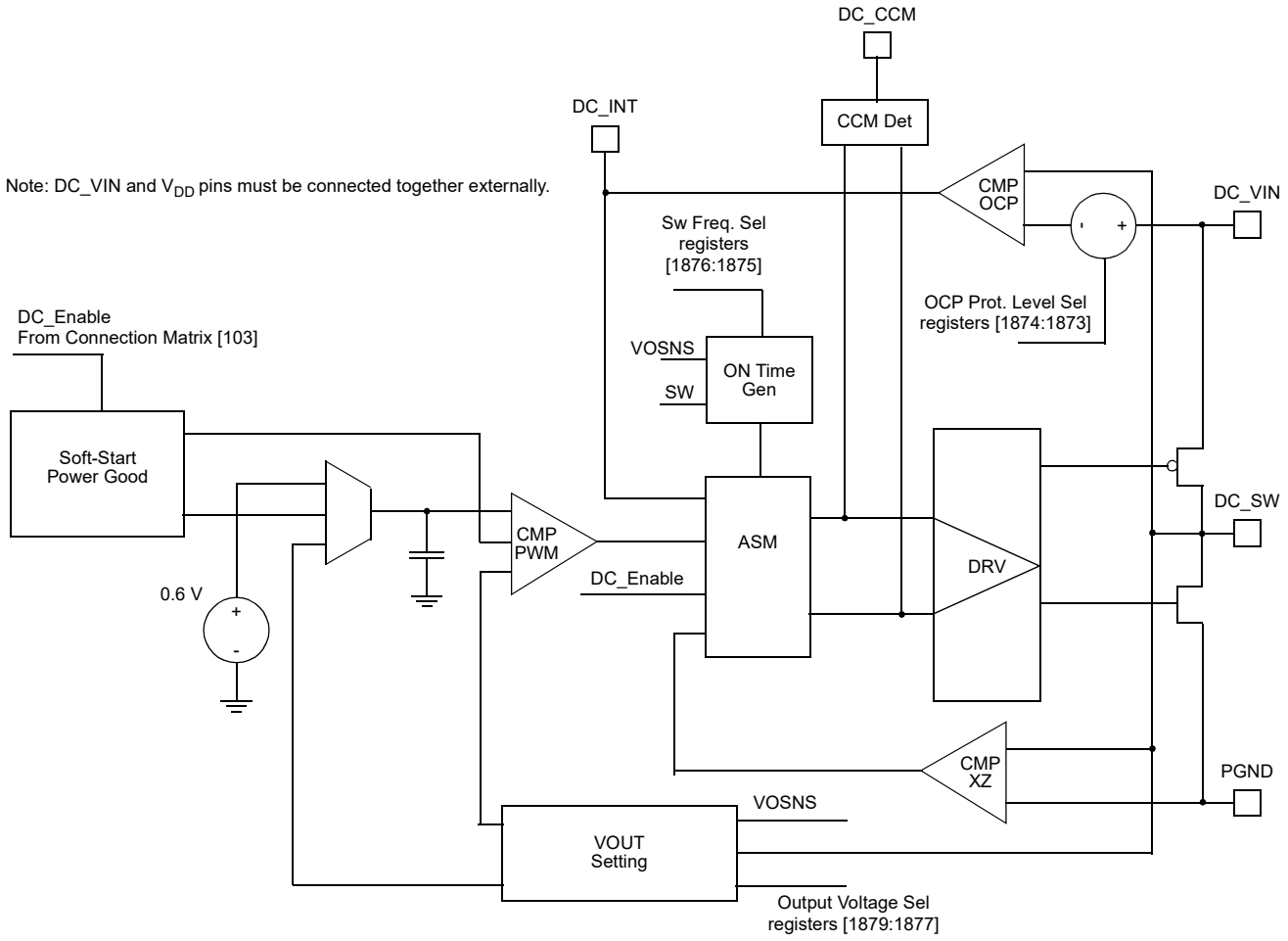


Figure 105: DC/DC Block Diagram

21.3 TYPICAL APPLICATION CIRCUIT

Figure 106 shows the typical application circuit for the Synchronous DC/DC Step Down Converter macrocell, including a selection of typical external components.

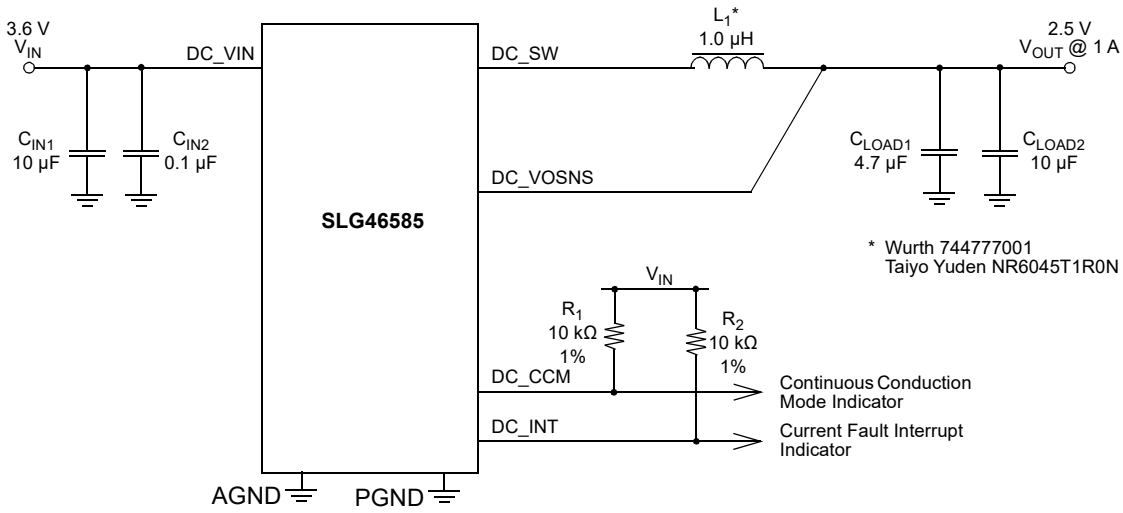


Figure 106: DC/DC Typical Application Circuit

21.4 DC/DC BUCK CONVERTER PINOUT DESCRIPTION

- ON/OFF command for the Synchronous DC/DC Step Down Converter is a matrix connection [831:824]. Its enable signal is edge sensitive. During pin transition from Low to High, the Buck Converter will be enabled. And during transition from High to Low, the Buck Converter will be disabled. This pin should never be floating.
- DC_VIN - DC/DC Buck Converter input voltage pin.
- DC_SW - DC/DC Buck Converter Switching Node. The SW is a pulse modulated signal that is connected to the inductor of the LC Filter Circuit.
- DC_VOSNS - DC/DC Buck Converter VOUT feedback (sense) input. This pin is connected to the Output Voltage at the load. An internal feedback circuit regulates the output voltage by comparing it with an internal reference generated by the DC_AGND. No external resistors are required.
- DC_AGND - DC/DC Buck Converter Analog Ground feedback. This pin is connected to the Output Ground at the load. This pin is the source for both internal feedback circuit and internal generated reference.
- DC_PGND - DC/DC Buck Converter Power Ground.
- DC_CCM - DC/DC Buck Converter digital output indicates whether the current mode is CCM or DCM.
- DC_INT - DC/DC Buck Converter digital output indicates whether the over-current protection circuit has been activated due to an over-current event or a thermal shutdown has occurred. The DC/DC Step Down Converter Fault Signal is routed to Matrix Input 3.

21.5 CONFIGURABLE PARAMETERS

The DC/DC Converter's output voltage, switching frequency and current limit threshold are configurable. To change the configuration in system, use I^2C to write the registers and then toggle the ON/OFF Signal.

Table 98: DC/DC Output Voltage Bit Settings

Output Voltage	registers [1879:1877]
1.2 V	000
1.5 V	001
1.8 V	010
2.5 V	011
3.0 V	100
3.3 V	101

Table 99: DC/DC Switching Frequency Bit Settings

Switching Frequency	registers [1876:1875]
1.5 MHz	00
2.0 MHz	01

Table 100: DC/DC Current Limit Bit Settings

Current Limit	registers [1874:1873]
2.5 A	00
2.0 A	10

21.6 OUTPUT VOLTAGE SELECTION

The Synchronous DC/DC Step Down Converter macrocell supports six user selectable output voltage levels. Register bits registers [1879:1877] control this selection.

The DC/DC VIN operating range is from 2.5 to 5.5. However, the input voltage must be an extra 20 to 25% greater than the output voltage due to the maximum duty-cycle limit. The maximum allowable duty cycle at 1.5 MHz is 80% and the maximum allowable duty cycle at 2 MHz is 75%. Refer to the Table 101 for the typical input voltage ranges for each selectable output voltage.

Table 101: DC/DC Output Voltage Selection

Input Voltage, 1.5 MHz	Input Voltage, 2.0 MHz	Output Voltage
2.5 V to 5.5 V	2.5 V to 5.5 V	1.2 V
2.5 V to 5.5 V	2.5 V to 5.5 V	1.5 V
2.5 V to 5.5 V	2.5 V to 5.5 V	1.8 V
3.125 V to 5.5 V	3.33 V to 5.5 V	2.5 V
3.75 V to 5.5 V	4.0 V to 5.5 V	3.0 V
4.125 V to 5.5 V	4.4 V to 5.5 V	3.3 V

21.7 SWITCHING FREQUENCY SELECTION

The Synchronous DC/DC Step Down Converter macrocell supports two user selectable output switching frequencies 1.5 MHz and 2 MHz. Register bits registers [1876:1875] control frequency selection.

The Switching Frequency Selection affects the allowable input voltage range for each selectable output voltage. Refer to the Table 101.

21.8 OVER-CURRENT PROTECTION LEVEL SELECTION

The Synchronous DC/DC Step Down Converter macrocell supports two user selectable current levels for the internal Over-Current Protection circuitry. Register bits registers [1874:1873] control current level selection, see Table 100. The Over Current Protection selections are dividers of the first register selection 00. So each subsequent selection is a ratio of the first current selection.

The Synchronous DC/DC Step Down Converter macrocell senses the current when the high-side MOSFET is on. If an over-current condition occurs, i.e. the inductor current is higher than the user selected level between 2.0 A or 2.5 A (current limit), the high-side MOSFET turns off for 2 µs, and the INT/pin will become active. Then the high-side MOSFET turns on again if VOUT is lower than the user set voltage. If the inductor current is still higher than the current limit, the high-side MOSFET turns off again. This process will repeat.

The converter has an INT pin which becomes active if an over-current condition occurs. User can feed this INT signal into an input pin of the PAK, and then the PAK processes the signal and turn on/off the buck converter. For example, the PAK counts 8 INT pulses continuously, and then sends an “off” signal to the buck and turns it off. After a 1ms pause (off-time), the PAK sends an “on” signal to the buck and turns it on. This is one of many possible solutions how the OCP hiccup handling can be implemented. Please refer to an application note for more details.

21.9 DC/DC THERMAL SHUTDOWN

The Thermal Limit is set at 125 °C with a 25 °C hysteresis. The device must cool down to 100 °C before attempting to restart. During thermal shutdown, the converter operation is disabled. The Buck can self-recover without toggling the Enable.

21.10 DC/DC UNDER VOLTAGE LOCKOUT

The Under Voltage Lockout is used to protect the converter from operating at an insufficient voltage. When the VIN is High enough to reach the UVLO High threshold voltage, the converter will soft start to the selected output voltage if the ON/OFF command is already High or transitions from Low to High. When the VIN decreases to its Low threshold voltage, the converter shuts down.

21.11 FAULT SIGNALS

The Fault Matrix Connection is an active High signal and signifies when there is a UVLO or a Thermal Shutdown. The output will shut off. The DC/DC Buck Converter has a self-recovery capability. In UVLO, the device will recover if the DC_VIN satisfies the UVLO condition. In Thermal Shutdown, the device will recover if the temperature drops below the hysteresis value.

The DC_INT is an active High signal and signifies when there is an Over Current Protection event. The DC/DC Buck Converter will need to be powered off and then powered back on through the ON/OFF signal in order to recover from the Over-Current event.

Table 102: DC/DC Output Voltage Selection

Fault	Fault Matrix Connection	DC_INT
UVLO	Yes	--
OCP	--	Yes
TS	Yes	--

21.12 DC/DC SOFT START

The DC/DC Soft Start begins after Under Voltage Lockout is satisfied and the Enable is toggled from Low to High. The time between Enable and Soft Start will vary based on how fast the bandgap is able to rise. Once the bandgap is settled, the Converter will enter the soft start sequence. In the soft-start sequence, the ramp time is 0.5 ms.

Any DC/DC Step Down Converter comparator outputs are ignored during the soft-start sequence. After soft-start ends, the output is compared internally to the reference.

If the device enters Over Current Protection, there is a minimum Over Current Protection discharge period before which the device will begin soft-start again. If the load is not released, the current in the inductor will build and the process repeats.

21.13 CONSTANT-ON-TIME

The constant-on-time control topology (COT) provides fast transient response and makes loop stabilization easier. Fault condition protection includes current limiting and thermal shutdown. An Open-Drain INT output signals the host when an over-current

condition is detected and an Open-Drain CCM output signals the host when the converter operates in full continuous conduction mode. The typical application circuit requires a minimum number of readily-available standard external components.

21.14 DC/DC CONTINUOUS CONDUCTION MODE (CCM)

The DC/DC Step Down Converter automatically switches into CCM when the regulating current exceeds the maximum deliverable current in DCM Mode. In Continuous Conduction Mode, the current through the inductor may reach zero for a while before charging again.

In this mode, the DC_CCM pin will be asserted.

21.15 DC/DC DISCONTINUOUS CONDUCTION MODE (DCM)

The DC/DC Step Down Converter automatically switches into DCM when the regulating current is below the minimum deliverable current in CCM Mode. In Discontinuous Conduction Mode, the current through the inductor may reach zero for a while before charging again.

21.16 DC/DC POWER DISSIPATION

Power Dissipation is estimated by the use of the efficiency chart for the buck.

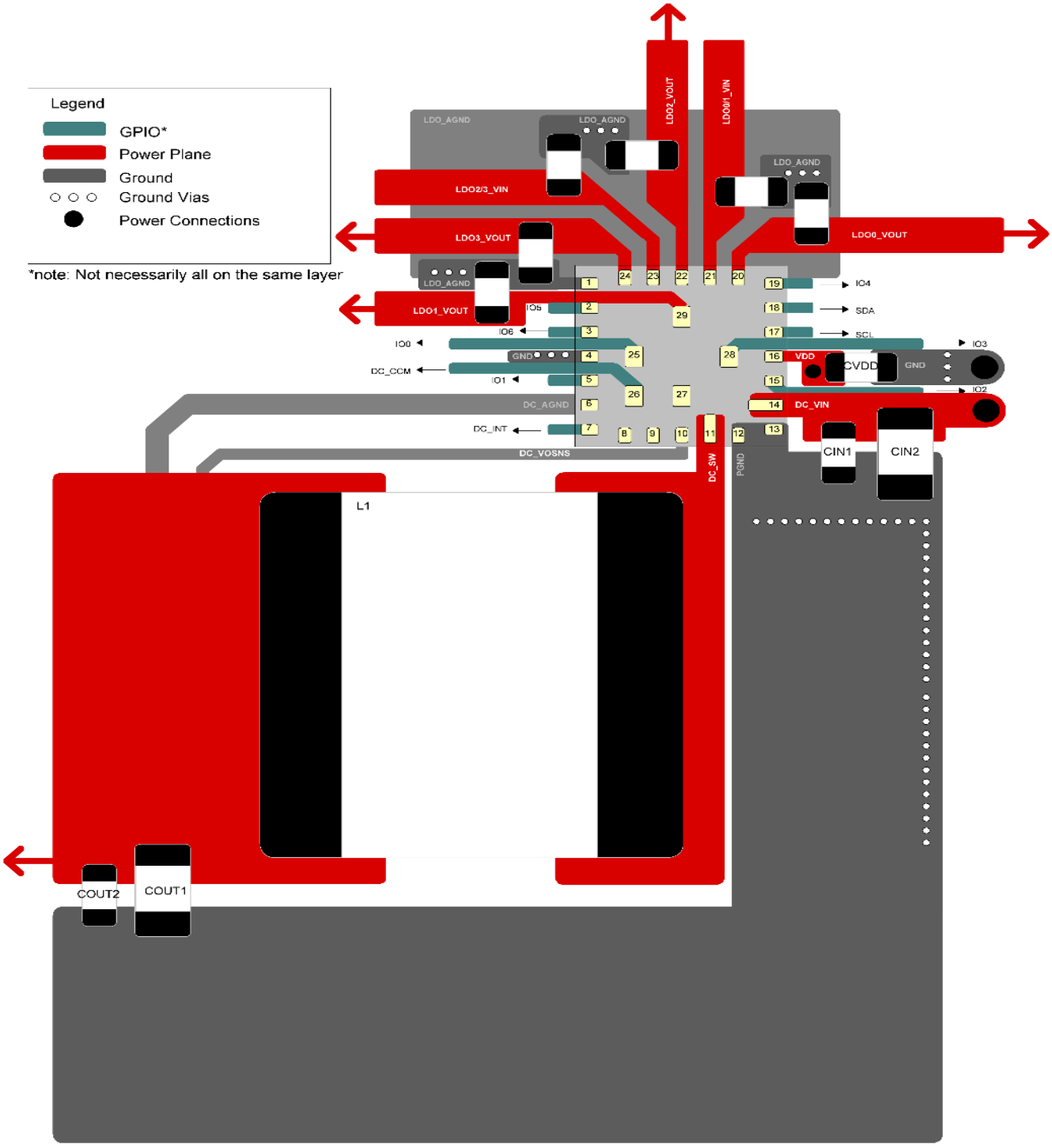


Figure 107: DC/DC Recommended PCB Layout

21.17 LAYOUT CONSIDERATION

Layout is important to avoid instability and noise coupling which can lead to system failures. DC/DC Converters are highly susceptible to instability and noise generated by high-current paths. At higher currents, both the DC/DC Converter and LDO are susceptible to thermal self-heating. Proper layout will mitigate, suppress and avoid these undesirable artifacts.

21.17.1 Current Loops

Determine the path of current through the DC/DC Converter and the LDO. Blue is the path of current through the power stage when the PMOS is enabled. Red is the path of current through the power stage when the NMOS is enabled. Green is the path of current through the LDO is enabled. The path of current for the Push-Pull digital signals are supplied by V_{DD}. Keep the digital logic bypass capacitor close by (labeled C_{VDD}).

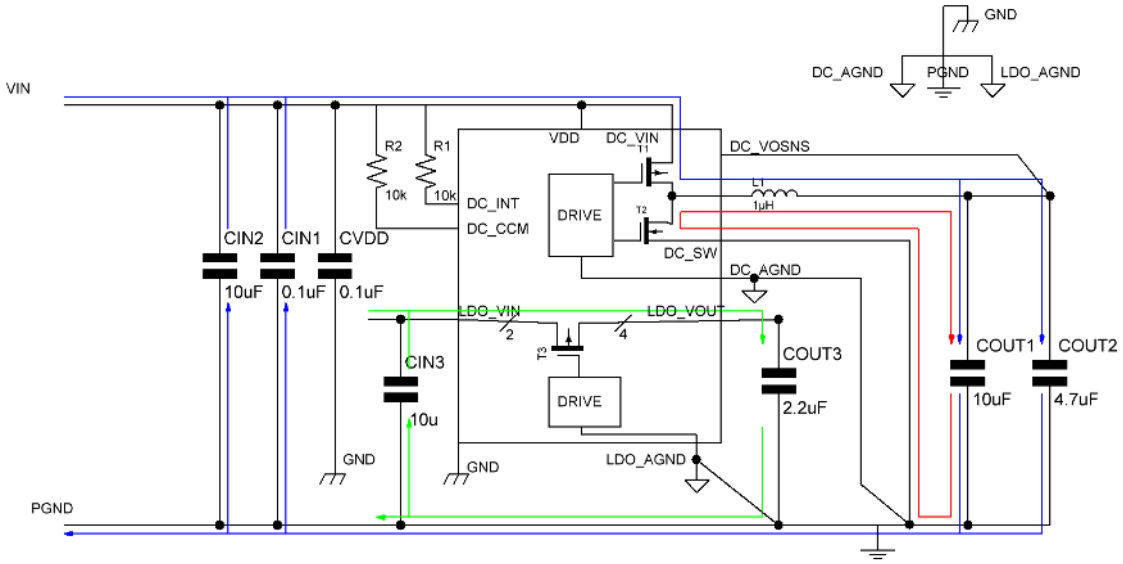


Figure 108: DC/DC Converter Current Loops

21.17.2 AC vs DC

The blue and red lines are both AC because of the switching DC DC converter. While the upper FET is On, current flows along the blue line. When the lower FET is On the current flows along the red line. The inductor prevents instantaneous changes in current and therefore the red/blue path through the inductor and output capacitors are DC. The green LDO path is always DC since there is no switching element.

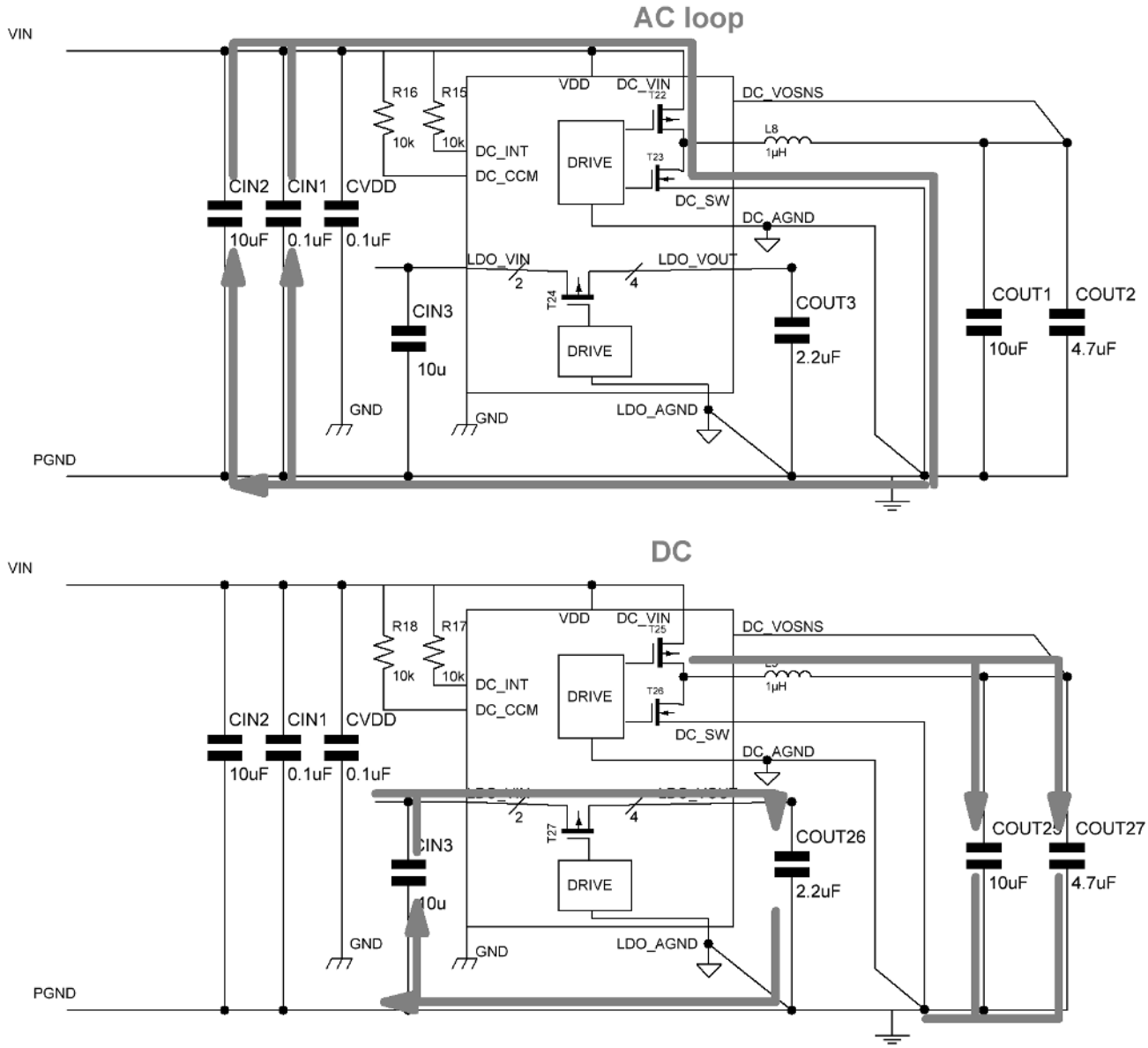


Figure 109: DC/DC Converter AC and DC Loops

21.17.3 DC/DC Converter

- AC Loop
  Place the bypass capacitor CIN1 close to Vin and PGND to reduce EMI and voltage spikes caused by V = Ldi/dt. Place vias near the capacitors to direct the current flow and ease thermal radiation.

- DC_SW and Inductor

  Rotate the inductor so that the SW node is turned away from the chip in order not to disrupt any other signals and the output capacitors are farthest from the AC Loop. Keep the DC_SW trace small in size, do not make the trace larger than it needs to be. Keep inductor terminals and other traces separated to avoid coupling noise through stray capacitance.

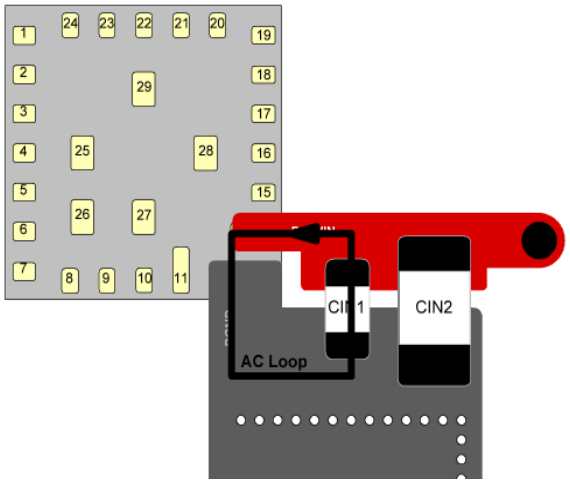


Figure 110: AC Loop

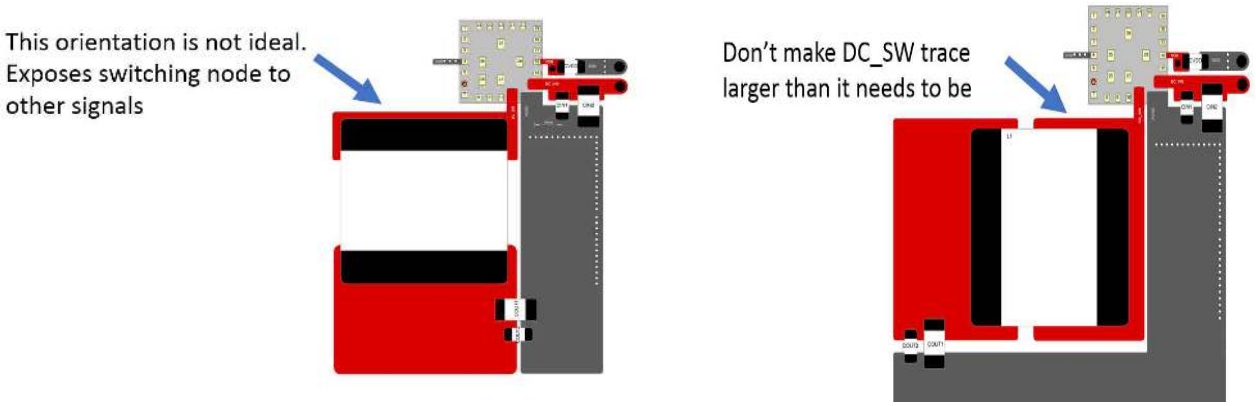


Figure 111: DC Switch and Inductor

- DC_VOSNS and DC_AGND

  DC_VOSNS taps the VOUT close to the output. Place this tap point at the output. DC_AGND should be similarly tapped at the output ground side. The purpose of these signals is for feedback loop and to generate a voltage reference. They are not intended for large current flow.

- DC_VIN, DC_SW and PGND

  Due to the MSTQFN-29 package pitch size, the thermal bottlenecks occur at the pin leads. The Buck current limit is based on the over-current selection. The width of the DC_SW and DC_VIN trace should be wide enough to avoid too much heating. General rule of thumb is to allow 2 mm per 1 A. PGND should be fairly large, flat and as continuous as possible. Preferably it should have a dedicated ground plane for the PGND and place bias to connect to the common GND.

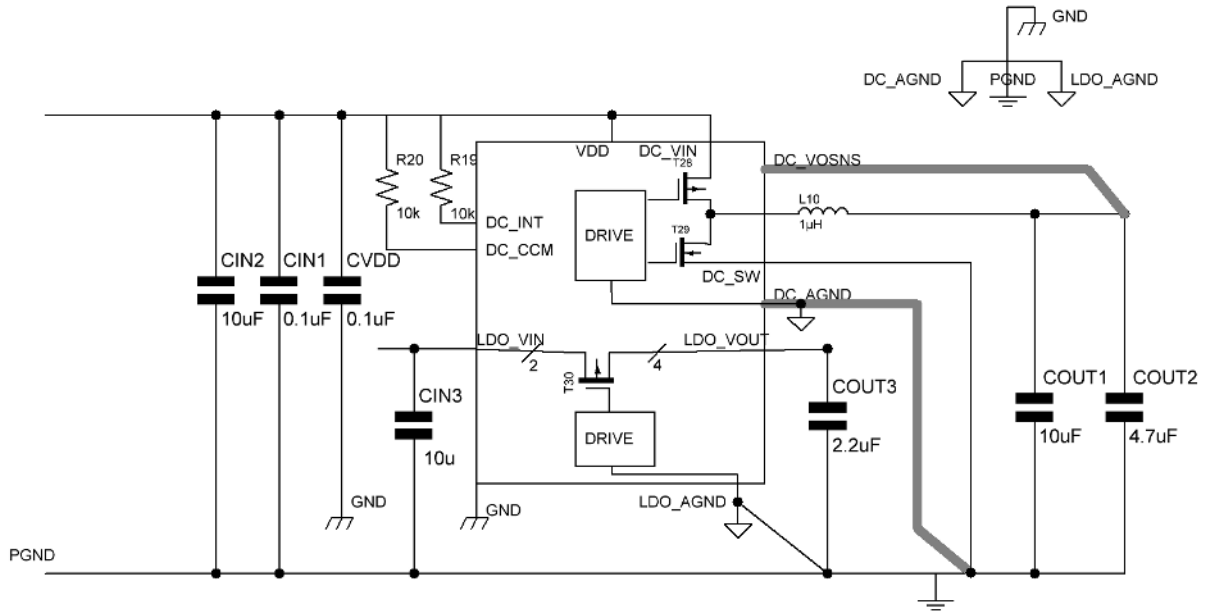


Figure 112: DC Switch and Inductor

21.17.4 DC/DC Converter

- LDO_VIN and LDO_VOUT
  For best performance, place input and output capacitors as close as possible. The smaller the capacitor size, the lower the voltage rating, but also the lower ESR.

- LDO Stability
  SLG46585 LDO requires very small inductance loops to guarantee stability. The total maximum inductance allowed is 5 nH (including packaging). Outside the packaging, the total maximum inductance is 2 nH. This equates to 3 mm. The entire LDO loop from LDO_VOUT to LDO_AGND should be no greater than 3 mm. Taking this into consideration, the LDO1_VOUT should be pulled out to the side closest to the LDO_AGND to minimize inductance.

- LDO_AGND
  Use another layer and multiple vias to connect all the LDO_AGNDs together. LDO_AGND needs to be wide to help dissipate the heat from the LDOs.

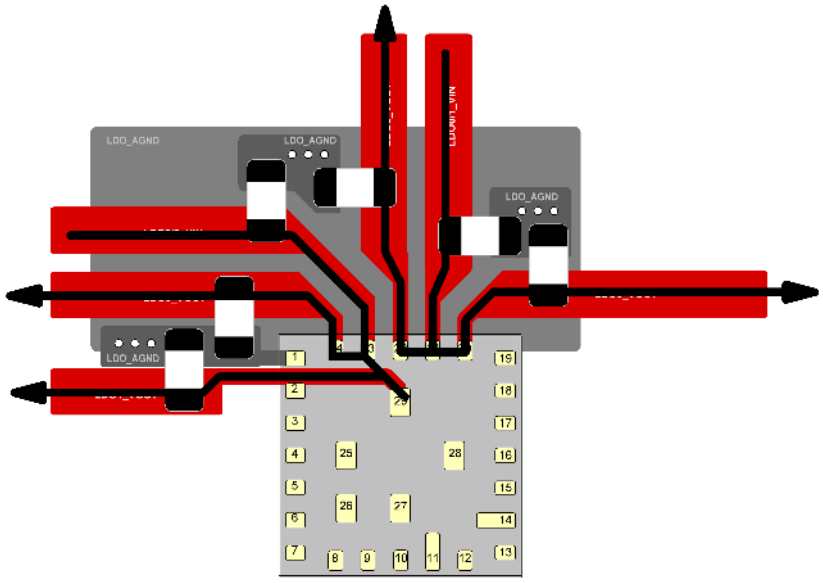


Figure 113: LDO_VIN and LDO_VOUT Current Flow

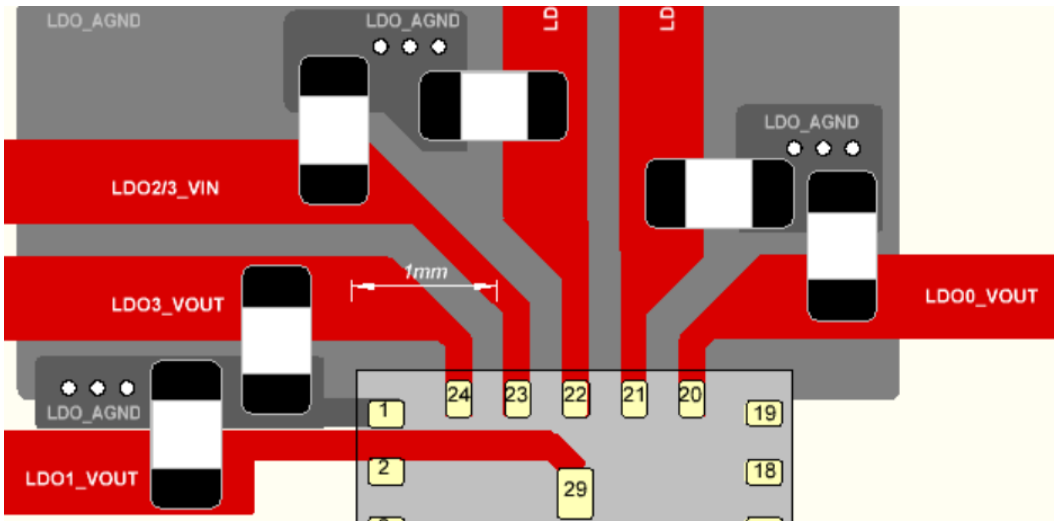


Figure 114: LDO Decoupling

Figure 115: LDO_AGND Layout

21.17.5 Digital

- C_{VDD}
  V_{DD} and GND power the digital side of the SLG46585. C_{VDD} is the bypass capacitor (value 0.1 µF). The GND and V_{DD} are on opposite ends of the chip. Use a layer underneath to connect the GND pin to the ground on C_{VDD}, which is placed as close as possible to V_{DD} pin

- Ground Source
  The Black Circle is the recommended location for connecting ground. It is in the middle, between the LDO and Buck. This is called star grounding. When the ground source is placed in a central location, the current comes out like a star keeping the ground currents going to the LDO and the Buck separated.

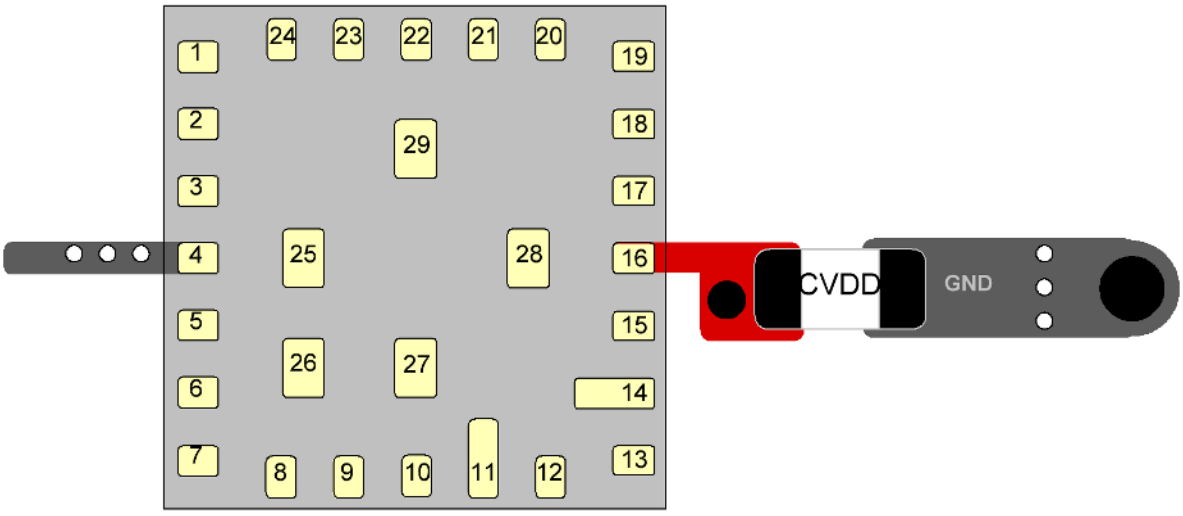


Figure 116: Ground Source for LDO and Buck

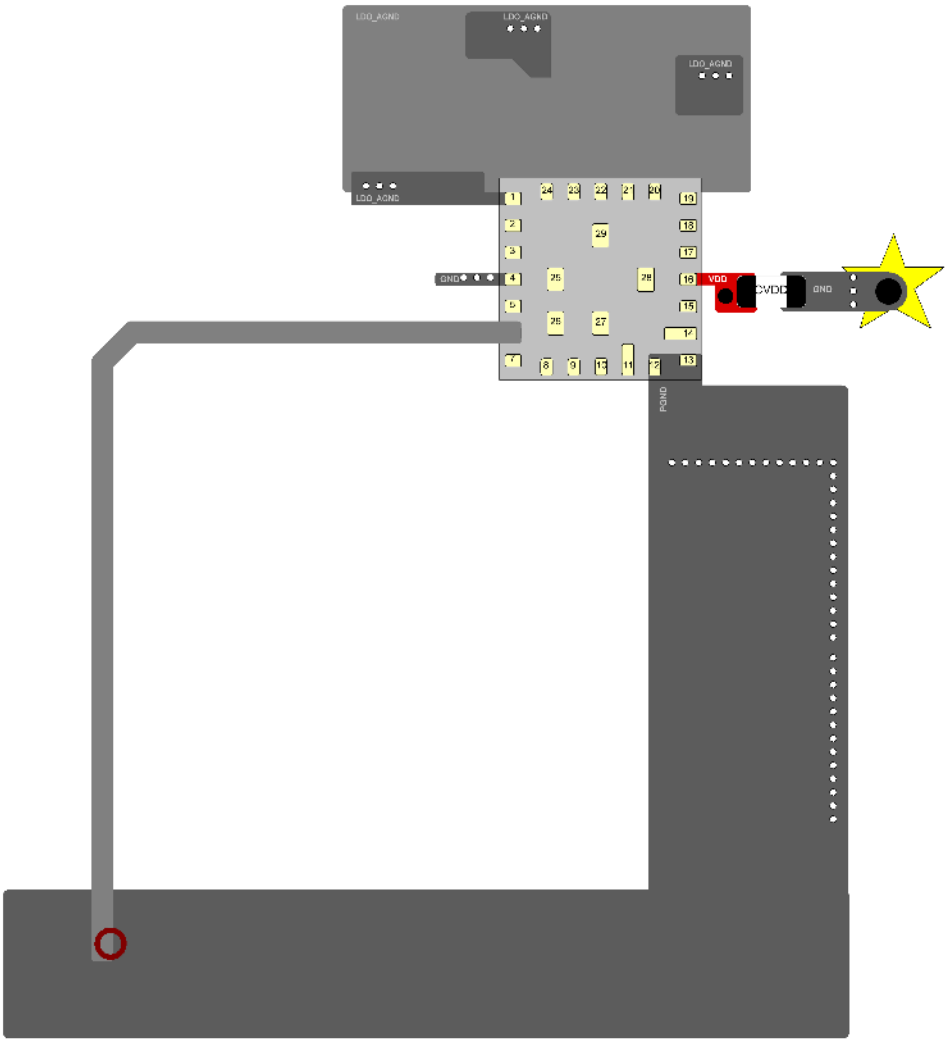


Figure 117: SLG46585 Ground Layout

- Digital Signals
  Shown in Teal, the digital signals should be wired on a separate routing layer. Since this device is in an MSP Package, a multi-layer layout is unavoidable if all pins are sued. The Pull-up resistors are not shown on DC_INT and DC_CCM to signal faults and CCM mode.

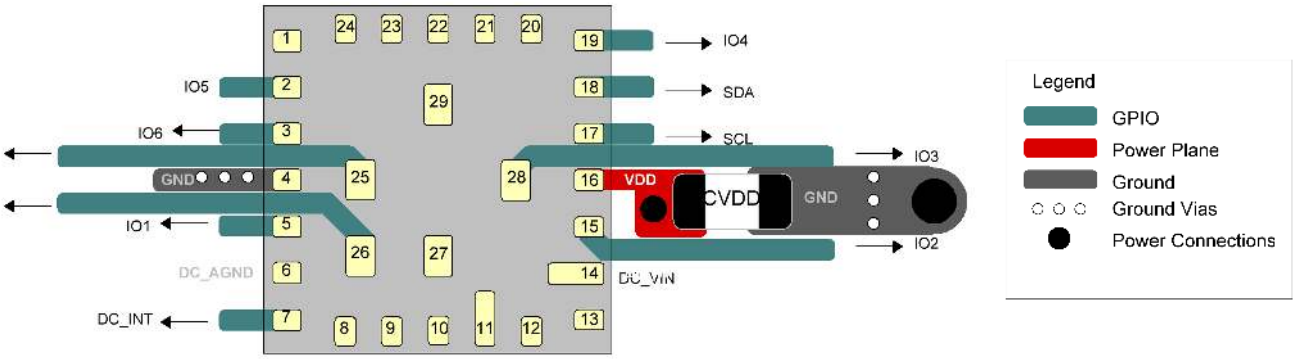


Figure 118: Digital Signals PCB Recommendation

21.18 TYPICAL PERFORMANCE CHARACTERISTICS

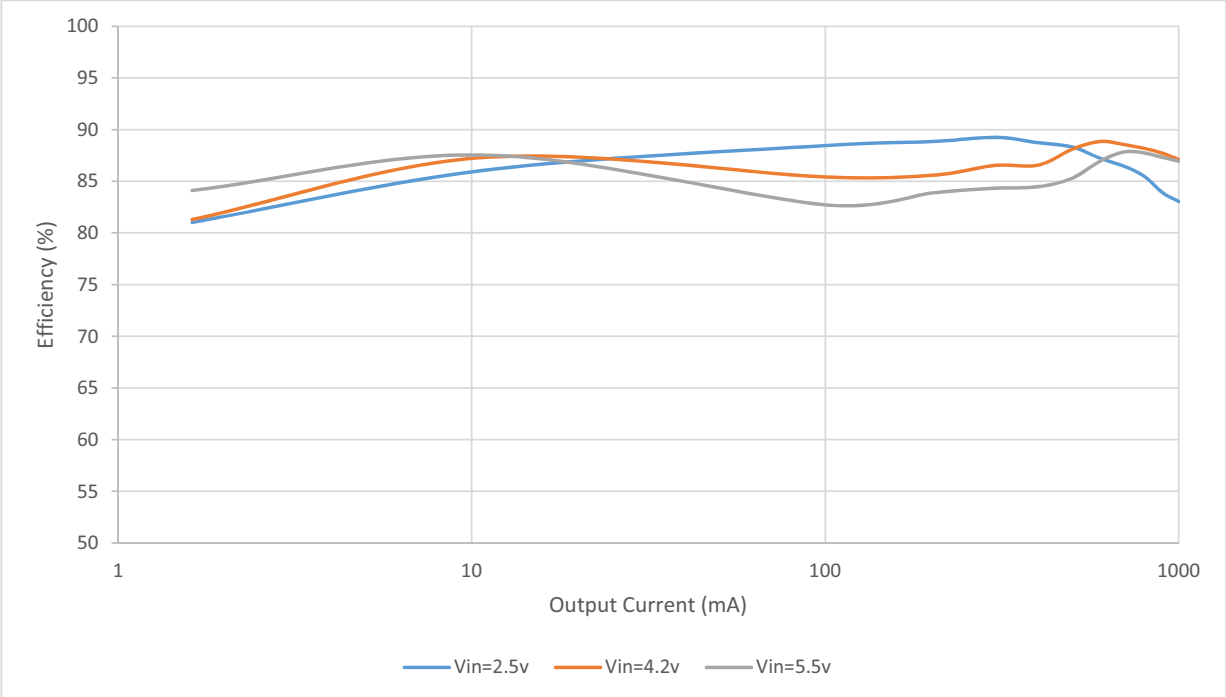


Figure 119: Efficiency vs. Output Current

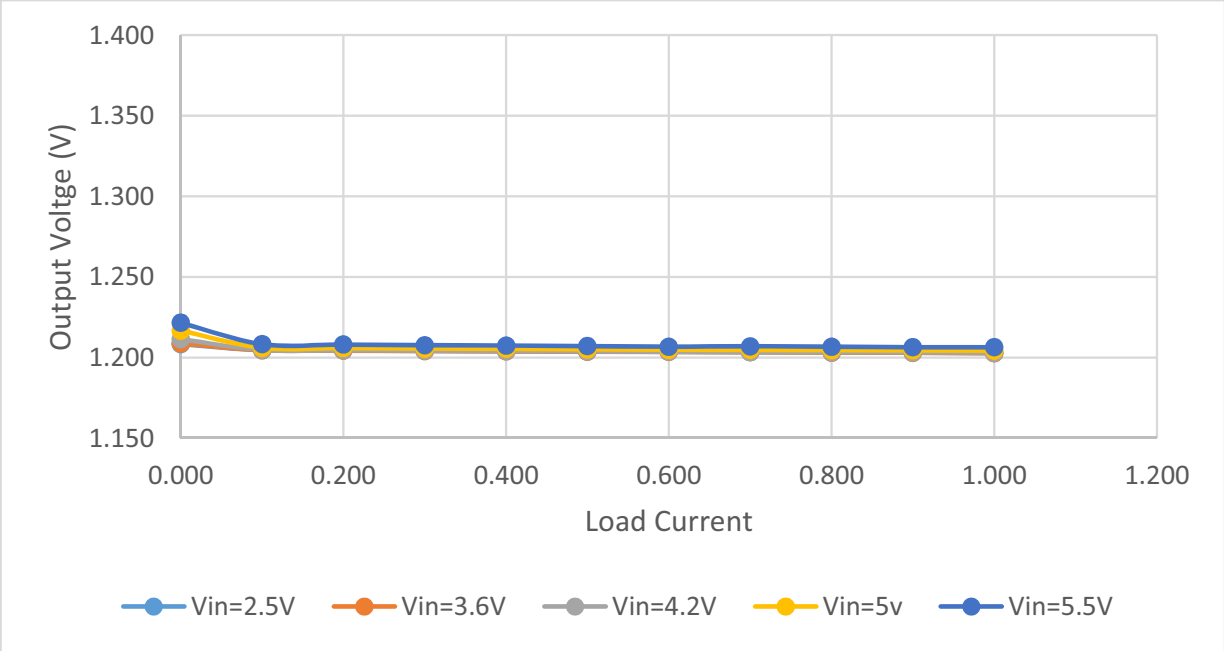


Figure 120: Output Voltage vs. Load Current

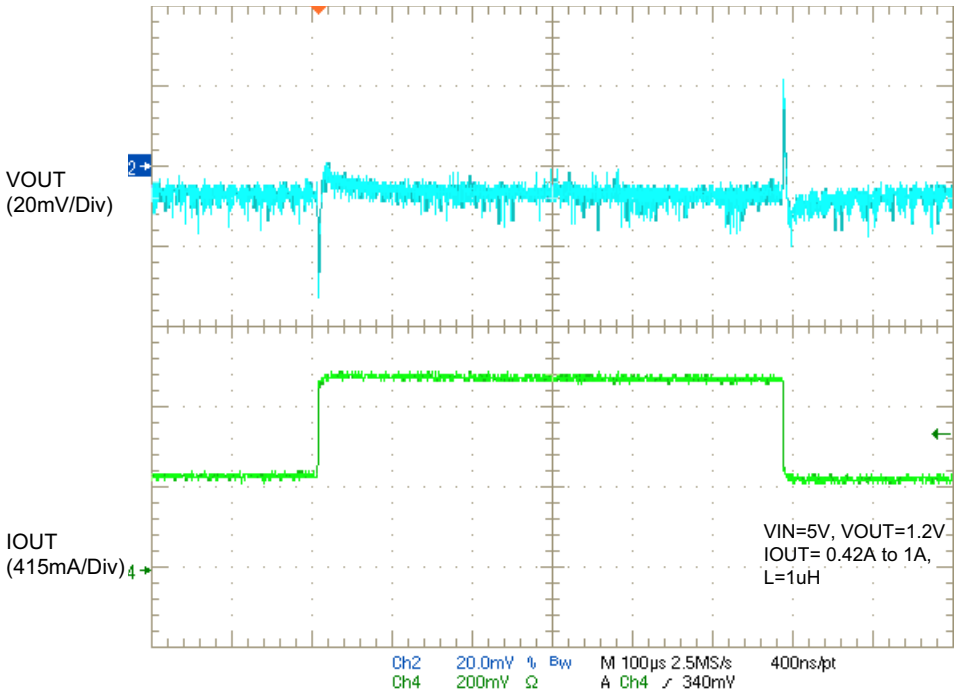


Figure 121: Load Transient Response

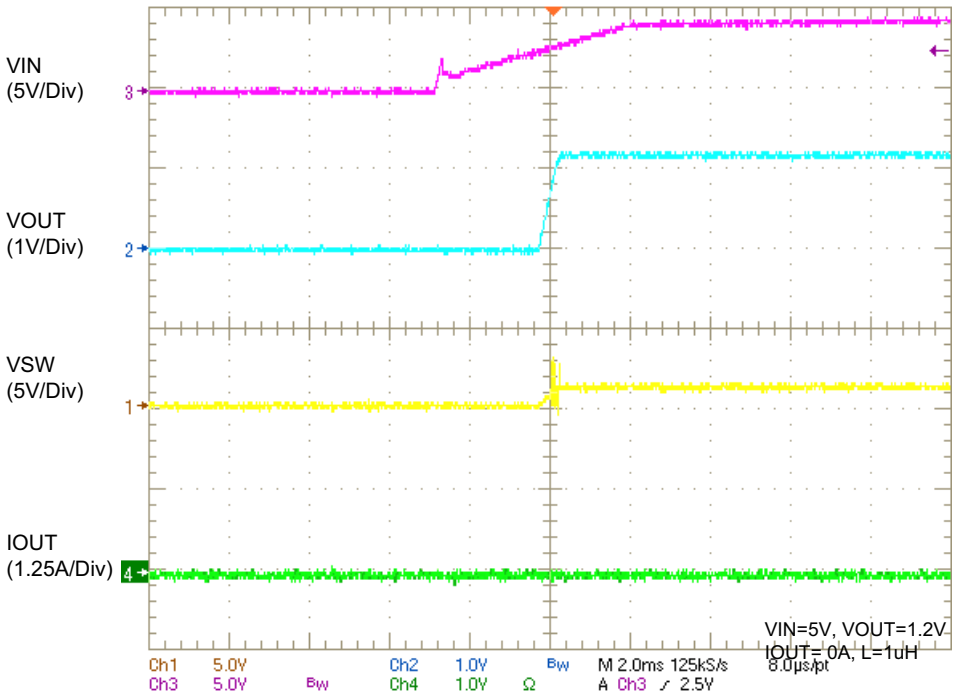


Figure 122: VIN Power Up without Load

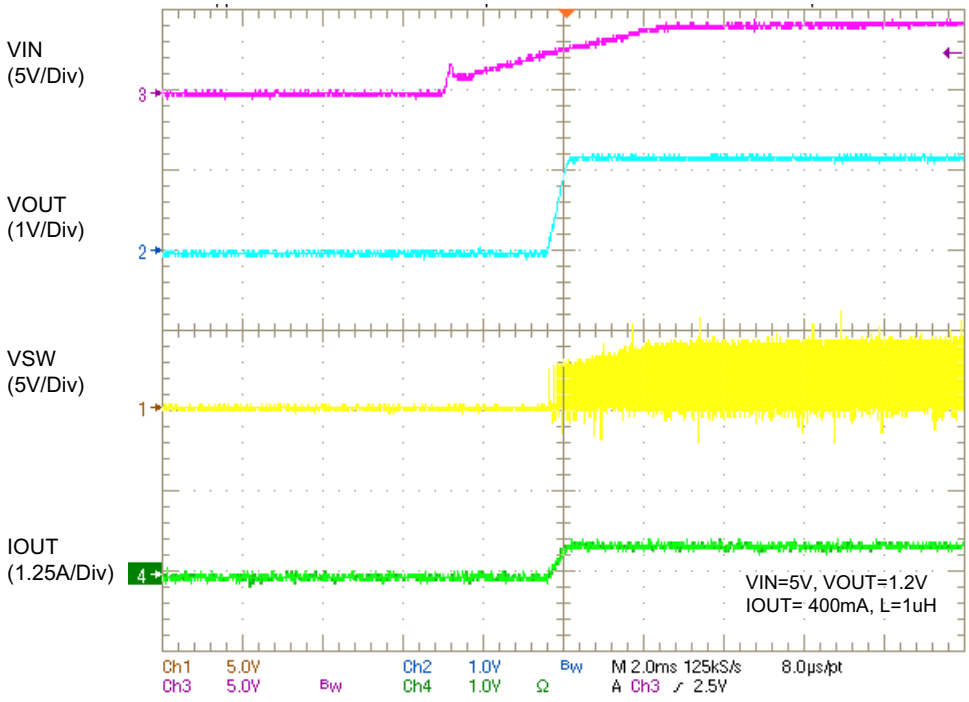


Figure 123: VIN Power Up with 400 mA Load

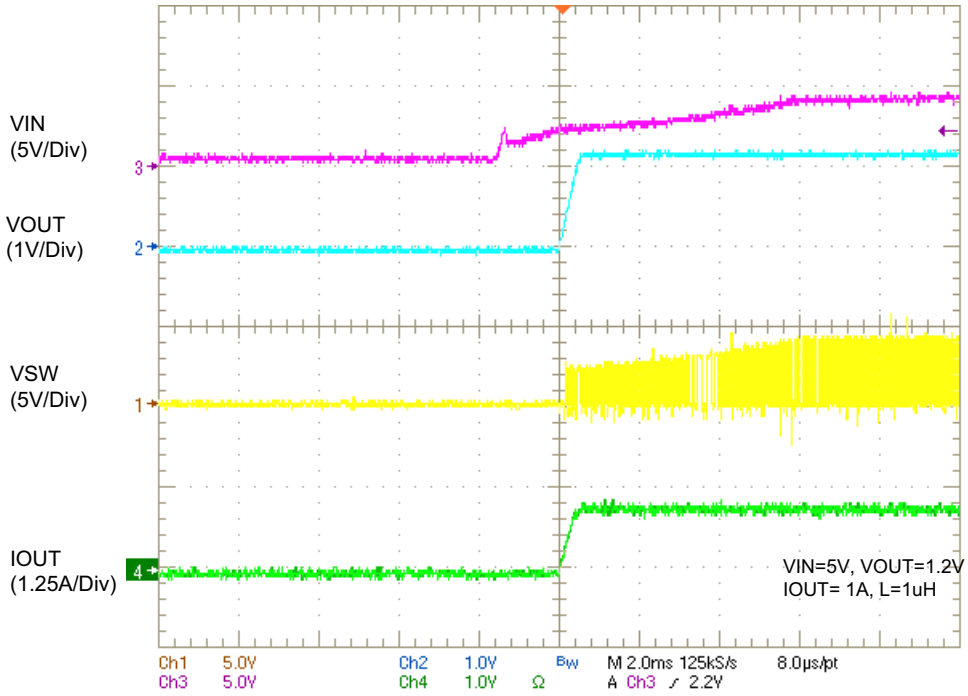


Figure 124: VIN Power Up with 1A Load

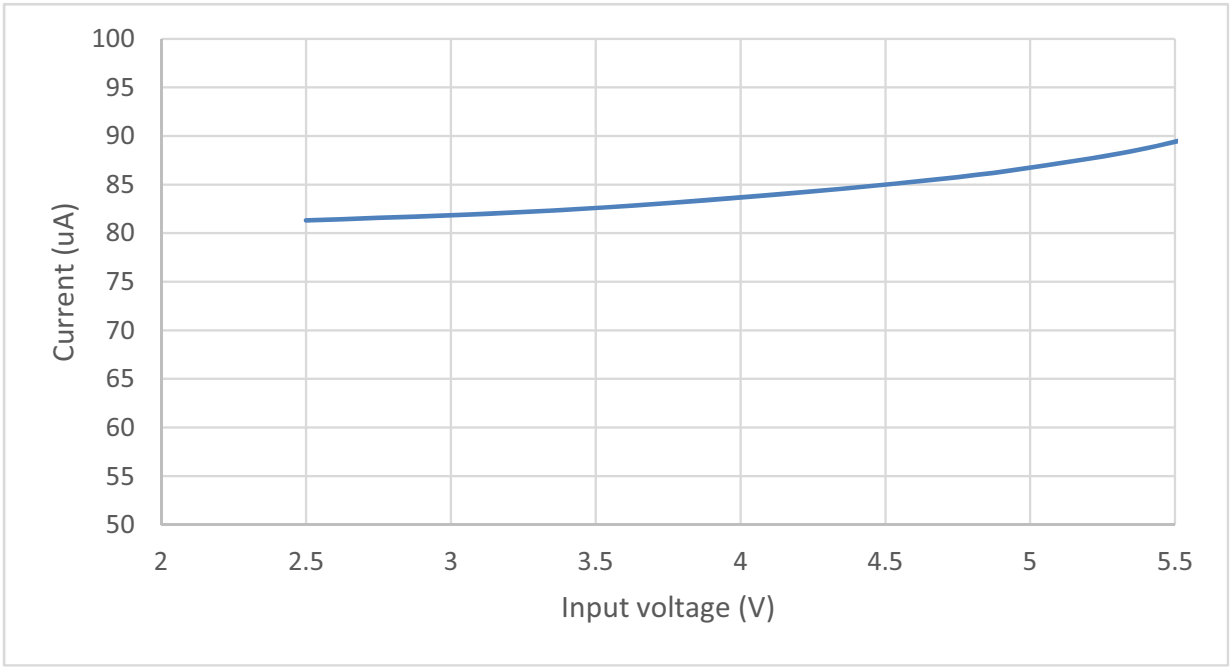


Figure 125: Low IQ Current vs. Input Voltage

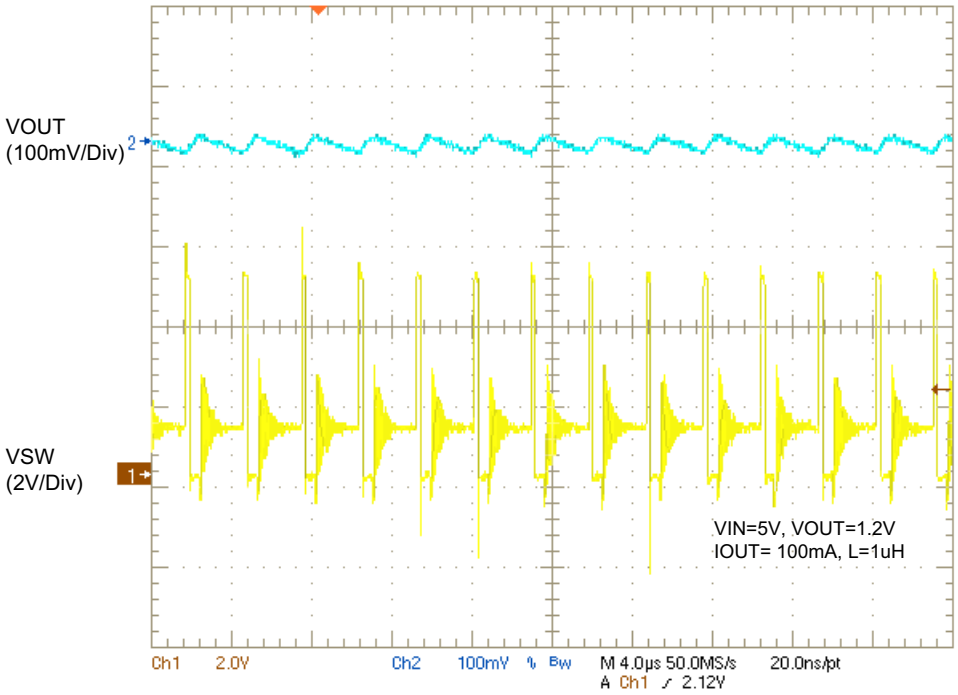


Figure 126: Output Ripple vs. IOUT = 100 mA

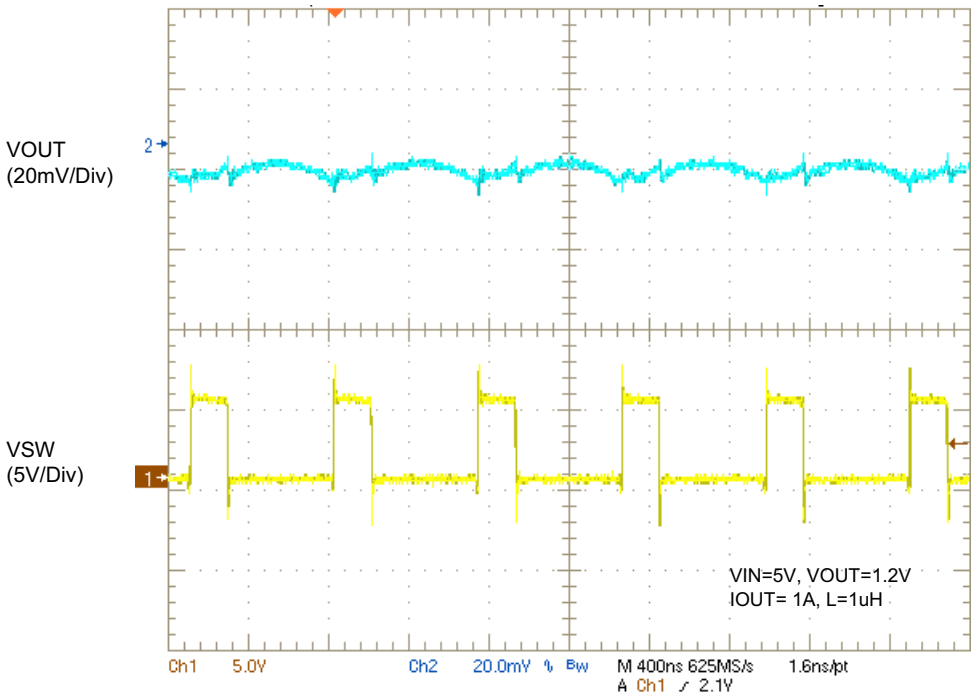


Figure 127: Output Ripple vs. IOUT = 1 A

22 Register Definitions

22.1 REGISTER MAP

Table 103: Register Map

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
Note: For register [0] to register [1495], I²C Read is valid (assuming register [1832] = 0), I²C Write is valid (assuming register [1871] = 0)				
Matrix Output				
5:0	Matrix OUT: ASM-state0-EN0		Valid	Valid
7:6	Reserved		Valid	Valid
13:8	Matrix OUT: ASM-state0-EN1		Valid	Valid
15:14	Reserved		Valid	Valid
21:16	Matrix OUT: ASM-state0-EN2		Valid	Valid
23:22	Reserved		Valid	Valid
29:24	Matrix OUT: ASM-state1-EN0		Valid	Valid
31:30	Reserved		Valid	Valid
37:32	Matrix OUT: ASM-state1-EN1		Valid	Valid
39:38	Reserved		Valid	Valid
45:40	Matrix OUT: ASM-state1-EN2		Valid	Valid
47:46	Reserved		Valid	Valid
53:48	Matrix OUT: ASM-state2-EN0		Valid	Valid
55:54	Reserved		Valid	Valid
61:56	Matrix OUT: ASM-state2-EN1		Valid	Valid
63:62	Reserved		Valid	Valid
69:64	Matrix OUT: ASM-state2-EN2		Valid	Valid
71:70	Reserved		Valid	Valid
77:72	Matrix OUT: ASM-state3-EN0		Valid	Valid
79:78	Reserved		Valid	Valid
85:80	Matrix OUT: ASM-state3-EN1		Valid	Valid
87:86	Reserved		Valid	Valid
93:88	Matrix OUT: ASM-state3-EN2		Valid	Valid
95:94	Reserved		Valid	Valid
101:96	Matrix OUT: ASM-state4-EN0		Valid	Valid
103:102	Reserved		Valid	Valid
109:104	Matrix OUT: ASM-state4-EN1		Valid	Valid
111:110	Reserved		Valid	Valid
117:112	Matrix OUT: ASM-state4-EN2		Valid	Valid
119:118	Reserved		Valid	Valid
125:120	Matrix OUT: ASM-state5-EN0		Valid	Valid
127:126	Reserved		Valid	Valid
133:128	Matrix OUT: ASM-state5-EN1		Valid	Valid
135:134	Reserved		Valid	Valid
141:136	Matrix OUT: ASM-state5-EN2		Valid	Valid
143:142	Reserved		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
149:144	Matrix OUT: ASM-state6-EN0		Valid	Valid
151:150	Reserved		Valid	Valid
157:152	Matrix OUT: ASM-state6-EN1		Valid	Valid
159:158	Reserved		Valid	Valid
165:160	Matrix OUT: ASM-state6-EN2		Valid	Valid
167:166	Reserved		Valid	Valid
173:168	Matrix OUT: ASM-state7-EN0		Valid	Valid
175:174	Reserved		Valid	Valid
181:176	Matrix OUT: ASM-state7-EN1		Valid	Valid
183:182	Reserved		Valid	Valid
189:184	Matrix OUT: ASM-state7-EN2		Valid	Valid
191:190	Reserved		Valid	Valid
197:192	Matrix OUT: ASM-state-nRST		Valid	Valid
199:198	Reserved		Valid	Valid
205:200	Matrix OUT: IN0 of LUT3_6 or Delay0 Input (or Counter0 RST Input)		Valid	Valid
207:206	Reserved		Valid	Valid
213:208	Matrix OUT: IN1 of LUT3_6 or External Clock Input of Delay0 (or Counter0)		Valid	Valid
215:214	Reserved		Valid	Valid
221:216	Matrix OUT: IN2 of LUT3_6		Valid	Valid
223:222	Reserved		Valid	Valid
229:224	Matrix OUT: IN0 of LUT3_7 or Delay1 Input (or Counter1 RST Input)		Valid	Valid
231:230	Reserved		Valid	Valid
237:232	Matrix OUT: IN1 of LUT3_7 or External Clock Input of Delay1 (or Counter1)		Valid	Valid
239:238	Reserved		Valid	Valid
245:240	Matrix OUT: IN2 of LUT3_7		Valid	Valid
247:246	Reserved		Valid	Valid
253:248	Matrix OUT: IN0 of LUT3_8 or Delay2 Input (or Counter2 RST Input)		Valid	Valid
255:254	Reserved		Valid	Valid
261:256	Matrix OUT: IN1 of LUT3_8 or External Clock Input of Delay2 (or Counter2)		Valid	Valid
263:262	Reserved		Valid	Valid
269:264	Matrix OUT: IN2 of LUT3_8		Valid	Valid
271:270	Reserved		Valid	Valid
277:272	Matrix OUT: IN0 of LUT3_9 or Delay3 Input (or Counter3 RST Input)		Valid	Valid
279:278	Reserved		Valid	Valid
285:280	Matrix OUT: IN1 of LUT3_9 or External Clock Input of Delay3 (or Counter3)		Valid	Valid
287:286	Reserved		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
293:288	Matrix OUT: IN2 of LUT3_9		Valid	Valid
295:294	Reserved		Valid	Valid
301:296	Matrix OUT: IN0 of LUT3_10 or Delay4 Input (or Counter4 RST Input)		Valid	Valid
303:302	Reserved		Valid	Valid
309:304	Matrix OUT: IN1 of LUT3_10 or External Clock Input of Delay4 (or Counter4)		Valid	Valid
311:310	Reserved		Valid	Valid
317:312	Matrix OUT: IN2 of LUT3_10		Valid	Valid
319:318	Reserved		Valid	Valid
325:320	Matrix OUT: IO0 Digital Output Source		Valid	Valid
327:326	Reserved		Valid	Valid
333:328	Matrix OUT: IO0 Output Enable		Valid	Valid
335:334	Reserved		Valid	Valid
341:336	Matrix OUT: IO1 Digital Output Source		Valid	Valid
343:342	Reserved		Valid	Valid
349:344	Reserved		Valid	Valid
351:350	Reserved		Valid	Valid
357:352	Reserved		Valid	Valid
359:358	Reserved		Valid	Valid
365:360	Matrix OUT: IO2 Digital Output Source		Valid	Valid
367:366	Reserved		Valid	Valid
373:368	Matrix OUT: IO2 Output Enable		Valid	Valid
375:374	Reserved		Valid	Valid
381:376	Matrix OUT: IO4 Digital Output Source		Valid	Valid
383:382	Reserved		Valid	Valid
389:384	Matrix OUT: IO4 Output Enable		Valid	Valid
391:390	Reserved		Valid	Valid
397:392	Matrix OUT: IO5 Digital Output Source		Valid	Valid
399:398	Reserved		Valid	Valid
405:400	Matrix OUT: IO6 Digital Output Source		Valid	Valid
407:406	Reserved		Valid	Valid
413:408	Matrix OUT: IO6 Output Enable		Valid	Valid
415:414	Reserved		Valid	Valid
421:416	Matrix OUT: ACMP0 PWR UP		Valid	Valid
423:422	Reserved		Valid	Valid
429:424	Matrix OUT: ACMP1 PWR UP		Valid	Valid
431:430	Reserved		Valid	Valid
437:432	Matrix OUT: ACMP2 PWR UP		Valid	Valid
439:438	Reserved		Valid	Valid
445:440	Matrix OUT: ACMP3 PWR UP		Valid	Valid
447:446	Reserved		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
453:448	Matrix OUT: Input of Filter_0 with fixed time edge detector		Valid	Valid
455:454	Reserved		Valid	Valid
461:456	Matrix OUT: Input of Filter_1 with fixed time edge detector		Valid	Valid
463:462	Reserved		Valid	Valid
469:464	Matrix OUT: Input of Programmable Delay & Edge Detector		Valid	Valid
471:470	Reserved		Valid	Valid
477:472	Matrix OUT: OSC 25kHz/2MHz PD (Power-Down)		Valid	Valid
479:478	Reserved		Valid	Valid
485:480	Matrix OUT: LPOSC PD (Power-Down)		Valid	Valid
487:486	Reserved		Valid	Valid
493:488	Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0		Valid	Valid
495:494	Reserved		Valid	Valid
501:496	Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0		Valid	Valid
503:502	Reserved		Valid	Valid
509:504	Matrix OUT: IN0 of LUT2_1 or Clock Input of DFF1		Valid	Valid
511:510	Reserved		Valid	Valid
517:512	Matrix OUT: IN1 of LUT2_1 or Data Input of DFF1		Valid	Valid
519:518	Reserved		Valid	Valid
525:520	Matrix OUT: IN0 of LUT2_2 or Clock Input of DFF2		Valid	Valid
527:526	Reserved		Valid	Valid
533:528	Matrix OUT: IN1 of LUT2_2 or Data Input of DFF2		Valid	Valid
535:534	Reserved		Valid	Valid
541:536	Matrix OUT: IN0 of LUT3_0 or Clock Input of DFF3		Valid	Valid
543:542	Reserved		Valid	Valid
549:544	Matrix OUT: IN1 of LUT3_0 or Data Input of DFF3		Valid	Valid
551:550	Reserved		Valid	Valid
557:552	Matrix OUT: IN2 of LUT3_0 or nRST (nSET) of DFF3		Valid	Valid
559:558	Reserved		Valid	Valid
565:560	Matrix OUT: IN0 of LUT3_1 or Clock Input of DFF4		Valid	Valid
567:566	Reserved		Valid	Valid
573:568	Matrix OUT: IN1 of LUT3_1 or Data Input of DFF4		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
575:574	Reserved		Valid	Valid
581:576	Matrix OUT: IN2 of LUT3_1 or nRST (nSET) of DFF4		Valid	Valid
583:582	Reserved		Valid	Valid
589:584	Matrix OUT: IN0 of LUT3_2 or Clock Input of DFF5		Valid	Valid
591:590	Reserved		Valid	Valid
597:592	Matrix OUT: IN1 of LUT3_2 or Data Input of DFF5		Valid	Valid
599:598	Reserved		Valid	Valid
605:600	Matrix OUT: IN2 of LUT3_2 or nRST (nSET) of DFF5		Valid	Valid
607:606	Reserved		Valid	Valid
613:608	Matrix OUT: IN0 of LUT3_3 or Clock Input of DFF6		Valid	Valid
615:614	Reserved		Valid	Valid
621:616	Matrix OUT: IN1 of LUT3_3 or Data Input of DFF6		Valid	Valid
623:622	Reserved		Valid	Valid
629:624	Matrix OUT: IN2 of LUT3_3 or nRST (nSET) of DFF6		Valid	Valid
631:630	Reserved		Valid	Valid
637:632	Matrix OUT: IN0 of LUT3_4 or Clock Input of DFF7		Valid	Valid
639:638	Reserved		Valid	Valid
645:640	Matrix OUT: IN1 of LUT3_4 or Data Input of DFF7		Valid	Valid
647:646	Reserved		Valid	Valid
653:648	Matrix OUT: IN2 of LUT3_4 or nRST (nSET) of DFF7		Valid	Valid
655:654	Reserved		Valid	Valid
661:656	Matrix OUT: IN0 of LUT3_11 or Input of Pipe Delay or Up/Down selection of Ripple Counter		Valid	Valid
663:662	Reserved		Valid	Valid
669:664	Matrix OUT: IN1 of LUT3_11 or nRST of Pipe Delay or nRST of Ripple Counter		Valid	Valid
671:670	Reserved		Valid	Valid
677:672	Matrix OUT: IN2 of LUT3_11 or Clock of Pipe Delay or Clock of Ripple Counter		Valid	Valid
679:678	Reserved		Valid	Valid
685:680	Matrix OUT: IN0 of LUT3_5 or Clock Input of DFF8		Valid	Valid
687:686	Reserved		Valid	Valid
693:688	Matrix OUT: IN1 of LUT3_5 or Data Input of DFF8		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
695:694	Reserved		Valid	Valid
701:696	Matrix OUT: IN2 of LUT3_5 or nRST (nSET) of DFF8		Valid	Valid
703:702	Reserved		Valid	Valid
709:704	Matrix OUT: IN0 of LUT4x2_0		Valid	Valid
711:710	Reserved		Valid	Valid
717:712	Matrix OUT: IN1 of LUT4x2_0		Valid	Valid
719:718	Reserved		Valid	Valid
725:720	Matrix OUT: IN2 of LUT4x2_0		Valid	Valid
727:726	Reserved		Valid	Valid
733:728	Matrix OUT: IN3 of LUT4x2_0		Valid	Valid
735:734	Reserved		Valid	Valid
741:736	Matrix OUT: LDO MODE1 Enable for LDO0/1/2/3		Valid	Valid
743:742	Reserved		Valid	Valid
749:744	Matrix OUT: LDO0_EN		Valid	Valid
751:750	Reserved		Valid	Valid
757:752	Matrix OUT: LDO1_EN		Valid	Valid
759:758	Reserved		Valid	Valid
765:760	Matrix OUT: LDO2_EN		Valid	Valid
767:766	Reserved		Valid	Valid
773:768	Matrix OUT: LDO3_EN		Valid	Valid
775:774	Reserved		Valid	Valid
781:776	Matrix OUT: LDO0 2nd VOUT Selection Enable		Valid	Valid
783:782	Reserved		Valid	Valid
789:784	Matrix OUT: LDO1 2nd VOUT Selection Enable		Valid	Valid
791:790	Reserved		Valid	Valid
797:792	Matrix OUT: LDO2 2nd VOUT Selection Enable		Valid	Valid
799:798	Reserved		Valid	Valid
805:800	Matrix OUT: LDO3 2nd VOUT Selection Enable		Valid	Valid
807:806	Reserved		Valid	Valid
813:808	Matrix OUT: RTC Clock		Valid	Valid
815:814	Reserved		Valid	Valid
821:816	Matrix OUT: RTC Trigger signal to read/write RTC CNT values		Valid	Valid
823:822	Reserved		Valid	Valid
829:824	Matrix OUT: ON/OFF command for Synchronous DC/DC Step Down Converter		Valid	Valid
831:830	Reserved		Valid	Valid
837:832	Matrix OUT: Reserved		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
839:838	Reserved		Valid	Valid
845:840	Matrix OUT: Reserved		Valid	Valid
847:846	Reserved		Valid	Valid
853:848	Matrix OUT: Reserved		Valid	Valid
855:854	Reserved		Valid	Valid
861:856	Matrix OUT: Reserved		Valid	Valid
863:862	Reserved		Valid	Valid
869:864	Matrix OUT: Reserved		Valid	Valid
871:870	Reserved		Valid	Valid
877:872	Reserved		Valid	Valid
879:878	Reserved		Valid	Valid
881:880	Reserved		Valid	Valid
884:882	LDO2/3 V_{DD} minimum Power Selection for LDO3	000: 2.5V, 001: 2.8V, 010: 3.0V, 011: 3.3V, 100: 3.6V, 101: 3.9V, 110: 4.4V, 111: 4.5V	Valid	Valid
887:885	LDO2/3 V_{DD} minimum Power Selection for LDO2	000: 2.5V, 001: 2.8V, 010: 3.0V, 011: 3.3V, 100: 3.6V, 101: 3.9V, 110: 4.4V, 111: 4.5V	Valid	Valid
895:888	Reserved		Valid	Invalid
903:896	CNT2 Counted Value for I²C read		Valid	Invalid
911:904	CNT4 Counted Value for I²C read		Valid	Invalid
919:912	Reserved		Valid	Invalid
927:920	Reserved		Valid	Invalid
935:928	Reserved		Valid	Invalid
943:936	Shadow buffer for RTC counter [7:0]		Valid	Valid
950:944	Shadow buffer for RTC counter [14:8]		Valid	Valid
951	Reserved		Valid	Valid
959:952	Shadow buffer for RTC counter [23:16]		Valid	Valid
967:960	Shadow buffer for RTC counter [31:24]		Valid	Valid
975:968	Shadow buffer for RTC counter [39:32]		Valid	Valid
983:976	Shadow buffer for RTC counter [47:40]		Valid	Valid
988:984	Reserved		Valid	Valid
989	Shadow buffer data transfer direction selection		Valid	Valid
990	Shadow buffer trigger signal selection		Valid	Valid
991	RTC 32-bit time counter clock source	0: From 15-bit counter divider 1: From RTC clock	Valid	Valid
999:992	Alarm DCMP [23:16]		Valid	Valid
1007:1000	Alarm DCMP [31:24]		Valid	Valid
1015:1008	Alarm DCMP [39:32]		Valid	Valid
1023:1016	Alarm DCMP [47:40]		Valid	Valid
IO0				
1024	Reserved		Valid	Valid
1025	IO0 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1027:1026	IO0 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
1029:1028	IO0 Mode Control (sig_io0_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
1031:1030	IO0 Mode Control (sig_io0_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO1				
1032	Reserved		Valid	Valid
1033	IO1 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
1034	IO1 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
1036:1035	IO1 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
1039:1037	IO1 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input & Open-Drain NMOS	Valid	Valid
Reserved				
1040	Reserved		Valid	Valid
1041	Reserved		Valid	Valid
1042	Reserved		Valid	Valid
1044:1043	Reserved		Valid	Valid
1047:1045	Reserved		Valid	Valid
Reserved				
1048	Reserved		Valid	Valid
1049	Reserved		Valid	Valid
1050	Reserved		Valid	Valid
1052:1051	Reserved		Valid	Valid
1055:1053	Reserved		Valid	Valid
IO2				
1056	Reserved		Valid	Valid
1057	IO2 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1059:1058	IO2 Pull-down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
1061:1060	IO2 Mode Control (sig_io2_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
1063:1062	IO2 Mode Control (sig_io2_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO3				
1064	Reserved		Valid	Valid
1065	Reserved		Valid	Valid
1067:1066	Reserved		Valid	Valid
1069:1068	IO3 Pull-down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
1071:1070	IO3 Mode Control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
SCL				
1072	Reserved		Valid	Valid
1073	Reserved		Valid	Valid
1074	Reserved		Valid	Valid
1076:1075	Reserved		Valid	Valid
1078:1077	SCL Mode Control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
1079	Reserved		Valid	Valid
SDA				
1080	Reserved		Valid	Valid
1081	SDA Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
1082	Reserved		Valid	Valid
1084:1083	Reserved		Valid	Valid
1086:1085	SDA Mode Control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
1087	Reserved		Valid	Valid
IO4				
1088	Reserved		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1089	IO4 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
1091:1090	IO4 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
1093:1092	IO4 Mode Control (sig_io4_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
1095:1094	IO4 Mode Control (sig_io4_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO5				
1096	Reserved		Valid	Valid
1097	IO5 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
1098	IO5 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
1100:1099	IO5 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
1103:1101	IO5 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input & Open-Drain NMOS	Valid	Valid
IO6				
1104	Reserved		Valid	Valid
1105	IO6 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
1107:1106	IO6 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
1109:1108	IO6 Mode Control (sig_io6_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
1111:1110	IO6 Mode Control (sig_io6_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
ACMP				
1112	ACMP1 Positive Input Source Select - ACMP0 IN+ Source	0: Disable 1: Enable	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1113	ACMP1 Analog Buffer Enable (Max. BW 1MHz)	0: Disable analog buffer 1: Enable analog buffer	Valid	Valid
1115:1114	ACMP1 Hysteresis Enable	00: 0 mV 01: 25 mV 10: 50 mV 11: 200 mV (01: for both external & internal Vref, 10 & 11: for only internal Vref, External Vref will not have 50 mV & 200 mV hysteresis.)	Valid	Valid
1116	ACMP0 Positive Input Source Select V_{DD}	0: Disable 1: Enable	Valid	Valid
1117	ACMP0 Analog Buffer Enable (Max. BW 1MHz)	0: Disable analog buffer 1: Enable analog buffer	Valid	Valid
1119:1118	ACMP0 Hysteresis Enable	00: 0 mV 01: 25 mV 10: 50 mV 11: 200 mV (01: for both external & internal Vref, 10 & 11: for only internal Vref, External Vref will not have 50 mV & 200 mV hysteresis.)	Valid	Valid
1120	ACMP3 Positive Input Source Select - ACMP2 IN+ Source	0: Disable 1: Enable	Valid	Valid
1123:1121	ACMP3 Hysteresis Enable	000: 0 mV 001: 25 mV 010: 50 mV 011: 200 mV 100: Reserved 101: Reserved 110: 100 mV 111: 150 mV (001: for both external & internal Vref, 010 & 011 & 110 & 111: for only internal Vref, External Vref will not have (50, 100, 150, 200) mV hysteresis.)	Valid	Valid
1124	ACMP2 Positive Input Source Select - ACMP0 IN+ Source	0: Disable 1: Enable	Valid	Valid
1127:1125	ACMP2 Hysteresis Enable	000: 0 mV 001: 25 mV 010: 50 mV 011: 200 mV 100: Reserved 101: Reserved 110: 100 mV 111: 150 mV (001: for both external & internal Vref, 010 & 011 & 110 & 111: for only internal Vref, External Vref will not have (50, 100, 150, 200) mV hysteresis.)	Valid	Valid
LUT				
1128	LUT3_4 or DFF7 with nRST/nSET Select	0: LUT3_4 1: DFF7 with nRST/nSET	Valid	Valid
1129	LUT3_3 or DFF6 with nRST/nSET Select	0: LUT3_3 1: DFF6 with nRST/nSET	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1130	LUT3_2 or DFF5 with nRST/nSET Select	0: LUT3_2 1: DFF5 with nRST/nSET	Valid	Valid
1131	LUT3_1 or DFF4 with nRST/nSET Select	0: LUT3_1 1: DFF4 with nRST/nSET	Valid	Valid
1132	LUT3_0 or DFF3 with nRST/nSET Select (Two consecutive DFFs if [1431]=1 for ASM)	0: LUT3_0 1: DFF3 with nRST/nSET	Valid	Valid
1133	LUT2_2 or DFF2 Select	0: LUT2_2 1: DFF2	Valid	Valid
1134	LUT2_1 or DFF1 Select	0: LUT2_1 1: DFF1	Valid	Valid
1135	LUT2_0 or DFF0 Select	0: LUT2_0 1: DFF0	Valid	Valid
LUT3				
1136	Reserved		Valid	Valid
1137	Reserved		Valid	Valid
1138	LUT3_5 or DFF8 with nRST/nSET Select	0: LUT3_5 1: DFF8 with nRST/nSET	Valid	Valid
1139	LUT3_10 or DLY/CNT4(8bits) Select	0: LUT3_10 1: DLY/CNT4(8bits)	Valid	Valid
1140	LUT3_9 or DLY/CNT3(8bits) Select	0: LUT3_9 1: DLY/CNT3(8bits)	Valid	Valid
1141	LUT3_8 or DLY/CNT2(8bits) Select	0: LUT3_8 1: DLY/CNT2(8bits)	Valid	Valid
1142	LUT3_7 or DLY/CNT1(8bits) Select	0: LUT3_7 1: DLY/CNT1(8bits)	Valid	Valid
1143	LUT3_6 or DLY/CNT0(8bits) Select	0: LUT3_6 1: DLY/CNT0(8bits)	Valid	Valid
LUT2				
1144	LUT2_1 [0]		Valid	Valid
1145	LUT2_1 [1]/DFF1 Initial Polarity Select	0: Low 1: High	Valid	Valid
1146	LUT2_1 [2]/DFF1 Output Select	0: Q output 1: nQ output	Valid	Valid
1147	LUT2_1 [3]/DFF1 or LATCH1 Select	0: DFF function 1: LATCH function	Valid	Valid
1148	LUT2_0 [0]		Valid	Valid
1149	LUT2_0 [1]/DFF0 Initial Polarity Select	0: Low 1: High	Valid	Valid
1150	LUT2_0 [2]/DFF0 Output Select	0: Q output 1: nQ output	Valid	Valid
1151	LUT2_0 [3]/DFF0 or LATCH0 Select	0: DFF function 1: LATCH function	Valid	Valid
1155:1152	Reserved		Valid	Valid
1156	LUT2_2 [0]		Valid	Valid
1157	LUT2_2 [1]/DFF2 Initial Polarity Select	0: Low 1: High	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1158	LUT2_2 [2]/DFF2 Output Select	0: Q output 1: nQ output	Valid	Valid
1159	LUT2_2 [3]/DFF2 or LATCH2 Select	0: DFF function 1: LATCH function	Valid	Valid
LUT3				
1163:1160	LUT3_0 [3:0]		Valid	Valid
1164	LUT3_0 [4]/DFF3 Initial Polarity Select	0: Low 1: High	Valid	Valid
1165	LUT3_0 [5]/DFF3 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
1166	LUT3_0 [6]/DFF3 Output Select	0: Q output 1: nQ output	Valid	Valid
1167	LUT3_0 [7]/DFF3 or LATCH3 Select	0: DFF function 1: LATCH function	Valid	Valid
1171:1168	LUT3_1 [3:0]		Valid	Valid
1172	LUT3_1 [4]/DFF4 Initial Polarity Select	0: Low 1: High	Valid	Valid
1173	LUT3_1 [5]/DFF4 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
1174	LUT3_1 [6]/DFF4 Output Select	0: Q output 1: nQ output	Valid	Valid
1175	LUT3_1 [7]/DFF4 or LATCH4 Select	0: DFF function 1: LATCH function	Valid	Valid
1179:1176	LUT3_2 [3:0]		Valid	Valid
1180	LUT3_2 [4]/DFF5 Initial Polarity Select	0: Low 1: High	Valid	Valid
1181	LUT3_2 [5]/DFF5 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
1182	LUT3_2 [6]/DFF5 Output Select	0: Q output 1: nQ output	Valid	Valid
1183	LUT3_2 [7]/DFF5 or LATCH5 Select	0: DFF function 1: LATCH function	Valid	Valid
1187:1184	LUT3_3 [3:0]		Valid	Valid
1188	LUT3_3 [4]/DFF6 Initial Polarity Select	0: Low 1: High	Valid	Valid
1189	LUT3_3 [5]/DFF6 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
1190	LUT3_3 [6]/DFF6 Output Select	0: Q output 1: nQ output	Valid	Valid
1191	LUT3_3 [7]/DFF6 or LATCH6 Select	0: DFF function 1: LATCH function	Valid	Valid
1195:1192	LUT3_4 [3:0]		Valid	Valid
1196	LUT3_4 [4]/DFF7 Initial Polarity Select	0: Low 1: High	Valid	Valid
1197	LUT3_4 [5]/DFF7 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
1198	LUT3_4 [6]/DFF7 Output Select	0: Q output 1: nQ output	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1199	LUT3_4 [7]/DFF7 or LATCH7 Select	0: DFF function 1: LATCH function	Valid	Valid
1203:1200	LUT3_5 [3:0]		Valid	Valid
1204	LUT3_5 [4]/DFF8 Initial Polarity Select	0: Low 1: High	Valid	Valid
1205	LUT3_5 [5]/DFF8 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
1206	LUT3_5 [6]/DFF8 Output Select	0: Q output 1: nQ output	Valid	Valid
1207	LUT3_5 [7]/DFF8 or LATCH8 Select	0: DFF function 1: LATCH function	Valid	Valid
Reserved				
1215:1208	Reserved		Valid	Valid
1223:1216	Reserved		Valid	Invalid
LUT3 & DLY/CNT				
1227:1224	LUT3_11 [3:0]/Pipe Delay OUT0 Select/Ripple Counter END[0],nSET[2:0]		Valid	Valid
1231:1228	LUT3_11 [7:4]/Pipe Delay OUT1 Select/Ripple Counter RSVD,MODE,END[2:1]	[1230] for Ripple counter MODE function: 0: FULL, 1: RANGE	Valid	Valid
1232	Reserved		Valid	Valid
1233	DLY/CNT4 Delayed Edge Output Selection	0: Default function from [1277] 1: Delayed edge detect	Valid	Valid
1234	DLY/CNT3 Delayed Edge Output Selection	0: Default function from [1269] 1: Delayed edge detect	Valid	Valid
1235	DLY/CNT2 Delayed Edge Output Selection	0: Default function from [1261] 1: Delayed edge detect	Valid	Valid
1236	DLY/CNT1 Delayed Edge Output Selection	0: Default function from [1253] 1: Delayed edge detect	Valid	Valid
1237	Pipe Delay Select or Ripple counter Select	0: Pipe Delay 1: Ripple Counter	Valid	Valid
1238	LUT3_11 or Pipe Delay Select	0: LUT3_11 1: Pipe Delay/Ripple counter by [1237]	Valid	Valid
1239	Pipe Delay OUT1 Polarity Select	0: Non-Inverted 1: Inverted	Valid	Valid
DLY/CNT0				
1241:1240	DLY0 Edge Select or Asynchronous CNT0 Reset	00: On both Falling and Rising Edges 01: on Falling Edge only 10: on Rising Edge only 11: No Delay on either Falling or Rising Edges/High Level Counter Reset	Valid	Valid
1244:1242	DLY/CNT0 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter4 Overflow	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1245	CNT0's Q are Set to data or Reset to 0s Selection (8bits)	0: Reset to 0s 1: Set to data ([1543:1536])	Valid	Valid
1247:1246	DLY/CNT0 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT1				
1249:1248	DLY1 Edge Select or Asynchronous CNT1 Reset	00: On both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges/High Level Counter Reset	Valid	Valid
1252:1250	DLY/CNT1 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter0 Overflow	Valid	Valid
1253	DLY/CNT1 Output Selection	0: Default Output 1: Edge Detector Output	Valid	Valid
1255:1254	DLY/CNT1 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT2				
1257:1256	DLY2 Edge Select or Asynchronous CNT2 Reset	00: On both Falling and Rising Edges 01: on Falling Edge only 10: on Rising Edge only 11: No Delay on either Falling or Rising Edges/High Level Counter Reset	Valid	Valid
1260:1258	DLY/CNT2 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter1 Overflow	Valid	Valid
1261	DLY/CNT2 Output Selection	0: Default Output 1: Edge Detector Output	Valid	Valid
1263:1262	DLY/CNT2 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT3				
1265:1264	DLY3 Edge Select or Asynchronous CNT3 Reset	00: On both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges/High Level Counter Reset	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1268:1266	DLY/CNT3 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter2 Overflow	Valid	Valid
1269	DLY/CNT3 Output Selection	0: Default Output 1: Edge Detector Output	Valid	Valid
1271:1270	DLY/CNT3 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT4				
1273:1272	DLY4 Edge Select or Asynchronous CNT4 Reset	00: On both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges/High Level Counter Reset	Valid	Valid
1276:1274	DLY/CNT4 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter3 Overflow	Valid	Valid
1277	DLY/CNT4 Output Selection	0: Default Output 1: Edge Detector Output	Valid	Valid
1279:1278	DLY/CNT4 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
Reserved				
1280	Reserved		Valid	Valid
1281	Reserved		Valid	Valid
1282	External Clock Source Select instead of 25kHz/2MHz	0: Internal Oscillator, 1: External Clock (EXT_CLK)	Valid	Valid
DLY/CNT Polarity Select				
1283	Select the Polarity of DLY/CNT4's Output	0: Default Output 1: Inverted Output	Valid	Valid
1284	Select the Polarity of DLY/CNT3's Output	0: Default Output 1: Inverted Output	Valid	Valid
1285	Select the Polarity of DLY/CNT2's Output	0: Default Output 1: Inverted Output	Valid	Valid
1286	Select the Polarity of DLY/CNT1's Output	0: Default Output 1: Inverted Output	Valid	Valid
1287	Select the Polarity of DLY/CNT0's Output	0: Default Output 1: Inverted Output	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
OSC				
1289:1288	LPOSC Clock Pre-divider	00: Div1, 01:Div2, 10: Div4, 11: Div16	Valid	Valid
1290	Force LPOSC Oscillator ON	0: Auto Power-On (if any CNT/DLY use LPOSC source) 1: Force Power-On	Valid	Valid
1292:1291	OSC Clock Pre-divider	00: Div1 01: Div2 10: Div4 11: Div8	Valid	Valid
1293	OSC Fast Start-Up Enable	0: Disable 1: Enable	Valid	Valid
1294	Oscillator (25kHz: RC-OSC, 2M: RC-OSC) Select	0: 25 kHz RC-OSC 1: 2 MHz RC-OSC	Valid	Valid
1295	Force Oscillator ON	0: Auto Power-On (if any CNT/DLY use 25K source) 1: Force Power-On	Valid	Valid
1298:1296	Internal OSC 25 kHz Frequency Divider Control for matrix input [28]	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64	Valid	Valid
1299	OSC Clock 25 kHz to matrix input [28] enable	0: Disable 1: Enable	Valid	Valid
1302:1300	Internal OSC 25 kHz Frequency Divider Control for matrix input [27]	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64	Valid	Valid
1303	OSC Clock 25 kHz to matrix input [27] enable	0: Disable 1: Enable	Valid	Valid
IO3				
1304	IO3 reset level polarity selection	0: Non-inverted 1: Inverted	Valid	Valid
1305	IO3 reset bypass selection	0: Edge selection 1: Level selection	Valid	Valid
1306	IO3 reset edge selection	0: Rising edge 1: Falling edge	Valid	Valid
1307	IO3 reset enable	0: Disable 1: Enable	Valid	Valid
1309:1308	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1311:1310	Delay Value Select for Programmable Delay & Edge Detector (V_{DD} = 3.3 V, typical)	00: 165 ns 01: 300 ns 10: 440 ns 11: 575 ns	Valid	Valid
ASM				
1314:1312	ASM_reg_init[2:0] for ASM state default set-up bits		Valid	Valid
1319:1315	Reserved		Valid	Valid
1322:1320	ASM_state0_dec8x1_EN1		Valid	Valid
1323	Reserved		Valid	Valid
1326:1324	ASM_state0_dec8x1_EN0		Valid	Valid
1327	Reserved		Valid	Valid
1330:1328	ASM_state1_dec8x1_EN0		Valid	Valid
1331	Reserved		Valid	Valid
1334:1332	ASM_state0_dec8x1_EN2		Valid	Valid
1335	ASM Rising Edge Detect Enable on EN2 of state0	0: Disable 1: Enable	Valid	Valid
1338:1336	ASM_state1_dec8x1_EN2		Valid	Valid
1339	ASM Rising Edge Detect Enable on EN2 of state1	0: Disable 1: Enable	Valid	Valid
1342:1340	ASM_state1_dec8x1_EN1		Valid	Valid
1343	Reserved		Valid	Valid
1346:1344	ASM_state2_dec8x1_EN1		Valid	Valid
1347	Reserved		Valid	Valid
1350:1348	ASM_state2_dec8x1_EN0		Valid	Valid
1351	Reserved		Valid	Valid
1354:1352	ASM_state3_dec8x1_EN0		Valid	Valid
1355	Reserved		Valid	Valid
1358:1356	ASM_state2_dec8x1_EN2		Valid	Valid
1359	ASM Rising Edge Detect Enable on EN2 of state2	0: Disable 1: Enable	Valid	Valid
1362:1360	ASM_state3_dec8x1_EN2		Valid	Valid
1363	ASM Rising Edge Detect Enable on EN2 of state3	0: Disable 1: Enable	Valid	Valid
1366:1364	ASM_state3_dec8x1_EN1		Valid	Valid
1367	Reserved		Valid	Valid
1370:1368	ASM_state4_dec8x1_EN1		Valid	Valid
1371	Reserved		Valid	Valid
1374:1372	ASM_state4_dec8x1_EN0		Valid	Valid
1375	Reserved		Valid	Valid
1378:1376	ASM_state5_dec8x1_EN0		Valid	Valid
1379	Reserved		Valid	Valid
1382:1380	ASM_state4_dec8x1_EN2		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1383	ASM Rising Edge Detect Enable on EN2 of state4	0: Disable 1: Enable	Valid	Valid
1386:1384	ASM_state5_dec8x1_EN2		Valid	Valid
1387	ASM Rising Edge Detect Enable on EN2 of state5	0: Disable 1: Enable	Valid	Valid
1390:1388	ASM_state5_dec8x1_EN1		Valid	Valid
1391	Reserved		Valid	Valid
1394:1392	ASM_state6_dec8x1_EN1		Valid	Valid
1395	Reserved		Valid	Valid
1398:1396	ASM_state6_dec8x1_EN0		Valid	Valid
1399	Reserved		Valid	Valid
1402:1400	ASM_state7_dec8x1_EN0		Valid	Valid
1403	Reserved		Valid	Valid
1406:1404	ASM_state6_dec8x1_EN2		Valid	Valid
1407	ASM Rising Edge Detect Enable on EN2 of state6	0: Disable 1: Enable	Valid	Valid
1410:1408	ASM_state7_dec8x1_EN2		Valid	Valid
1411	ASM Rising Edge Detect Enable on EN2 of state7		Valid	Valid
1414:1412	ASM_state7_dec8x1_EN1		Valid	Valid
1415	Reserved		Valid	Valid
Filter/Edge Detector				
1417:1416	Select the edge mode of Edge Detector_1	00: Rising Edge 01: Falling Edge 10: Both Edge 11: Delay	Valid	Valid
1418	Filter_1/Edge Detector_1 output Polarity Select	0: Filter_1 output 1: Filter_1 output inverted	Valid	Valid
1419	Filter_1 (Typ. 50nS @V_{DD} = 3.3 V) or Edge Detector_1 (Typ. 125nS @V_{DD} = 3.3 V) Select	0: Filter_1 1: Edge Detector_1	Valid	Valid
1421:1420	Select the edge mode of Edge Detector_0	00: Rising Edge 01: Falling Edge 10: Both Edge 11: Delay	Valid	Valid
1422	Filter_0/Edge Detector_0 output Polarity Select	0: Filter_0 output 1: Filter_0 output inverted	Valid	Valid
1423	Filter_0 (Typ. 70 ns @V_{DD} = 3.3 V) or Edge Detector_0 Select (Typ. 125 ns @ V_{DD}=3.3 V)	0: Filter_0 1: Edge Detector_0	Valid	Valid
Vref/Bandgap				
1424	Reserved		Valid	Valid
1426:1425	Reserved		Valid	Valid
1427	Reserved		Valid	Valid
1428	Vref Op Amp Offset Chopper Enable	0: Disable 1: Enable	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1429	Reserved	0: Disable 1: Enable	Valid	Valid
1430	Reserved	0: 2 MHz 1: 1 MHz	Valid	Valid
1431	Two consecutive DFFs enable for ASM	0: Disable 1: Enable	Valid	Valid
1434:1432	CP function selection & Power divider (V_{DD}/3, V_{DD}/4) ON/OFF	100: CP Auto ON/OFF (Use for 1.71 V<V_{DD}<5.5 V) X10: CP always OFF (Use for 2.7 V<V_{DD}), XX1: CP always ON (Use for V_{DD}<2.7 V) 0XX: Power divider off (if there is no use of V_{DD}/3,V_{DD}/4 @ACMP negative in)	Valid	Valid
1435	Reserved		Valid	Valid
1436	Force Bandgap ON	0: Auto-Mode 1: Enable (if chip is Power-Down, the Band-gap will Power-Down even if it is Set to 1).	Valid	Valid
1437	NVM Power-Down	0: None (Or Programming Enable) 1: Power-Down (Or Programming Disable)	Valid	Valid
1438	Reserved		Valid	Valid
1439	GPIO Quick Charge Enable	0: Disable 1: Enable	Valid	Valid
Wake/Sleep				
1440	Reserved		Valid	Valid
1441	Reserved		Valid	Valid
1442	ACMP0 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
1443	ACMP1 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
1444	ACMP2 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
1445	ACMP3 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
1446	Wake Sleep Output State When WS Oscilla-tor is Power-Down if DLY/CNT0 Mode Selec-tion is "11"	0: Low 1: High	Valid	Valid
1447	Wake Sleep Ratio Control Mode Selection if DLY/CNT0 Mode Selection is "11"	0: Default Mode 1: Wake Sleep Ratio Control Mode	Valid	Valid
LDO				
1448	LDO1 PS_Mode_Gate (LDO1 turn-on/off is controlled by LDO1_EN matrix output)	0: LDO Mode Enable 1: Power switch Mode Enable	Valid	Valid
1449	LDO1 Start-up Ramping Slope Divide Enable	0: Disable 1: Enable (Div 8 of 1600])	Valid	Valid
1450	LDO1 Over-current & Short-current Detection Enable	0: Disable 1: Enable	Valid	Valid
1451	LDO1 Discharge resistor Enable	0: No discharge resistor 1: 300 ohm discharge resistor	Valid	Valid
1452	LDO0 PS_Mode_Gate (LDO0 turn-on/off is controlled by LDO0_EN matrix output)	0: LDO Mode Enable 1: Power switch Mode Gate Enable	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1453	LDO0 Start-up Ramping Slope Divide Enable	0: Disable 1: Enable (Div 8 of [1592])	Valid	Valid
1454	LDO0 Over-current & Short-current Detection Enable	0: Disable 1: Enable	Valid	Valid
1455	LDO0 Discharge resistor Enable	0: No discharge resistor 1: 300 Ohm discharge resistor	Valid	Valid
1456	LDO3 PS_Mode_Gate (LDO3 turn-on/off is controlled by LDO3_EN matrix output)	0: LDO Mode Enable 1: Power switch Mode Gate Enable	Valid	Valid
1457	LDO3 Start-up Ramping Slope Divide Enable	0: Disable 1: Enable (Div 8 of [1616])	Valid	Valid
1458	LDO3 Over-current & Short-current Detection Enable	0: Disable 1: Enable	Valid	Valid
1459	LDO3 Discharge resistor Enable	0: No discharge resistor 1: 300 Ω discharge resistor	Valid	Valid
1460	LDO2 PS_Mode_Gate (LDO2 turn-on/off is controlled by LDO2_EN matrix output)	0: LDO Mode Enable 1: Power switch Mode Gate Enable	Valid	Valid
1461	LDO2 Start-up Ramping Slope Divide Enable	0: Disable 1: Enable (Div 8 of [1608])	Valid	Valid
1462	LDO2 Over-current & Short-current Detection Enable	0: Disable 1: Enable	Valid	Valid
1463	LDO2 Discharge resistor Enable	0: No discharge resistor 1: 300 Ω discharge resistor	Valid	Valid
1465:1464	Reserved		Valid	Invalid
1467:1466	Reserved		Valid	Invalid
1469:1468	Reserved		Valid	Invalid
1471:1470	Reserved		Valid	Invalid
1479:1472	Reserved Reserved		Valid	Invalid
1487:1480	Reserved		Valid	Invalid
1488	ACMP1 100 µA Current Source Enable	0: Disable 1: Enable	Valid	Valid
1489	Reserved		Valid	Valid
1490	Reserved		Valid	Valid
1491	LDO2 VOUT output connection enable to ACMP3	0: Default ACMP function 1: Enable LDO2 VOUT function	Valid	Valid
1492	LDO0 VOUT output connection enable to ACMP3	0: Default ACMP function 1: Enable LDO0 VOUT function	Valid	Valid
1493	TS output connection enable to ACMP2	0: Default ACMP function 1: Enable TS function	Valid	Valid
1494	LDO2/3 VIN connection enable to ACMP1	0: Default ACMP function 1: Enable UVLO1 function	Valid	Valid
1495	LDO0/1 VIN connection enable to ACMP0	0: Default ACMP function 1: Enable UVLO0 function	Valid	Valid
1496	Reserved		Valid	Valid
1497	Reserved		Valid	Valid
1498	Reserved		Valid	Valid
1499	Reserved		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1503:1500	Reserved		Valid	Valid
1519:1504	LUT4x2_0 Output0 [15:0]		Valid	Valid
1535:1520	LUT4x2_0 Output1 [15:0]		Valid	Valid
LUT/DLY/CNT Control Data				
1543:1536	LUT3_6 [7:0] or DLY/CNT0 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
1551:1544	LUT3_7 [7:0] or DLY/CNT1 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
1559:1552	LUT3_8 [7:0] or DLY/CNT2 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
1567:1560	LUT3_9 [7:0] or DLY/CNT3 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
1575:1568	LUT3_10 [7:0] or DLY/CNT4 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
1577:1576	Reserved		Valid	Invalid
1579:1578	Reserved		Valid	Invalid
1581:1580	Reserved		Valid	Invalid
1583:1582	Reserved		Valid	Invalid
1584	UVLO1_HW_enable (Enable UVLO1 output Hard-Wire connection to LDO2/3)	0: Disable UVLO1 HW connect 1: Enable UVLO1 HW connect	Valid	Valid
1585	UVLO0_HW_enable (Enable UVLO0 output Hard-Wire connection to LDO0/1)	0: Disable UVLO0 HW connect 1: Enable UVLO0 HW connect	Valid	Valid
1588:1586	LDO0/1 V_{DD} minimum Power Selection for LDO1	000: 2.5 V 001: 2.8 V 010: 3.0 V 011: 3.3 V 100: 3.6 V 101: 3.9 V 110: 4.4 V 111: 4.5 V	Valid	Valid
1591:1589	LDO0/1 V_{DD} minimum Power Selection for LDO0	000: 2.5 V 001: 2.8 V 010: 3.0 V 011: 3.3 V 100: 3.6 V 101: 3.9 V 110: 4.4 V 111: 4.5 V	Valid	Valid
1592	LDO0 Start-up Ramping Slope Selection	0: 10 V/ms 1: 20 V/ms	Valid	Valid
1594:1593	Reserved		Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1599:1595	LDO0 Vref Selection	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.50v, 01111:2.50v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.85v, 10101:2.90v, 10110:3.00v, 10111:3.10v, 11000:3.20v, 11001:3.30v, 11010:3.40v, 11011:3.50v, 11100:3.60v, 11101:4.00v, 11110:4.10v, 11111:4.20v	Valid	Valid
1600	LDO1 Start-up Ramping Slope Selection	0: 10 V/ms 1: 20 V/ms	Valid	Valid
1602:1601	Reserved		Valid	Valid
1607:1603	LDO1 Vref Selection	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.50v, 01111:2.50v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.85v, 10101:2.90v, 10110:3.00v, 10111:3.10v, 11000:3.20v, 11001:3.30v, 11010:3.40v, 11011:3.50v, 11100:3.60v, 11101:4.00v, 11110:4.10v, 11111:4.20v	Valid	Valid
1608	LDO2 Start-up Ramping Slope Selection	0: 10 V/ms 1: 20 V/ms	Valid	Valid
1610:1609	Reserved		Valid	Valid
1615:1611	LDO2 Vref Selection	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.50v, 01111:2.50v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.85v, 10101:2.90v, 10110:3.00v, 10111:3.10v, 11000:3.20v, 11001:3.30v, 11010:3.40v, 11011:3.50v, 11100:3.60v, 11101:4.00v, 11110:4.10v, 11111:4.20v	Valid	Valid
1616	LDO3 Start-up Ramping Slope Selection	0: 10 V/ms 1: 20 V/ms	Valid	Valid
1618:1617	Reserved		Valid	Valid
1623:1619	LDO3 Vref Selection	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.50v, 01111:2.50v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.85v, 10101:2.90v, 10110:3.00v, 10111:3.10v, 11000:3.20v, 11001:3.30v, 11010:3.40v, 11011:3.50v, 11100:3.60v, 11101:4.00v, 11110:4.10v, 11111:4.20v	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
ACMP0				
1628:1624	ACMP0- IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}: ACMP0- /3 11001: V_{DD}: ACMP0- /4 11010: IO4: EXT_Vref 11011: IO4: EXT_Vref /2	Valid	Valid
1630:1629	ACMP0 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
1631	ACMP0 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1:ON	Valid	Valid
ACMP1				
1636:1632	ACMP1-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}: ACMP1- /3 11001: V_{DD}: ACMP1- /4 11010: IO4: EXT_Vref 11011: IO4: EXT_Vref /2	Valid	Valid
1638:1637	ACMP1 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
1639	ACMP1 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
ACMP2				
1644:1640	ACMP2-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}: ACMP2- /3 11001: V_{DD}: ACMP2- /4 11010: IO4: EXT_Vref 11011: IO4: EXT_Vref /2	Valid	Valid
1646:1645	ACMP2 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
1647	ACMP2 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid
ACMP3				
1652:1648	ACMP3-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}: ACMP3- /3 11001: V_{DD}: ACMP3- /4 11010: IO4: EXT_Vref 11011: IO4: EXT_Vref /2	Valid	Valid
1654:1653	ACMP3 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
1655	ACMP3 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid
Misc.				
1656	TS_HW_enable (Enable Temp sensor output Hard-Wire connection to LDO0/1/2/3)	0: Disable TS HW connect 1: Enable TS HW connect	Valid	Valid
1657	Switch from “Matrix OUT: LPOSC PD” to “Matrix OUT: LPOSC Force On”	0: OSC PD 1: OSC Force On (Matrix Output [60])	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1658	Switch from "Matrix OUT: OSC 25KHz/2MHz PD" to "Matrix OUT: OSC 25KHz/2MHz Force On"	0: OSC PD 1: OSC Force On (Matrix Output [59])	Valid	Valid
1659	Reserved		Valid	Invalid
1660	Reserved		Valid	Invalid
1661	Reserved		Valid	Invalid
1662	I²C reset bit with reloading NVM into Data register	0: Keep existing condition 1: Reset execution	Valid	Valid
1663	IO Latching Enable During I²C Write Interface	0: Disable 1: Enable	Valid	Invalid
1671:1664	RAM 8 outputs for ASM-state0		Valid	Valid
1679:1672	RAM 8 outputs for ASM-state1		Valid	Valid
1687:1680	RAM 8 outputs for ASM-state2		Valid	Valid
1695:1688	RAM 8 outputs for ASM-state3		Valid	Valid
1703:1696	RAM 8 outputs for ASM-state4		Valid	Valid
1711:1704	RAM 8 outputs for ASM-state5		Valid	Valid
1719:1712	RAM 8 outputs for ASM-state6		Valid	Valid
1727:1720	RAM 8 outputs for ASM-state7		Valid	Valid
1735:1728	User configurable RAM/OTP Byte 0		Valid	Valid
1743:1736	User configurable RAM/OTP Byte 1		Valid	Valid
1751:1744	User configurable RAM/OTP Byte 2		Valid	Valid
1759:1752	User configurable RAM/OTP Byte 3		Valid	Valid
1767:1760	User configurable RAM/OTP Byte 4		Valid	Valid
1775:1768	User configurable RAM/OTP Byte 5		Valid	Valid
1783:1776	User configurable RAM/OTP Byte 6		Valid	Valid
1791:1784	User configurable RAM/OTP Byte 7		Valid	Valid
1792	LDO0_EN_Gate (By this bit = 1, Matrix Output: LDO0_EN will be enabled.)	0: Disable 1: Enable	Valid	Valid
1793	LDO0 VOUT_SEL_Gate	0: Default VOUT selection 1: Enable 2nd VOUT selection	Valid	Valid
1794	Mode1_EN_Gate (By this bit = 1, Matrix Output: LDO MODE1_Enable for LDO0/1/2/3 will be enabled.)	0: Disable LDO_LP_MODE_EN matrix output 1: Enable LDO_LP_MODE_ EN matrix output	Valid	Valid
1799:1795	LDO0 2nd Vref Selection	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.50v, 01111:2.50v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.85v, 10101:2.90v, 10110:3.00v, 10111:3.10v, 11000:3.20v, 11001:3.30v, 11010:3.40v, 11011:3.50v, 11100:3.60v, 11101:4.00v, 11110:4.10v, 11111:4.20v	Valid	Valid
1800	LDO1_EN_Gate (By this bit = 1, Matrix Output: LDO1_EN will be enabled.)	0: Disable 1: Enable	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1801	LDO1 VOUT_SEL_Gate	0: Default VOUT selection 1: Enable 2nd VOUT selection	Valid	Valid
1802	Reserved		Valid	Valid
1807:1803	LDO1 2nd Vref Selection	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.50v, 01111:2.50v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.85v, 10101:2.90v, 10110:3.00v, 10111:3.10v, 11000:3.20v, 11001:3.30v, 11010:3.40v, 11011:3.50v, 11100:3.60v, 11101:4.00v, 11110:4.10v, 11111:4.20v	Valid	Valid
1808	LDO2_EN_Gate (By this bit = 1, Matrix Output: LDO2_EN will be enabled.)	0: Disable 1: Enable	Valid	Valid
1809	LDO2 VOUT_SEL_Gate	0: Default VOUT selection 1: Enable 2nd VOUT selection	Valid	Valid
1810	Reserved		Valid	Valid
1815:1811	LDO2 2nd Vref Selection	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.50v, 01111:2.50v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.85v, 10101:2.90v, 10110:3.00v, 10111:3.10v, 11000:3.20v, 11001:3.30v, 11010:3.40v, 11011:3.50v, 11100:3.60v, 11101:4.00v, 11110:4.10v, 11111:4.20v	Valid	Valid
1816	LDO3_EN_Gate (By this bit = 1, Matrix Output: LDO3_EN will be enabled.)	0: Disable 1: Enable	Valid	Valid
1817	LDO3 VOUT_SEL_Gate	0: Default VOUT selection 1: Enable 2nd VOUT selection	Valid	Valid
1818	Reserved		Valid	Valid
1823:1819	LDO3 2nd Vref Selection	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.50v, 01111:2.50v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.85v, 10101:2.90v, 10110:3.00v, 10111:3.10v, 11000:3.20v, 11001:3.30v, 11010:3.40v, 11011:3.50v, 11100:3.60v, 11101:4.00v, 11110:4.10v, 11111:4.20v	Valid	Valid
1831:1824	Reserved		Valid	Valid
1832	NVM Data Read Disable (From NVM): ID[24] for BANK0/1/2 only	0: Disable (Programmed data can be read.) 1: Enable (Programmed data can't be read.)	Valid	Invalid
1833	Reserved		Valid	Invalid
1835:1834	Reserved Reserved		Valid	Invalid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1839:1836	Reserved		Valid	Invalid
1847:1840	8-bit Pattern ID Byte 0 (From NVM): ID[23:16]		Valid	Valid
1855:1848	Reserved		Valid	Invalid
1863:1856	Reserved		Valid	Invalid
1867:1864	I²C Control Code Bit [3:0]	Value for slave address	Valid	Invalid
1868	I²C 1 MHz operation enable	0: Up to 400 kHz 1: 1 MHz operation	Valid	Invalid
1869	Reserved		Valid	Invalid
1870	BANK0/1/2/3 I²C-write protection bit	0: Writable 1: Non-writable	Valid	Invalid
1871	BANK0/1/2 I²C-write protection bit	0: Writable 1: Non-writable	Valid	Invalid
1872	Reserved		Invalid	Invalid
1874:1873	SEL_OCP[1:0] for Synchronous DC/DC Step Down Converter control	00: 2.5 A 10: 2.0 A	Invalid	Invalid
1876:1875	SEL_FSW[1:0] for Synchronous DC/DC Step Down Converter control	00: 1.5 MHz 01: 2.0 MHz 10: Reserved 11: Reserved	Invalid	Invalid
1879:1877	SEL_VO[2:0] for Synchronous DC/DC Step Down Converter control	000: 1.2 V 001: 1.5 V 010: 1.8 V 011: 2.5 V 100: 3.0 V 101: 3.3 V 110: Reserved 111: Reserved	Invalid	Invalid
1880	Reserved		Invalid	Invalid
1881	Reserved		Invalid	Invalid
1882	Reserved		Invalid	Invalid
1887:1883	Reserved		Invalid	Invalid
1891:1888	Reserved		Invalid	Invalid
1895:1892	Reserved		Invalid	Invalid
1899:1896	Reserved		Invalid	Invalid
1903:1900	Reserved		Invalid	Invalid
1904	Reserved		Invalid	Invalid
1905	Reserved		Invalid	Invalid
1907:1906	Reserved		Invalid	Invalid
1911:1908	Reserved		Invalid	Invalid
1919:1912	ASM State output [7:0]		Invalid	Invalid
Matrix Input				
1920	Matrix Input 0	VSS	Valid	Invalid
1921	Matrix Input 1	IO0 Digital Input	Valid	Invalid
1922	Matrix Input 2	IO1 Digital Input	Valid	Invalid

Table 103: Register Map (Continued)

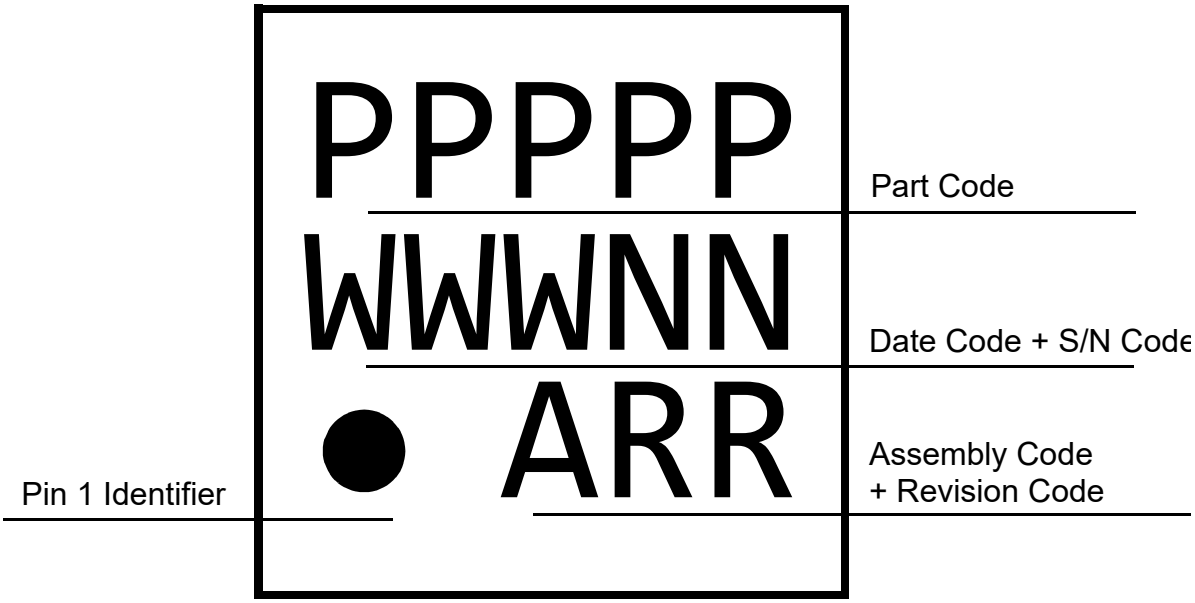
Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1923	Matrix Input 3	Synchronous DC/DC Step Down Converter Fault B	Valid	Invalid
1924	Matrix Input 4	VSS	Valid	Invalid
1925	Matrix Input 5	IO2 Digital Input	Valid	Invalid
1926	Matrix Input 6	LUT2_0/DFF0 Output	Valid	Invalid
1927	Matrix Input 7	LUT2_1/DFF1 Output	Valid	Invalid
1928	Matrix Input 8	LUT2_2/DFF2 Output	Valid	Invalid
1929	Matrix Input 9	LUT3_0/DFF3 Output	Valid	Invalid
1930	Matrix Input 10	LUT3_1/DFF4 Output	Valid	Invalid
1931	Matrix Input 11	LUT3_2/DFF5 Output	Valid	Invalid
1932	Matrix Input 12	LUT3_3/DFF6 Output	Valid	Invalid
1933	Matrix Input 13	LUT3_4/DFF7 Output	Valid	Invalid
1934	Matrix Input 14	LUT3_6/CNT_DLY0(8bit) Output	Valid	Invalid
1935	Matrix Input 15	LUT3_7/CNT_DLY1(8bit) Output	Valid	Invalid
1936	Matrix Input 16	LUT3_8/CNT_DLY2(8bit) Output	Valid	Invalid
1937	Matrix Input 17	LUT3_9/CNT_DLY3(8bit) Output	Valid	Invalid
1938	Matrix Input 18	LUT3_10/CNT_DLY4(8bit) Output	Valid	Invalid
1939	Matrix Input 19	LUT3_11/Pipe Delay (1st stage) Output/ Ripple counter Q[0]	Valid	Invalid
1940	Matrix Input 20	LUT3_5/DFF8 Output	Valid	Invalid
1941	Matrix Input 21	LUT4X2 Output0	Valid	Invalid
1942	Matrix Input 22	LUT4X2 Output1	Valid	Invalid
1943	Matrix Input 23	RTC CNT 1 second Output	Valid	Invalid
1944	Matrix Input 24	RTC DCOMP Output	Valid	Invalid
1945	Matrix Input 25	Pipe Delay Output0/Ripple counter Q[1]	Valid	Invalid
1946	Matrix Input 26	Pipe Delay Output1/Ripple counter Q[2]	Valid	Invalid
1947	Matrix Input 27	Internal OSC Post-Divided by 1/2/3/4/8/12/ 24/64 Output (25KHz/2MHz)	Valid	Invalid
1948	Matrix Input 28	Internal OSC Post-Divided by 1/2/3/4/8/12/ 24/64 Output (25KHz/2MHz)	Valid	Invalid
1949	Matrix Input 29	LPOSC Output	Valid	Invalid
1950	Matrix Input 30	Filter0/Edge Detect0 Output	Valid	Invalid
1951	Matrix Input 31	Filter1/Edge Detect1 Output	Valid	Invalid
1952	Matrix Input 32	I²C_virtual_0 Input	Valid	Valid
1953	Matrix Input 33	I²C_virtual_1 Input	Valid	Valid
1954	Matrix Input 34	I²C_virtual_2 Input	Valid	Valid
1955	Matrix Input 35	I²C_virtual_3 Input	Valid	Valid
1956	Matrix Input 36	I²C_virtual_4 Input	Valid	Valid
1957	Matrix Input 37	I²C_virtual_5 Input	Valid	Valid
1958	Matrix Input 38	I²C_virtual_6 Input	Valid	Valid
1959	Matrix Input 39	I²C_virtual_7 Input	Valid	Valid

Table 103: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
1960	Matrix Input 40	RAM_0 Output for ASM-state	Valid	Invalid
1961	Matrix Input 41	RAM_1 Output for ASM-state	Valid	Invalid
1962	Matrix Input 42	RAM_2 Output for ASM-state	Valid	Invalid
1963	Matrix Input 43	RAM_3 Output for ASM-state	Valid	Invalid
1964	Matrix Input 44	RAM_4 Output for ASM-state	Valid	Invalid
1965	Matrix Input 45	RAM_5 Output for ASM-state	Valid	Invalid
1966	Matrix Input 46	RAM_6 Output for ASM-state	Valid	Invalid
1967	Matrix Input 47	RAM_7 Output for ASM-state	Valid	Invalid
1968	Matrix Input 48		Valid	Invalid
1969	Matrix Input 49	LDO0 FAULTB	Valid	Invalid
1970	Matrix Input 50	LDO1 FAULTB	Valid	Invalid
1971	Matrix Input 51	LDO2 FAULTB	Valid	Invalid
1972	Matrix Input 52	LDO3 FAULTB	Valid	Invalid
1973	Matrix Input 53	IO3 Digital Input (GPI)	Valid	Invalid
1974	Matrix Input 54	IO4 Digital Input	Valid	Invalid
1975	Matrix Input 55	IO5 Digital Input	Valid	Invalid
1976	Matrix Input 56	IO6 Digital Input	Valid	Invalid
1977	Matrix Input 57	ACMP_0 Output	Valid	Invalid
1978	Matrix Input 58	ACMP_1 Output	Valid	Invalid
1979	Matrix Input 59	ACMP_2 Output	Valid	Invalid
1980	Matrix Input 60	ACMP_3 Output	Valid	Invalid
1981	Matrix Input 61	Programmable Delay with Edge Detector Output	Valid	Invalid
1982	Matrix Input 62	nRST_core as matrix input	Valid	Invalid
1983	Matrix Input 63	V_{DD}	Valid	Invalid
Reserved				
1991:1984	Reserved		Valid	Invalid
1999:1992	Reserved		Valid	Invalid
2007:2000	Reserved		Valid	Invalid
2015:2008	Reserved		Valid	Valid
2023:2016	Reserved		Valid	Invalid
2031:2024			Valid	Invalid
2032	Reserved		Valid	Valid
2033			Valid	Valid
2034	Reserved		Valid	Valid
2035	Reserved		Valid	Invalid
2039:2036	Reserved		Valid	Valid
2047:2040	Reserved		Valid	Valid

23 Package Top Marking System Definition

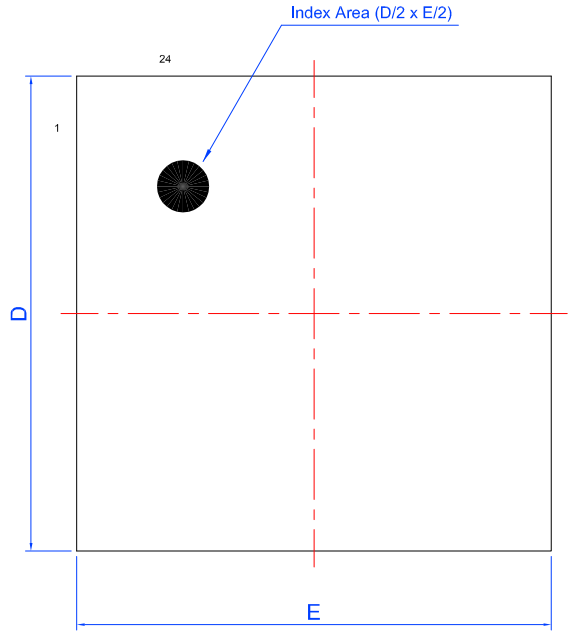
23.1 MSTQFN 29L 3 MM X 3 MM X 0.55 MM 0.4P PACKAGE



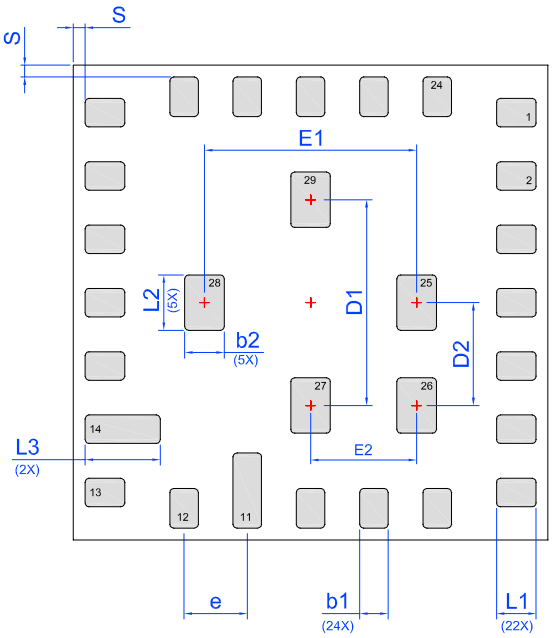
24 Package Information

24.1 PACKAGE OUTLINES FOR MSTQFN 29L 3 MM X 3 MM 0.4P FC PACKAGE

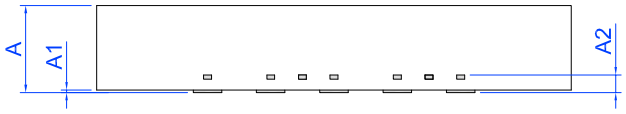
JEDEC MO-220, Variation WECE
IC Net Weight: 0.0121 g



Marking View



BTM View



Side view

UNIT: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.00	-	0.01	E	2.95	3.00	3.05
A2	0.11 REF			e	0.40 BSC		
b1	0.13	0.18	0.23	L1	0.20	0.25	0.30
b2	0.20	0.25	0.30	L2	0.30	0.35	0.40
S	0.075 REF			L3	0.425	0.475	0.525
D1	1.30 BSC			E1	1.34 BSC		
D2	0.65 BSC			E2	0.67 BSC		

24.2 MSTQFN HANDLING

Be sure to handle MSTQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle MSTQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

24.3 SOLDERING INFORMATION

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm^3 (nominal). More information can be found at www.jedec.org.

25 Ordering Information

Part Number	Type
SLG46585M	29-Pin MSTQFN
SLG46585MTR	29-Pin MSTQFN - Tape and Reel (3k units)

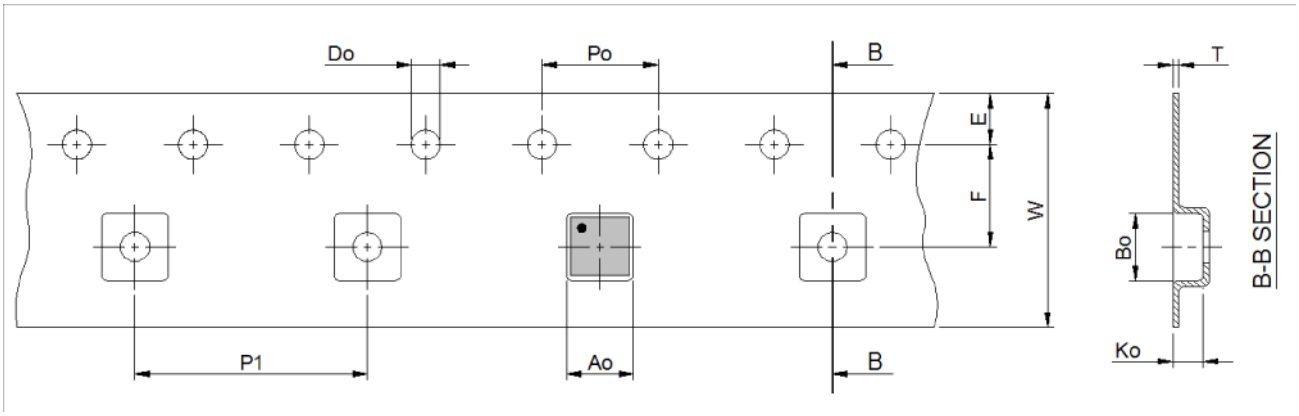
Note 1 Use SLG46585M to order. Shipments are automatically in Tape and Reel.
Note 2 "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

25.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
MSTQFN 29L 3 mm x 3 mm 0.4P Green	29	3 x 3 x 0.55	5,000	10,000	330/100	42	336	42	336	12	8

25.2 CARRIER TAPE DRAWING AND DIMENSIONS

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)	Tape Thickness (mm)
	A0	B0	K0	P0	P1	D0	E	F	W	T
MSTQFN 29L 3 mm x3 mm 0.4P Green	3.3	3.3	0.8	4	8	1.55	1.75	5.5	12	0.3



Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

Refer to EIA-481 specification

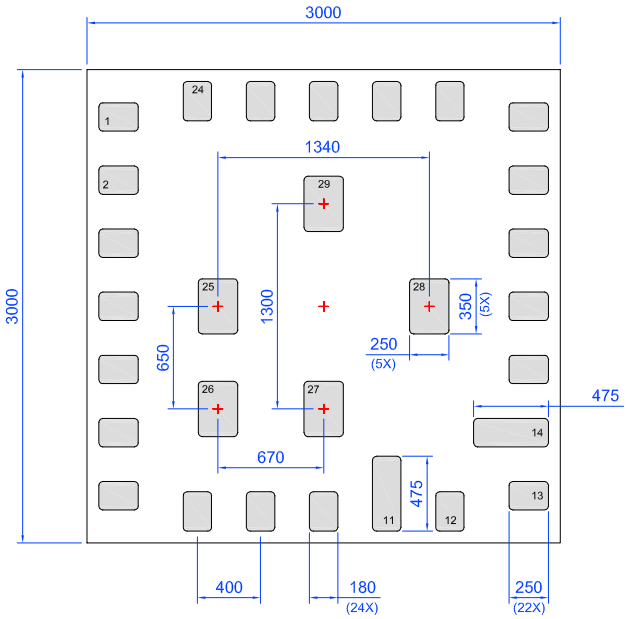
26 Layout Guidelines

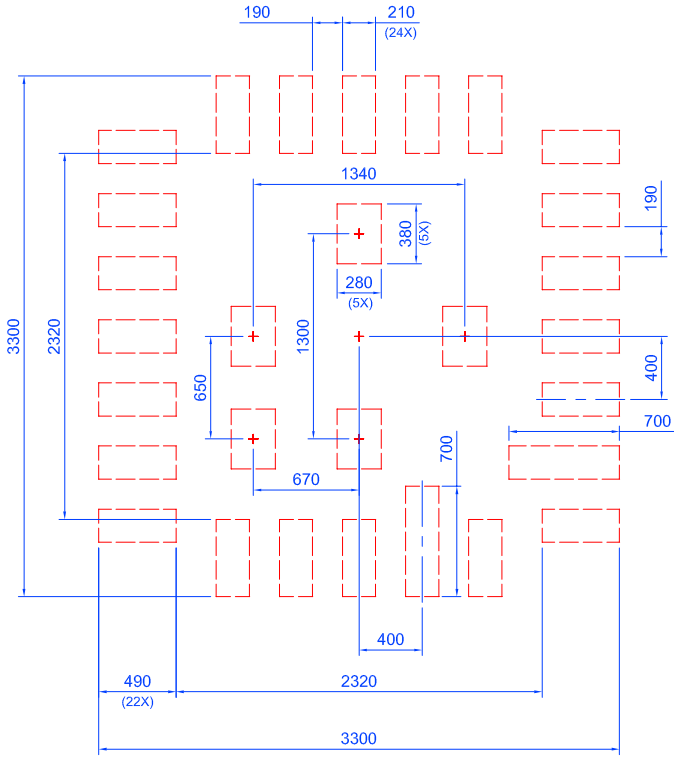
26.1 MSTQFN 29L 3 MM X 3 MM X 0.55 MM 0.4P PACKAGE

Exposed Pad
(Laser Marking view-PKG face down)

Recommended Land Pattern
(PKG face down)

Units: µm





Units: µm

Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed
ACMPL	Analog Comparator Low Power
AGND	Analog Ground

B

BG	Bandgap
BW	Bandwidth

C

CCM	Continuous Conduction Mode
CLK	Clock
CMO	Connection matrix output
CNT	Counter

D

DCM	Discontinuous Conduction Mode
DCMP	Digital Comparator
DFF	D Flip-Flop
DLY	Delay

E

ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

H

HP	High Power

I

IN	Input
IQ	Quiescent Current
IO	Input/Output

L

LBW	Low Bandwidth
LDO	Low Dropout Regulator
LP	Low Power
LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OCP	Over-Current Protection
OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OTP	one time programmable
OUT	Output

P

PD	Power-Down
PGen	Pattern Generator
PGND	Power Ground
POR	Power-On Reset
PP	Push-Pull
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write
RTC	Real Time Clock

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt Trigger
SS	Soft Start

SV	nSET Value
SW	Switch

T

T_C	Case temperature
TS	Temperature Sensor

U

UVLO	Under Voltage Lockout

V

VOSNS	DC/DC Converter VOUT feedback (sense) input
Vref	Voltage Reference

W

WOSMT	Without Schmitt Trigger
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
3.8	1-Jun-2023	Added IC Net Weight in section Package Information
3.7	3-Mar-2023	Added notes to section Ordering Information
3.6	16-Feb-2023	Corrected tables LDO HP MODE EC and LDO LP MODE EC
3.5	17-May-2022	Corrected section Over-Current Limit and Short-Circuit Detection
3.4	7-Mar-2022	Updated R_{PUP} and R_{PDWN} in section Electrical Characteristics Renesas rebranding Updated section CNT/DLY/FSM Timing Diagrams Corrected Reset Command Timing figure Updated Pin Block Diagrams
3.3	18-Sept-2018	Added graphs in subsection Oscillator Accuracy Updated 1.73 kHz OSC Frequency Limits and Errors Corrected Low Power Oscillator frequency Added section ACMP Typical Performance Table Gain Divider Input Resistance added to section Analog Comparators Updated according to new template Corrected LDO mode name Updated according to Dialog's Writing Guideline Fixed typos Corrected list of Pins connected to appropriate Power rails
3.2	15-Mar-2018	Fixed typos Added new subsection Electrostatic Discharge Ratings Added Parameter Short Circuit Protection Updated Registers Read/Write Protection Options
3.1	17-Dec-2018	Updated LDO Typical Application Performance Updated Oscillator Power-On Delay graphs Updated after review Added new subsection LDO efficiency
3.0	22-Nov-2018	Final version

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Renesas Electronics Corporation's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.