

EtherCAT<sup>®</sup> Interface for High-Performance C2000<sup>™</sup> MCU

This reference design demonstrates how to connect an EtherCAT ET1100 slave controller to a C2000 Delfino<sup>™</sup> MCU. The interface supports both de-multiplexed address/data busses for maximum bandwidth and minimum latency, and a serial peripheral interface (SPI) mode for low pin-count EtherCAT communication. The slave controller offloads the processing of 100 Mbps Ethernet-based fieldbus communication, thereby, eliminating CPU overhead for these tasks.

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#### 1 Introduction

#### 1.1 Features

- High-Performance Real-Time Control MCU Paired With Low-Latency Ethernet-Based Communication •
- High-Bandwidth, Low-Latency Interface to Beckhoff ET1100 EtherCAT Slave Controller •
- Supports Both Asynchronous Parallel and SPI Connections ٠
- **Glueless Interface** ٠
- Eliminates CPU Overhead for EtherCAT Frame Processing •

#### 1.2 Applications

- Industrial Drives
- Servo Motor Drives ٠
- Manufacturing Robotics
- **CNC Machinery**
- Remote I/O ٠



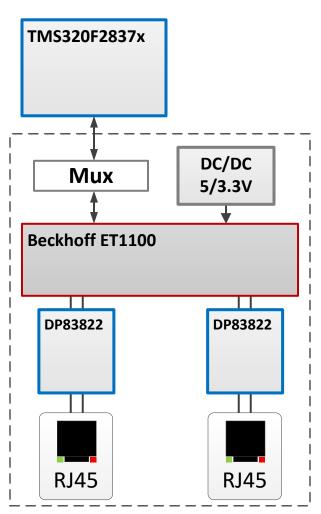


Figure 1. TMDSECATCNCD379D Block Diagram



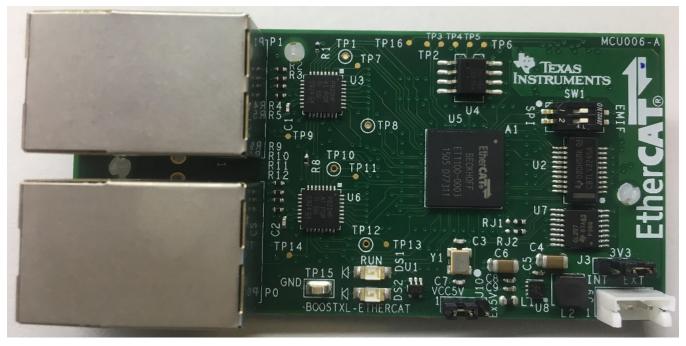


Figure 2. TMDSECATCNCD379D Adapter Board

## 1.3 DesignDRIVE

For more information on DesignDRIVE technology for industrial drive applications, see the following links:

- http://www.ti.com/c2000drives
- http://training.ti.com/c2000-designdrive
- http://www.ti.com/tool/designdrive

## 2 System Overview

## 2.1 System Description

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The TMDSECATCNCD reference design is an adapter board for TI F2837x controlCARDs. When coupled with a C2000 MCU, it uses a Beckhoff ET1100 EtherCAT Slave Controller (ESC) and TI Ethernet PHYs to enable the creation of EtherCAT slave nodes. The adapter board format uses a 60-pin high-density connector that can support both asynchronous parallel and SPI interfaces.

This user's guide illustrates how to set up the EtherCAT adapter board module, initialize the ET1100 subsystem for first use, and install and configure the Beckhoff TwinCAT 3 software for use as an EtherCAT master in a test setup. Example code is provided to configure both SPI and external memory interface (EMIF) interfaces and run simple read and write tests across an EtherCAT network.



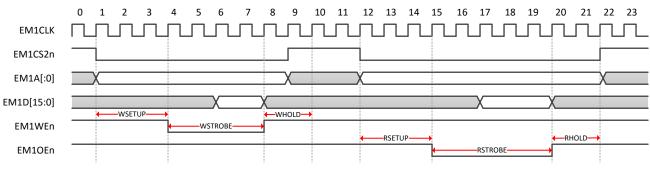
Figure 3. TMDSECATCNCD379D controlCARD and Adapter Board

# 2.2 Key System Specifications

### Table 1. EMIF Configuration and Timing Settings for ET1100 PDI

PARAMETER	DESCRIPTION	VALUE	DELAY <sup>(1)</sup>
ТА	Read-to-Write Turnaround time	1	5 ns
RHOLD	Address and CSn hold after OEn LH edge	1	5 ns
RSTROBE	Read Strobe time in units of EMIF Clocks	64	320 ns
RSETUP	Address and CSn to OEn assertion delay	1	5 ns
WHOLD	Write Hold time after WE deassertion	1	5 ns
WSTROBE	Write Strobe (WE) width	2	10 ns
WSETUP	Address and CSn setup time to WE assertion	1	5 ns
EW	Extended Wait Mode	ENABLE	-
SS	Strobe Select Mode	DISABLE	-

(1) F2837x system with Fsysclk = 200 MHz.







### 2.3 Block Diagram

Figure 6 shows the block diagram of the SPI and EMIF interfaces. In both configurations, the F2837x runs the EtherCAT slave stack while the ET1100 is used to offload the EtherCAT Slave Controller (ESC) frame processing, FMMU, and SyncManager operations.

Certain pins on the ET1100 are used on both the SPI and asynchronous interfaces, which requires the SN74CBTLV3257 mux and SN74CBTLV3245 buffer to steer these signals to the appropriate GPIO on the F2837x MCU.

The EtherCAT adapter board features an on-board DC-DC 5V–3.3V converter, which allows the 3.3V VDD to be either sourced from the C2000 controlCARD or generated locally from an off-board 5V source.

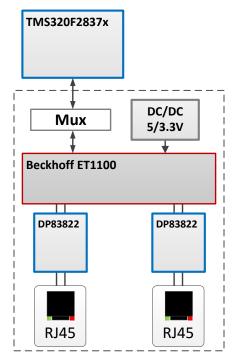


Figure 5. Block Diagram

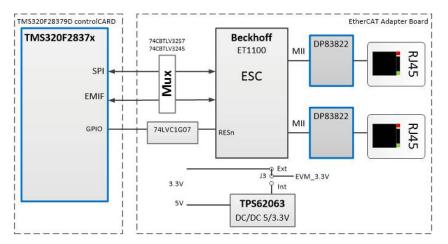


Figure 6. F2837x SPI and EMIF Connections to the EtherCAT Slave Controller

## 2.4 Highlighted Products

#### 2.4.1 TMS320F28379D

The Delfino TMS320F2837x is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as industrial drives and servo motor control; solar inverters and converters; digital power; transportation; and power line communications. Complete development packages for digital power and industrial drives are available as part of the powerSUITE and DesignDRIVE initiatives. The F2837x supports a new dual-core C28x architecture that significantly boosts system performance while integrated analog and control peripherals allow designers to consolidate control architectures and eliminate multiprocessor use in high-end systems.

In the TMDSECATCNCD379D design, the F2837x receives EtherCAT data from the ET1100 through either a serial (SPI) interface or an asynchronous parallel memory interface (EMIF). Figure 7 shows the use of EMIF2, but either EMIF can be used to interface to the ET1100. Note that GPIOs 93 and 94 are for future expansion to address a larger memory space. They are not used in the example code.

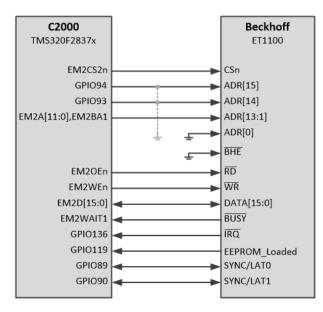
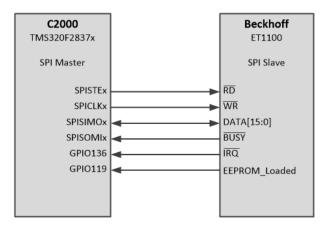


Figure 7. EMIF Interface to ET1100 EtherCAT Slave Controller



## Figure 8. SPI Interface to ET1100 EtherCAT Slave Controller



System Overview

#### 2.4.2 **DP83822**

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The DP83822 is a low power single-port 10/100 Mbps Ethernet PHY. It provides all physical layer functions needed to transmit and receive data over both standard twisted-pair cables or connect to an external fiber optic transceiver. Additionally, the DP83822 provides flexibility to connect to a MAC through a standard MII, RMII or RGMII interface.

### 2.4.3 **TPS62063**

The TPS6206x is a family of highly efficient synchronous step-down DC-DC converters. They provide up to 1.6-A output current. With an input voltage range of 2.7-V to 6-V, the device is a perfect fit for power conversion from 5-V or 3.3-V system supply rails. The TPS6206x operates at 3-MHz fixed frequency and enters power save mode operation at light load currents to maintain high efficiency over the entire load current range. The power save mode is optimized for low-output voltage ripple. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high.

In this reference design, the converter enables power to be supplied from either the controlCARD or an external 5-V source.

#### 2.4.4 SN74LVC1G07

This single buffer/driver is designed for 1.65-V to 5.5-V  $V_{CC}$  operation. The output of the SN74LVC1G07 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

In this design, the open-drain buffer connects a GPIO from the F28379D controlCARD to the ET1100 EtherCAT slave controller reset pin, thereby, enabling independent reset of both devices.

#### 2.4.5 SN74CBTLV3245A

The SN74CBTLV3245A provides eight bits of high-speed bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as one 8-bit switch. When output enable (OE) is low, the 8-bit bus switch is on, and port A is connected to port B. When OE is high, the switch is open and the high-impedance state exists between the two ports.

In this TI Design, the bus switch isolates selected ET1100 outputs from the F28379D controlCARD GPIOs when the EMIF interface is not used (SPI mode). Note that the bus switches are optional in a design using only a single interface type.

## 2.4.6 SN74CBTLV3257

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The SN74CBTLV3257 device is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable (OE) input is high.

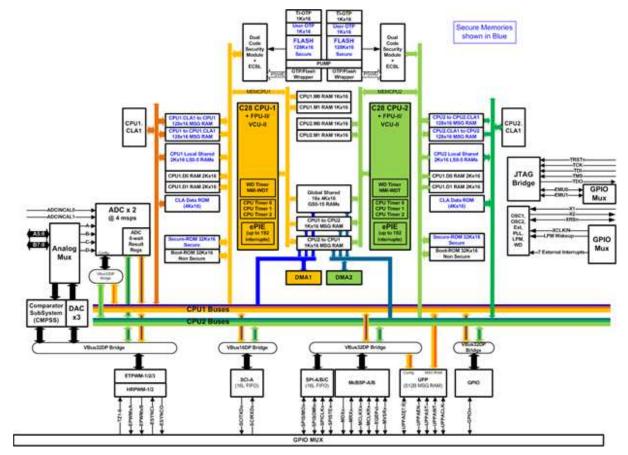
This multiplexer connects selected GPIOs to the ET1100 depending on the interface mode (EMIF or SPI). Note that the multiplexer is optional in a design using only a single interface type.

## 2.4.6.1 Beckhoff ET1100 EtherCAT Slave Controller (ESC)

The ET1100 device is an EtherCAT Slave Controller (ESC). It handles all communications between the EtherCAT fieldbus and the F2837x interface (either SPI or EMIF).

For more information, see http://www.beckhoff.com.





2.4.7 TMS320F2837xD Delfino Microcontroller Functional Diagram

Figure 9. TMS320F2837xD Functional Diagram



#### 2.4.8 Ethernet PHY Functional Diagram

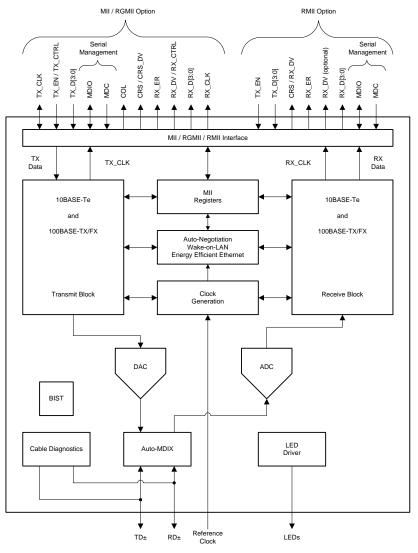


Figure 10. DP83822 Functional Diagram

## 2.4.9 SN74CBTLV3245A Functional Diagram

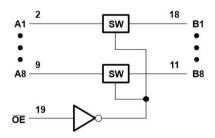


Figure 11. SN74CBTLV3245A Functional Diagram





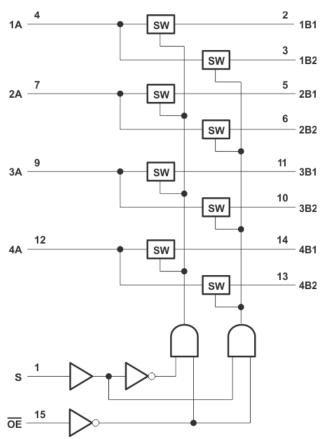


Figure 12. SN74CBTLV3257 Functional Diagram

## 2.4.11 ET1100 Functional Diagram

Bechoff data sheet: http://download.beckhoff.com/download/document/io/ethercat-development-products/ethercat\_et1100\_datasheet\_v1i9.pdf.



Getting Started (Hardware)

### **3** Getting Started (Hardware)

This document describes an F28379D controlCARD adapter board. The adapter board can support either an EMIF or an SPI interface.



Figure 13. Stacked F28379D ControlCard + EtherCAT Adapter Board

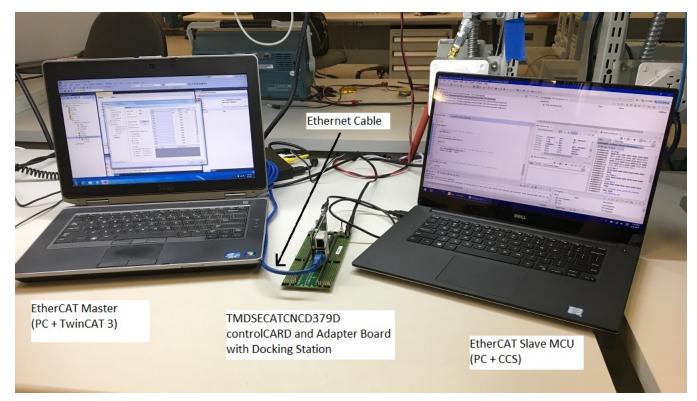


Figure 14. EtherCAT Test Setup



## 3.1 EtherCAT Master Configuration Using TwinCAT3

### 3.1.1 Download and Install TwinCAT3 From the Beckhoff website

The TwinCAT3 software is available from the Beckhoff website at http://www.beckhoff.com. Follow the left sidebar to Download  $\rightarrow$  Software  $\rightarrow$  TwinCAT 3  $\rightarrow$  TE1xxx | Engineering. As of this writing, the most recent version of this software is TwinCAT 3.1 – eXtended Automation Engineering (XAE) v 3.1.4022.0.

### 3.1.2 Verify the TwinCAT Runtime is Active

 Check for the EtherCAT icon in the notification panel in the lower-right corner as shown in Figure 15. If this is absent, open the notification panel and check in the popup window for the TCSwitchRuntime. Right click on this icon and select Tools → TCSwitchRuntime.



Figure 15. TwinCAT Runtime Icon in Windows Toolbar

2. Verify that the TCSwitch Runtime is active. The "Deactivate" button should be showing as illustrated in Figure 16. If this button reads "Activate", click that button to start the TCSwitchRuntime.

TcSwitchRuntime	×						
	Version 1.11						
TwinCAT 3.1 Build 4018 is active							
	-						
Switch Deactivate							
Save Log Clear Log							
MDPUA-Server Service does not exist.							
Starting TF3300 Scope Server TF3300 Scope Server service enabled successfully. Service start pending TF3300 Scope Server started successfully.							
Starting TcAdsSerialCommServer TcAdsSerialCommServer Service does not exist.							
Starting TcAdsWcfHost Service start type is Manual and hence could not be started. **DONE**							

## Figure 16. TwinCAT Runtime Dialog Box

3. If the TCSwitchRuntime is not found in steps 1 and 2 above, then locate the runtime in the file system. A typical location is: "C:\TwinCAT\TcSwitchRuntime\TcSwitchRuntime.exe". Note that it is NOT commonly found in the Start Menu.



Getting Started (Hardware)

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# 3.2 Start TwinCAT3 and Verify That TwinCAT is Running in Visual Studio

- 1. Locate the TwinCAT XAE, which can be found in one of three places:
  - (a) Start menu  $\rightarrow$  under Beckhoff  $\rightarrow$  TwinCAT3  $\rightarrow$  TwinCAT XAE (VS 2010).
  - (b) Desktop icon is shown in Figure 17.



## Figure 17. TwinCAT3 XAE Desktop Icon

(c) Notification panel icon  $\rightarrow$  right click and select TwinCAT XAE (VS 2010).



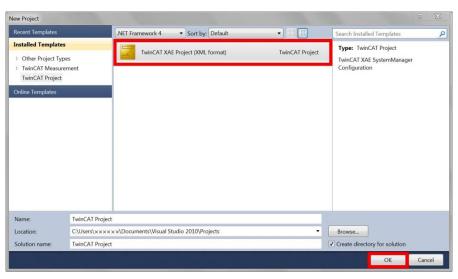
Figure 18. TwinCAT3 Icon in Toolbar

 Verify that TwinCAT is running under Visual Studio. "TwinCAT" and "PLC" should both appear in the main toolbar as shown in 1. If these menu items are not shown, then the TC3 runtime is NOT running. Go back to step Figure 19 to restart the TC3 runtime.

File Edit	View GitExt	Debug	TwinCAT	PLC	Tools	Scope	Window	Help
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Figure 19. Visual Studio Menus for TwinCAT3

- 3. Open a new EtherCAT project.
  - (a) File  $\rightarrow$  New  $\rightarrow$  Project.



## Figure 20. TwinCAT3 New Project Dialog



- 4. Verify that a Realtime Ethernet Adapter is installed.
  - (a) TwinCAT → Show Realtime Ethernet Compatible Devices If no RT adapter is installed, select one from the list of Compatible devices and click "Install", then exit this popup.

hernet Adapters	Update List
Installed and ready to use devices (realtime capable) Local Area Connection - TwinCAT-Intel PCI Ethernet Adapter (Gigabit)	Install
Installed and ready to use devices(for demo use only) Compatible devices	Update
Incompatible devices Wireless Network Connection - DW1520 Wireless N WLAN Half-Mini Card	Bind
S Disabled devices	Unbind
	Enable
	Disable

Figure 21. TwinCAT3 EtherNet Adapter Dialog

- 5. Scan for the newly installed Realtime adapter by clicking TwinCAT  $\rightarrow$  Scan.
  - (a) A popup indicating TwinCAT has found the adapter that should appear (see Figure 22).

he Edit View Project Build Debug TaleCAT PL	C Tooly Surper Window Help	
1-3-3-333 11 13 10-0-5	- 🔄 🕐 Ralease 🔹 TwinCAT ICT (x64) 🔹 🧐 Status	· [47 - 3 - 3 - 3
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olution Explorer X Toolbox		Promition
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III PLC	V Device 2 (EtherGAT) J. and Area Connection (Intel/R) 8(577) M Gepahl Net]	08
III SAFETY		Concel
+ III 50		Select All
<ul> <li>To Devices</li> <li>M Device 2 (OtherCAS)</li> </ul>		

Figure 22. TwinCAT3 Discovery of Ethernet Adapter

(b) Click "OK", then click "Yes" to the following two popups (see Figure 23).

Microsoft Visual Studio	Microsoft Visual Studio
Scan for boxes	Activate Free Run
Yes No	Yes No

Figure 23. TwinCAT3 Master Scan for Slaves and Free Run Activation



(c) The screen view shown in Figure 24 should now be visible in TwinCAT3, indicating that the Master and Slave are connected and prepared for use. Note that "Box 1" appears at the bottom of the image, indicating that TwinCAT has discovered the EtherCAT slave. If this is the first time that the slave has been connected and the EEPROM has not yet been programmed, the "Box n ()" label (for example, "TI\_C2KESC") will not be visible.

🥶 TwinCAT Project - Microsoft Visual Studi	io								and the second secon	_ 0 ×
File Edit View Project Build Debug	g TwinCAT PLC Tools S	cope Windo	w Help							
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Solution Explorer X. Toolbox							-	Properties		+ 4 ×
6								Device 2 (EtherCAT)	EtherCAT Master	
Solution 'TwinCAT Project' (1 project)								a: 01 ( 15)		
Initial Solution TwineAT Project (1 project)     Initial Solution TwineAT Project								<ul> <li>Misc</li> </ul>		
SYSTEM								(Name)	Device 2 (EtherCAT)	
MOTION								Disabled	SMDS_NOT_DISABLED	
PLC								ItemType	2	
SAFETY								PathName	TIID^Device 2 (EtherCAT)	
Green								<ul> <li>Persistent</li> </ul>		
✓ ■ 1/0								SaveInOwnFile	False	
Pevices										
<ul> <li>Device 2 (EtherCAT)</li> </ul>										
17 Image										
Image Info										
SyncUnits										
inputs										
Outputs										
a InfoData								-		
<ul> <li>Box 1 (TI_C2KESC)</li> </ul>								Misc		
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Description		File	Line	Colu	Project					
Creating project 'IwinCAT Project' project	creation successful.									

Figure 24. TwinCAT Solution Explorer Showing EtherCAT Master (Device 2) and Slave (Box1, TI\_C2kESC)

6. The EtherCAT Master is now ready for communication with the Slave device.



## 3.3 Configuring the EtherCAT Adapter Board Interface for EMIF or SPI Operation

The EtherCAT adapter board must be configured prior to power-up to select between the EMIF or SPI interface from the C28x to the ET1100 slave controller. Options for power source and interface type are available through jumpers and/or DIP switches as described in Figure 25 and Table 2.

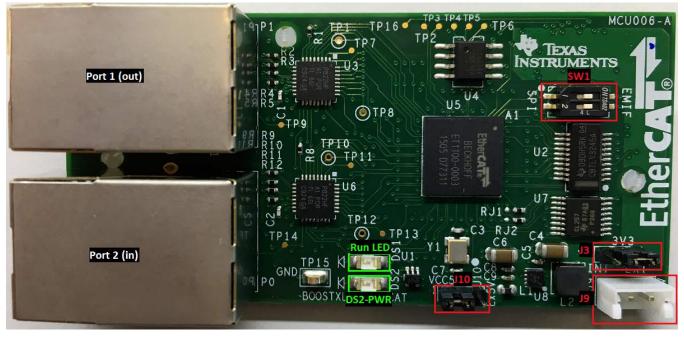


Figure 25. EtherCAT Adapter Board LED and Switch Locations

## Table 2. EtherCAT LED and Switch Usage Descriptions

NAME	OPTIONS	DESCRIPTION
Switches/Jumpers		
SW1	L – SPI R – EMIF	Selects between EMIF and SPI Interface Modes
J3	1-2 off-board 2-3 on-board	Off-board: 3.3 V is provided directly from attached controlCARD On-board: 3.3 V is generated by the on- board regulator from a separate 5 V supply.
LEDs		
RUN LED	State Machine Status <sup>(1)</sup>	Off: ET1100 Device is in INIT state. On: ET1100 Device is in Operational state.
DS2/PWR LED	3.3 V Power	ON indicates 3.3 V is being supplied to the board. For details, see the schematics in Figure 38.

 Additional RUN LED states provided in the ET1100 Digital I/O Signals table of the ET1100 data sheet, which is located at: http://download.beckhoff.com/download/document/io/ethercat-development-products/ethercat\_et1100\_datasheet\_v1i9.pdf.



Getting Started (Hardware)

## 3.4 Preparing the Adapter Board for EtherCAT Communcation Using TwinCAT3

After installing the TwinCAT3 software in the previous section and verifying connectivity between the EtherCAT Master and the slave node, the ESC EEPROM must be programmed to enable communication to the C28x device over either the EMIF or SPI PDI. The following procedure writes the binary file associated with the selected PDI type into the EEPROM:

1. After starting up the TwinCAT software in Section 3.1, the screen should look something like Figure 26. Double clicking the EtherCAT slave (labelled "Box 1" in the figure) brings up the EtherCAT properties window on the right. Click "Advanced Settings".

Contract Project - Microsoft Visual Studio		
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Solution Explorer X Toolbox -	TwinCAT Project	<b>▼</b> ₽>
<ul> <li>Solution 'TwinCAT Project' (1 project)</li> <li>TwinCAT Project</li> <li>SYSTEM</li> <li>MOTION</li> <li>PLC</li> <li>SAFETY</li> <li>C++</li> <li>I/O</li> <li>Devices</li> <li>Device 2 (EtherCAT)</li> <li>Image</li> <li>Image</li> <li>Image</li> <li>Image</li> </ul>	General       EtherCAT       DC       Process Data       Startup       CoE - Online       Online         Type:       TI_C2KESC         Product/Revision:       1414070274 / 18         Auto Inc Addr:       0         EtherCAT Addr:       1001        Advanced Settings         Identification Value:       0          Previous Port:       Master	
<ul> <li>SyncUnits</li> <li>Inputs</li> <li>Outputs</li> <li>InfoData</li> <li>Box 1 (TI_C2KESC)</li> </ul>	Name         Online         Type         Size         >A         In/         Us         Linked to                Switch 1          0          BIT          0.1          39.0          Inp          0                Switch 2          0          BIT          0.1          39.1          Inp          0                Switch 3          0          BIT          0.1          39.2          Inp          0                 Switch 3          0          BIT          0.1          39.2          Inp          0                 TwinCAT Project                             TwinCAT Project	▼ ₽ 2
O Errors 1 0 Warnings 0 O Mess Description File	ages Clear Line Colu Project	

Figure 26. TwinCAT Project EtherCAT Tab



2. In the advanced settings popup windows, select "Smart View" to bring up detailed information about the EtherCAT Slave PDI. Click "Write E2PROM". Note that, prior to initialization, this view shows a "blank" configuration.

General	Smart View				
- Behavior - Timeout Settin	Config Data (evaluated t	rom ESC)	Device Identity (hex)		
- Identification	E <sup>2</sup> PROM Size (Byte):	128 👻	Vendor Id:	0x000000	00
-FMMU / SM	PDI Type:	0 👻	Product Code:	0x000000	00
-Init Command Mailbox	Device Emulation	n (state machine emulation)	Revison No.:	0x000000	00
Distributed Clock	SPI / 8 / 16 µC Interfa	Ce	Serial No.:	0x000000	00
ESC Access	BUSY Open Dra	in BUSY High Active	Product Revision:		
Configured	32 Bit Interface		Mailbox		
- Enhanced Li	WD Open Drain	WD High Active	CoE SoE	EoE	FoE
-Hex Editor -FPGA	Input Latch		Bootstrap Configuration		
Memory	Sync Signal Configura	ation	Out Start/Length:	0	0
	SYNC0 Open Dr	ain SYNC0 High Active	5		
	SYNC0 Enabled	SYNC0 to PDI IRQ	In Start/Length:	0	0
	SYNC1 Open Dr	-	Standard Configuration		
	SYNC1 Enabled		Out Start/Length:	0	0
	Impulse Length (µs)	0	In Start/Length:	0	0
	Write E <sup>2</sup> PROM	Read E <sup>2</sup> PROM			
< III >					

Figure 27. TwinCAT "Smart View" Slave Properties Window Showing Blank Slave

- 3. Click "Browse" to find the desired EEPROM binary associated with either the SPI or EMIF interface in the TMDSECATCNCD379D\_PDI\_HAL\_API directory downloaded from the project site.
  - (a) pdi\_test\_app\_spi.bin for SPI interface
  - (b) pdi\_test\_app\_emif.bin for EMIF interface
  - (c) Click "OK".



Figure 28. TwinCAT3 EEPROM File Dialog



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4. After TwinCAT writes the EEPROM (in this case for the SPI), the following "Smart View" window showing a valid configuration with PDI Type = "SPI slave" should appear (see Figure 29).

Advanced Settings			×
<ul> <li>General</li> <li>Mailbox</li> <li>Distributed Clock</li> <li>ESC Access</li> <li>E<sup>2</sup>PROM</li> <li>Configured</li> <li>Enhanced Li</li> <li>Smart View</li> <li>Hex Editor</li> <li>FPGA</li> <li>Memory</li> <li>S2 Bit Interface</li> <li>WD Open Drain</li> <li>INT High Active</li> <li>INT High Active</li> <li>Input Latch</li> <li>Sync0 Open Drain</li> <li>SYNC0 High Active</li> <li>SYNC0 to PDI IRQ</li> <li>SYNC1 Copen Drain</li> <li>SYNC1 to PDI IRQ</li> <li>Impulse Length (µs):</li> <li>0.100</li> </ul>	Device Identity (hex) Vendor Id: Product Code: Revison No.: Serial No.: Product Revision: Mailbox CoE SoE AoE Bootstrap Configuration Out Start/Length: In Start/Length: In Start/Length: In Start/Length:	0x0000058 0x5449000 0x000000 0x0200000 EoE 4096 5120	02 12
4 111 >			OK Cancel

## Figure 29. TwinCat "Smart View" Slave Properties Window Showing Programmed EEPROM

5. The EtherCAT Slave controller is now prepared for communication with the MCU.



# 3.5 EEPROM Configuration Values

The first 15 bytes of the EEPROM hold MCU-related configuration. This is readable via several ESC register addresses. The options used in these demonstrations are:

ESC Register Address[Bit]	Value	Description
Common Settings	I	!
0x140	0x05 – SPI 0x08 – EMIF	PDI type
0x141[0]	Off	Device emulation
0x141[1]	All Ports On	Enhanced Link Detection
0x141[3:2]	DC Latch + Sync Unit	DC Units power saving
ASYNC16 Settings		· · · · · · · · · · · · · · · · · · ·
0x150[1:0]	Push-pull active high	BUSY output driver/polarity
0x150[3:2]	Push-pull active low	IRQ output driver/polarity
0x150[4]	Active low	BHE polarity
0x150[7]	Active low	RD polarity
0x152[0]	Normal delay	Read BUSY delay
0x151[2]	LATCH input	SYNC0/LATCH0
0x151[3]	On	Map to AL Event Request
0x151[6]	LATCH input	SYNC1/LATCH1
0x151[7]	On	Map to AL Event Request
SPI Settings	L	
0x150[1:0]	Mode 3	SPI mode
0x150[3:2]	Push-pull active low	SPI_IRQ output driver/polarity
0x150[4]	Active low	SPI_SEL polarity
0x150[5]	Normal sample	Data Out sample mode
0x151[1:0]	Push-pull active low	Output driver/polarity
0x151[2]	SYNC output	SYNC0/LATCH0
0x151[3]	On	Map to AL Event Request
0x151[5:4]	Push-pull active low	Output driver/polarity
0x151[6]	SYNC output	SYNC1/LATCH1
0x151[7]	On	Map to AL Event Request

#### Table 3. EEPROM MCU Configuration

## 4 Getting Started (Firmware)

- → → ↑ 📊 « development\_kits → TMDSECATCNCD379DKIT →

Generated\_SSC

- SSCToolC28xPatch
- TMDSECATCNCD379D\_EchoBack\_Demo
- TMDSECATCNCD379D\_EtherCAT\_Solution\_Ref
- TMDSECATCNCD379D\_PDI\_HAL\_API

### Figure 30. TMDSECATCNCD379DKIT controlSUITE Folders



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The firmware package for this kit consists of a Process Data Interface (PDI) demo using the hardware abstraction layer (HAL), C2000 patches for the Beckhoff slave stack code (SSC), a reference project for the SSC, and a precompiled echo-back demo that uses the patched SSC. All of this software is designed for C2000 F2837x MCUs. Each demo has build configurations for SPI and EMIF. To change between these interfaces, set both of the switches in switch block SW1 (Figure 25) on the adapter board accordingly.

The PDI demo sets up and tests basic communication between the EtherCAT master and the EtherCAT slave controller. The echo-back demo shows an example of higher-level communication between the master and slave.

- **NOTE:** For EtherCat Developers: The EtherCAT Technology Group (ETG) recommends membership for parties implementing EtherCAT in a machine or machine line. For additional information about EtherCAT and ETG membership, see the following links:
  - EtherCAT FAQs: https://www.ethercat.org/en/faq.html
  - EtherCAT Technology Group site: https://www.ethercat.org

## 4.1 PDI HAL Test Demo

The PDI test application contains a hardware abstraction layer (HAL) that handles all of the configuration details for the EMIF or SPI interface. This Code Composer Studio<sup>TM</sup> (CCS) 7.x project also performs some simple read/write tests to verify correct functioning of communication with the ET1100 slave controller.

The CCS project files for pdi\_hal\_test\_app can be downloaded from the design directory at http://www.ti.com/tool/TMDSECATCNCD379D. The files install into the C:\TI\controlSUITE\development\_kits\TMDSECATCNCD379DKIT directory. Once downloaded, import this project into CCS 7.0 or later using the procedure below:

- 1. File  $\rightarrow$  Import... (an "Import" popup window appears).
- 2. Select "Code Composer Studio" → CCS Projects. Click "Next".
- 3. Use "Select search-directory" and click "Browse" to find the pdi\_hal\_test\_app source directory.
- 4. Select pdi\_hal\_test\_app from the list of Discovered projects:
  - (a) Leave the "Automatically import referenced projects" box checked.
  - (b) Checking the box for "Copy projects into workspace" is optional.
  - (c) Click "Finish". The CCS project will appear in the project explorer window.

### 4.1.1 Test Setup

The main purpose of this test is to demonstrate the usage of the PDI between the C28x processor and the ET1100 EtherCAT Slave Controller.

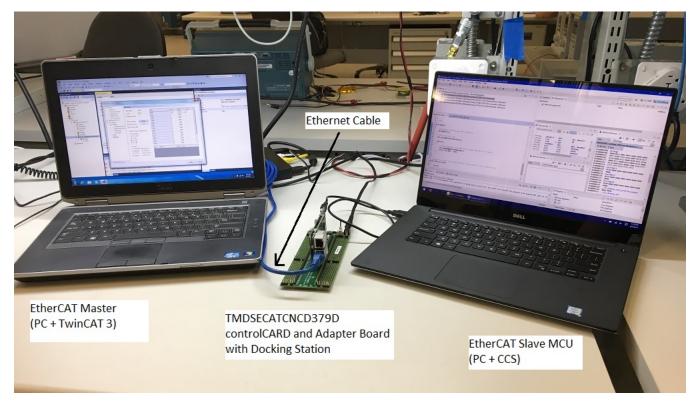


Figure 31. EtherCAT Test Setup

The test setup in Figure 31 shows a C2000 F28379D controlCARD with attached EtherCAT adapter board and two PCs. The left PC connects to the adapter board through a standard Ethernet cable connected to Port 0, and runs TwinCAT 3 software, which provides EtherCAT Master functionality. The right PC connects to the controlCARD directly through the USB connector and runs the EtherCAT Hardware abstraction layer (HAL) software on the CCS 7.x development environment. The HAL software in this example performs the following functions:

- Initialize the C28x hardware and the selected PDI interface (SPI or EMIF)
- Execute reads/writes to the ET1100 User RAM
- Execute reads from ET1100 register space

The intent of this project is to demonstrate the usage of the PDI. Therefore, no EtherCAT stack is included in this demo.

Note that the HAL software supports both the SPI and EMIF as PDI interfaces. The user must choose the proper settings when building the project. Correct jumper settings on the adapter board are also required for proper operation. These settings are described in Section 3.3.



Getting Started (Firmware)

## 4.1.1.1 Running Simple ESC Interface Test on C28x

After downloading the software from the project directory at http://www.ti.com/tool/TIDM-DELFINO-ETHERCAT and importing the project into CCS, perform the following steps to exercise the PDI HAL:

1. Open the example project pdi\_hal\_test\_app in CCS. The file pdi\_test\_appl.c has the main routine. The following code is of interest:

ESC_HWInit()	Initializes the C28x MCU and the PDI
ESC_setupPDITestInterface()	Set-up PDI interface and initialize test variables and ET1100 RAM over PDI
ESC_debugUpdateESCRegLogs()	Keep updating ET1100 registers in a loop. User can add to the list of registers to read in the escRegs data structure.

```
80 void main()
81 {
82
       //Initialize C28x MCU and HAL interface
83
      ESC_HWInit();
84
85
      //setup PDI for test
86
      ESC_setupPDITestInterface();
87
88
      while(1)
89
      {
90
           //Keep updating local RAM with ET1100 registers for debug
91
           ESC_debugUpdateESCRegLogs();
92
          DELAY_US(1000 * 500);
93
      }
94
95 }
```

## Figure 32. CCS Example Project: pdi\_hal\_test\_app

 Right click on the project and set the desired active build configuration. Figure 33 shows the available configurations, which provides options for program storage (flash and RAM) and interface type (EMIF, SPI-C):



Project Exp	alorer 🕅	
	I_test_app [Active4_F2837xl	D_CCARD_SPIC_RAMJ
> 🐰 Bin		
> 🔊 Inc		Build
	F2837xD_CCARD_EMIF_FLASH	2
		configurations
	F2837xD_CCARD_SPIC_FLASH	
	F2837xD_CCARD_SPIC_RAM	
🗸 🥟 apt	•	
	pdi_test_appl.c	
	pdi_test_appl.h	
🗸 🦳 🗸		
· · · · · · · · · · · · · · · · · · ·	2837x_RAM_Ink_cpu1_big.cmd	
	2837x_FLASH_Ink_cpu1.cmd	
🗸 🗸 🗸		
	etherCAT_slave_c28x_hal.c	
	etherCAT_slave_c28x_hal.h	
	F2837xD_CodeStartBranch.asm	
	F2837xD_CpuTimers.c	
	F2837xD_DefaultISR.c	
	F2837xD_device.h	
	F2837xD_Emif.c	
	F2837xD_GlobalVariableDefs.c	
	F2837xD_Gpio.c	
	F2837xD_PieCtrl.c	
	F2837xD_PieVect.c	
	F2837xD_Spi.c	
	F2837xD_SysCtrl.c	
	F2837xD_usDelay.asm	
> .h	F28x_Project.h	

Figure 33. EtherCAT HW Abstraction Layer Project



Getting Started (Firmware)

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For this example, choose build configuration (4\_F2837xD\_CCARD\_SPIC\_RAM) by right clicking on the project name and selecting "Build Configuration"  $\rightarrow$  Set Active  $\rightarrow$  (4 F2837xD\_CCARD\_SPIC\_RAM).

Start TwinCAT3 on the EtherCAT Master PC as described in Section 3.2. Note that double clicking the EtherCAT slave node ("Box 2" in Figure 34) opens up a properties windows, from which the "Advanced Settings window" can be opened. This is used later in the demo.

ION	General	Memory							
TY Behavior									
	- Timeout Settings	Start Offset:	0	Offs		Dec	Hex	Cha	ar 🔒
	Identification	Length:	0400	0000 E	SC Rev/Type	17	0011	4	1.003
vices Device 2 (EtherCAT)	-FMMU / SM -Init Commands	Working Counter:	1	0002 ESC Build		3	0003		
Image	Distributed Clock			0004 S	M/FMMU Cnt	2056	0808		
Image-Info	ESC Access	Auto Reload	Reload	0006 P	orts/DPRAM	3848	0f08		
SyncUnits Inputs	E <sup>2</sup> PROM FPGA	Compact View	Write	0008 F		252	00fc		
Outputs	Memory	Use Fixed Addr				0 000			
InfoData		EtherCAT Slave C	ontroller Type	000c		0 000			
<ul> <li>Box 2 (P00000001 R03160001)</li> <li>appings</li> </ul>		Cunspecified		000e 0010 Phys Addr		0 0			
abhurða						0	0000		
		IP core		0012 Configured Statio 0014		0	0000		
		ET1100 ET1200				0	0000		
		Erizoo		0016		0 00			*
		PDI Type	16 µC (8, a)	Bits	Name		Value	Enum	
		O Unspecified O Digital (4)	6 16 μC (0, a)	0-7	FMMU cnt		8	2502500	
		© SPI (5)	① 16 μC (10, s)	8-15	SM cnt		8	-	
	Bridge (7)	@ 8 µC (11. s)	0.12	Jamene	_	0			

Figure 34. TwinCAT3 Advanced Settings Dialog

3. Start the debugger and open the memory browser window as shown in Figure 35. The "escRegs" data array contains a list of ET1100 register addresses and values. These get updated in the *ESC\_debugUpdateESCRegLogs()* function.

le pdi_test_appl.c		Memory Browser      E      Disassembly	13 18 V P
<pre>1085 ESC_debugAddESCRegsAddress(0x100 /*, "dlc1", 4*/);</pre>		Data - escRegs	8
<pre>1086 ESC_debugAddESCRegsAddress(0x102 /*, "dlc2", 4*/);</pre>		Data:0x121c2 - 0x000121C2 <memory 1="" rendering=""> 13</memory>	
<pre>1087 ESC_debugAddESCRegsAddress(0x110 /*, "dls", 2*/);</pre>		16-Bit Hex - TI Style	
1088 ESC_debugAddESCRegsAddress(0x310 /*, "llc1", 2*/);			
<pre>1089 ESC_debugAddESCRegsAddress(0x312 /*, "llc2", 2*/); 1090 ESC_debugAddESCRegsAddress(0xE00 /*, "porv", 4*/);</pre>		0x000121C2 escRegs	
<pre>1090 ESC_debugAddESCRegsAddress(0xE00 /*, "porv", 4*/); 1091 ESC debugAddESCRegsAddress(0x510 /*, "miis", 4*/);</pre>		0x000121C2 0000 FFFF 0002 FFFF 0004 FFFF 0008 FFFF 0100 FFFF 0102 FFFF 0110 FFFF 0310 FFFF 0312 FFFF 0E00 FF	FF 0510
1092 ESC debugAddESCRegsAddress(0x512 /*, "mils", 4 7);		0x000121D7 FFFF 0512 FFFF 0514 FFFF 0516 FFFF 0518 FFFF 051A FFFF 1000 FFFF FFFF FFFF FFFF FFFF FF	
1093 ESC debugAddESCRegsAddress(0x514 /*, "phyd", 4*/);		0x000121EATI_cleanup_ptr 0x000121EA 0000 0000	
1094 ESC debugAddESCRegsAddress(0x516 /*, "mila", 4*/);		0x000121ECTI_dtors_ptr	
<pre>1095 ESC_debugAddESCRegsAddress(0x518 /*, "port0", 5*/);</pre>		0x000121EC 0000 0000	
<pre>1096 ESC_debugAddESCRegsAddress(0x51A /*, "port1", 5*/);</pre>		0x000121EE lock	
<pre>1097 ESC_debugAddESCRegsAddress(0x1000 /*, "RAM address", 11*/);</pre>		9x000121EE 91B4 0000	
1098		0x000121F0 unlock	
1099		0x000121F0 91B4 0000 0000 0000 0000 0000 0000 0000 0	
1100 //Now wait till EEPROM is loaded		0x00012200 CpuTimer1	
1101 do		0x00012200 0C08 0000 0000 0000 0000 0000 0000	
1102 { 1103 pdi control = ESC readWordNonISR(0x0140 /*ESC PDI CONTROL OFFSET*/):		0x00012208 CpuTimer2	
<pre>pdi_control = ESC_readWordNonISR(0x0140 /*ESC_PDI_CONTROL_OFFSET*/); 1104#ifdef INTERFACE SPI</pre>		0x00012208 0C10 0000 0000 0000 0000 0000 0000 00	
1105 } while (((pdi control & 0xFF) != 0x05)); //SPI PDI		0x00012210 CpuTimer0	
1106 #else		0x00012210 0C00 0000 0000 0000 0000 0000 0	
1107 } while (((pdi control & 0xFF) != 0x08)); //EMIF PDI		0x00012223 0000 0000 0000 0000 0000 0000 0	
1108 #endif		0x0001225F 0000 0000 0000 0000 0000 0000 0000	
1109			
1110		0x00012279 0000 0000 0000 0000 0000 0000 0000	0000 0000
1111 // NOW EEPROM is loaded and PDI is either EMIF (16 bit) or SPI.	Ξ.	0x0001228E 0000 0000 0000 0000 0000 0000 0000	00 0000
1112 // ET1100 RAM read/write tests; On ET1100 RAM being at 0x1000 and can go up to 0x6	FFF	0x000122A3 0000 0000 0000 0000 0000 0000 0000	00 0000
1113	Ŧ	0x00012288 0000 0000 0000 0000 0000 0000 0	000000
( III	- F	0x000122CD 0000 0000 0000 0000 0000 0000 0000	00 0000

Figure 35. Device Debug Memory Window at INIT Time

**NOTE:** The ESC RUN LED will NOT be on during the memory tests, which is described in the following sections. For more information, see the ET1100 data sheet.

#### ESC RAM READ TEST



4. Open up the "advanced settings" window in TwinCAT3 and go to the memory browser at ESC Access → Memory and view Start Offset = 1000h as shown in Figure 36.

🗇 General	Memory								_				
-Behavior Timeout Settings	Start Offset.	1000	Offs		Dec	-							
Identification	Length:	0400	1000		4660		Offs			Des	11	Char	
- FMMU / SM Init Commands	Working Counter:	1	1002		22136		Uns			Dec	Hex	Char	=
Distributed Clock		Reload	1004		0		1000			4660	1234	4.	
ESC Access	Auto Reload	Write	1006		0		1002			22136	5678	xV	
FPGA	Use Fixed Addr	vynie	1008		0		1002			22130		~*	
Memory			100a		0		1004			0	0000		
		EtherCAT Slave Controller Type	11		1006	1006		0	0000				
	O Unspecified		100e		0								
	IP core		1010		0	0000							
	ET1100 ET1200		1012 1014		0	0000							
	@E11200		1014		0	0000			*				
	PDI Type	@ 16 uC (8 a)	Bits	Name		Value	Enum						
	Digital (4) SPI (5) Bridge (7)	© 16 μC (0, a) © 8 μC (9, a) © 16 μC (10, s) © 8 μC (11, s)											

Figure 36. TwinCAT3 Memory Read Window

5. In CCS, view the Expressions window and add "escRegs" as a watched expression. Note that, as data is entered into the window in TwinCAT, the values read on the CCS side are identical.

		🔋 Memory Browser 📟 Disas	sembly 📽 Expressions 🛛		
		Expression	Туре	Value	Address
☐ pdi_test_applc	Memory Br Expression	🛛 🥏 escRegs	struct esc_et1100_re	0x000121C2@Data	0x000121C2@Da
<pre>1122 //please refer to ET1100 datasheet for more details 1123 for (test_address = ESC_PDI_RAM_START_ADDRESS_OFFSET; test_address &lt;= ESC_PDI_RAM_END</pre>	<ul> <li>escRegs</li> <li>test_adc</li> </ul>	⋈• test_address	unsigned long	0x00001000 (Hex)	0x0000040A@Da
1124 #endif 1125 { 1126 -	Intest_da	ø⊧ dtest_data	unsigned long	0x56781234 (Hex)	0x00000408@Da
1127     dtest_data = ESC_readDNordNonISR(test_address);       1128     ESC_writeDNord(NMEADF00D, test_address);       1129     dtest_data = ESC_readDNordNonISR(test_address);		Add new expression			
<pre>1130 1131 1132 1133 1133 1133 1133 1134 1134</pre>	ddress); test_add				

## Figure 37. EtherCAT Write to Memory From CCS Project

## ESC RAM WRITE TEST



#### Getting Started (Firmware)

6. Figure 38 shows program control after execution of the first 32-bit write and 32-bit read from PDI to ET100 address 0x1000.

	/	🕽 Memory Browser 📟 Disas	ssembly 👫 Expressions 🛛		
	/	Expression	Туре	Value	Address
a pdi_test_applc 🛙 🗟 ethercat_slave_c28x_halc 🕸	U Memory brow	🖻 🥏 escRegs	struct esc_et1100_re	0x000121C2@Data	0x000121C2@Da
1121 // which is equivalent to 0x2800 to 0x2FF of the C28x EMIF2 address space. //please refer to ET1100 dataSheet for more details 1123 for (test_address = ESC_PDI_RAW_START_ADDRESS_OFFSET; test_address <= ESC_PDI_RAM_END	Expression	(x)= test_address	unsigned long	0x00001000 (Hex)	0x0000040A@Da
1122 Tor (test_audress = Est_Poi_num_sinkt_numess_orrst; test_audress k= Est_Poi_num_enu 1124#endif 1125 {	test_addres     dest_data     Add new ex	(x)= dtest data	unsigned long	0xBAADF00D (Hex)	0x00000408@Da
1126 1127 dtest_dnesESC_readDWordNonISR(test_address); 1128 ESC_writeDWord(0xDrawr000_test_address);	Add new ex	🖶 Add new expression			
ESC_writeDWord(0)	xBAADF00 _readDWo	rdNonISR(test_addre D, test_address); rdNonISR(test_addre _t)0xBAADF00D)			

Figure 38. CCS Project Write to EtherCAT Slave

7. The TwinCAT Master view of the ESC memory address showing the results of the write from CCS.

General	Memory										
-Behavior - Timeout Settings	Start Offset	1000	Offs	Offs				Dec		Hex	Char
Identification FMMU / SM Init Commands	Length: Working Counter:	1	1000 1002	1000				61453		f00d	
ESC Access ESC Access	Auto Reload	Reload		1002				47789		baad	
- FPGA - Memory	Use Fixed Addr			1004				0		0000	
	EtherCAT Slave C Unspecified ESC 10/20	ontroller Type	100c 100e 1006					0		0000	
	IP core		1010		0	0000			_		
	ET1100 ET1200		1012 1014		0	0000					
	PDI Type		1016		0	0000	-	1	<b>T</b>		
	Cunspecified Digital (4) SPI (5) Bridge (7)	<ul> <li>● 16 µC (8. a)</li> <li>● 8 µC (9. a)</li> <li>● 16 µC (10. s)</li> <li>● 8 µC (11. s)</li> </ul>	Bits	Name		Value	Enum				

Figure 39. TwinCAT3 Master Read of Data Written to EtherCAT Slave

## 4.1.1.2 TwinCAT3 Troubleshooting

Common issues in TwinCAT3 usage:

- Problem: EtherCAT network fails to initialize
  - Other Descriptions: "Reload Devices" fails, "Scan" for devices fails, "Restart EtherCAT in config mode" fails.
- Solutions:
  - Power-cycle the controlCARD
  - Check to make sure a RealTime Ethernet Driver is available.
    - $\label{eq:twinCAT} \text{TwinCAT} \rightarrow \text{``Show RealTime Ethernet Compatible Devices''. This opens a popup window below.}$
    - Look for the first line "Installed and ready to use devices (realtime capable)".
       In this example, there are NO adapters installed!
    - Select a compatible device; here it is "Local Area Connection  $\rightarrow$  Intel ...." and click "Install".
    - Close the window by clicking "X" in the upper right corner.



hernet Adapters	Update List
Installed and ready to use devices(realtime capable)	Install
Compatible devices     Local Area Connection - Intel(R) Ethernet Connection (3) I218-LM #3	Update
Incompatible devices Wireless Network Connection - Intel(R) Dual Band Wireless-AC 7265 Q Disabled devices	Bind
	Unbind
	Enable
	Disable
	Show Bindings

Figure 40. TwinCAT3 Ethernet Adapter Installation



#### Getting Started (Firmware)

#### 4.1.2 Other Interfaces

It is possible to use EMIF1, SPI-A, or SPI-B to communicate with the ET1100, although the F28379D controlCARD and adapter board hardware do not support this directly. This functionality is implemented in the software and can be used on a custom board.

To use EMIF1, select one of the EMIF build configurations (\_1\_F2837xD\_CCARD\_EMIF\_FLASH or \_2\_F2837xD\_CCARD\_EMIF\_RAM). Uncomment the #define for USE\_EMIF1 on line 526 of etherCAT\_slave\_c28x\_hal.h:

525 //LAUNCHXL Rev2.0 J9 connector option for accessing ET1100 526 / /#define USE\_EMIF1 See Uncomment 527 528 #ifdef CONTROLCARD //for Controlcard definitions 529 #ifdef INTERFACE SPI 530 531 #ifdef USE\_EMIF1 532 #error "user cannot use EMIF1 with SPI Configurations of project" 533 #endif 534 extern void ESC\_SPIInit(void); extern void ESC\_SPIRead(uint16\_t offset\_addr,uint16\_t numbytes, uint16\_t\* buffer); 535 extern void ESC\_SPIWrite(uint16\_t offset\_addr,uint16\_t \*wrdata, uint16\_t numwords) ; 536 537 #define ESC\_SPI\_INT\_GPI0 136 538 539 //on ET1100 it is 8KB of RAM 540 #define ESC PDI RAM START ADDRESS OFFSET 541 0x1000 #define ESC\_PDI\_RAM\_END\_ADDRESS\_OFFSET 0x2FFF 542 543 544 #define ESC SYNC0 GPIO 113 545 #define ESC SYNC1 GPIO 114 #define ESC\_RESET\_ET1100\_GPI0 546 137 #define ESC\_EEPROM\_LOADED\_GPIO 547 119 548 #else //#ifdef INTERFACE\_SPI 549 550 551 extern void setup\_emif1\_pinmux\_async\_16bit(Uint16 cpu\_sel); extern void ESC\_EMIF2SetupPinmuxAsync16Bit(Uint16 cpu\_sel); 552 extern void ESC\_EMIF2WriteBlock(uint16\_t\* pData, uint16\_t offset\_addr,uint16\_t numwords); 553 554 #ifdef USE EMIF1 //LaunchPAD XL EMIF1 J9 connector option 555 556 //on ET1100 it is 8KB of RAM #define ESC\_PDI\_RAM\_START\_ADDRESS\_OFFSET 557 0x1000 #define ESC\_PDI\_RAM\_END\_ADDRESS\_OFFSET 558 0x2FFF #define ESC\_EMIF\_INT\_GPIO 559 107 #define ESC\_SYNC0\_GPI0 560 86 561 #define ESC\_SYNC1\_GPI0 87 #define ESC\_RESET\_ET1100\_GPI0 562 108 #define ESC\_EEPROM\_LOADED\_GPIO 52 //this was 33 on LAUNCXL Rev1.1 563 564 #else // #ifdef ESC USE EMIF1 //USE EMIF2 565

Figure 41. Code Change for Using EMIF1



To use another SPI module, select one of the SPI build configurations (\_3\_F2837xD\_CCARD\_SPIC\_FLASH or \_4\_F2837xD\_CCARD\_SPIC\_RAM). Add USE\_SPIA or USE\_SPIB to the predefined symbols list in the project build options. Remove USE\_SPIC from the list:

General	
✓ Build	
<ul> <li>C2000 Compiler</li> </ul>	Configuration: _4_F2837xD_CCARD_SPIC_RAM [ Active ]
Processor Options	
Optimization	
Include Options	
Performance Advisor	Pre-define NAME (define, -D)
Predefined Symbols	CPU1
> Advanced Options	PDI_HAL_TEST Remove USE_SPIC, add
> C2000 Linker	INTERFACE_SPI USE_SPIA or USE_SPIB
C2000 Hex Utility [Disabled]	CONTROLCARD
C2000 Hex Oulity [Disabled]	USE_SPIC

## Figure 42. Project Configuration Change for Using SPI-A or SPI-B

This change affects the code in etherCAT\_slave\_c28x\_hal.c:

1032	//	
1033	<pre>#ifdef INTERFACE_SPI</pre>	
1034	//TxCnt=0;	Define USE_SPIA or
1035	<pre>SPI_XmitInProgress=0;</pre>	USE SPIB in the project
1036		=
1037	<pre>//InitSpiaGpio();</pre>	build options
1038	#ifdef USE_SPIA	
1039	<pre>SpixRegs = &amp;SpiaRegs</pre>	
1040	ESC_SPIAGpioInit();	
1041	#elif USE_SPIC	
1042	<pre>SpixRegs = &amp;SpicRegs</pre>	
1043	ESC_SPICGpioInit();	
1044	#else	
1045	<pre>SpixRegs = &amp;SpibRegs</pre>	
1046	ESC_SPIBGpioInit();	
1047	#endif	
1048	ESC_SPIInitFIF0();	

### Figure 43. SPI Selection and GPIO Configuration Code



Getting Started (Firmware)

#### 4.2 EchoBack Demo

The EchoBack demo is a precompiled demonstration of the slave stack code. It emulates a bank of switches (inputs) and LEDs (outputs). The master controls the LEDs. The slave loops back the virtual LED signals into the virtual switches, so the master can read back the output state.

ent_kits  TMDSECATCNCD379DKIT  TMDSECATCNCD379D_EchoB	ack_Demo
New folder	
Name	Date
expressions_window_inputsOuputs.txt	6/29
TMDSECATCNCD379D EtherCAT slave (ASYNC16).xml	7/25
TMDSECATCNCD379D EtherCAT slave (SPI).xml	7/25
TMDSECATCNCD379D_EchoBack_Demo_ASYNC16_FLASH.out	8/9/
TMDSECATCNCD379D_EchoBack_Demo_SPI_FLASH.out	8/9/
TMDSECATCNCD379D_EchoBackDemo_Manifest.txt	7/25

#### Figure 44. EchoBack Demo Files

#### 4.2.1 Slave Setup

On the slave side, simply load the .out file for the chosen interface (ASYNC16 or SPI) using the CCS debugger. Run the program. To observe the variables, right-click in the Expressions window and choose Import. Select the expressions\_window\_inputsOutputs.txt file from the EchoBack demo directory, which is shown above.

#### 4.2.2 Master Setup

The first step on the master side is to program the ET1100's EEPROM using TwinCAT. Unlike the PDI demo, this time the EEPROM is programmed using provided XML files, which can be seen in the directory listing above. Copy these XML files into the C:\TwinCAT\3.1\Config\lo\EtherCAT directory. Follow the same procedure as for the PDI demo (described in the Getting Started (Hardware) section of this document), but instead of clicking on Browse to select a binary EEPROM file, choose the appropriate TI option from the Available EEPROM Descriptions.

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Write EEPROM	×
Available EEPROM Descriptions:	OK Cancel
	Browse

## Figure 45. EchoBack EEPROM Configurations

Once the EEPROM is programmed, scan for devices again. If you've previously used another EtherCAT configuration such as the PDI demo, you will be prompted to overwrite the box description. To do so, click on Copy All, then OK.



nd Items:	Disable >	Configured Items:
TI Box 2 (TMDSECATCNCD379D EtherCAT slave (ASYNC16))	Ignore > Delete >	Box 1 (P00000001 R03160001)
	> Copy Before >	
	> Change to >	
	OK Cancel	

Figure 46. Overwriting Box Information

If the demo is running on the slave slide, a TwinCAT master can be used to toggle the LEDs and read the switch states. To toggle an LED, expand the box in the Solution Explorer pane. Click on "LEDs process data mapping" to see a list of the LEDs. Right-click on an LED and choose one of the Online Write options to set the LED value. The written value should appear immediately in the list.



Getting Started (Firmware)

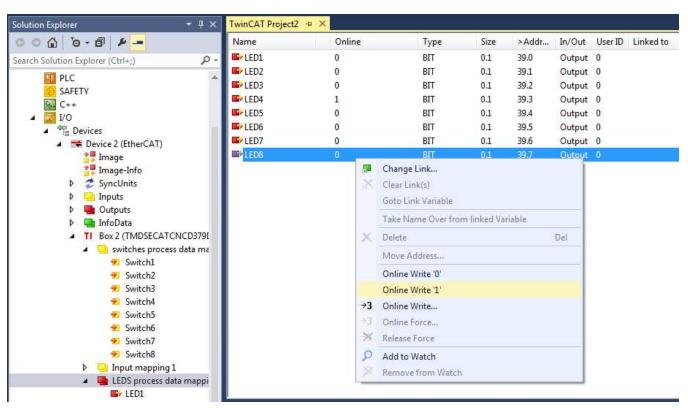


Figure 47. Writing to the LEDs

The LED values are looped back to the switches. The switches can be viewed by clicking on "switches process data mapping". Their values should match the LED values seen in "LEDs process data mapping".



#### Getting Started (Firmware)

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Solution Explorer 🛛 🔻 👎	× TwinCAT Project2	+ X						
G C 🔂 TO - 🗊 🖌 🗕	Name	Online	Туре	Size	>Addr	In/Out	User ID	Linked to
Search Solution Explorer (Ctrl+;)	o 🗸 📌 Switch1	0	BIT	0.1	39.0	Input	0	
Device 2 (EtherCAT)	🖉 🔁 Switch2	0	BIT	0.1	39.1	Input	0	
Timage	🖉 🔁 Switch3	0	BIT	0.1	39.2	Input	0	
ariage ariage Image-Info	🔁 🔁 Switch4	1	BIT	0.1	39.3	Input	0	
<ul> <li>SyncUnits</li> </ul>	🔁 Switch5	0	BIT	0.1	39.4	Input	0	
Inputs	👻 Switch6	0	BIT	0.1	39.5	Input	0	
Outputs	🛛 🔁 Switch7	0	BIT	0.1	39.6	Input	0	
InfoData	👻 Switch8	1	BIT	0.1	39.7	Input	0	
TI Box 2 (TMDSECATCNCD379)	at a start of the							
🔺 🛁 switches process data m								
👻 Switch1								
🔁 Switch2								
🔁 Switch3								
🔁 Switch4								
🔁 Switch5								
🔁 Switch6								
🔁 Switch7								
🔁 Switch8								
🔺 🛄 Input mapping 1								
🔁 DataToMaster								
🔁 ModeResponse								
🔁 SpeedPosFbk								
🔺 🔚 LEDS process data map	pi							
EP LED1								
EP LED2								
ED3								



This shows that full loopback has been achieved. The master can both read from and write to the slave.

## 4.3 Slave Stack Code

For information on the slave stack code patches as well as build and debugging instructions, see the *TMDSECATCNCD379D EtherCAT Solution Reference Guide* (SPRUIG9).

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