FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

ICS840304I

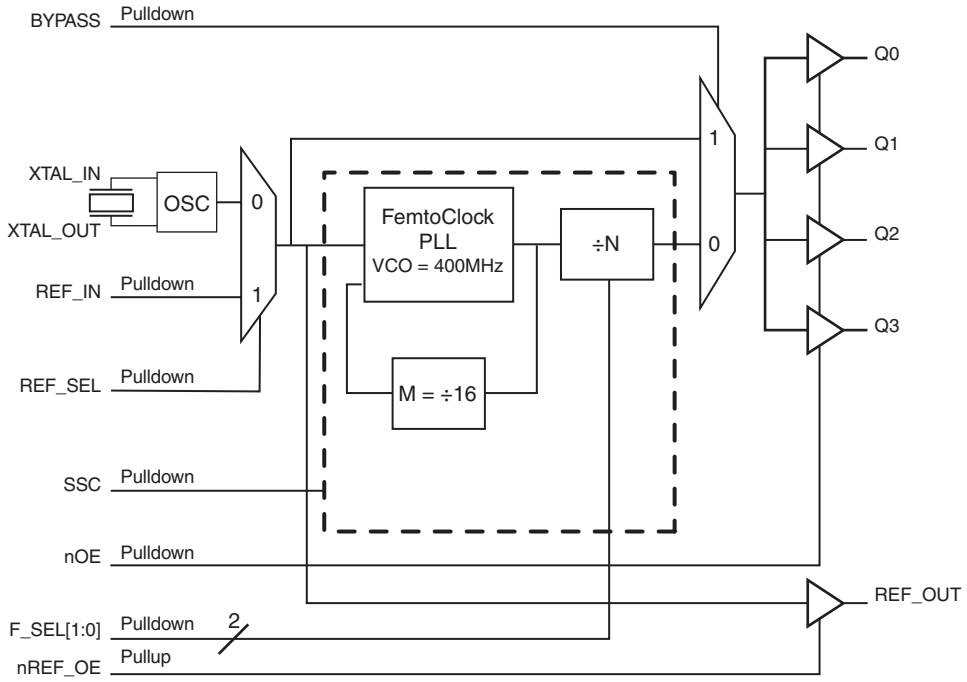
General Description

ICS840304I is an optimized PCI-X and PCI-e clock generator and a member of the HiperClocks™ family of high performance clock solutions from IDT. The ICS840304I uses a 25MHz parallel crystal to generate 33.33MHz to 133.33MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solutions. The device supports 1% downspread spread spectrum clocking. The ICS840304I has excellent phase jitter (<1ps rms) over integration range of 1.5MHz - 22MHz. Designed for Backplane, networking and industrial applications, the ICS840304I can also drive the high-speed PCI-X and PCI-e SerDes clock inputs of communication processors, DSPs, switches and bridges.

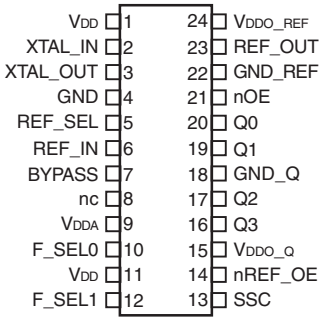
Features

- Four LVCMOS/LVTTL outputs, 20Ω typical output impedance
  One REF_OUT LVCMOS/LVTTL clock output
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended clock input
- Support the following output frequencies: 33.33MHz, 66.67MHz, 100MHz or 133.33MHz
- VCO: 400MHz
- PLL and N divider bypass and output enable
- RMS phase jitter @100MHz, using a 25MHz crystal, (1.5MHz - 22MHz): 0.46ps (typical) @ 3.3V
- Supports SSC, 1% downspread
- Full 3.3V and 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS840304I
24-Lead, 173-MIL TSSOP
4.4mm x 7.8mm x 0.92mm body package
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 11	V_{DD}	Power		Core supply pins.
2, 3	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
4	GND	Power		Power supply ground.
5	REF_SEL	Input	Pulldown	Reference select pin. When HIGH selects REF_IN. When LOW, selects crystal. LVCMOS/LVTTL interface levels.
6	REF_IN	Input	Pulldown	Reference clock input. LVCMOS/LVTTL interface levels.
7	BYPASS	Input	Pulldown	When HIGH bypasses PLL. When LOW, selects N divider. LVCMOS/LVTTL interface levels.
8	nc	Unused		No connect.
9	V_{DDA}	Power		Analog supply pin.
10, 12	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels. See Table 3A.
13	SSC	Input	Pulldown	SSC control pin. LVCMOS/LVTTL interface levels. See Table 3B.
14	nREF_OE	Input	Pullup	Reference output enable pin. LVCMOS/LVTTL interface levels.
15	V_{DDO_Q}	Power		Output supply pin for Q0:Q3 outputs.
16, 17, 19, 20	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels. 20Ω typical output impedence.
18	GND_Q	Power		Power supply ground for Q0:Q3 outputs.
21	nOE	Input	Pulldown	Active LOW output enable. When logic HIGH, the outputs are Hi-Z. When logic LOW, the outputs are enabled. LVCMOS/LVTTL interface levels.
22	GND_REF	Power		Power supply ground for REF_OUT.
23	REF_OUT	Output		Reference clock output.
24	V_{DDO_REF}	Power		Output power supply for REF_OUT.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DDO} = 3.465V		TBD		pF
		V_{DDO} = 2.625V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			20		Ω

TABLE 3A. FREQUENCY SELECT FUNCTION TABLE

Inputs				Output Frequency (MHz)
F_SEL1	F_SEL0	M Divider Value	N Divider Value	
0	0	16	12	33.33
1	0	16	6	66.67
0	1	16	4	100
1	1	16	3	133.33

TABLE 3B. SSC FUNCTION TABLE

Input	Mode
SSC	
0 (default)	SSC Off
1	1% Downspread

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_Q}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.24	3.3	V_{DD}	V
V_{DDO_Q}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			141		mA
I_{DDA}	Analog Supply Current			24		mA
I_{DDO_Q}	Output Supply Current			18		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_Q}$ = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.24	2.5	V_{DD}	V
V_{DDO_Q}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			132		mA
I_{DDA}	Analog Supply Current			24		mA
I_{DDO_Q}	Output Supply Current			18		mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ± 5%	-0.3		0.8	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	REF_IN, REF_SEL, BYPASS, nOE, SSC, F_SEL0, F_SEL1	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		nREF_OE	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	REF_IN, REF_SEL, BYPASS, nOE, SSC, F_SEL0, F_SEL1	V_{DD} = 3.465V or 2.625, V_{IN} = 0V	-5			µA
		nREF_OE	V_{DD} = 3.465V or 2.625, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO_Q} = 3.3V±5%	2.6			V
			V_{DDO_Q} = 2.5V±5%	1.8			V
V_{OL}	Output Low Voltage: NOTE 1		V_{DDO_Q} = 3.3V±5% or 2.5V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO_Q}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.44		26.5625	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_Q} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			33.33		MHz
				66.67		MHz
				100		MHz
				133.33		MHz
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	33.33MHz (Integration Range: 1.5MHz to 10MHz)		0.49		ps
		66.67MHz (Integration Range: 1.5MHz to 10MHz)		0.43		ps
		100MHz (Integration Range: 1.5MHz to 22MHz)		0.46		ps
		133.33MHz (Integration Range: 1.5MHz to 22MHz)		0.47		ps
*t*jit(per)	Period Jitter; NOTE 3			30		ps
*t*sk(o)	Output Skew; NOTE 4, 5			50		ps
F_M	SSC Modulation Frequency; NOTE 6	F_{OUT} = 33.33MHz, 66.67MHz, 100MHz, 133.33MHz	29		33.33	kHz
F_{MF}	SSC Modulation Factor; NOTE 6	F_{OUT} = 33.33MHz, 66.67MHz, 100MHz, 133.33MHz		1.25		%
SSC_{red}	Spectral Reduction; NOTE 4	F_{OUT} = 33.33MHz, 66.67MHz, 100MHz, 133.33MHz	7	10		dB
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		1.3		ns
odc	Output Duty Cycle			50		%

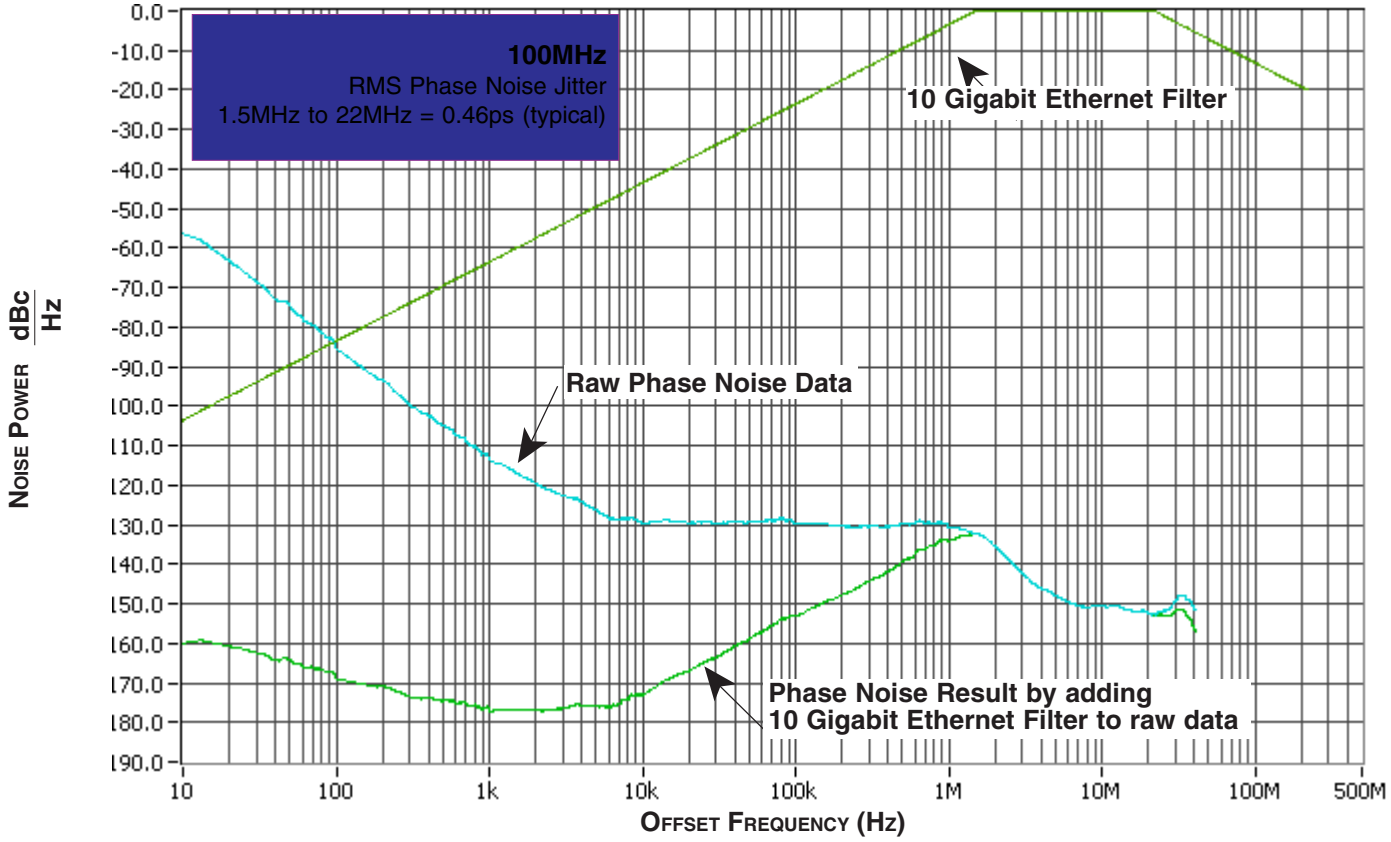
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Spread Spectrum clocking disabled.
NOTE 3: Jitter performance using crystal inputs.
NOTE 4: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO\_Q}/2$.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Spread Spectrum clocking enabled.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_Q} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

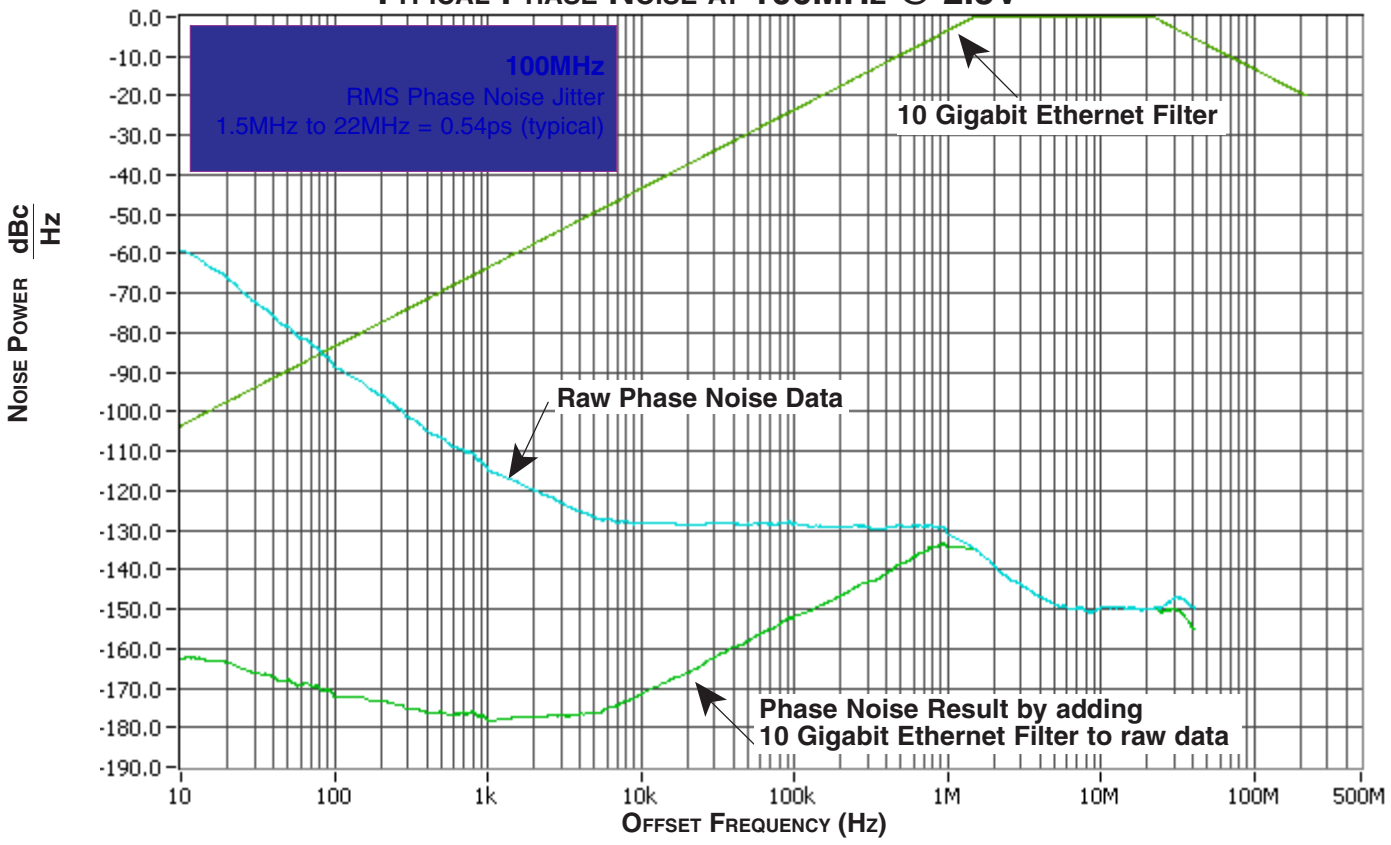
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			33.33		MHz
				66.67		MHz
				100		MHz
				133.33		MHz
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	33.33MHz (Integration Range: 1.5MHz to 10MHz)		0.50		ps
		66.67MHz (Integration Range: 1.5MHz to 10MHz)		0.45		ps
		100MHz (Integration Range: 1.5MHz to 22MHz)		0.54		ps
		133.33MHz (Integration Range: 1.5MHz to 22MHz)		0.58		ps
*t*jit(per)	Period Jitter; NOTE 3			35		ps
*t*sk(o)	Output Skew; NOTE 4, 5			50		ps
F_M	SSC Modulation Frequency; NOTE 6	F_{OUT} = 33.33MHz, 66.67MHz, 100MHz, 133.33MHz	29		33.33	kHz
F_{MF}	SSC Modulation Factor; NOTE 6	F_{OUT} = 33.33MHz, 66.67MHz, 100MHz, 133.33MHz		1.25		%
SSC_{red}	Spectral Reduction; NOTE 4	F_{OUT} = 33.33MHz, 66.67MHz, 100MHz, 133.33MHz	7	10		dB
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		1.3		ns
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Spread Spectrum clocking disabled.
NOTE 3: Jitter performance using crystal inputs.
NOTE 4: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO\_Q}/2$.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Spread Spectrum clocking enabled.

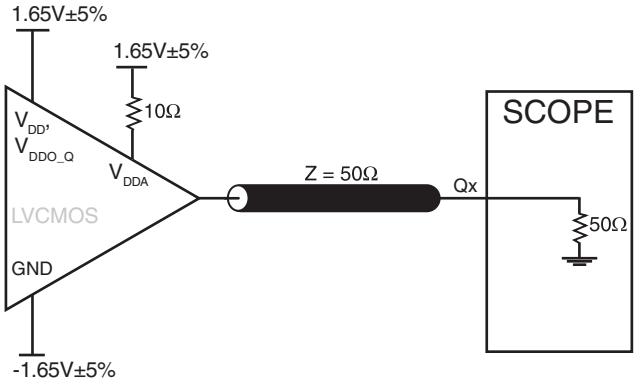
Typical Phase Noise at 100MHz @ 3.3V



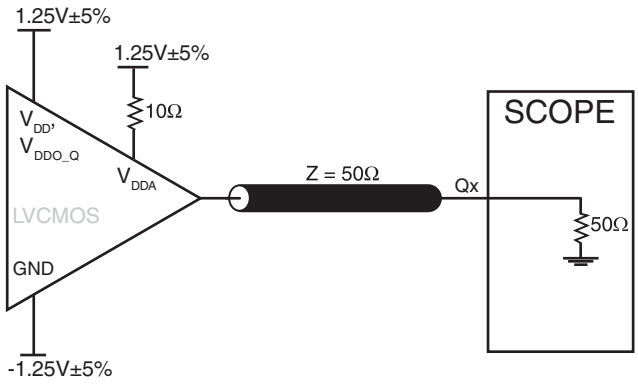
Typical Phase Noise at 100MHz @ 2.5V



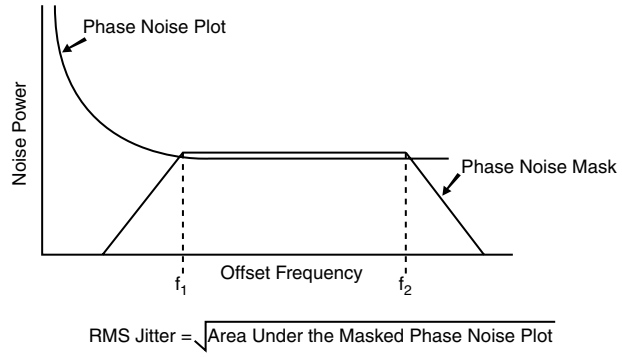
PARAMETER MEASUREMENT INFORMATION



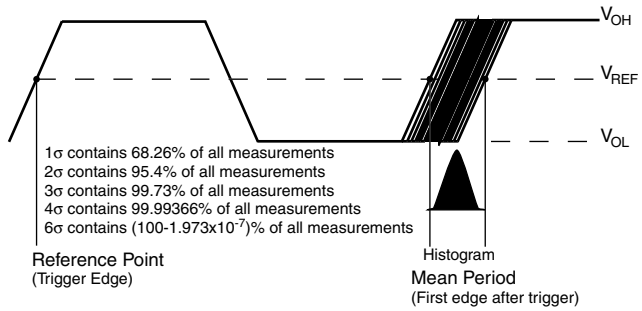
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



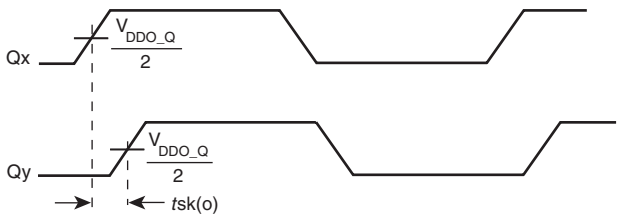
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



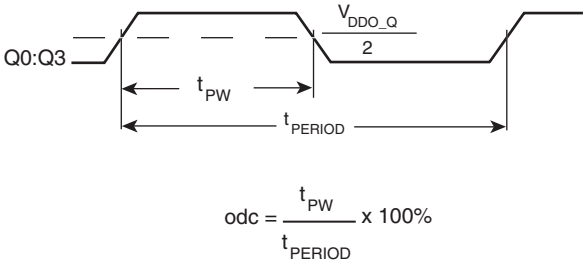
RMS PHASE JITTER



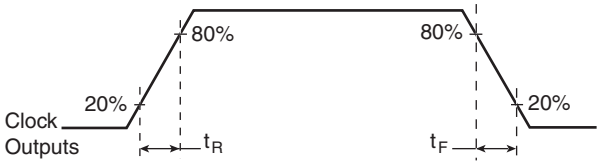
PERIOD JITTER



OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840304I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO_Q} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

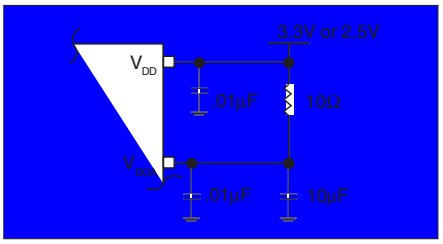


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840304I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

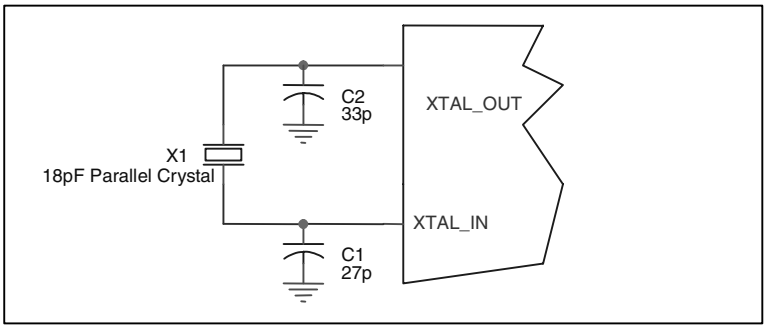


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

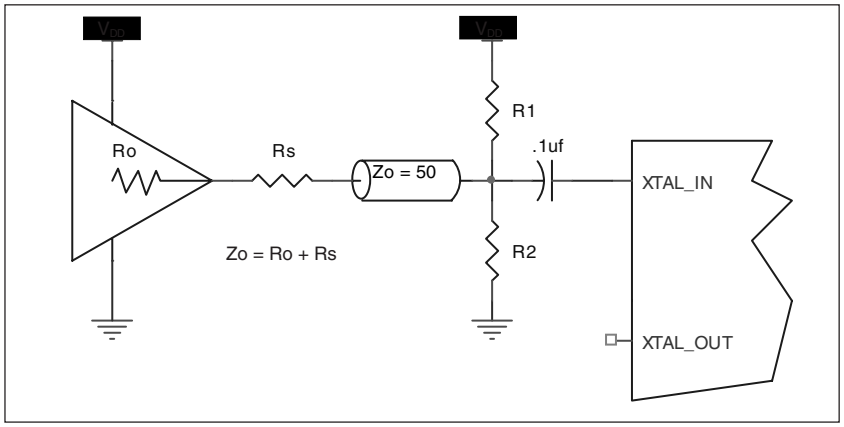


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN INPUT:
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32kHz triangle waveform is used with 1% down-spread (+0.0% / 1%) from the nominal clock frequency. An example of a triangle frequency modulation profile is shown in *Figure 4A* below.

The ICS840304I triangle modulation frequency deviation will not exceed TBD down-spread from the nominal clock frequency (+0.0% / 1%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 4B.* The ratio of this width to the fundamental frequency is typically 1%, and will not exceed TBD. The resulting spectral reduction will be greater than 7dB, as shown in Figure 4B. It is important to note the ICS840304I 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

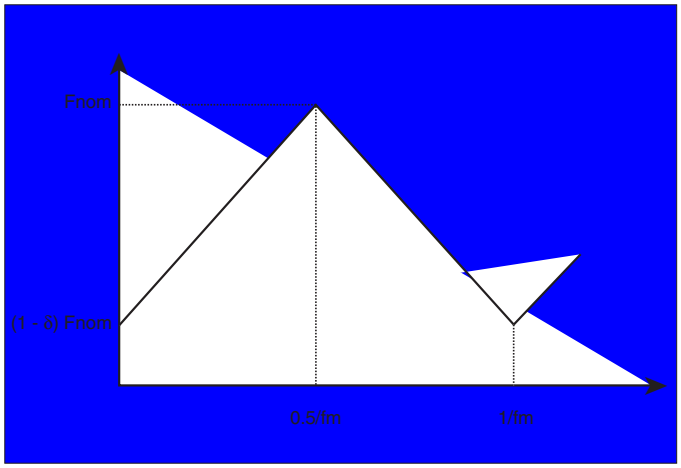


Figure 4A. Triangle Frequency Modulation

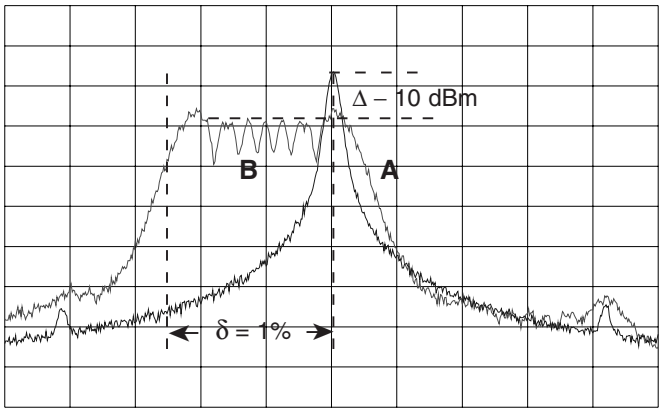


Figure 4B. Clock Output in Frequency Domain
(A) Spread-Spectrum OFF
(B) Spread-Spectrum ON

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS840304I is: 4465

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

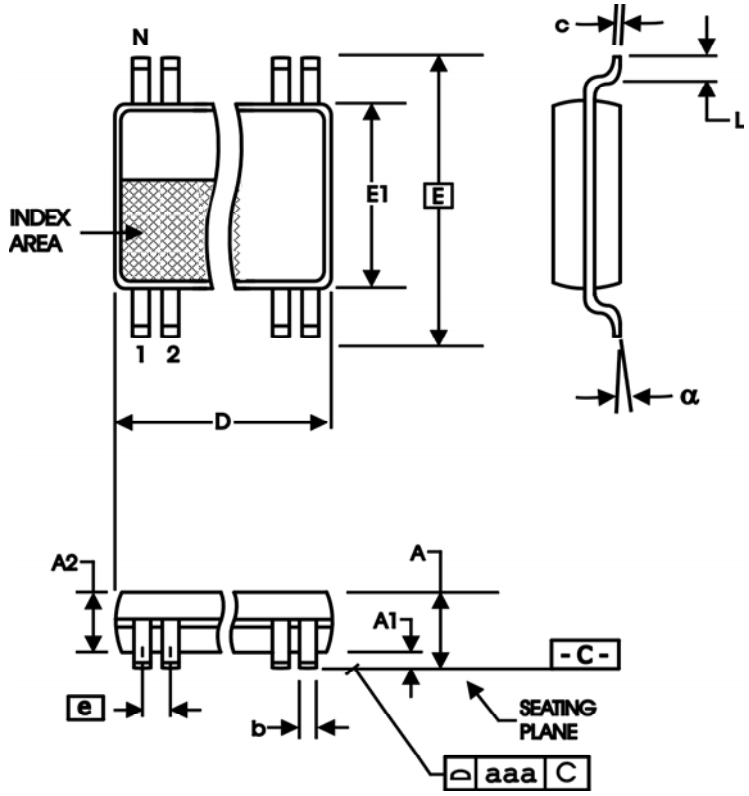


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840304BGI	ICS840304BGI	24 Lead TSSOP	tube	-40°C to 85°C
ICS840304BGIT	ICS840304BGI	24 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS840304BGILF	ICS840304BGIL	24 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS840304BGILFT	ICS840304BGIL	24 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com