DEMO CIRCUIT 1435A
QUICK START GUIDE

LTC3615 DUAL 4 MHz, 3A SYNCHRONOUS STEP-DOWN DC/DC CONVERTER

DESCRIPTION

Demonstration circuit 1435 is a dual output regulator consisting of two constant-frequency step-down converters, based on the LTC3615 dual channel monolithic synchronous buck regulator. The DC1435 has an input voltage range of 2.25V to 5.5V, with each regulator capable of delivering up to 3A of output current. The DC1435 can operate in Burst Mode™, pulse-skip or forced continuous mode. In shutdown, the DC1435 requires less than 100 uA total. The DC1435 is a very efficient circuit: over 90% for either circuit. The LTC3615 comes in a 24 Pin QFN or leaded package, which each having an exposed pad on the bottom-side of the IC for better thermal performance. These features, plus a programmable operating frequency range from 400 kHz to 4 MHz (2.25 MHz switching frequency with the RT pin connected to INTVcc), make the DC1435 demo board an ideal circuit for use industrial or distributed power applications. **Gerber files for this circuit are available. Call the LTC Factory.**

QUICK START PROCEDURE

The DC1435 is easy to set up to evaluate the performance of the LTC3615. For a proper measurement equipment configuration, set up the circuit according to the diagram in Fig. 1.

NOTE: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the Vin or Vout and GND terminals. See the proper scope probe technique in figure 2.

Please follow the procedure outlined below for proper operation.

1. Connect the input power supply to the Vin and GND terminals. Connect the loads between the Vout and GND terminals. Refer to figure 1 for the proper measurement equipment setup.

Before proceeding to operation, insert jumper shunts XJP1 and XJP2 into the OFF positions of headers J1 and J2, shunt XJP5 into the 180°out-of-phase position of PHASE header J5, shunts XJP3 and XJP4 into the soft-start (EXT SS) positions of headers J3 and J4, shunt XJP7 into the forced continuous mode (FCM) position of MODE header JP7, shunt XJP6 into the 2 MHz (RT) position of the frequency (Rt/SYNC) header JP6, shunts XJPCOMP1 and XJPCOMP2 into the external compensation (ECMP) positions of headers JITH1 and JITH2, and shunt XJP1 into the Vout1 voltage options of choice of header JP1-4: 1.8V, 2.5V, 3.3V, or user select, and shunt XJP2 into the Vout2 voltage options of choice of header JP1-3: 1.2V, 1.5V, 1.8V, or user select.

2. Apply 5.5V at Vin. Measure both Vouts; they should read 0V. If desired, one can measure the shutdown supply current at this point. The supply current will be less than 100 uA in shutdown.

3. Turn on Vout1 and Vout2 by shifting shunts XJP1 and XJP2 from the OFF positions to the ON positions. Both output voltages should be within a tolerance of +/- 2%.

4. Vary the input voltage from the min. Vin (which is dependent on Vout) to 5.5V, and the load currents from 0 to 3A. Both output voltages should be within +/- 4% tolerance.

5. Set the load current of both outputs to 3A and the input voltage to 5.5V, and then measure each output ripple voltage (refer to figure 2 for proper measurement technique); they should each measure less than 30 mVAC. Also, observe the voltage waveform at either switch node of each regulator. The switching frequencies should be between 1.6 MHz and 2.4 MHz (T = 625 ns and 417 ns). In all cases, both switch node waveforms should be rectangular in shape, and 180° out-of-phase with each other. Change the shunt position on header J5 to set the switch waveforms in phase with respect to each other. To operate the ckt.s in Burst Mode™ or pulse-skip mode, change the shunt in header J7. When finished, insert shunts XJP1 and XJP2 to the OFF position(s) and disconnect the power.

Warning - If the power for the demo board is carried in long leads, the input voltage at the part could "ring", which could affect the operation of the circuit or even exceed the maximum voltage rating of the IC. To eliminate the ringing, a small tantalum capacitor (for instance, AVX part # TPSW107M010R0150) is inserted on the pads between the input power and return terminals on the bottom of the demo board. The (greater) ESR of the tantalum will dampen the (possible) ringing voltage due to the use of long input leads. On a normal, typical PCB, with short traces, this capacitor is not needed.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITIONS	VALUE
Minimum Input Voltage		2.25V
Maximum Input Voltage		5.5V
Run	RUN Pin = GND	Shutdown
	RUN Pin = V_{IN}	Operating
Output Voltage V_{OUT1}	V_{IN} = 2.5V to 5.5V, I_{OUT1} = 0A to 3A	1.8V ±4% (1.728V – 1.872V)
	V_{IN} = 3.3V to 5.5V, I_{OUT1} = 0A to 3A	2.5V ±4% (2.4V – 2.6V)
	V_{IN} = 3.9V to 5.5V, I_{OUT1} = 0A to 3A	3.3V ±4% (3.168V – 3.432V)
Typical Output Ripple V_{OUT1}	V_{IN} = 5V, I_{OUT1} = 3A (20 MHz BW)	< 30m$V_{P–P}$
Output Regulation V_{OUT1}	Line	±1%
	Load	±1%
Output Voltage V_{OUT2}	V_{IN} = 2.25V to 5.5V, I_{OUT2} = 0A to 3A	1.2V ±4% (1.152V – 1.248V)
		1.5V ±4% (1.44V - 1.56V)
	V_{IN} = 2.5V to 5.5V, I_{OUT2} = 0A to 3A	1.8V ±4% (1.728V – 1.872V)
Typical Output Ripple V_{OUT2}	V_{IN} = 5V, I_{OUT2} = 3A (20 MHz BW)	< 30m$V_{P–P}$
Output Regulation V_{OUT2}	Line	±1%
	Load	±1%
Nominal Switching Frequencies	RT Pin connected to 200k	2 MHz
	RT Pin = $INTV_{CC}$	2.25 MHz
Burst Mode™ Operation	Channel 1: Vin = 5V, Vout1 = 3.3V	Iout1 = 600 mA
	Channel 2: Vin = 5V, Vout2 = 1.8V	Iout2 = 700 mA
Pulse-Skip Operation	Channel 1: Vin = 5V, Vout1 = 3.3V	Iout1 = 600 mA
	Channel 2: Vin = 5V, Vout2 = 1.8V	Iout2 = 700 mA
Phase	Phase Pin = SV_{IN}	180°Out-of-Phase
	Phase Pin OPEN	90°Out-of-Phase
	Phase Pin = GND	In Phase

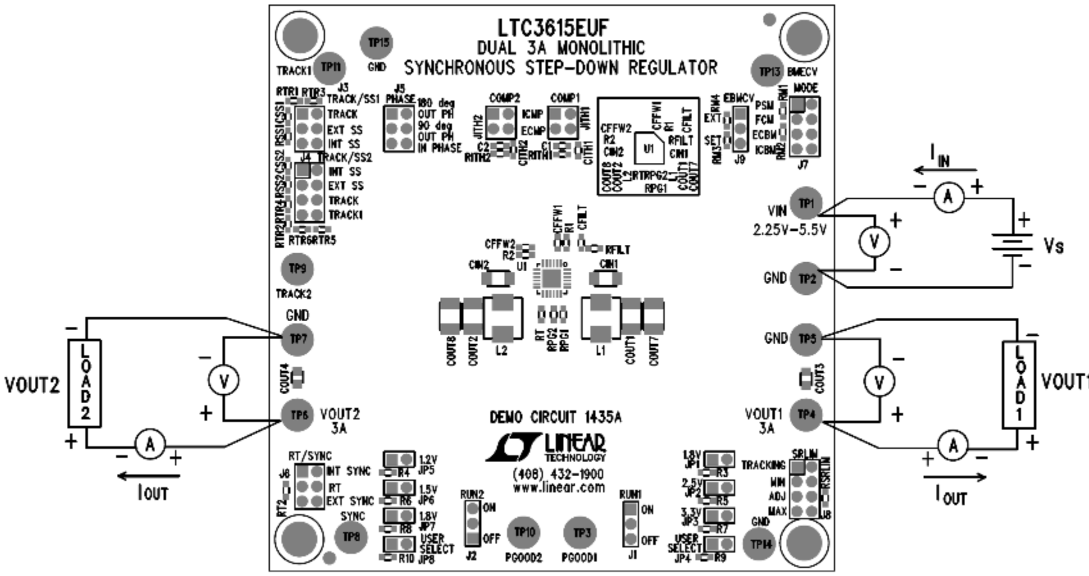


Figure 1. **Proper Measurement Equipment Setup**

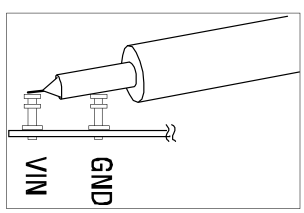


Figure 2. **Measuring Input or Output Ripple**

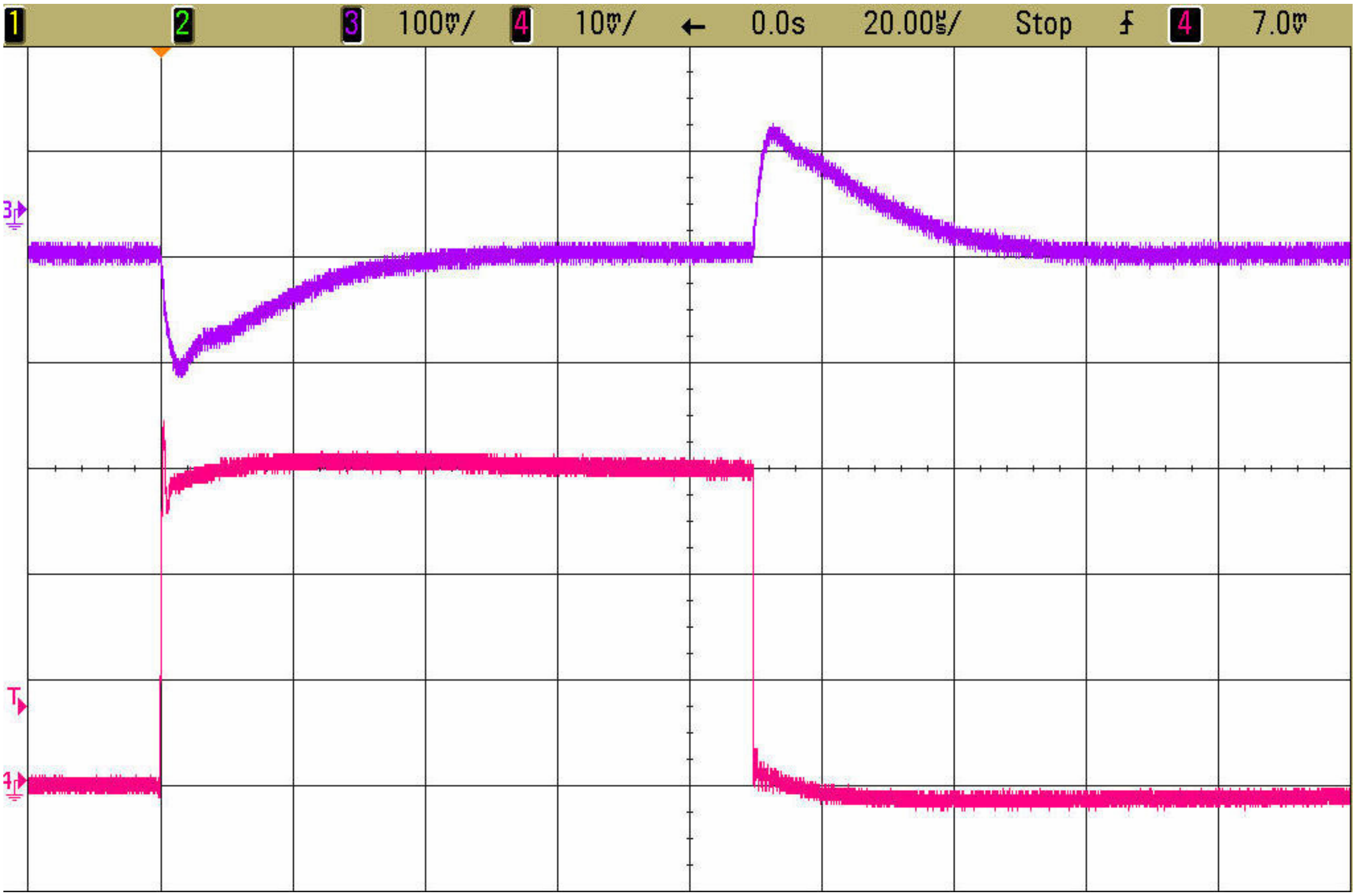


Figure 3. V_{OUT1} Load Step Response

V_{IN} = 5V, V_{OUT1} = 3.3V, 3A Load Step

Forced Continuous Mode F_{SW} = 2 MHz
External Compensation: Rith = 43k, Cith = 220 pF
Trace 3: Output Voltage (100mV/div AC)
Trace 4: Output Current (1A/div)

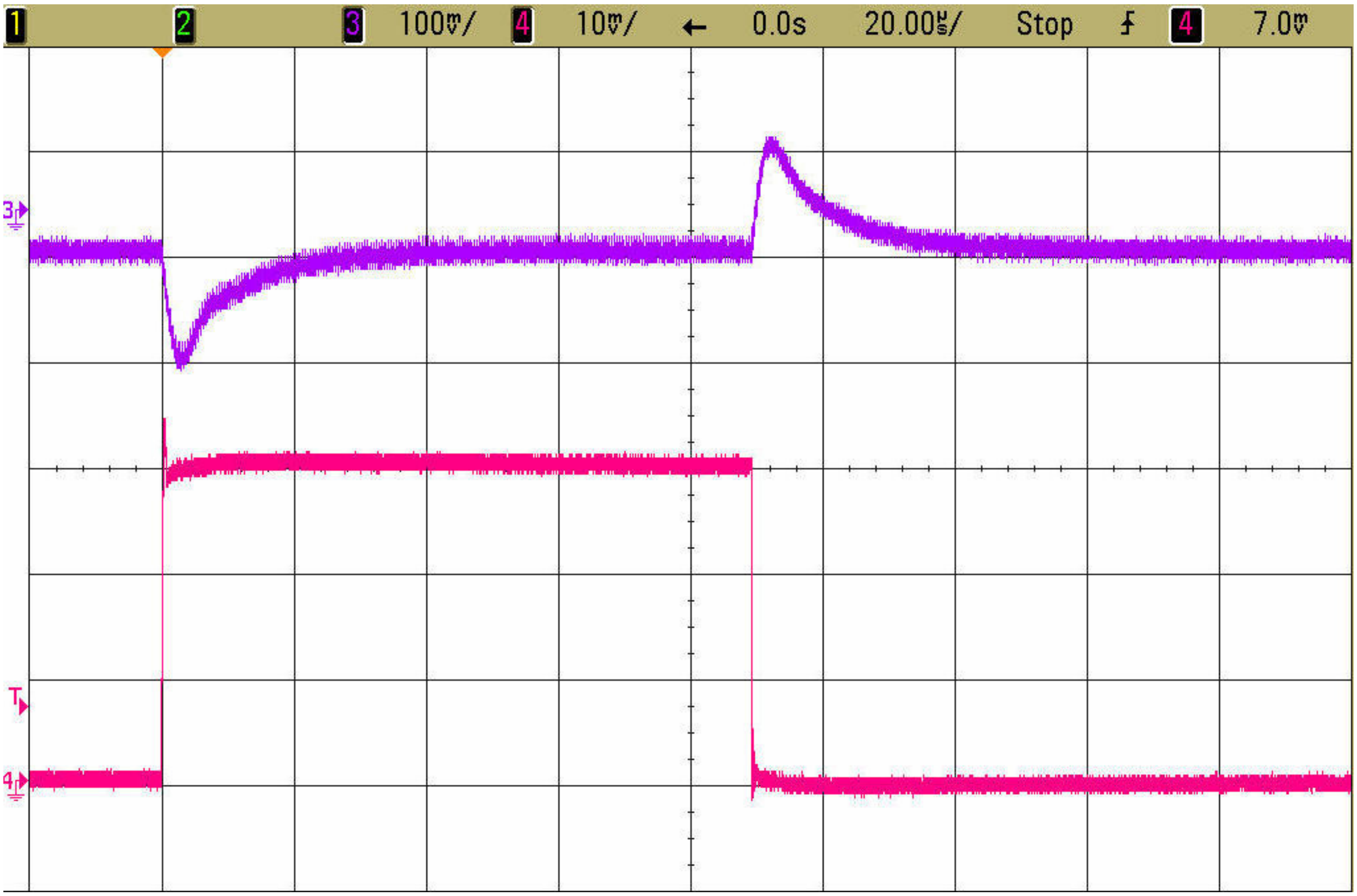


Figure 4. V_{OUT2} Load Step Response

V_{IN} = 3.3V, V_{OUT2} = 1.8V, 3A Load Step

Forced Continuous Mode F_{SW} = 2 MHz
External Compensation: Rith = 43k, Cith = 220 pF
Trace 3: Output Voltage (100mV/div AC)
Trace 4: Output Current (1A/div)

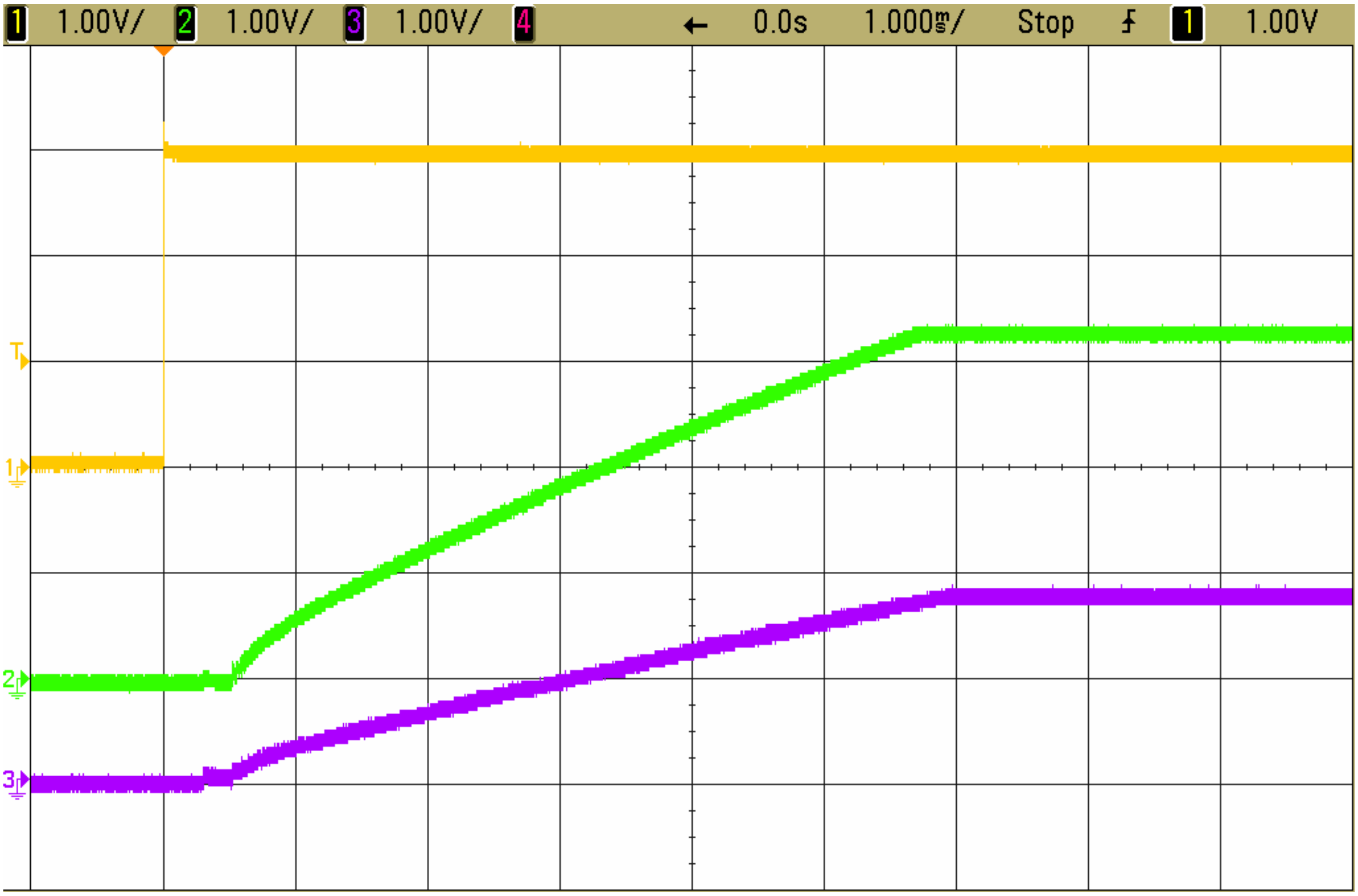
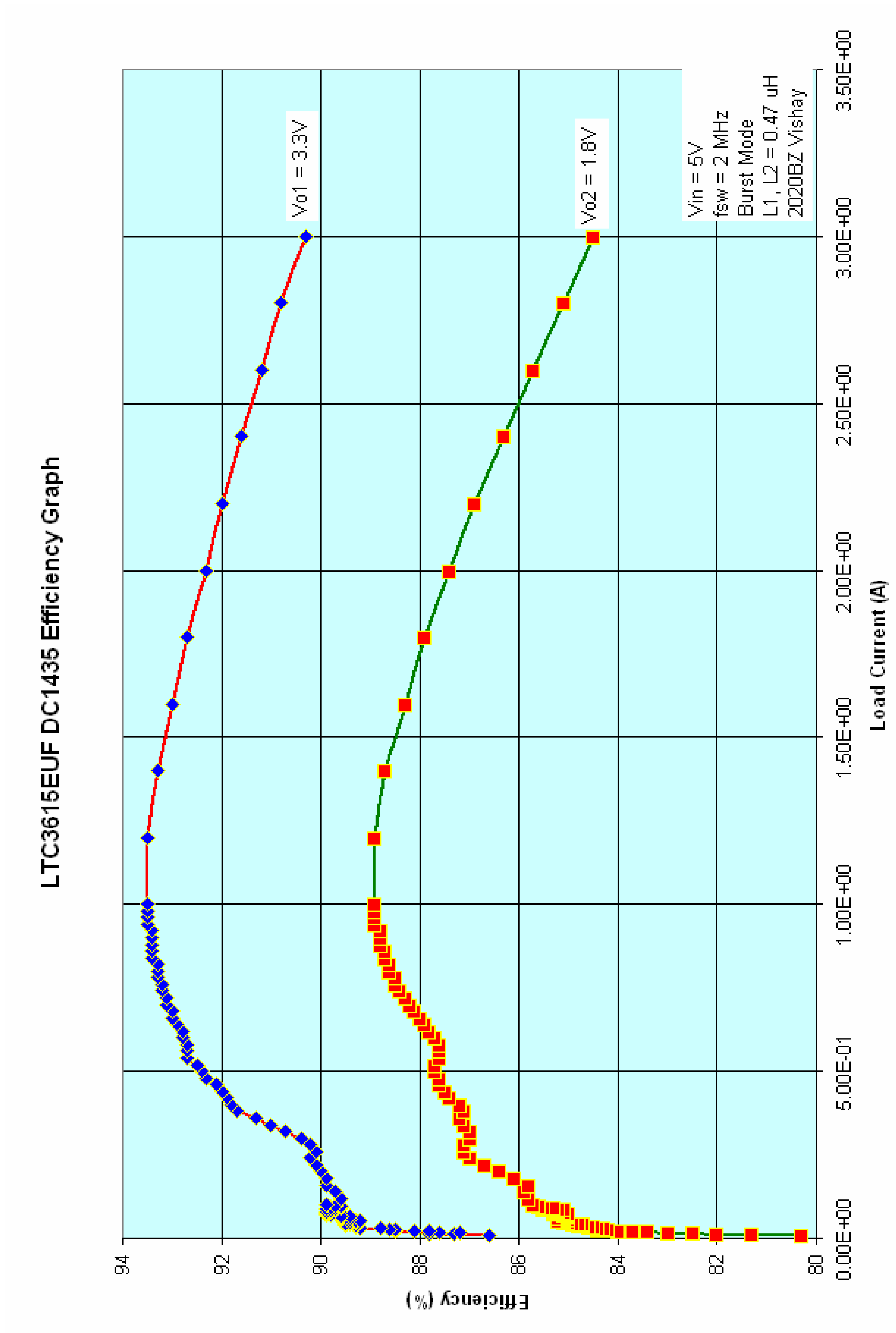


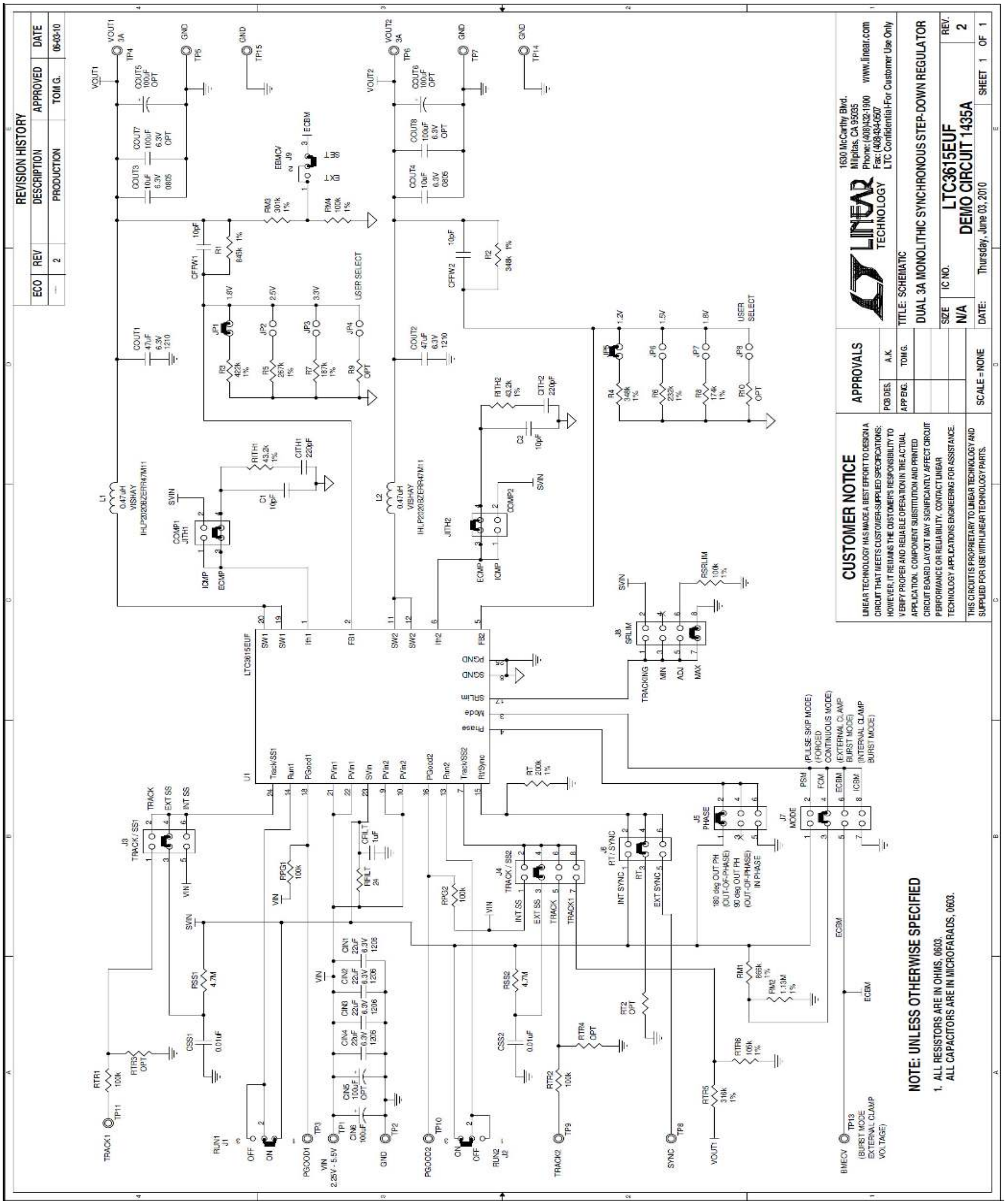
Figure 5. **Start-Up Operation**

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, 3A Loads
V_{RUN} = 2.5V

Forced Continuous Mode F_{SW} = 2 MHz
External Compensation: Rith = 43k, Cith = 220 pF
Trace 1: RUN Voltage (1V/div)
Trace 2: Channel 1 Output Voltage (1V/div)
Trace 3: Channel 2 Output Voltage (1V/div)



LTC3615EUF DC1435 Efficiency Graph
Efficiency (%)
Load Current (A)
94
92
90
88
86
84
82
80
0.00E+00
5.00E-01
1.00E+00
1.50E+00
2.00E+00
2.50E+00
3.00E+00
3.50E+00
Vo1 = 3.3V
Vo2 = 1.8V
Vin = 5V
fsw = 2 MHz
Burst Mode
L1, L2 = 0.47 uH
2020BZ Vishay


REVISION HISTORY
PRODUCTION
TOM G.
06-03-10
CUSTOMER NOTICE
NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0603.
ALL CAPACITORS ARE IN MICROFARADS, 0603.
LTC3615EUF
DUAL 3A MONOLITHIC SYNCHRONOUS STEP-DOWN REGULATOR
LTC3615EUF
DEMO CIRCUIT 1435A
Thursday, June 03, 2010
SCALE = NONE