IBM PowerPC 750CL Microprocessor Revision Level DD2.x

Datasheet

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1. General Information

The IBM® PowerPC® 750™CL RISC microprocessor is a 32-bit implementation of the IBM PowerPC family. This document contains pertinent physical and electrical characteristics of the IBM PowerPC 750CL RISC Microprocessor revision DD2.X single chip module (SCM). The PowerPC 750CL Microprocessor is also referred to as the 750CL throughout this document.

1.1 Features

This section summarizes the features of the 750CL implementation of the PowerPC Architecture™. Major features of the 750CL include the following:

- Branch processing unit
  - Fetches four instructions per clock
  - Processes one branch per cycle and can resolve two speculations
  - Executes single speculative stream during fetch of another speculative stream
  - Has a 512-entry branch history table (BHT) for dynamic prediction
- Dispatch unit
  - Has full hardware detection of dependencies, which are resolved in the execution units
  - Dispatches two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point)
  - Has serialization control (predispatch, postdispatch, execution, serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Load/store unit
  - Has single-cycle load or store cache access (byte, halfword, word, doubleword)
  - Has effective address generation
  - Allows hits under misses (one outstanding miss)
  - Has single-cycle misaligned access within a doubleword boundary
  - Has alignment, zero padding, sign extend for integer register file
  - Converts floating-point internal format (using alignment and normalization)
  - Sequences for load/store multiples and string operations
  - Has store gathering
  - Has cache and translation lookaside buffer (TLB) instructions
  - Supports big-endian and little-endian byte addressing
  - Supports misaligned little-endian in hardware

- Fixed-point units
  - Fixed-point unit 1 (FXU1): multiply, divide, shift, rotate, arithmetic, logical
  - Fixed-point unit 2 (FXU2): shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shift, rotate, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point unit
  - Support for IEEE-754 standard single-precision and double-precision floating-point arithmetic
  - 3-cycle latency, 1-cycle throughput, single-precision multiply-add
  - 3-cycle latency, 1-cycle throughput, double-precision add
  - 4-cycle latency, 2-cycle throughput, double-precision multiply-add
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes Condition Register (CR) logical instructions and miscellaneous system instructions
  - Has special register transfer instructions
- Level 1 (L1) cache structure
  - 32 KB, 32-byte line, 8-way set-associative instruction cache
  - 32 KB, 32-byte line, 8-way set-associative data cache
  - Single-cycle cache access
  - Pseudo least-recently-used (PLRU) replacement
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports PowerPC memory coherency modes
  - Nonblocking instruction and data cache (supports hits under one outstanding miss)
  - No snooping of instruction cache
- Memory management unit
  - 128 entry, 2-way set-associative instruction TLB
  - 128 entry, 2-way set-associative data TLB
  - Hardware reload for TLBs
  - Eight instruction block address translation (BAT) arrays and eight data BATs
  - Virtual memory support for up to 4 petabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Level 2 (L2) cache
  - 256 KB, 64-byte line, 2-way set-associative on-chip cache memory
  - Internal L2 cache controller with 2 K-entry tag array
  - Copy-back or write-through data cache (on a page basis, or for all L2)

    - 64-byte cache line organized as two 32-byte sectors
    - L2 frequency at core speed
    - Selectable 32-byte, 64-byte, or 128-byte L2 cache loads
    - Error correction code (ECC) protection on cache array
- Bus interface
    - Compatible with the 60x processor interface
    - Has a 32-bit address bus
    - Has a 64-bit data bus (also supports 32-bit data bus mode)
    - Supports bus-to-core frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 8.5x, 9x, 9.5x, and 10x
    - Bus transaction pipeline depth of 2, 3, or 4 transactions (selectable)
- Testability
    - Level sensitive scan design (LSSD)
    - JTAG interface

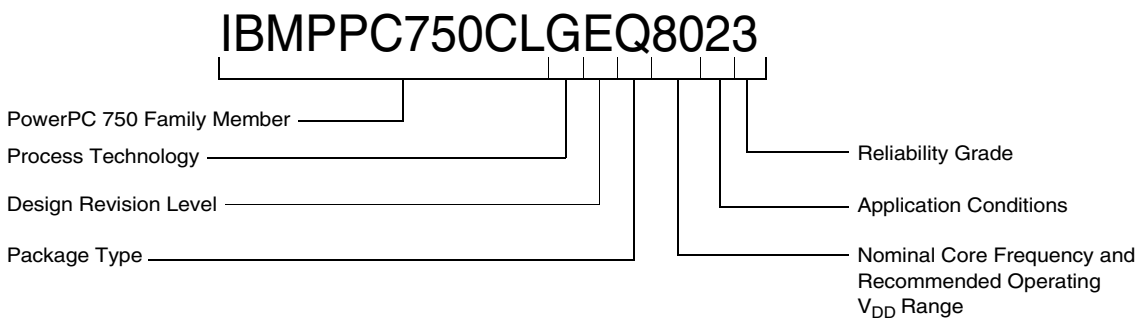
1.2 Processor Version Register

The 750CL has the following Processor Version Register (PVR) values for the respective design revision levels.

Table 1-1. 750CL Processor Version Register (PVR)

750CL Design Revision Level	PVR
DD2.0	0x00087210

1.3 Part Number Information



Process Technology	G = 10KE
Design Revision Level	E = DD2.0
Package Type	Q = Lead-free flip chip plastic ball grid array (FCPBGA)
Nominal Core Frequency and Recommended Operating V_{DD} Range	Part Designator / Max. Core Frequency / Recommended V_{DD} Range / Nominal V_{DD} Reference Only A0 / 1 GHz / 1.24 V to 1.30 V / 1.27 V 90 / 900 MHz / 1.15 V to 1.25 V / 1.20 V 80 / 800 MHz / 1.10 V to 1.20 V / 1.15 V 73 / 733 MHz / 1.10 V to 1.20 V / 1.15 V 60 / 600 MHz / 1.00 V to 1.10 V / 1.05 V 50 / 500 MHz / 0.95 V to 1.05 V / 1.00 V 40 / 400 MHz / 0.90 V to 1.00 V / 0.95 V See note 4.
Application Conditions	Junction temperature (T_J) = 0°C to 105°C. This field is set to “2” for 800 MHz and slower parts numbers. It is set to “3” for 900 MHz and 1 GHz part numbers.
Reliability Grade	3 = Grade 3; less than 100 failures in time (FIT) average failure rate (AFR). 60°C average T_J, nominal V_{DD}, 40 K power-on hours (POH). See note 3 and *Section 1.4 Reliability Information*.

Notes:

1. The T_J range, nominal core frequency, and V_{DD} range specified by the part number become part of the recommended operating conditions for the part number. Also see *Table 3-2, Recommended Operating Conditions,* on page 22.
2. The lower voltage shown in the recommended V_{DD} range is the minimum V_{DD} at which the part will operate while at the maximum T_J and maximum core frequency. If V_{DD} decreases below the minimum value, some parts will not operate correctly at maximum T_J and maximum core frequency.
3. Some early DD2.0 part numbers (IBMPPC750CLGEQ4024, IBMPPC750CLGEQ5024, IBMPPC750CLGEQ6024, IBMPPC750CLGEQ7324, IBMPPC750CLGEQ8024, IBMPPC750CLGEQ9024, IBMPPC750CLGEQA024) contained a “4” for the reliability grade. Subsequent reliability testing showed that these parts qualified as reliability grade 3. The part numbers were then changed to show the actual reliability grade. All of the IBMPPC750CLGEQxxx4 parts are grade 3 reliability.
4. V_{DD} values are to be measured from KV_{DD} to KGND.

1.4 Reliability Information

The 750CL parts described in this datasheet with a "3" in the reliability grade field of the part number (see *Section 1.3 Part Number Information*) are known as grade 3 parts. Grade 3 parts for PowerPC 750 family processors have the following features:

- An average failure rate (AFR) target of 100 failures in time (FIT) over a lifetime of 40 K POH
- An early failure rate (EFR) of 250 FIT during the first 8700 POH

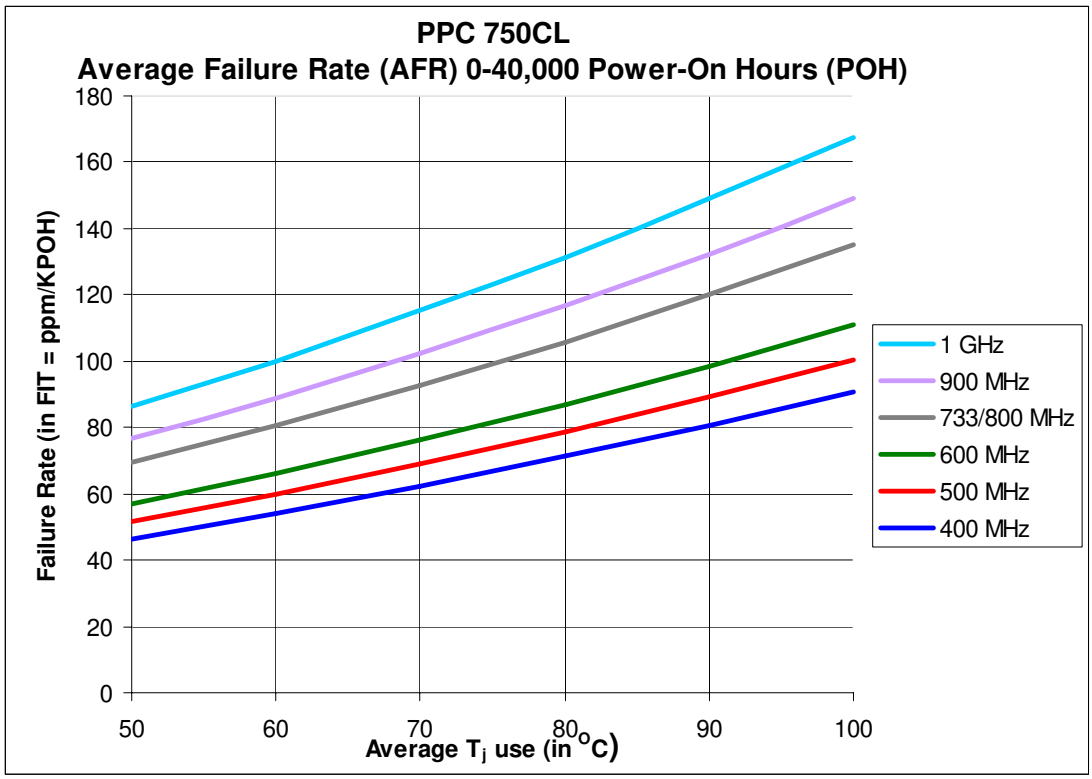
FIT rates are averages and are computed to 70% confidence. For more information, see the latest *IBM Burlington Quality Monitor Report* available on IBM CustomerConnect.

Figure 1-1 shows the calculated target AFR of the 750CL parts. The FIT rates in *Figure 1-1* are defined as a set of average use conditions that include the average junction temperature (T_J), the average processor core voltage (V_{DD}), and the average core frequency (F_{CORE}) of the processor.

Each processor is assumed to be operating with an average V_{DD} equal to the nominal V_{DD} for the part, as shown in *Section 1.3, Part Number Information,* on page 12.

Note: The calculated FIT rate curves in *Figure 1-1* are included for reference only. These curves are based on the known characteristics of this technology; they are not guaranteed to accurately reflect the performance of every population of 750CL parts.

Figure 1-1. Effect of Average Use Condition on Reliability



1.4.1 Package Reliability

The lifetime of the 750CL can be reduced if it is exposed to an extreme number and severity of temperature cycles.

The 750CL FCPBGA module features a silicon die that is connected to a plastic laminate substrate by a number of solder balls. The thermal coefficient of expansion (CTE) of the silicon and the plastic are unequal, which creates mechanical stress on the interconnect as the temperature changes. In normal operation, large temperature changes are usually the result of turning the power on and off (on/off cycles). Smaller temperature changes (mini-cycles) are caused by a number of factors, including the change of the 750CL from nap or sleep mode to full-on operation. Mini-cycles cause smaller temperature changes so are less stressful than on/off cycles, but both must be considered when assessing the package reliability in a specific application.

Figure 1-2 on page 15, *Figure 1-3* on page 16, *Figure 1-4* on page 17, and *Figure 1-5* on page 18 show the maximum number of on/off cycles and mini-cycles that can occur over the life of the 750CL without reducing the lifetime of the part. These limits are more than adequate for most applications. If a particular application falls outside the stated limits, the designer should review the expected application conditions to see if realistic values are being used. Often, minor tweaking and trade-offs can be made in order to bring the application into compliance. Contact your IBM PowerPC field applications engineer or ppcsupp@us.ibm.com for information or assistance.

To use the figures to verify that the expected on/off cycles and mini-cycles do not reduce the reliability of the 750CL:

1. Choose the expected amplitude of the mini-cycles for the target system. Use *Figure 1-2* for 20°C mini-cycles, *Figure 1-3* for 30°C mini-cycles, *Figure 1-4* for 40°C mini-cycles, and *Figure 1-5* for 50°C mini-cycles.
2. Choose the curve that represents the amplitude of the on/off temperature cycles in the target system. The graphs assume that the low point of the temperature cycle (T_J[low]) is 20°C. The high point of the temperature cycle (T_J[high]) is labeled for each curve (as 60°C, 70°C, 80°C, 90°C, or 100°C).
3. The envelope of acceptable temperature cycles is defined as the area below the appropriate curve.

For example, suppose the target system is expected to experience mini-cycles of 20° amplitude, and on/off cycles that vary T_J from 90°C down to 20°C and back. See *Figure 1-2* for 20°C mini-cycles. Any combination of on/off cycles and mini-cycles that is on or below the 90° curve will not reduce the reliability of the part:

- 9000 on/off cycles and 1000 mini-cycles
- 8000 on/off cycles and more than 10,000 mini-cycles
- 7000 on/off cycles and approximately 30,000 mini-cycles
- 4000 on/off cycles and approximately 70,000 mini-cycles

There is some overlap in the graphs. For example, a power cycle could cycle the temperature from 20°C to 70°C, which is a 50°C cycle. In this case, these cycles can be considered either on/off cycles or mini-cycles, whichever is more favorable.

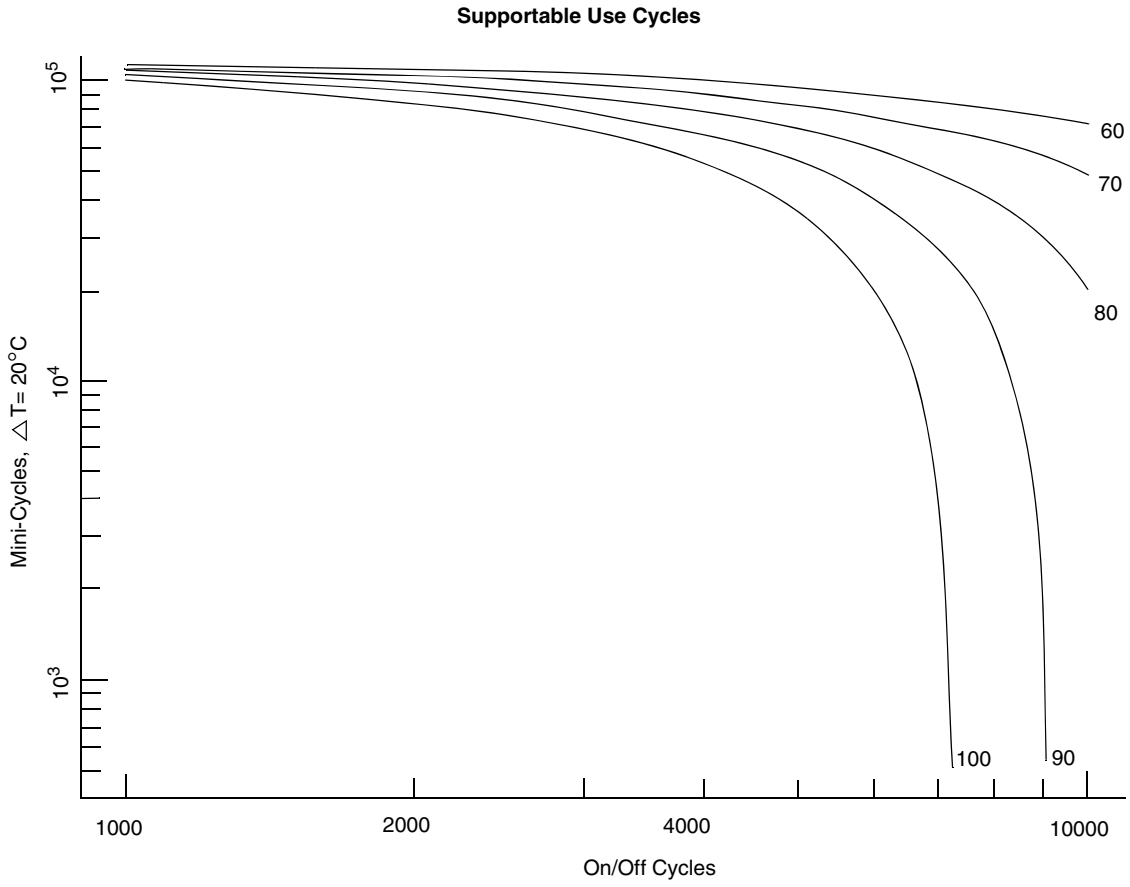
Note: The graphs in *Figure 1-2* through *Figure 1-5* were generated using the following assumptions, and are not valid under other conditions:

- T_J (high) is 100°C or less.
- The maximum junction temperature that the part will experience is T_J(high) + 20°C, not to exceed 105°C. The part will experience this maximum junction temperature for no more than 10% of its lifetime.
- Mini-cycles vary T_J from T(high) down to a lower temperature and back. For example, in *Figure 1-2*, the lower temperature is T(high) - 20°C.
- T(high) and the amplitude of the mini-cycles represent the median expected values.

- At least 90% of the on/off cycles will vary T_J from no higher than T_J(high) down to 20°C, and no more than 10% of the on/off cycles will vary from T_J(high) + 20°C down to 20°C. Note that operating the 750CL with T_J over 105°C is not allowed.
- On/off cycles and mini-cycles are assumed to be approximately evenly spread over the life of the processor.

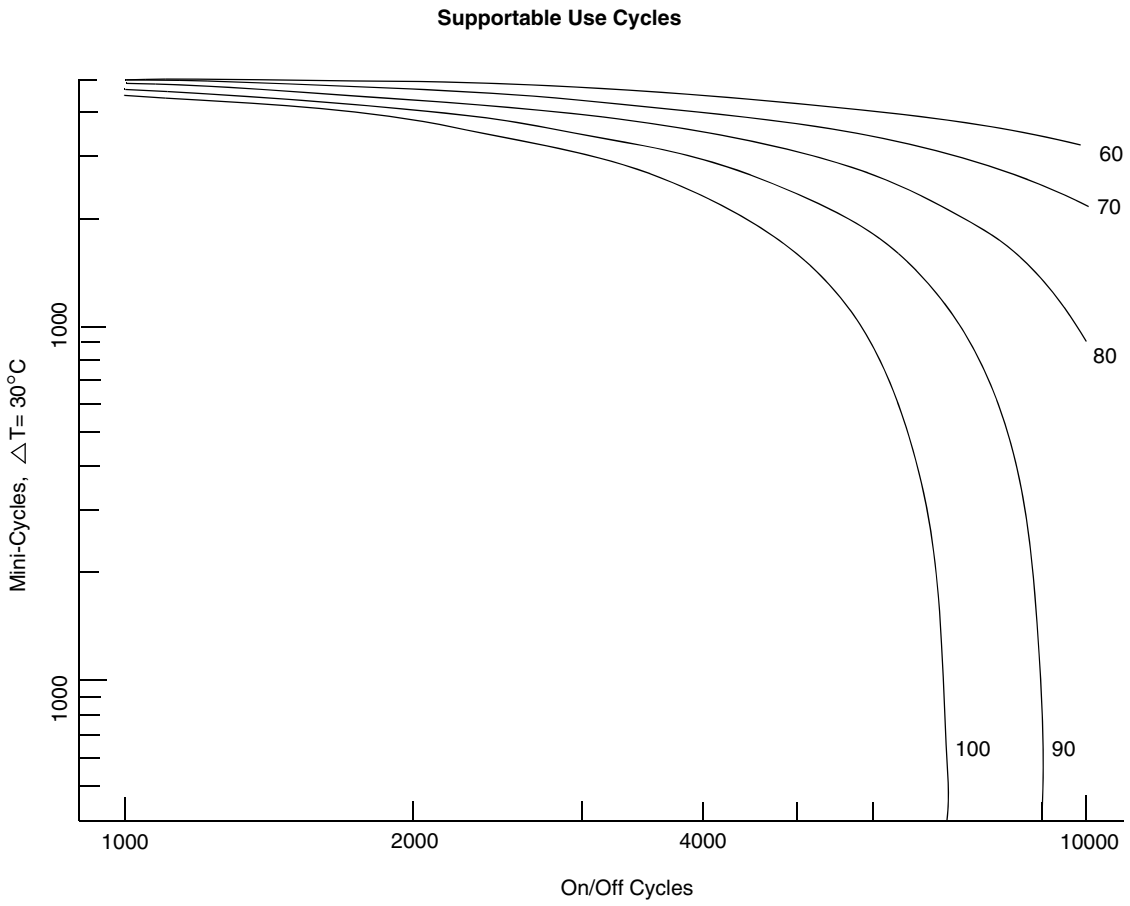
Note: The graphs are approximate. Prudent engineering margins should be used in all calculations.

Figure 1-2. Supported Temperature Cycles, Mini-Cycle Amplitude = 20°C



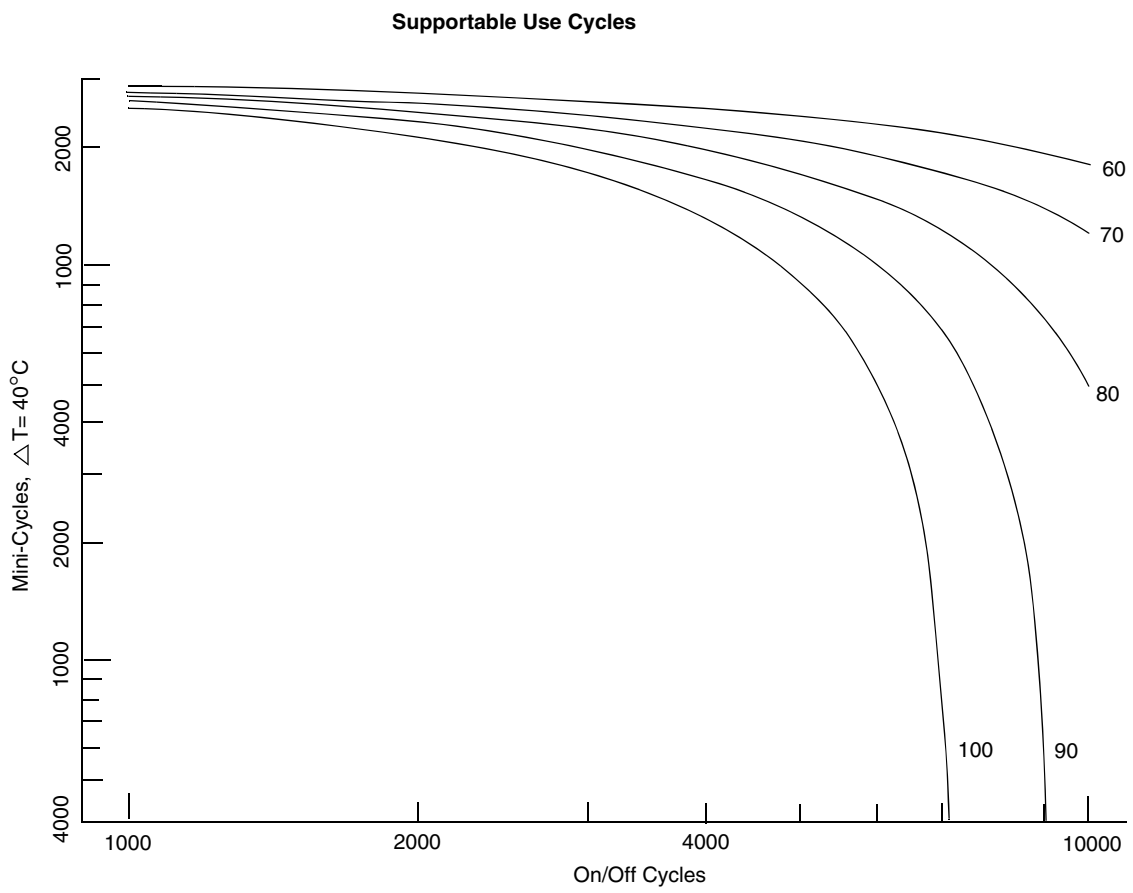
Notes:
750CL T_J (nom), as noted.
On/off cycle T (high).
Curves as shown.

Figure 1-3. Supported Temperature Cycles, Mini-Cycle Amplitude = 30°C



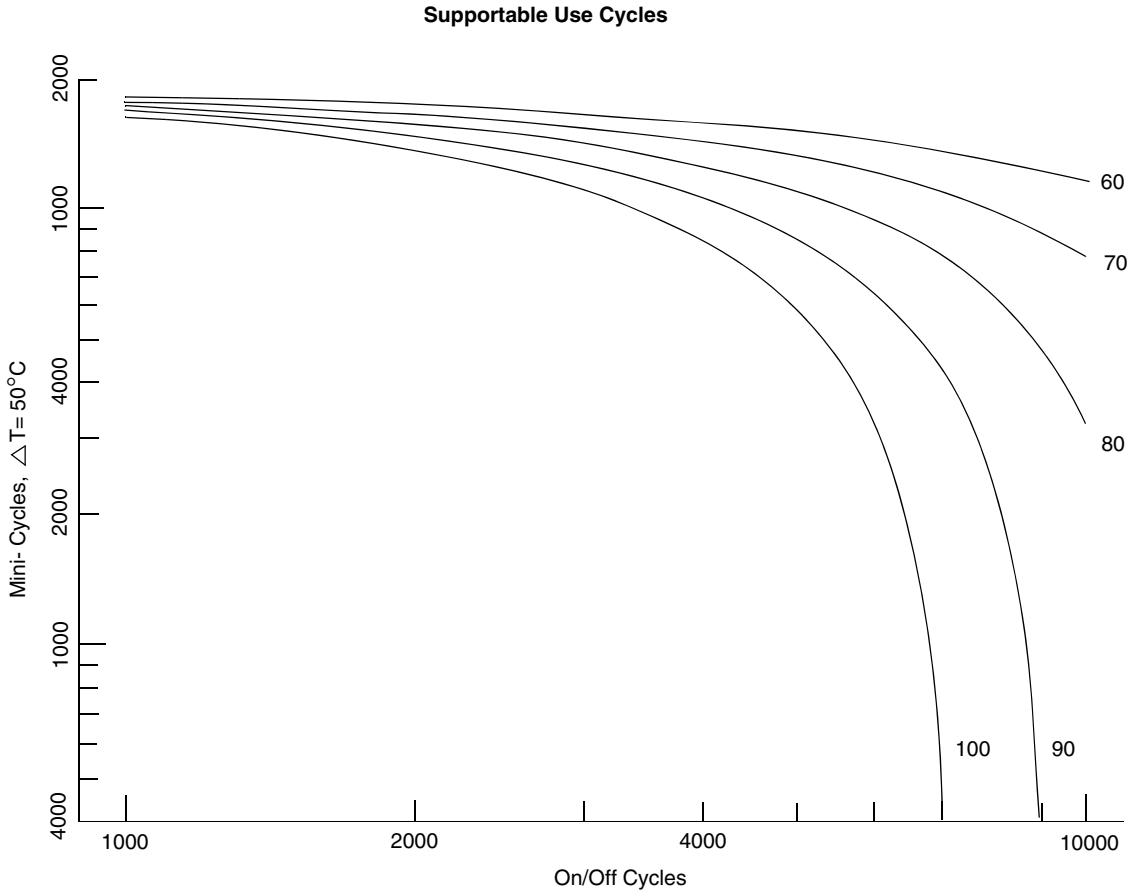
Notes:
750CL T_J (nom), as noted.
On/off cycle T (high).
Curves as shown.

Figure 1-4. Supported Temperature Cycles, Mini-Cycle Amplitude = 40°C



Notes:
750CL T_J (nom), as noted.
On/off cycle T (high).
Curves as shown.

Figure 1-5. Supported Temperature Cycles, Mini-Cycle Amplitude = 50°C



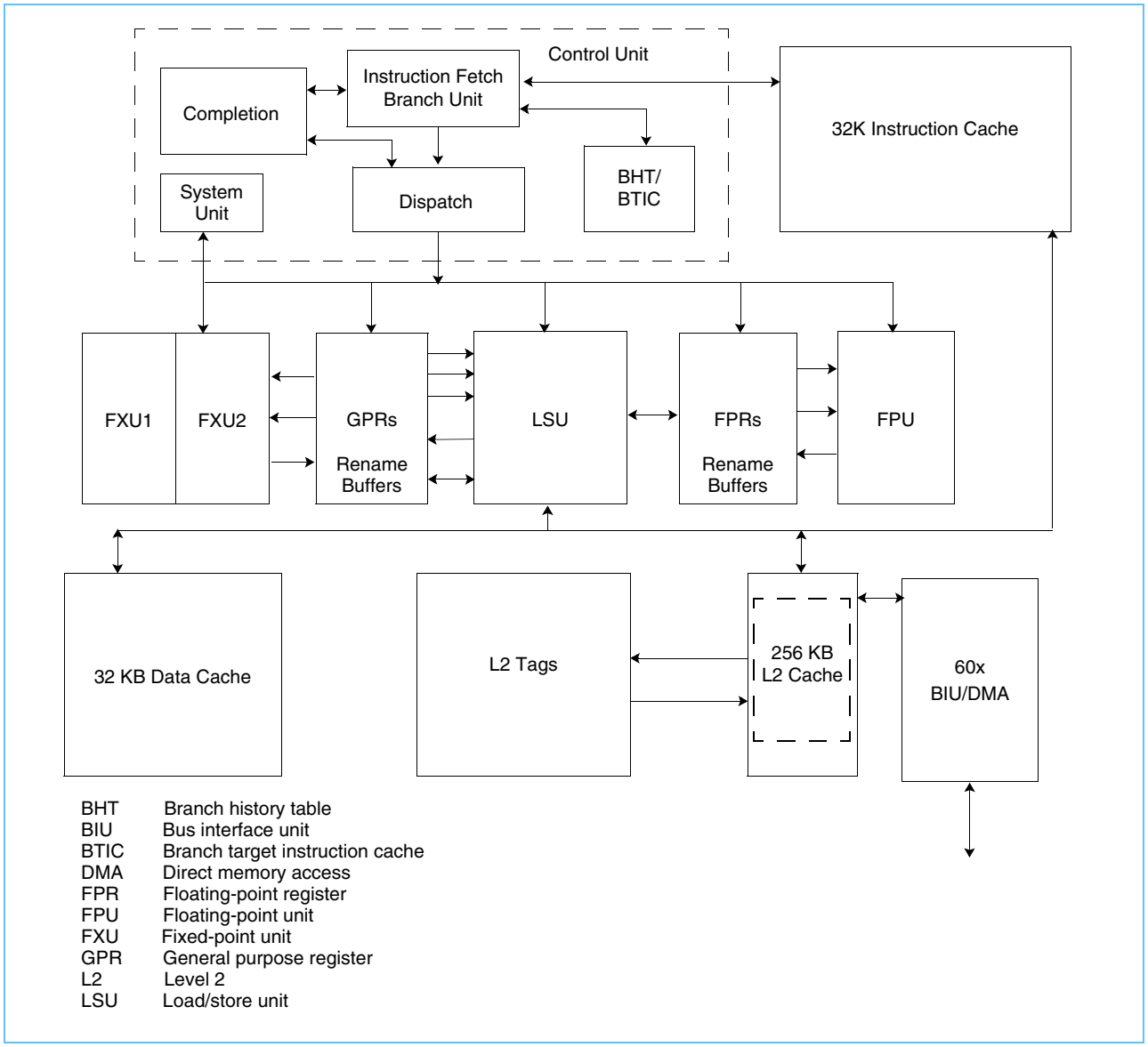
Notes:
750CL T_J (nom), as noted.
On/off cycle T (high).
Curves as shown.

2. Overview

The IBM PowerPC 750CL RISC Microprocessor, also called the 750CL, is targeted for high-performance, low-power systems using a 60x bus. The 750CL also includes an internal 256 KB L2 cache with an on-board error correction code (ECC) algorithm.

2.1 Block Diagram

Table 2-1. PowerPC 750CL Microprocessor Block Diagram



2.2 General Parameters

Table 2-2. 750CL General Parameters

Item	Description
Technology	90 nm copper silicon-on-insulator (SOI) technology Low-K dielectric 8 layer metal wirings CMOS 10KE
Die Size	15.92 sq. mm (3.99 × 3.99 mm)
Logic design	Fully static
Package	278-pin flip chip plastic ball grid array (FCPBGA) 21 × 21 mm (1.0 mm pitch) 0.6 mm ball size
Core power supply	0.95 V nominal to 1.25 V nominal, depending on the part number
I/O power supply	1.15 V nominal or 1.8 V nominal

3. Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the 750CL.

The 750CL provides V_{DD} voltage sense pins KV_{DD} and KGND. All measurements of V_{DD} are to be made using these pins.

3.1 DC Electrical Characteristics

The tables in this section describe the DC electrical characteristics for the 750CL.

Table 3-1. Absolute Maximum Ratings

Characteristic	Symbol	1.15 V	1.8 V	Units	Notes
Core supply voltage	V_{DD}	-0.3 to 1.4	-0.3 to 1.4	V	3, 4, 7
Phase-locked loop (PLL) supply voltage	AV_{DD}	-0.3 to 1.4	-0.3 to 1.4	V	3, 4, 5
60x bus supply voltage	OV_{DD}	-0.3 to 1.4	-0.3 to 2.0	V	3, 4
Input voltage	V_{IN}	-0.3 to 1.4	-0.3 to 2.0	V	2
Storage temperature range	T_{STG}	JEDEC J-STD-033		°C	

Notes:

1. Functional and tested operating conditions are given in *Section 3-2, Recommended Operating Conditions,* on page 22. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed above may affect device reliability or cause permanent damage to the device.
2. **Caution**: Transient V_{IN} overshoots of up to OV_{DD} + 0.8 V, with a maximum of 2.6 V for 1.8 V operation, and undershoots down to GND – 0.8 V, are allowed for up to 5 ns.
3. **Caution**: OV_{DD} must not exceed V_{DD} or AV_{DD} by more than 1.8 V continuously. OV_{DD} may exceed V_{DD} or AV_{DD} by up to 2.0 V for up to 20 ms during power-on or power-off. OV_{DD} must not exceed V_{DD} or AV_{DD} by more than 2.0 V for any amount of time.
4. **Caution**: V_{DD} and AV_{DD} must not exceed OV_{DD} by more than 1.0 V continuously. V_{DD} and AV_{DD} may exceed OV_{DD} by up to 1.4 V for up to 20 ms during power-on or power-off. V_{DD} and AV_{DD} must not exceed OV_{DD} by more than 1.4 V for any amount of time.
5. **Caution**: AV_{DD} must not exceed V_{DD} by more than 0.5 V at any time.
6. Electrostatic discharge (ESD) ratings:
   M = 200 V EIA/JEDEC Standard JESD22-A115-A
   CDM = 800 V JEDEC TM C101B.01
   HBM = 1000 V EIA/JEDEC Standard JESD22-A114-C
7. V_{DD} values are to be measured from KV_{DD} to KGND.

Table 3-2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit	Notes
Core supply voltage	V_{DD}	See note 2	V	2
60X bus I/O supply voltage (1.15 V)	OV_{DD}	1.15±.05	V	
60X bus I/O supply voltage (1.8 V)	OV_{DD}	1.8±5%	V	
PLL supply voltage	AV_{DD}	See note 2	V	1, 2
Input voltage	V_{IN}	GND to OV_{DD}	V	
Die-junction temperature	T_J	0 to 105	°C	

Notes:
1. See *Section 5.3, PLL Power Supply Filtering,* on page 45 for AV_{DD} noise filtering requirements.
2. The core supply voltage (V_{DD}) and PLL supply voltage (AV_{DD}) are specified by the part number. See *Section 1.3, Part Number Information,* on page 12 for the recommended operating V_{DD} range for each part number.

Table 3-3. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
FCPBGA package thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	2	°C/W
FCPBGA package thermal resistance, junction-to-lead thermal resistance (typical)	θ_{JB}	13	°C/W

Note: θ_{JC} is the internal resistance from the junction to the top surface of the package. A heatsink is generally required to ensure that the die junction temperature is maintained within the limits defined in *Table 3-2, Recommended Operating Conditions,* on page 22.

Note: Thermal resistance values are based on modeling only.

Table 3-4. DC Electrical Specifications
See *Table 3-2* on page 22 for recommended operating conditions.

Characteristic	Symbol	Value		Unit	Notes
		Min.	Max.		
Input high voltage	$V_{IH\ (1.15\ V)}$	0.75	—	V	
	$V_{IH\ (1.8\ V)}$	1.20	—	V	
Input low voltage	$V_{IL\ (1.15\ V)}$	—	0.40	V	
	$V_{IL\ (1.8\ V)}$	—	0.60	V	
Input leakage current, V_{IN} = applies to all OV_{DD} levels	I_{IN}	—	10	μA	
Hi-Z (off state) leakage current, V_{IN} = applies to all OV_{DD} levels	I_{TSI}	—	10	μA	
Output high voltage, I_{OH} = -4 mA	$V_{OH\ (1.15\ V)}$	0.90	—	V	
Output high voltage, I_{OH} = -4 mA	$V_{OH\ (1.8\ V)}$	1.30	—	V	
Output low voltage, I_{OL} = 4 mA	$V_{OL\ (1.15\ V)}$	—	0.30	V	
Output low voltage, I_{OL} = 4 mA	$V_{OL\ (1.8\ V)}$	—	0.40	V	
Capacitance, V_{IN} = 0 V, f = 1 MHz	C_{IN}	—	5	pF	1
Single-Ended SYSCLK Clock Specifications					
SYSCLK input high voltage	$V_{IH\ (1.15\ V)}$	0.8	—	V	
	$V_{IH\ (1.8\ V)}$	1.20	—	V	
SYSCLK input low voltage	$V_{IL\ (1.15\ V)}$	—	0.30	V	
	$V_{IL\ (1.8\ V)}$	—	0.30	V	
Differential SYSCLK Clock Specifications					
SYSCLK and $\overline{\text{SYSCLK}}$ single-ended swing	CSV_{SW}	175	450	mV (P - P)	
SYSCLK and $\overline{\text{SYSCLK}}$ differential swing	CDV_{SW}	350	900	mV (P - P)	
SYSCLK and $\overline{\text{SYSCLK}}$ differential cross point	CDV_{CP}	400	750	mV	
SYSCLK and $\overline{\text{SYSCLK}}$ input capacitance	CC_{IN}	—	5	pF	

Notes:
1. Capacitance values are guaranteed by design and characterization and are not tested.

Table 3-5. Power Consumption
See *Table 3-2* on page 22 for recommended operating conditions.

Mode	Part Number	V_{DD} Range (For Reference)	Frequency (MHz)	T_J (°C)	Nominal V_{DD} (V)	Power (W)	Notes
Maximum	IBMPPC750CLGEQ40xx	0.90 V to 1.00 V	400	105	0.95	1.7	1, 2, 3, 4
Maximum	IBMPPC750CLGEQ50xx	0.95 V to 1.05 V	500	105	1.00	2.0	1, 2, 3, 4
Maximum	IBMPPC750CLGEQ60xx	1.00 V to 1.10 V	600	105	1.05	2.7	1, 2, 3, 4
Maximum	IBMPPC750CLGEQ73xx	1.10 V to 1.20 V	733	105	1.15	4.8	1, 2, 3, 4
Maximum	IBMPPC750CLGEQ80xx	1.10 V to 1.20 V	800	105	1.15	5.6	1, 2, 3, 4
Maximum	IBMPPC750CLGEQ90xx	1.15 V to 1.25 V	900	105	1.20	8.4	1, 2, 3, 4
Maximum	IBMPPC750CLGEQA0xx	1.24 V to 1.30 V	1000	105	1.27	10.5	1, 2, 3, 4
Nap/Sleep Maximum	IBMPPC750CLGEQ40xx	—	400	50	0.95	0.4	1, 2, 3, 4
Nap/Sleep Maximum	IBMPPC750CLGEQ50xx	—	500	50	1.00	0.52	1, 2, 3, 4
Nap/Sleep Maximum	IBMPPC750CLGEQ60xx	—	600	50	1.05	0.68	1, 2, 3, 4
Nap/Sleep Maximum	IBMPPC750CLGEQ73xx	—	733	50	1.15	1.55	1, 2, 3, 4
Nap/Sleep Maximum	IBMPPC750CLGEQ80xx	—	800	50	1.15	1.55	1, 2, 3, 4
Nap/Sleep Maximum	IBMPPC750CLGEQ90xx	—	900	50	1.20	2.75	1, 2, 3, 4
Nap/Sleep Maximum	IBMPPC750CLGEQA0xx	—	1000	50	1.27	3.70	1, 2, 3, 4

Notes:
1. These values apply for all valid 60× buses. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent, but is typically less than 2% of V_{DD} power.
2. For each part number, maximum power is measured at nominal V_{DD} and at the indicated T_J and frequency, using parts with worst-case process parameters and running RC5-72. RC5-72 runs hotter than typical production code, but it is possible to design code that runs even hotter than RC5-72.
3. Previous IBM PowerPC processors specified the power dissipation of the processor without regard to the part number. In contrast, the 750CL power dissipation specification is specific to a particular part number. Each power specification is specific to four conditions: processor part number, processor actual operating frequency, processor actual junction temperature, and processor actual V_{DD}.
4. V_{DD} values are to be measured from KV_{DD} to KGND.

3.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the 750CL. After fabrication, parts are sorted by maximum processor core frequency as shown in *Section 3.3, Clock Specifications,* on page 25 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL configuration (PLL_CFG[0:4]) signals.

3.3 Clock Specifications

Table 3-6 provides the clock AC timing specifications as defined in *Figure 3-1* on page 26.

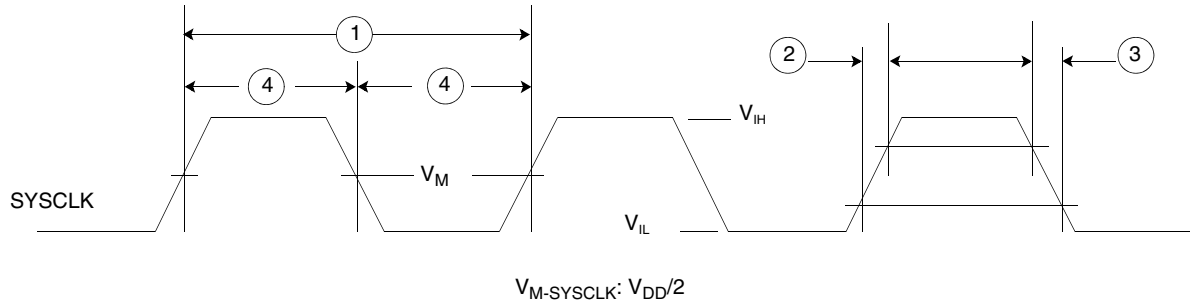
Table 3-6. Clock AC Timing Specifications
See *Table 3-2* on page 22 for recommended operating conditions.[1, 3, 5]

Figure 3-1 Timing Reference	Characteristic	Value		Unit	Notes
		Min.	Max.		
	Processor frequency	400	1000	MHz	
	SYSCLK frequency	50	240	MHz	
	Internal PLL relock time	—	100	μs	4
	Internal PLL reset time	10	—	μs	5
Single-Ended SYSCLK Specifications					
2, 3	SYSCLK slew rate, single-ended	1.0	2.5	V/ns	2
4	SYSCLK duty cycle measured at $V_{m\text{-}SYsClk}$, single-ended	25	75	%	
	Jitter, over any 10 consecutive cycles	—	160	ps	6
	Jitter, over any 50 consecutive cycles	—	240	ps	6
	Jitter, over any 100 consecutive cycles	—	380	ps	6
	Jitter, over any 1000 consecutive cycles	—	640	ps	6
Differential SYSCLK and $\overline{\text{SYSCLK}}$ Specifications					
2, 3	SYSCLK and $\overline{\text{SYSCLK}}$ slew rate, differential	1.50	3.0	V/ns	7
4	SYSCLK and $\overline{\text{SYSCLK}}$ duty cycle measured at $V_{m\text{-}SYsClk}$, differential	40	60	%	
	Jitter, cycle-to-cycle	—	200	ps (P - P)	
	Jitter, long term	—	2.5	%	8

Notes:

1. **Caution:** The SYSCLK frequency and the PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in *Table 5-1, 750CL Microprocessor PLL Configuration,* on page 44 for valid PLL_CFG[0:4] settings.
2. The slew rate for the single-ended SYSCLK inputs is measured from 0.4 to 0.75 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. Also note that hard reset (HRESET) must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
5. Midpoint voltage (V_M) for SYSCLK and $\overline{\text{SYSCLK}}$ is $V_{DD}/2$. The SYSCLK and $\overline{\text{SYSCLK}}$ input voltage range depends on OV_{DD}, but V_M is a function of V_{DD}.
6. This is the maximum deviation from nominal in the timing of the rising edge of SYSCLK over the indicated number of cycles.
7. The slew rate for SYSCLK and $\overline{\text{SYSCLK}}$ is measured between the 10% and 90% points of each clock input.
8. Long term jitter is given as a percentage of the input clock period occurring over a 10 μs interval.

Figure 3-1. SYSCLK Input Timing Diagram



3.4 Spread Spectrum Clock Generator

3.4.1 Design Considerations

When designing with the spread spectrum clock generator (SSCG), there are a number of design issues that must be taken into account.

SSCG creates a controlled amount of long-term jitter. For a receiving PLL in the 750CL to operate in this environment, it must be able to accurately track the SSCG clock jitter.

The accuracy to which the 750CL PLL can track the SSCG clock is referred to as tracking skew. When performing system timing analysis, the tracking skew must be added or subtracted to the I/O timing specifications because the tracking skew appears as a static phase error between the internal PLL and the SSCG clock.

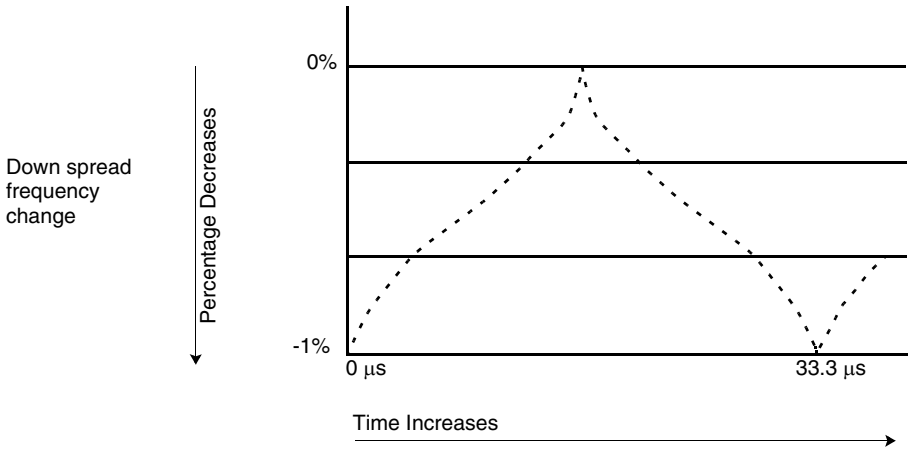
To minimize the impact on I/O timings, the following SSCG configuration is recommended:

- Down spread mode, less than or equal to 1% of the maximum frequency
- A modulation frequency of 32 kHz or less
- Linear sweep modulation or “Hershey’s Kiss” (as in a Lexmark[1] profile) modulation profile as shown in *Figure 3-2* on page 27

In this configuration, the tracking skew is less than 100 ps.

1. See patent 5,631,920.

Figure 3-2. Linear Sweep Modulation Profile



3.5 60x Bus Input AC Specifications

Table 3-7 provides the 60x bus AC timing specifications defined in *Figure 3-4* and *Figure 3-5* on page 30.

Table 3-7. 60x Bus Input AC Timing Specifications
See *Table 3-2* on page 22 for operating conditions.[1, 4, 5]

Figure 3-4 and 3-5 Timing Reference	Characteristic	Part Numbers ≤ 733 MHz		Part Numbers > 733 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
10a	Input setup: SYSCLK to all inputs valid	1.6	—	1.15	—	ns	8
10c	Mode select input setup to HRESET, TLBISYNC, QACK, and DRTRY	8	—	8	—	SYSCLK cycles	2
11a	Input hold: SYSCLK to inputs invalid	—	600	—	350	ps	
11c	HRESET to mode select input hold TLBISYNC, QACK, and DRTRY	0	—	0	—	SYSCLK cycles	3
V_M	Measurement reference voltage for inputs					—	
V_{IL-AC}	AC timing reference levels	—	0.2	—	0.2	V	6
V_{IH-AC}		OV_{DD}-0.2	—	OV_{DD}-0.2	—		

Notes:
1. Input specifications are measured from the midpoint voltage (V_M) of the signal in question to the V_M of the rising edge of the input SYSCLK. Timings are measured at the pin (see *Figure 3-4* on page 29). Timing values apply while OV_{DD} = 1.5 V nominal and OV_{DD} = 1.8 V nominal.
2. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
3. This specification is for configuration mode select only. Also note that the HRESET must be held asserted for a *minimum of 255 bus clocks* after the PLL relock time during the power-on reset sequence.
4. All values are guaranteed by design, and are not tested.
5. See *Section 3.5.1* on page 28 and *Figure 3-3* on page 29 for input setup timing definitions.
6. Input reference signal levels used to establish the timings defined in this table.
7. Input slew rate refers to the slew rate between V_{IH-AC} and V_{IL-AC} timing reference levels.
8. INT, SMI, MCP, and CHKSTP_IN must remain asserted until recognized by the processor.

Table 3-7. 60x Bus Input AC Timing Specifications
See *Table 3-2* on page 22 for operating conditions.[1, 4, 5]

Figure 3-4 and 3-5 Timing Reference	Characteristic	Part Numbers ≤ 733 MHz		Part Numbers > 733 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
Slew Rate	Reference input slew rate	1.0	—	1.0	—	V/ns	7

Notes:
1. Input specifications are measured from the midpoint voltage (V_M) of the signal in question to the V_M of the rising edge of the input SYSCLK. Timings are measured at the pin (see *Figure 3-4* on page 29). Timing values apply while OV_{DD} = 1.5 V nominal and OV_{DD} = 1.8 V nominal.
2. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
3. This specification is for configuration mode select only. Also note that the HRESET must be held asserted for a *minimum of 255 bus clocks* after the PLL relock time during the power-on reset sequence.
4. All values are guaranteed by design, and are not tested.
5. See *Section 3.5.1* on page 28 and *Figure 3-3* on page 29 for input setup timing definitions.
6. Input reference signal levels used to establish the timings defined in this table.
7. Input slew rate refers to the slew rate between V_{IH-AC} and V_{IL-AC} timing reference levels.
8. INT, SMI, MCP, and CHKSTP_IN must remain asserted until recognized by the processor.

3.5.1 Input Setup Timing

The information in this subsection is provided to clarify the criteria used to establish the timings in *Table 3-7*. The 60x Bus Input AC Timing Specifications shown in *Table 3-7* are not altered by this clarification. The valid input signal levels remain V_{IH} and V_{IL}.

The input setup times shown as 10a in *Table 3-7* specify the required time from the input signal crossing V_M to the rising edge of SYSCLK crossing V_M.

For the timings in *Table 3-7* to be valid, the falling edge of the input signal shown in *Table 3-7* is assumed to transition through V_M and cross V_{IL-AC} at the slew rate specified in *Table 3-7*. Input signals that do not reach the V_{IL-AC} boundary, or that slew from V_M to V_{IL-AC} more slowly than specified, will result in longer input setup times.

In the same way, on the rising edge, the input signal must continue past V_M and cross the V_{IH-AC} boundary within the specified minimum slew rate. Input signals that do not reach the V_{IH-AC} boundary within the slew rate specified will result in longer input setup times.

Figure 3-4 on page 29 provides the input timing diagram for the 750CL.

Figure 3-3. Input Timing Definition

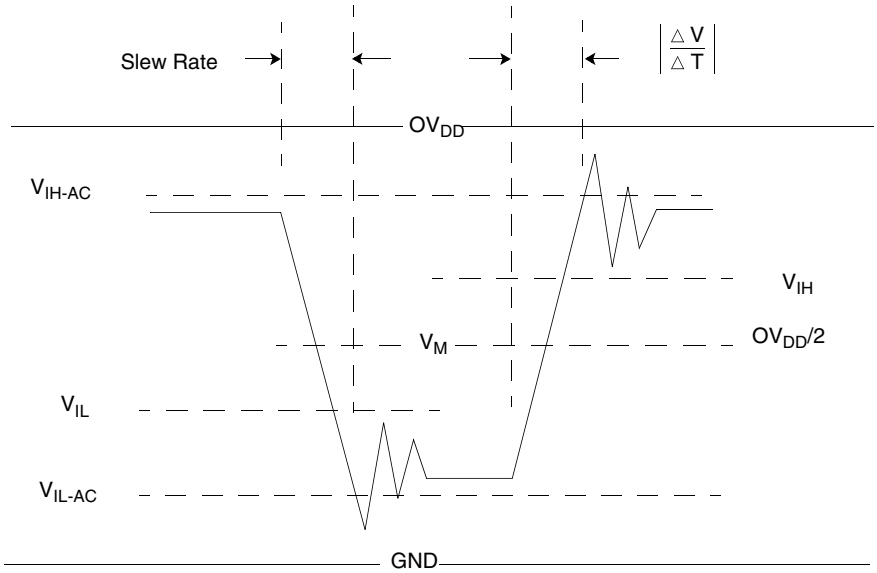
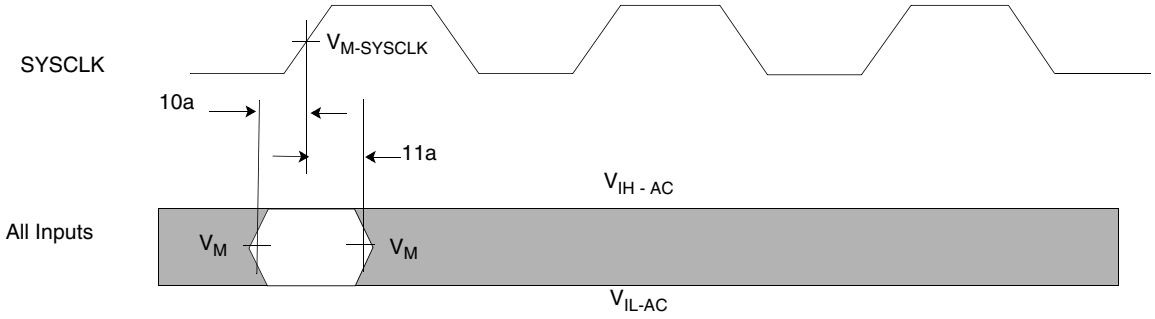


Figure 3-4. Input Timing Diagram

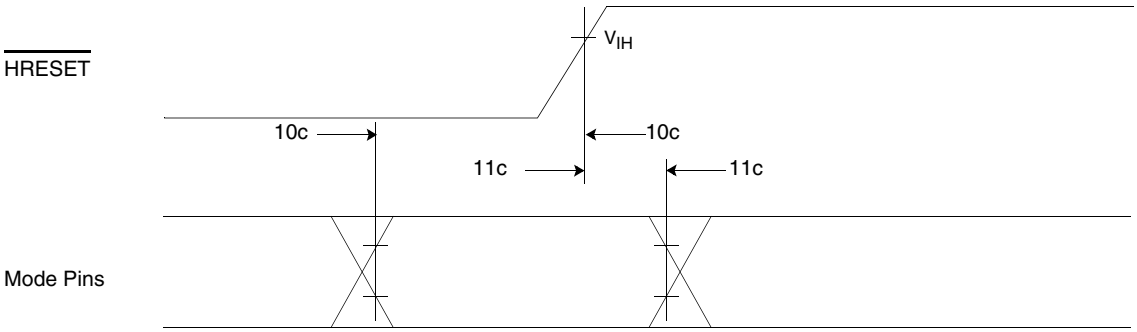


V_M = Midpoint Voltage (OV_{DD}/2)

Note: The minimum slew rate specified in *Table 3-7* on page 27 is required to achieve the input timings specified. See *Section 3.5.1, Input Setup Timing,* on page 28 and *Figure 3-3* for additional information.

Figure 3-5 provides the mode select input timing diagram for the 750CL.

Figure 3-5. Mode Select Input Timing Diagram



3.5.2 Following $\overline{\text{HRESET}}$ Deassertion

Previous PowerPC processors begin arbitrating for the bus shortly after the deassertion of $\overline{\text{HRESET}}$. In contrast, the 750CL waits about 25000 bus clock cycles following the deassertion of $\overline{\text{HRESET}}$ to begin arbitrating for the bus. Until that time, the processor is effectively held in reset. The bus logic and other bus agents should not assume that the 750CL is monitoring the bus until the 750CL first asserts BR (or TS, if the bus is parked on the processor).

3.6 60x Bus Output AC Specifications

Table 3-8 provides the 60x bus output AC timing specifications for the 750CL as defined in *Figure 3-7* on page 33.

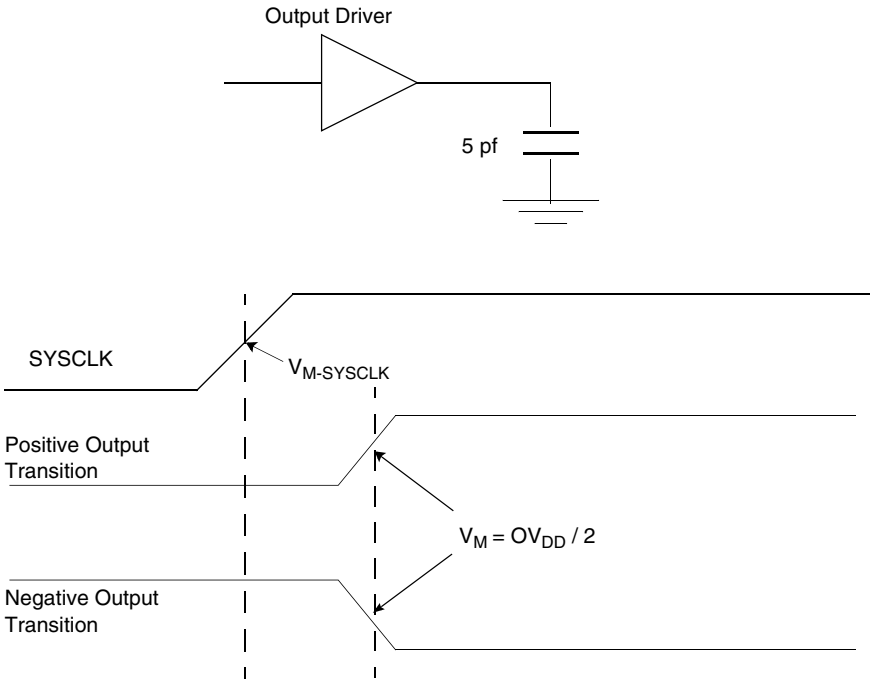
Table 3-8. 60x Bus Output AC Timing Specifications
See *Table 3-2* on page 22 for operating conditions.[1, 4, 5]

Figure 3-7 Timing Reference	Characteristic	Part Numbers ≤ 733 MHz		Part Numbers > 733 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
12	SYSCLK to Output Driven (Output Enable Time)	200	—	200	—	ps	
13	SYSCLK to Output Valid	—	2.6	—	2.6	ns	
14	SYSCLK to Output Invalid (Output Hold)	500	–	500	–	ps	
15	SYSCLK to Output High Impedance (all signals except address retry [ARTRY], address bus busy [ABB], and data bus busy [DBB])	—	2.8	—	2.8	ns	
16	SYSCLK to $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ high impedance after precharge	—	1.0	—	1.0	t_{SYSCLK}	2
17	SYSCLK to $\overline{\text{ARTRY}}$ high impedance before precharge	—	2.7	—	2.7	ps	
18	SYSCLK to $\overline{\text{ARTRY}}$ precharge enable	$(0.2 \times t_{SYSCLK}) + 0.2$	—	$(0.2 \times t_{SYSCLK}) + 0.2$	—	ps	3
19	Maximum delay to $\overline{\text{ARTRY}}$ precharge	—	1.0	—	1.0	t_{SYSCLK}	2, 3
20	SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	—	2.0	—	2.0	t_{SYSCLK}	2, 3

Notes:

1. All output specifications are measured from the V_M of the rising edge of SYSCLK to the midpoint of the output signal in question using a test load as shown in *Figure 3-6* on page 32. Both input and output timings are measured at the pin. Timings are determined by design. Timing values apply while OV_{DD} = 1.5 V nominal and OV_{DD} = 1.8 V nominal.
2. t_{SYSCLK} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
3. Nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}.
4. Guaranteed by design and characterization, and not tested.
5. See *Figure 3-6* on page 32 and *Figure 3-7* on page 33 for output loading and timing definitions.

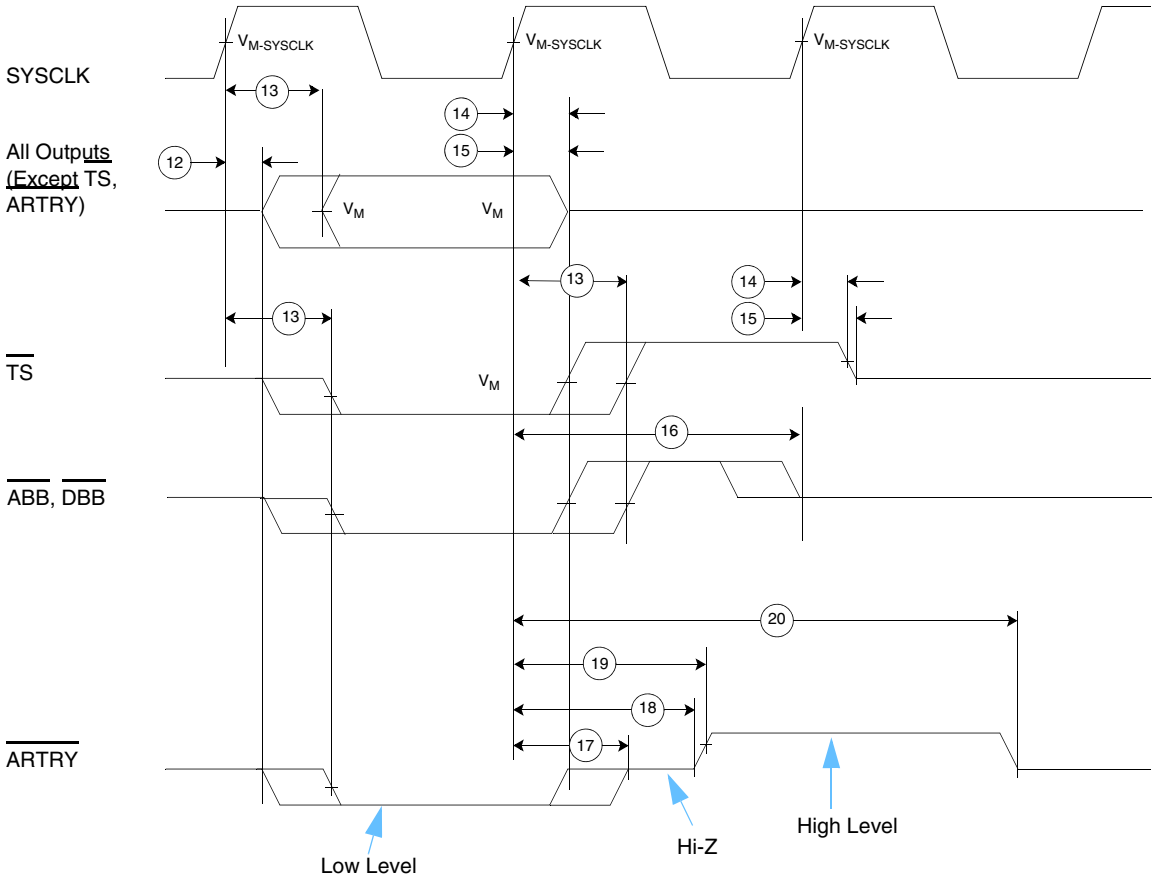
Figure 3-6. Output Valid Timing Definition



Output Transition defined between SYSCLK at V_M and the respective transition level.

Note: The timing definition is valid using the termination model shown here with timings referenced to the respective pin of the specified output driver.

Figure 3-7. Output Timing Diagram for 750CL



Note: SYSCLK V_M as defined in *Section 3.3, Clock Specifications,* on page 25.
Output V_M as defined in *Figure 3-6, Output Valid Timing Definition,* on page 32.

3.6.1 IEEE 1149.1 AC Timing Specifications

Table 3-9 provides the IEEE 1149.1 (JTAG) AC timing specifications. The five JTAG signals are: test data input (TDI), test data output (TDO), test mode select (TMS), test clock (TCK), and test reset (TRST).

Table 3-9. JTAG AC Timing Specifications (Independent of SYSCLK)
See *Table 3-2* on page 22 for operating conditions.

Number	Characteristic	Min.	Max.	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at +0.55 V	15	—	ns	
3	TCK rise and fall times	0	2	ns	4
4	Specification obsolete, intentionally omitted	—	—	—	
5	$\overline{\text{TRST}}$ assert time	25	—	ns	1
6	Boundary-scan input data setup time	1	—	ns	2
7	Boundary-scan input data hold time	3	—	ns	2
8	TCK to output data valid	2	5	ns	3, 5
9	TCK to output high impedance	2	5	ns	3, 4
10	TMS, TDI data setup time	1	—	ns	
11	TMS, TDI data hold time	1	—	ns	
12	TCK to TDO data valid	1	5	ns	5
13	TCK to TDO high impedance	2	5	ns	4
14	TCK to output data invalid (output hold)	0	—	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. Guaranteed by design.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by characterization and not tested.
5. Minimum specification guaranteed by characterization and not tested.

Figure 3-8 provides the JTAG clock input timing diagram.

Figure 3-8. JTAG Clock Input Timing Diagram

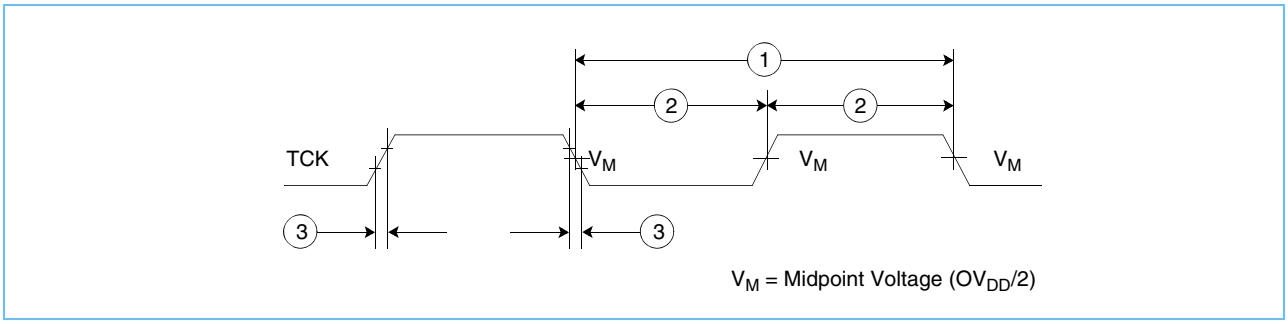


Figure 3-9 provides the $\overline{\text{TRST}}$ timing diagram.

Figure 3-9. $\overline{TRST}$ Timing Diagram

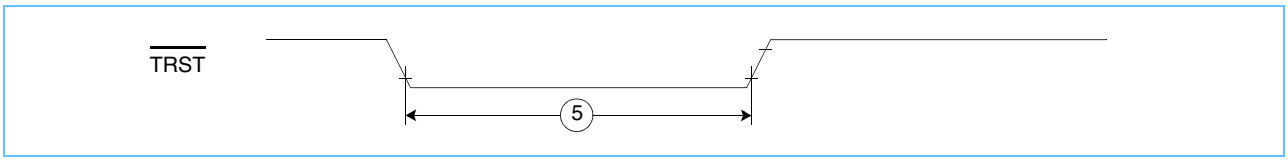


Figure 3-10 provides the boundary-scan timing diagram.

Figure 3-10. Boundary-Scan Timing Diagram

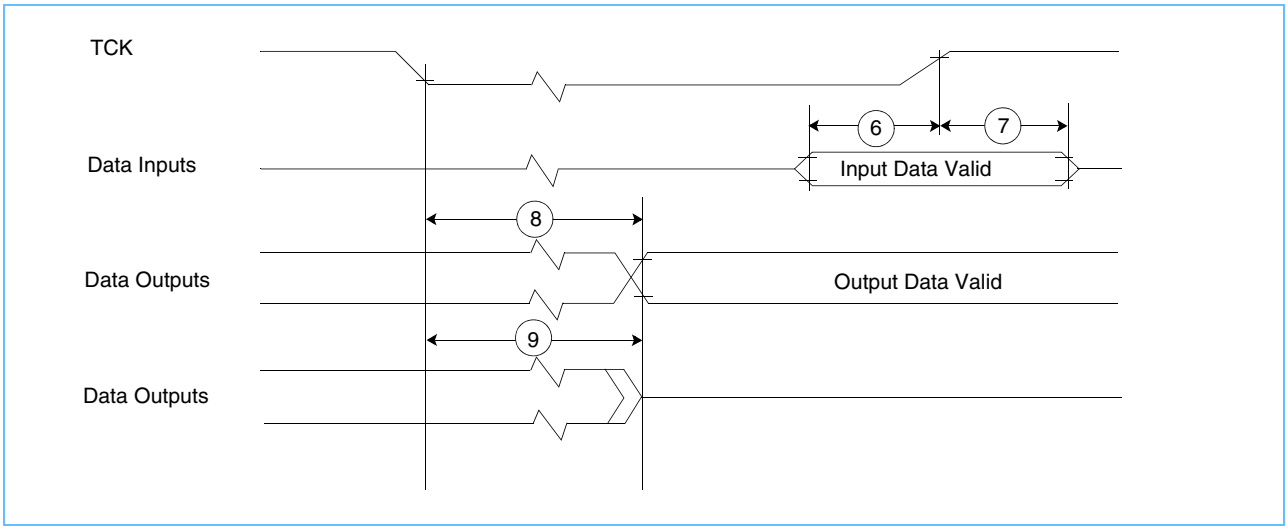
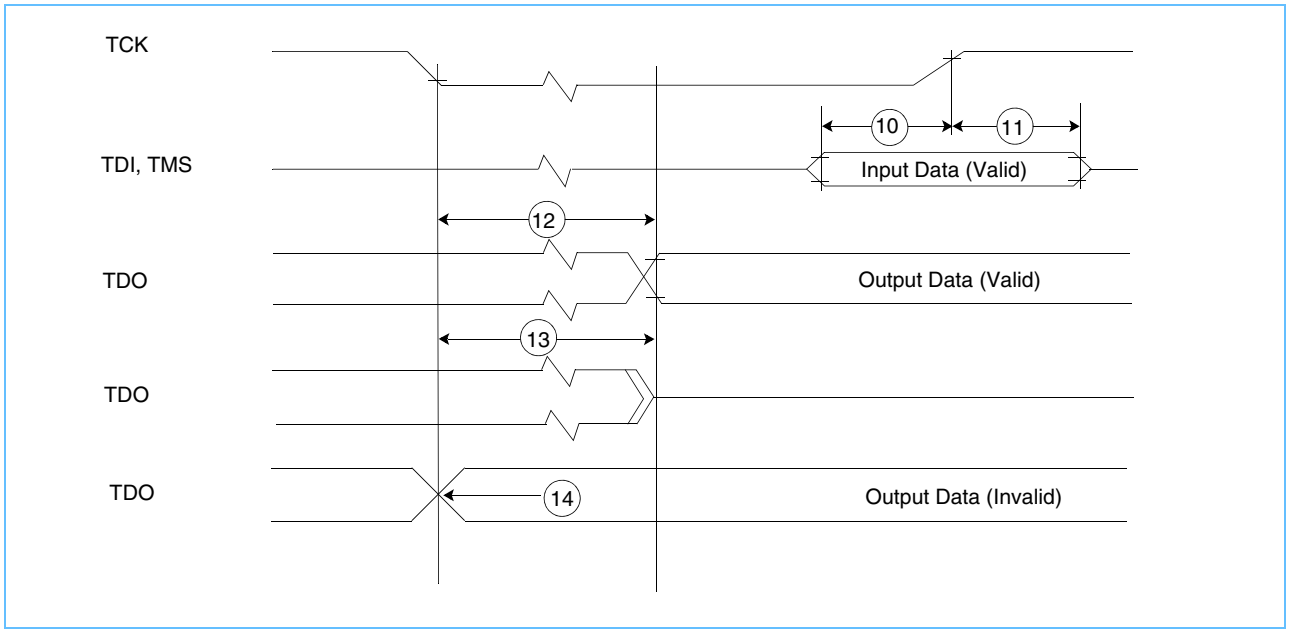


Figure 3-11 provides the test access port timing diagram.

Figure 3-11. Test Access Port Timing Diagram



4. Dimensions and Signal Assignments

IBM offers a flip chip plastic ball grid array (FCPBGA) that supports 278 balls for the 750CL package. This is a signal and power compatible footprint to the PowerPC 750GX RISC microprocessor module. The 750CL pinout, power dissipation, timing, and signal definitions are not completely identical to the 750GX. See the *PowerPC 750CL DD1.2 Differences from 750GX Application Note* for details.

4.1 Package

4.1.1 Overview

FCPBGA packages are suited for applications requiring much higher I/O counts and better electrical performance than that offered by enhanced plastic ball grid array (EPBGA) and high-performance ball grid array (HPBGA) packages. They are recommended for applications having medium electrical performance and power dissipation requirements.

4.1.2 Features

- Low dielectric-constant organic build-up substrate
- Flip chip die attach; BGA second-level interconnect
- Two-layer core
- JEDEC-compliant packages

4.2 Mechanical Specifications

Figure 4-1. Package Drawing (Bottom and Side View)

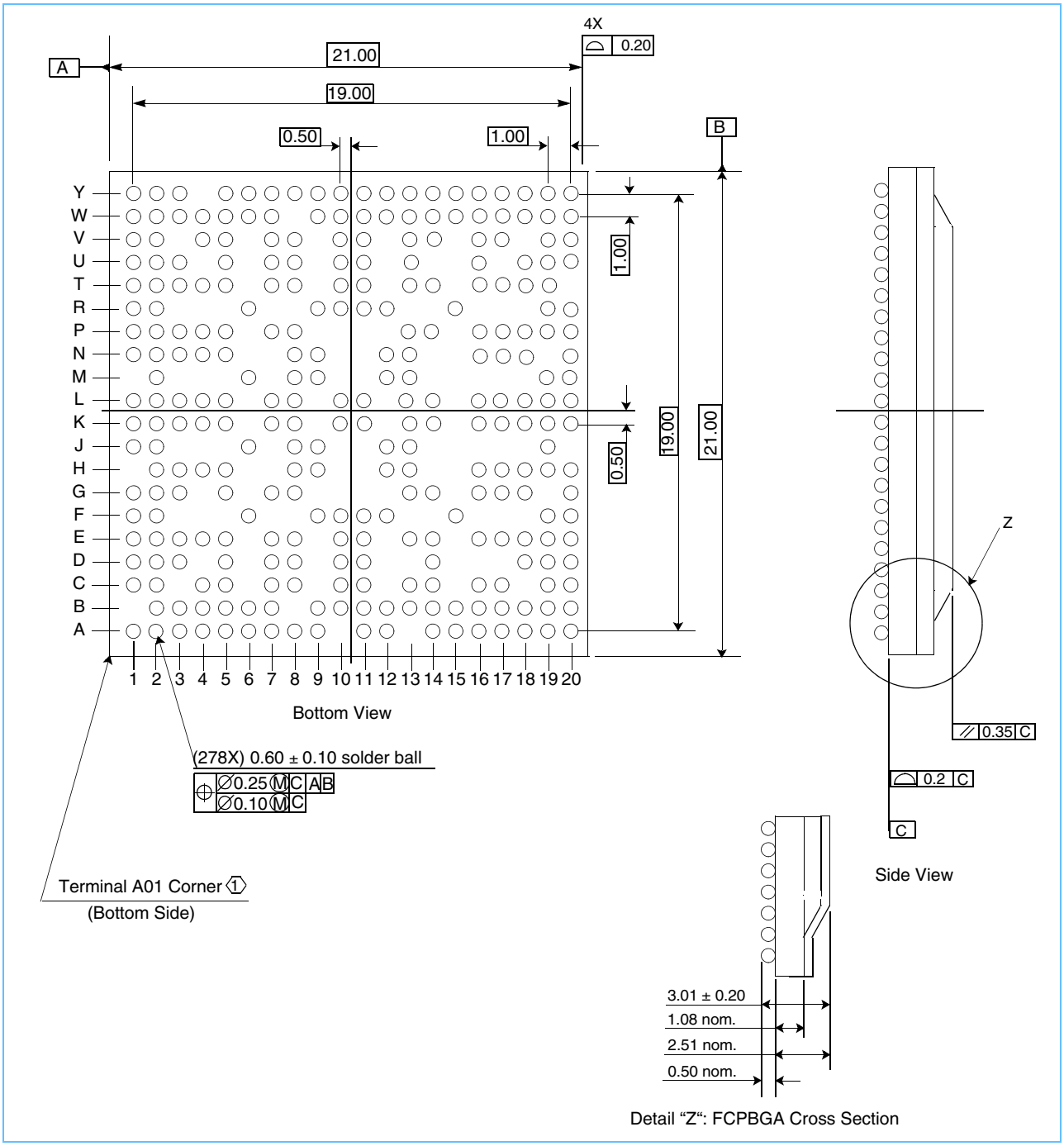
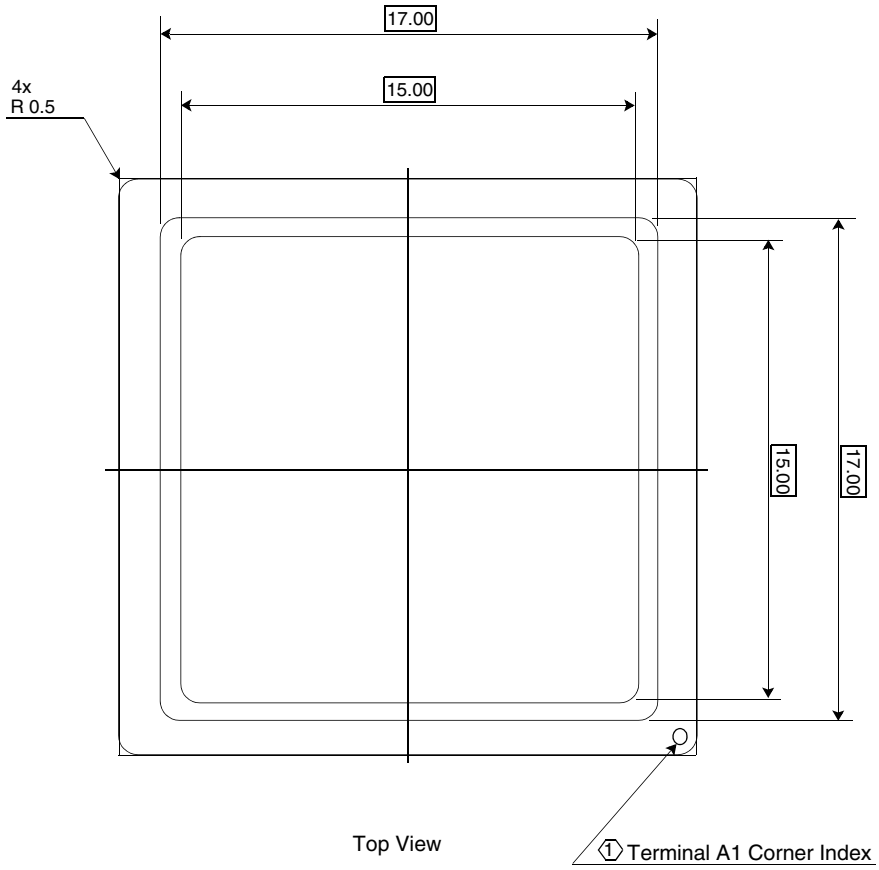


Figure 4-2. Package Drawing (Top View)



Notes:

1. The terminal A1 corner must be identified on the top surface of the package by using a corner chamfer, ink, laser or metallized markings, indentation, or other feature of package body. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner.
2. Package conforms to JEDEC Design standard MS-034.

4.3 Microprocessor Ball Placement

Figure 4-3. PowerPC 750CL Microprocessor Ball Placement

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	A6	A8	A3	A2	A0	DH31	DH25	DH26	NB	DH22	DH19	DH18	DH16	DH15	DH14	NB	DH9	DH10	DH4	DH2
19	A13	GND	A5	A4	A1	DH29	NB	DH28	DH23	DH24	DH21	DH20	NB	DH17	DH11	DH8	DH6	DH5	GND	DH3
18	A11	A10		**OVDD**	GND		**OVDD**	GND		VDD	VDD		GND	**OVDD**		GND	**OVDD**		DH0	PLL_CFG0
17	A12	TT1	**OVDD**		A9		DH30	DH27		GND	GND		DH12	DH13		DH1		**OVDD**	PLL_CFG1	PLL_CFG2
16	A14	A15	GND	NB	A7		GND	**OVDD**		**OVDD**	**OVDD**		**OVDD**	GND		DH7	PLL_CFG3	GND	SYSCLK	**EFUSE**
15	TT3	$\overline{\text{TS}}$				VDD									VDD				$\overline{\text{SYSCLK}}$	**AVDD**
14	TSIZ0	TT2	**OVDD**	TT0	GND		**OVDD**			GND	GND			**OVDD**		GND	NB	**OVDD**	PLL_CFG4	**AGND**
13	NB	TT4	GND	NB	VDD		GND	GND	VDD	VDD	VDD	VDD	GND	GND		VDD	~~LSSD~~ MODE	GND	L2_TSTCLK	L1_TSTCLK
12	$\overline{\text{TA}}$	TSIZ1				VDD		GND	GND			GND	GND		VDD				$\overline{\text{MCP}}$	$\overline{\text{CKSTP\_OUT}}$
11	$\overline{\text{TBST}}$	TSIZ2	VDD	GND	**OVDD**	GND				VDD	VDD				GND	**OVDD**	GND	VDD	$\overline{\text{TLBISYNC}}$	$\overline{\text{HRESET}}$
10	NB	A16	VDD	GND	**OVDD**	GND				GND	GND				GND	**OVDD**	GND	VDD	$\overline{\text{SMI}}$	$\overline{\text{CKSTP\_IN}}$
9	A18	A17				VDD		GND	VDD			VDD	GND		VDD				BVSEL	$\overline{\text{INT}}$
8	$\overline{\text{AACK}}$	NB	GND	A21	VDD		GND	GND	VDD	VDD	VDD	VDD	GND	GND		VDD	$\overline{\text{QREQ}}$	GND	NB	$\overline{\text{QACK}}$
7	A20	A19	**OVDD**	A24	GND		**OVDD**			GND	GND			**OVDD**		GND	$\overline{\text{DBB}}$	**OVDD**	$\overline{\text{ARTRY}}$	$\overline{\text{SRESET}}$
6	$\overline{\text{DBWO}}$	A23				VDD			THRMD2			THRM D1			VDD				$\overline{\text{TEA}}$	$\overline{\text{ABB}}$
5	A22	A26	GND	A25	A31		GND	**OVDD**		**OVDD**	**OVDD**		**OVDD**	GND		CLK_OUT	$\overline{\text{WT}}$	GND	TDO	$\overline{\text{DBG}}$
4	A28	A27	**OVDD**		DL3		NB	DL13		GND	GND		DL23	DL26		$\overline{\text{CI}}$		**OVDD**	$\overline{\text{BG}}$	NB
3	A29	A30		**OVDD**	GND		**OVDD**	GND		VDD	VDD		GND	**OVDD**		GND	**OVDD**		$\overline{\text{DRTRY}}$	BR
2	DL0	GND	DL2	DL6	DL5	DL11	DL10	DL12	DL16	DL15	DL19	DL20	DL22	DL27	DL28	TCK	DL30	TDI	GND	KVDD
1	DL1	NB	DL4	DL8	DL7	DL9	DL14	NB	DL18	DL17	DL21	NB	DL24	DL25	DL29	DL31	$\overline{\text{TRST}}$	TMS	$\overline{\text{GBL}}$	KGND

Note: This view is looking down from above the 750CL placed and soldered on the system board.
NB: There is no ball in this position.
Blank: There is no ball in this position.
NC: No connect - do not connect to this ball.

4.4 Pinout Listings

Table 4-1 contains the pinout listing for the 750CL FCPBGA package.

Table 4-1. Pinout Listing for the FCPBGA Package (Sheet 1 of 3)

Signal Name	Pin Number	Active	Input/Output	Notes
A[0:31]	E20, E19, D20, C20, D19, C19, A20, E16, B20, E17, B18, A18, A17, A19, A16, B16, B10, B9, A9, B7, A7, D8, A5, B6, D7, D5, B5, B4, A4, A3, B3, E5.	High	Input/Output	
$\overline{\text{AACK}}$	A8	Low	Input	
$\overline{\text{ABB}}$	Y6	Low	Input/Output	
AGND	Y14	—	—	
$\overline{\text{ARTRY}}$	W7	Low	Input/Output	
AV_{DD}	Y15	—	—	
$\overline{\text{BG}}$	W4	Low	Input	
$\overline{\text{BR}}$	Y3	Low	Output	
BVSEL	W9	—	Input	3
$\overline{\text{CKSTP\_OUT}}$	Y12	Low	Output	
$\overline{\text{CI}}$	T4	Low	Output	
$\overline{\text{CKSTP\_IN}}$	Y10	Low	Input	
CLK_OUT	T5		Output	
$\overline{\text{DBB}}$	U7	Low	Output	
$\overline{\text{DBG}}$	Y5	Low	Input	
$\overline{\text{DBWO}}$	A6	Low	Input	
DH[0:31]	W18, T17, Y20, Y19, W20, V19, U19, T16, T19, U20, V20, R19, N17, P17, R20, P20, N20, P19, M20, L20, M19, L19, K20, J19, K19, G20, H20, H17, H19, F19, G17, F20	High	Input/Output	
DL[0:31]	A2, A1, C2, E4, C1, E2, D2, E1, D1, F1, G2, F2, H2, H4, G1, K2, J2, K1, J1, L2, M2, L1, N2, N4, N1, P1, P4, P2, R2, R1, U2, T1	High	Input/Output	
$\overline{\text{DRTRY}}$	W3	Low	Input	
EFUSE	Y16	N/A	Input	8
$\overline{\text{GBL}}$	W1	Low	Input/Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. BVSEL low selects single-ended clock input on SYSCLK. BVSEL high selects differential clock input on SYSCLK and $\overline{\text{SYSCLK}}$.
4. TCK must be tied high or low for normal machine operation.
5. No ball is installed in this location.
6. SYSCLK is the active low clock input used with SYSCLK in differential mode. In single-ended mode, SYSCLK is used as the clock input, and $\overline{\text{SYSCLK}}$ is grounded.
7. Must be connected to OV_{DD} during normal operation.
8. Must be connected to GND during normal operation.
9. Kelvin V_{DD} and GND for voltage regulator sensing.
10. On DD1.x, this signal must be pulled up to OV_{DD} for normal operation. On DD2.x, this signal selects the I/O operating voltage such that a pulldown to GND selects 1.8 V and a pull up to OV_{DD} selects 1.15 V.

Table 4-1. Pinout Listing for the FCPBGA Package (Sheet 2 of 3)

Signal Name	Pin Number	Active	Input/Output	Notes
GND	B2, B19, C5, C8, C13, C16, D10, D11, E3, E7, E14, E18, F10, F11, G5, G8, G13, G16, H3, H8, H9, H12, H13, H18, J12, K4, K7, K10, K14, K17, L4, L7, L10, L14, L17, M12, N3, N8, N9, N12, N13, N18, P5, P8. P13, P16, R10, R11, T3, T7, T14, T18, U10, U11, V5, V8, V13,V16, W2, W19,	—	—	
$\overline{\text{HRESET}}$	Y11	Low	Input	
$\overline{\text{INT}}$	Y9	Low	Input	
KGND	Y1	—	—	9
KV_{DD}	Y2	—	—	9
L1_TSTCLK	Y13	High	Input	8
L2_TSTCLK	W13	High	Input	10
$\overline{\text{LSSD\_MODE}}$	U13	Low	Input	1
$\overline{\text{MCP}}$	W12	Low	Input	
NB	U14, Y4, D16, D13, A13, B8, T20, N19, J20, G19, B1, G4, H1, M1, A10, W8	—	—	5
OV_{DD}	C4, C7, C14, C17, D3, D18, E10, E11, G3, G7, G14, G18, H5, H16, K5, K16, L5, L16, N5, N16, P3, P7, P14, P18, T10, T11, U3, U18, V4, V7, V14, V17	—	—	2
PLL_CFG[0:4]	Y18, W17, Y17, U16, W14	High	Input	
$\overline{\text{QACK}}$	Y8	Low	Input	
$\overline{\text{QREQ}}$	U8	Low	Output	
$\overline{\text{SMI}}$	W10	Low	Input	
$\overline{\text{SRESET}}$	Y7	Low	Input	
SYSCLK	W16	High	Input	6
$\overline{\text{SYSCLK}}$	W15	Low	Input	6
$\overline{\text{TA}}$	A12	Low	Input	
$\overline{\text{TBST}}$	A11	Low	Input/Output	
TCK	T2	High	Input	4
TDI	V2	High	Input	
TDO	W5	High	Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. BVSEL low selects single-ended clock input on SYSCLK. BVSEL high selects differential clock input on SYSCLK and $\overline{\text{SYSCLK}}$.
4. TCK must be tied high or low for normal machine operation.
5. No ball is installed in this location.
6. SYSCLK is the active low clock input used with SYSCLK in differential mode. In single-ended mode, SYSCLK is used as the clock input, and $\overline{\text{SYSCLK}}$ is grounded.
7. Must be connected to OV_{DD} during normal operation.
8. Must be connected to GND during normal operation.
9. Kelvin V_{DD} and GND for voltage regulator sensing.
10. On DD1.x, this signal must be pulled up to OV_{DD} for normal operation. On DD2.x, this signal selects the I/O operating voltage such that a pulldown to GND selects 1.8 V and a pull up to OV_{DD} selects 1.15 V.

Table 4-1. Pinout Listing for the FCPBGA Package (Sheet 3 of 3)

Signal Name	Pin Number	Active	Input/Output	Notes
$\overline{\text{TEA}}$	W6	Low	Input	
THRMD1	M6	See *Section 5.6* on page 48		
THRMD2	J6			
$\overline{\text{TLBISYNC}}$	W11	Low	Input	
TMS	V1	High	Input	
$\overline{\text{TRST}}$	U1	Low	Input	
$\overline{\text{TS}}$	B15	Low	Input/Output	
TSIZ[0:2]	A14, B12, B11	High	Output	
TT[0:4]	D14, B17, B14, A15, B13	High	Input/Output	
V_{DD}	C10, C11, E8, E13, F6, F9, F12, F15, J8, J9, J13, K3, K8, K11, K13, K18, L3, L8, L11, L13, L18, M8, M9, M13, R6, R9, R12, R15, T8, T13, V10, V11	—	—	2
$\overline{\text{WT}}$	U5	Low	Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. BVSEL low selects single-ended clock input on SYSCLK. BVSEL high selects differential clock input on SYSCLK and $\overline{\text{SYSCLK}}$.
4. TCK must be tied high or low for normal machine operation.
5. No ball is installed in this location.
6. SYSCLK is the active low clock input used with SYSCLK in differential mode. In single-ended mode, SYSCLK is used as the clock input, and $\overline{\text{SYSCLK}}$ is grounded.
7. Must be connected to OV_{DD} during normal operation.
8. Must be connected to GND during normal operation.
9. Kelvin V_{DD} and GND for voltage regulator sensing.
10. On DD1.x, this signal must be pulled up to OV_{DD} for normal operation. On DD2.x, this signal selects the I/O operating voltage such that a pulldown to GND selects 1.8 V and a pull up to OV_{DD} selects 1.15 V.

5. System Design Information

This section provides electrical and thermal design recommendations for successful applications on the 750CL.

5.1 Reference Clock Selection

The PowerPC 750CL microprocessor supports either single-ended or differential clock inputs. The reference clock is selected with the pin BVSEL. BVSEL set to GND selects a single-ended reference clock. BVSEL set to OV_{DD} selects differential clock inputs.

For single-ended clock operation, the reference clock should be applied to pin SYSCLK. The pin $\overline{\text{SYSCLK}}$ should be tied to GND.

For differential clock operation, the differential reference clocks should be applied to pin SYSCLK and SYSCLK. The recommended board terminations are either:

- 50 Ω impedance to GND on pin SYSCLK and 50 Ω impedance to GND on pin $\overline{\text{SYSCLK}}$ or
- 100 Ω impedance between pins SYSCLK and $\overline{\text{SYSCLK}}$

5.2 PLL Configuration

Table 5-1 shows the PLL configuration for the 750CL for nominal frequencies.

Table 5-1. 750CL Microprocessor PLL Configuration (Sheet 1 of 2)

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)
Binary	Decimal	
00100	4	2×
00101	5	2.5×
00110	6	3×
00111	7	3.5×
01000	8	4×
01001	9	4.5×
01010	10	5×
01011	11	5.5×
01100	12	6×
01101	13	6.5×
01110	14	7×
01111	15	7.5×
10000	16	8×
10001	17	8.5×

Notes:
1. The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PTBFR).

Table 5-1. 750CL Microprocessor PLL Configuration (Sheet 2 of 2)

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)
Binary	Decimal	
10010	18	9×
10011	19	9.5×
10100	20	10×

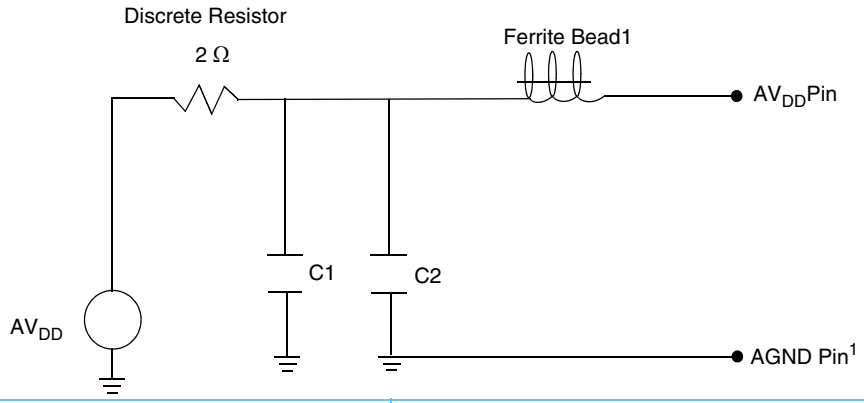
Notes:
1. The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PTBFR).

5.3 PLL Power Supply Filtering

The 750CL microprocessor has an AV_{DD} signal that provides power to the clock generation PLL.

To ensure stability of the internal clock, the power supplied to the AV_{DD} input signals should be filtered using a circuit similar to the one shown in *Figure 5-1*. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible.

Figure 5-1. PLL Power Supply Filter Circuit



Item	Description/Value
Resistor	2 Ω
C1	0.1 μF Ceramic
C2	10.0 μF Ceramic
Ferrite Bead	30 Ω (typical) - Murata BLM21P300S or similar

Notes:
1. Connected to ground without a filter.

5.4 Decoupling Recommendations

Capacitor decoupling is required for the 750CL. Decoupling capacitors act to reduce high-frequency chip switching noise and provide localized bulk charge storage to reduce major power-surge effects. Guidelines for high-frequency noise decoupling will be provided in a separate application note. Bulk decoupling requires a more complete understanding of the system and system power architecture, which is beyond the scope of this document.

High-frequency decoupling capacitors should be located as close as possible to the processor with low lead inductance to the ground and voltage planes.

Decoupling capacitors are recommended on the back of the card, directly opposite the module. The recommended placement and number of decoupling capacitors, 34 V_{DD}-GND capacitors and 44 OV_{DD}-GND capacitors, are described in *Figure 5-2* on page 47. The recommended decoupling capacitor specifications are provided in *Table 5-2*. The placement and usage described here are guidelines for decoupling capacitors and should be applied for system designs.

Table 5-2. Recommended Decoupling Capacitor Specifications

Item	Description
Decoupling capacitor specifications	Type X5R or Y5V 10 V minimum 0402 size 40 × 20 mils, nominally 1.0 mm × 0.5 mm ±0.1 mm on both dimensions
	100 nF
Recommended minimum number of decoupling capacitors on the back of the card	34 V_{DD}-GND capacitors 44 OV_{DD}-GND capacitors

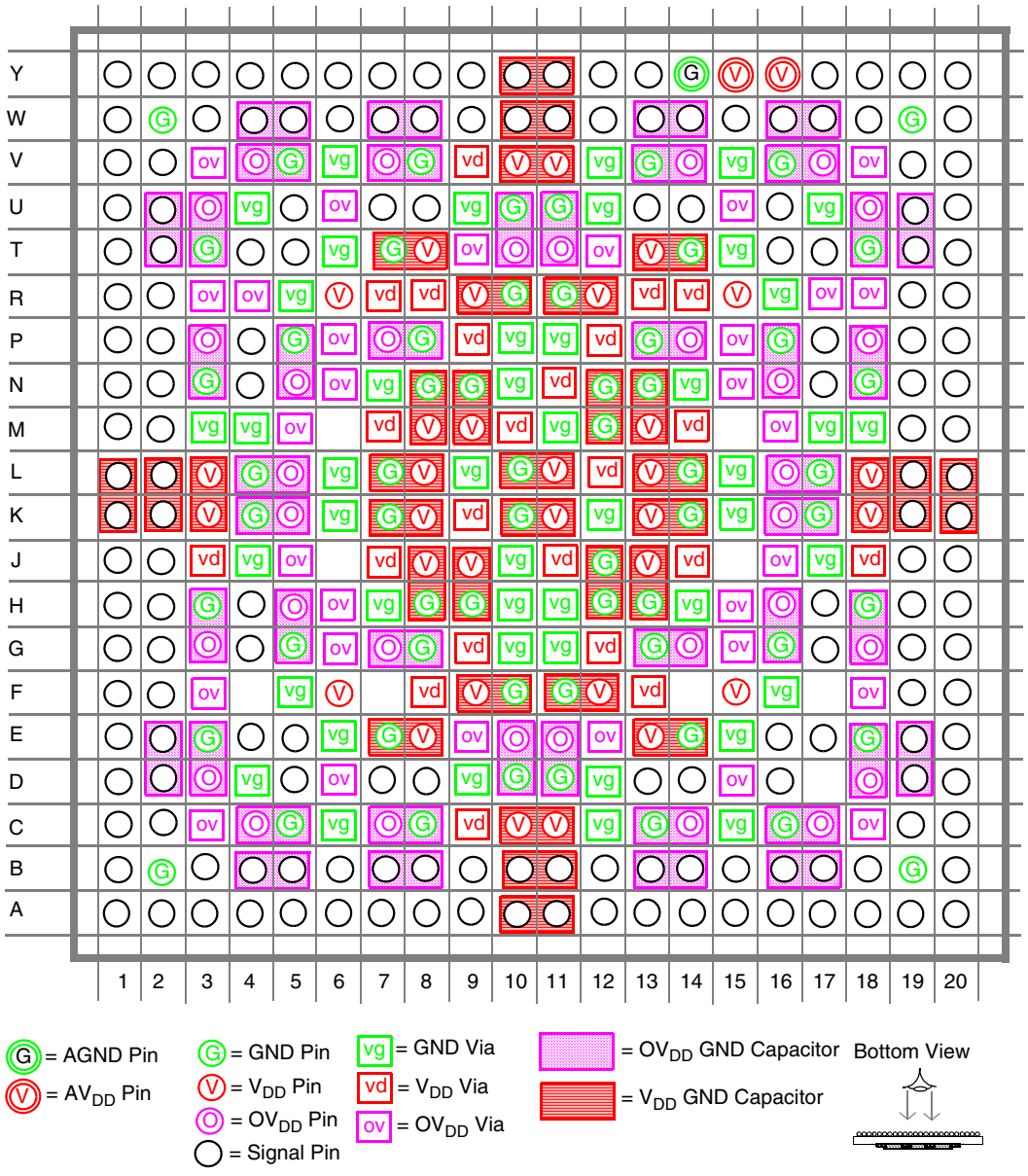
Note: The decoupling capacitor electrodes are located directly opposite their corresponding BGA pins where possible. Also, each electrode for each decoupling capacitor needs to be connected to one or more BGA pins (balls) with a short electrical path. Thus, through-vias adjacent to the decoupling capacitors are recommended.

The card designer can expand on the decoupling capacitor recommendations by doing the following:

- Adding additional decoupling capacitors.
  If using additional decoupling capacitors, verify that these additional capacitors do not reduce the number of card vias or cause the vias to lose proximity to each capacitor electrode.
- Adding additional through-vias or blind-vias.
  Card technologies are available that will reduce the inductance between the decoupling capacitor and the BGA pin (ball). Replacing single vias with multiple vias is highly recommended. Place GND vias close to V_{DD} or OV_{DD} vias to reduce loop inductance.

Figure 5-2 on page 47 shows the mapping of power, ground, and signal pin assignments, and the recommended layout of decoupling capacitors under application conditions. In test mode, pins C11 and G8 can be used as Kelvin probes, in which case the pins should be disconnected from card GND and V_{DD}. Capacitors should not be connected to the Kelvin pins during Kelvin probe voltage measurements.

Figure 5-2. Orientation and Layout of the 750CL Decoupling Capacitors



For more information, see the *PowerPC 750FX Power Supply Layout and Bypassing Application Note,* which also applies to the PowerPC 750CL.

5.5 Connection Recommendations

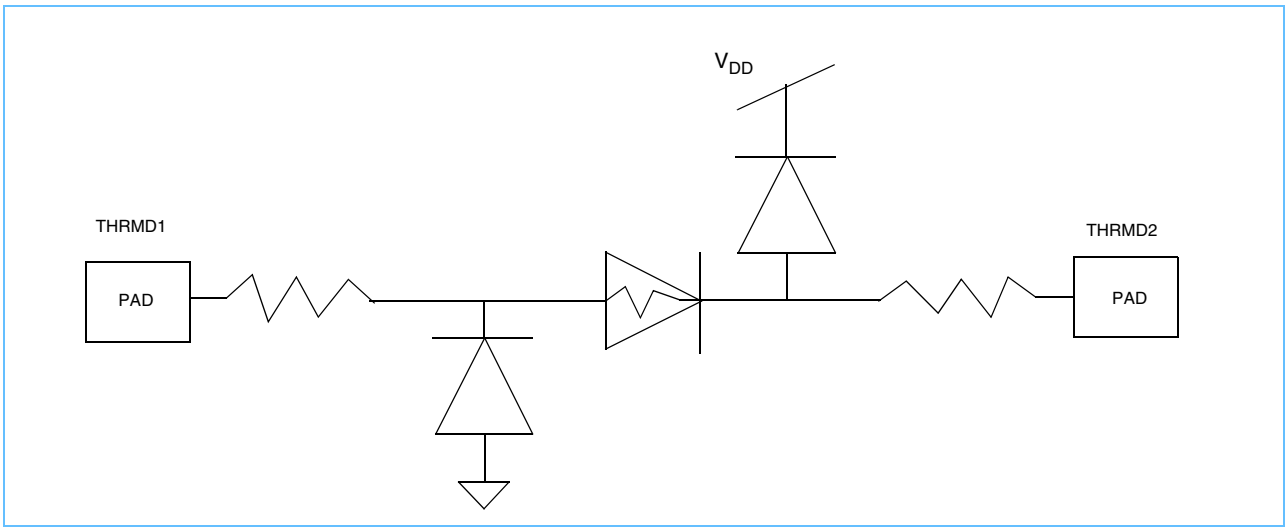
To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All no-connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, AV_{DD}, and GND pins of the 750CL.

5.6 Die Temperature Monitor

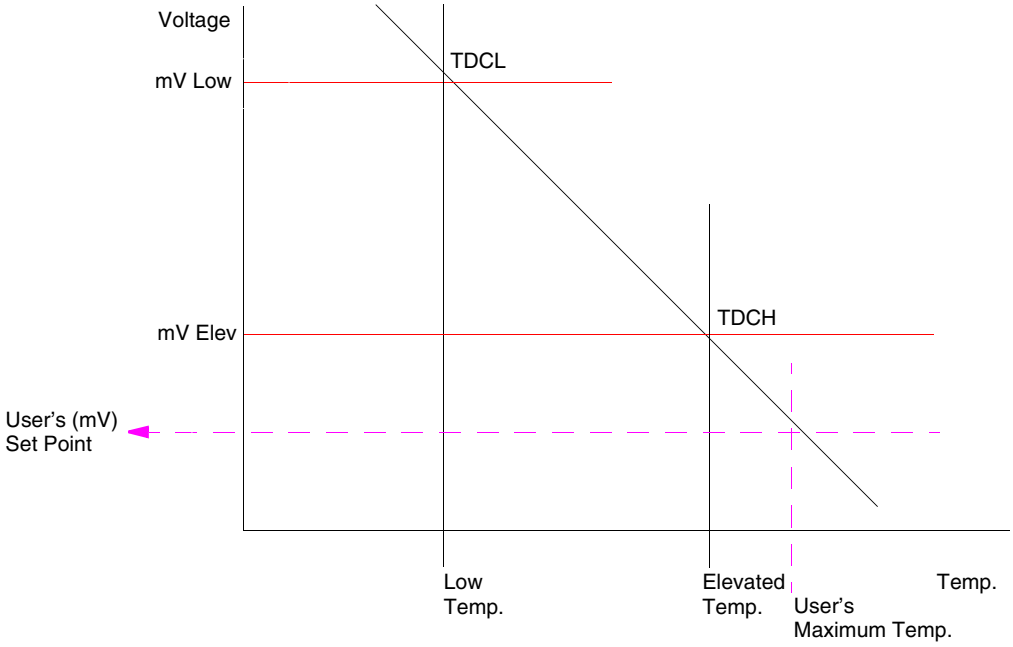
The PowerPC 750CL microprocessor features an on-board temperature sensing diode for determining the chip junction temperature, T_J. A schematic of the thermal diode is shown in *Figure 5-3*. The thermal diode is placed within the die circuitry in proximity of the hottest area on the die. Its terminals are then connected to pins THRMD1 and THRMD2.

Figure 5-3. Thermal Diode Schematic



The procedure for monitoring temperature involves forcing a 100 μA current through the diode and measuring the resultant voltage. The measured voltage can then be used to interpolate the junction temperature using two reference voltage/temperature data points that are preset at the factory. The reference points are stored in the 750CL Thermal Diode Calibration Registers, TDCL and TDCH. TDCL contains the diode voltage from forcing 100 μA through the diode at a low temperature (both voltage and temperature included in the register). TDCH contains the diode voltage from forcing 100 μA through the diode at a high temperature (also included in the register). Consult the *IBM PowerPC 750CL RISC Microprocessor User's Manual* for the specific format of the registers. The graph in *Figure 5-4* on page 49 illustrates the procedure for determining the chip junction temperature based on the user's voltage measurement and the reference points provided in the calibration registers.

Figure 5-4. Interpolating Chip Junction Temperature Using Thermal Calibration Registers and User Voltage Measurement



5.7 Output Buffer DC Impedance

The 750CL 60x drivers were characterized over various process, voltage, and temperature conditions. To measure driver impedance, an external resistor is connected to the chip pad, either to OV_{DD} or GND. Then the value of the resistor is varied until the pad voltage is $OV_{DD}/2$ (see *Figure 5-5, Driver Impedance Measurement,* on page 50).

The output impedance is actually the average of two resistances: the resistance of the pullup device and the resistance of pulldown device. When Data is held high, SW1 is closed (SW2 is open), and R_N is trimmed until Pad = $OV_{DD}/2$; R_N then becomes the resistance of the pullup devices. When Data is held low, SW2 is closed (SW1 is open), and R_P is trimmed until Pad = $OV_{DD}/2$; R_P then becomes the resistance of the pulldown devices. With a properly designed driver, R_P and R_N are close to each other in value; then driver impedance equals $(R_P + R_N)/2$.

Figure 5-5. Driver Impedance Measurement

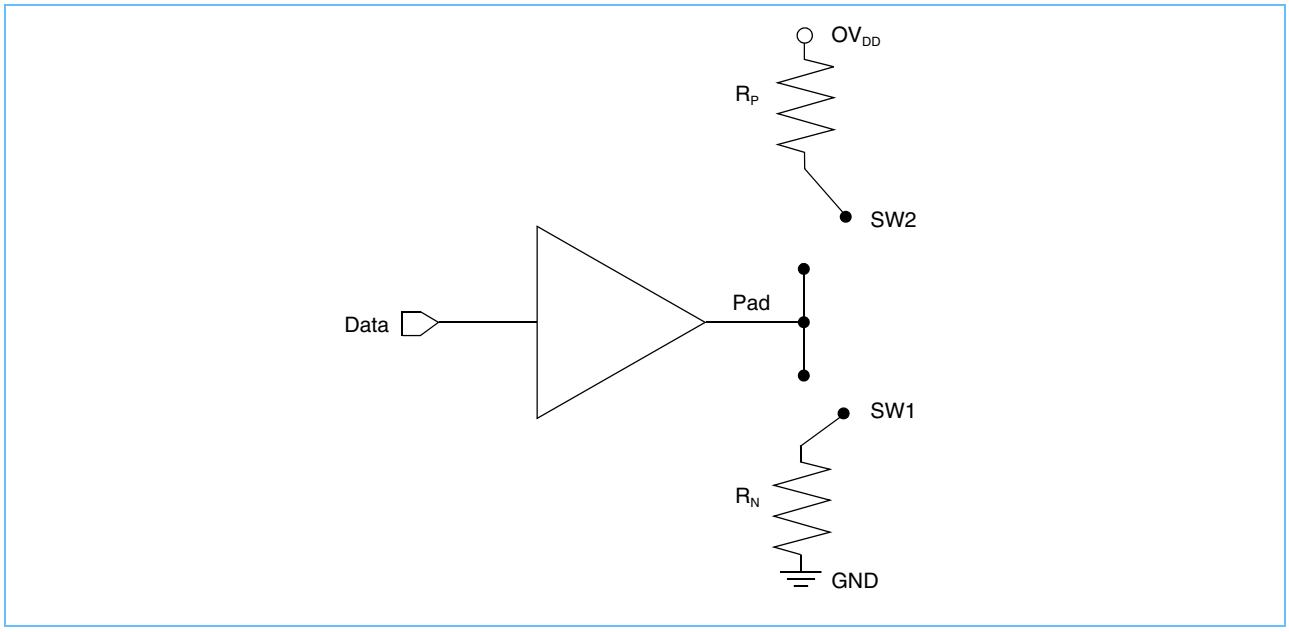


Table 5-3 summarizes the driver impedance characteristics needed to design a typical process.

Table 5-3. Driver Impedance Characteristics

Process	60× Impedance (Ω)	OV_{DD} (V)	T (^{o}C)
Worst	37	1.15	65
Typical	42	1.15	65
Best	50	1.15	65
Worst	35	1.8	65
Typical	42	1.8	65
Best	50	1.8	65

5.7.1 Input/Output Usage

Table 5-4 provides details on the input/output usage of the 750CL signals. The “Usage Group” column refers to the general functional category of the signal.

In the 750CL, certain input/output signals have pullups and pulldowns, which may or may not be enabled. In *Table 5-4,* the “Input/Output with Internal Pullup Resistors” column defines which signals have these pullups or pulldowns and their active or inactive state. The “Level Protect” column defines which signals have the designated function added to their input/output cell. For more about level protection, see *Section 5.10.1* on page 63.

Table 5-4. Input/Output Usage (Sheet 1 of 4)

750CL Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
A[0:31]	High	Input/Output	Address Bus		Keeper			1, 3, 4
$\overline{\text{AACK}}$	Low	Input	Address Termination		Keeper		Must be actively driven	3, 4, 5
$\overline{\text{ABB}}$	Low	Input/Output	—		Keeper	1 K Ω	Pullup required to OV_{DD}	3, 4, 5
AGND	—	—	Power Supply					
$\overline{\text{ARTRY}}$	Low	Input/Output	Address Termination		Keeper	1 K Ω	Pullup required to OV_{DD}	3, 4, 5
AV_{DD}	—	—	PLL Power Supply					
$\overline{\text{BG}}$	Low	Input	Address Arbitration		Keeper		Active driver or pulldown	3, 4, 5
$\overline{\text{BR}}$	Low	Output	Address Arbitration		Keeper		Chip actively drives	3, 4, 5
BVSEL	N/A	Input	Mode Select	Internal pullup enabled		1 K Ω	Pullup/pulldown, as required	5
$\overline{\text{CI}}$	Low	Output	Transfer Attributes		Keeper			1, 3, 4
$\overline{\text{CKSTP\_IN}}$	Low	Input	Interrupt/Resets		Keeper		Must be actively driven	3, 4, 5

Notes:

1. Depends on the system design. The electrical characteristics of the 750CL do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. HRESET, SRESET, and TRST are signals used for RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the IBM PowerPC 750CL RISC Microprocessor (see *Figure 5-6* on page 55 and *Section 5.11.3.1* on page 66).
3. The 750CL provides protection from meta-stability on inputs through the use of a “keeper” circuit on specific inputs (see *Section 5.10* on page 63 for a more detailed description).
4. If a system design requires a signal level to be maintained while not being actively driven, an external resistor or device must be used (keepers assure no meta-stability of inputs but do not guarantee a level).
5. The 750CL does not require external pullups on address and data lines. Control lines must be treated individually.
6. Mode Select pins require the proper state at HRESET to configure the operating mode of the processor (see *Table 5-7, Summary of Mode Select,* on page 63).
7. Use SYSCLK for single-ended operation: ground $\overline{\text{SYSCLK}}$. For differential clock mode, a 50 Ω resistor to GND is required on both SYSCLK and $\overline{\text{SYSCLK}}$. See *Reference Clock Selection* on page 44. For single-ended operation, BVSEL must be continuously low. For differential operation, BVSEL must be continuously pulled, driven, or connected to OV_{DD}. See *Table 4-1, Pinout Listing for the FCPBGA Package,* on page 41.

Table 5-4. Input/Output Usage (Sheet 2 of 4)

750CL Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
$\overline{\text{CKSTP\_OUT}}$	Low	Output	Interrupt/Resets		Keeper	1 K Ω	Pullup required to OV_{DD}	3, 4, 5
CLK_OUT	High	Output	—		Keeper			3, 4
$\overline{\text{DBB}}$	Low	Input/Output	—		Keeper	1 K Ω	Pullup required to OV_{DD}	3, 4, 5
$\overline{\text{DBG}}$	Low	Input	Data Arbitration		Keeper		Active driver or tie low	3, 4, 5
$\overline{\text{DBWO}}$	Low	Input	Mode Select/Control		Keeper		Must be actively driven	3, 4, 6
DH[0:31]	High	Input/Output	Data Bus		Keeper			1, 3, 4
DL[0:31]	High	Input/Output	Data Bus		Keeper			1, 3, 4
$\overline{\text{DRTRY}}$	Low	Input	Mode Select/Control		Keeper		Must be actively driven	3, 4, 6
EFUSE		Input	Factory				Must be tied to GND	
$\overline{\text{GBL}}$	Low	Input/Output	Transfer Attributes		Keeper			1, 3, 4
GND	—	—	Power Supply					
$\overline{\text{HRESET}}$	Low	Input	Interrupt/Resets		Keeper		Active driver	2, 3, 4, 5
$\overline{\text{INT}}$	Low	Input	Interrupt/Resets		Keeper		Active driver or pullup	3, 4, 5
L1_TSTCLK	High	Input	Factory	Internal pullup disabled		1 K Ω	Pulldown required	5
L2_TSTCLK	High	Input	Mode Select	Internal pullup disabled		1 K Ω	DD2.x pullup/pulldown as required	5 see *Table 4-1*
$\overline{\text{LSSD\_MODE}}$	Low	Input	Factory	Internal pullup disabled		1 K Ω	Pullup required to OV_{DD}	5

Notes:

1. Depends on the system design. The electrical characteristics of the 750CL do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. HRESET, SRESET, and TRST are signals used for RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the IBM PowerPC 750CL RISC Microprocessor (see *Figure 5-6* on page 55 and *Section 5.11.3.1* on page 66).
3. The 750CL provides protection from meta-stability on inputs through the use of a “keeper” circuit on specific inputs (see *Section 5.10* on page 63 for a more detailed description).
4. If a system design requires a signal level to be maintained while not being actively driven, an external resistor or device must be used (keepers assure no meta-stability of inputs but do not guarantee a level).
5. The 750CL does not require external pullups on address and data lines. Control lines must be treated individually.
6. Mode Select pins require the proper state at HRESET to configure the operating mode of the processor (see *Table 5-7, Summary of Mode Select,* on page 63).
7. Use SYSCLK for single-ended operation: ground $\overline{\text{SYSCLK}}$. For differential clock mode, a 50 Ω resistor to GND is required on both SYSCLK and $\overline{\text{SYSCLK}}$. See *Reference Clock Selection* on page 44. For single-ended operation, BVSEL must be continuously low. For differential operation, BVSEL must be continuously pulled, driven, or connected to OV_{DD}. See *Table 4-1, Pinout Listing for the FCPBGA Package,* on page 41.

Table 5-4. Input/Output Usage (Sheet 3 of 4)

750CL Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
$\overline{\text{MCP}}$	Low	Input	Interrupt/Resets		Keeper		Active driver or pullup	3, 4, 5
OV_{DD}	—	—	Power Supply					
PLL_CFG[0:4]	High	Input	Mode Select/Control		Keeper	1 K Ω	Pullup/pulldown, as required	3, 4, 5
$\overline{\text{QACK}}$	Low	Input	Mode Select/Control		Keeper		Must be actively driven	3, 4, 5, 6
$\overline{\text{QREQ}}$	Low	Output	Status/Control		Keeper		Chip actively drives	3, 4, 5
$\overline{\text{SMI}}$	Low	Input	—		Keeper			3, 4
$\overline{\text{SRESET}}$	Low	Input	Interrupt/Resets		Keeper		Active driver required	2, 3, 4, 5
SYSCLK	High	Input	Clock				Active driver	7
$\overline{\text{SYSCLK}}$	Low	Input	Clock				Active driver	7
$\overline{\text{TA}}$	Low	Input	Data Termination		Keeper		Active driver	3, 4, 5
$\overline{\text{TBST}}$	Low	Input/Output	Transfer Attributes		Keeper			1, 3, 4
TCK	High	Input	JTAG	Internal pullup disabled		1 K Ω	Pulldown required	5
TDI	High	Input	JTAG	Internal pullup enabled				5
TDO	High	Output	JTAG		Keeper			3, 4
$\overline{\text{TEA}}$	Low	Input	Data Termination		Keeper		Active driver or pullup	3, 4, 5
THRMD1								
THRMD2								
$\overline{\text{TLBISYNC}}$	Low	Input	Mode Select/Control		Keeper		Must be actively driven	3, 4, 6

Notes:

1. Depends on the system design. The electrical characteristics of the 750CL do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. HRESET, SRESET, and TRST are signals used for RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the IBM PowerPC 750CL RISC Microprocessor (see *Figure 5-6* on page 55 and *Section 5.11.3.1* on page 66).
3. The 750CL provides protection from meta-stability on inputs through the use of a “keeper” circuit on specific inputs (see *Section 5.10* on page 63 for a more detailed description).
4. If a system design requires a signal level to be maintained while not being actively driven, an external resistor or device must be used (keepers assure no meta-stability of inputs but do not guarantee a level).
5. The 750CL does not require external pullups on address and data lines. Control lines must be treated individually.
6. Mode Select pins require the proper state at HRESET to configure the operating mode of the processor (see *Table 5-7, Summary of Mode Select,* on page 63).
7. Use SYSCLK for single-ended operation: ground $\overline{\text{SYSCLK}}$. For differential clock mode, a 50 Ω resistor to GND is required on both SYSCLK and $\overline{\text{SYSCLK}}$. See *Reference Clock Selection* on page 44. For single-ended operation, BVSEL must be continuously low. For differential operation, BVSEL must be continuously pulled, driven, or connected to OV_{DD}. See *Table 4-1, Pinout Listing for the FCPBGA Package,* on page 41.

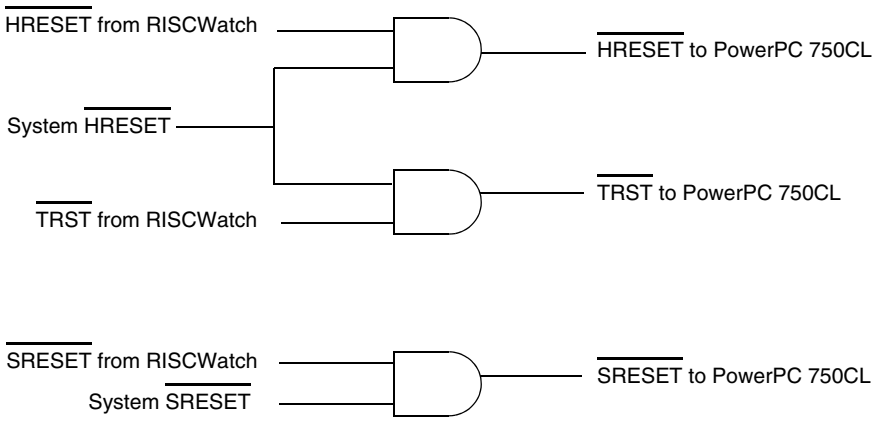
Table 5-4. Input/Output Usage (Sheet 4 of 4)

750CL Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
TMS	High	Input	JTAG	Internal pullup enabled				5
$\overline{\text{TRST}}$	Low	Input	JTAG	Internal pullup enabled				2, 5
$\overline{\text{TS}}$	Low	Input/Output	Address Start		Keeper	1 K Ω	Pullup required to OV_{DD}	3, 4, 5
TSIZ[0:2]	High	Output	Transfer Attributes		Keeper			1, 3, 4
TT[0:4]	High	Input/Output	Transfer Attributes		Keeper			1, 3, 4
V_{DD}	—	—	Power Supply					
$\overline{\text{WT}}$	Low	Output	Transfer Attributes		Keeper			1, 3, 4

Notes:

1. Depends on the system design. The electrical characteristics of the 750CL do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. HRESET, SRESET, and TRST are signals used for RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the IBM PowerPC 750CL RISC Microprocessor (see *Figure 5-6* on page 55 and *Section 5.11.3.1* on page 66).
3. The 750CL provides protection from meta-stability on inputs through the use of a “keeper” circuit on specific inputs (see *Section 5.10* on page 63 for a more detailed description).
4. If a system design requires a signal level to be maintained while not being actively driven, an external resistor or device must be used (keepers assure no meta-stability of inputs but do not guarantee a level).
5. The 750CL does not require external pullups on address and data lines. Control lines must be treated individually.
6. Mode Select pins require the proper state at HRESET to configure the operating mode of the processor (see *Table 5-7, Summary of Mode Select,* on page 63).
7. Use SYSCLK for single-ended operation: ground $\overline{\text{SYSCLK}}$. For differential clock mode, a 50 Ω resistor to GND is required on both SYSCLK and $\overline{\text{SYSCLK}}$. See *Reference Clock Selection* on page 44. For single-ended operation, BVSEL must be continuously low. For differential operation, BVSEL must be continuously pulled, driven, or connected to OV_{DD}. See *Table 4-1, Pinout Listing for the FCPBGA Package,* on page 41.

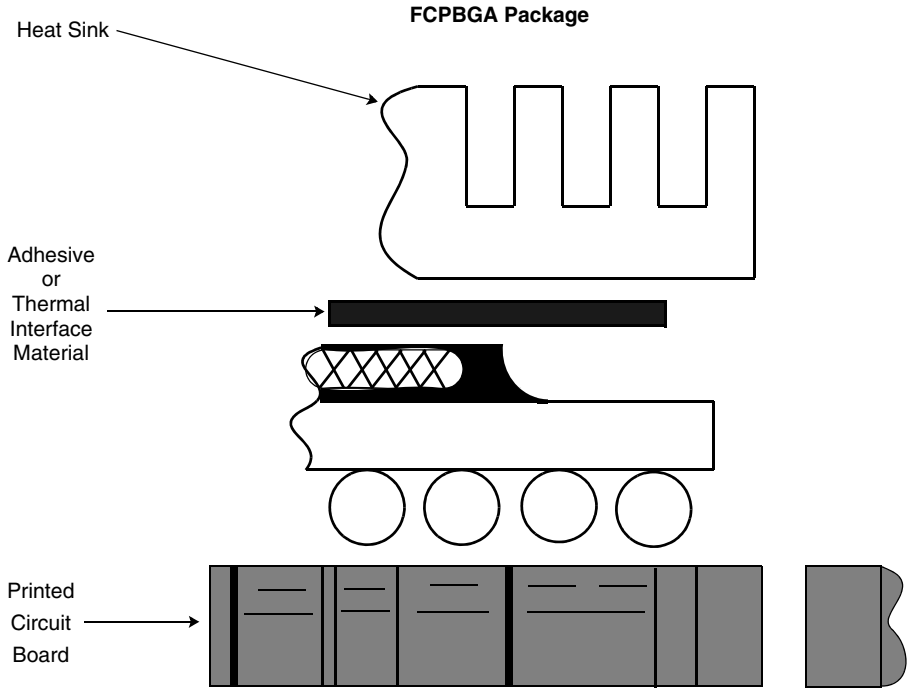
Figure 5-6. IBM RISCWatch JTAG to HRESET, TRST, and SRESET Signal Connector



5.8 Thermal Management Information

This section provides thermal management information for the FCPBGA package for air cooled applications. Proper thermal control design is primarily dependent upon the system-level design; that is, the heat sink, air flow, and the thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, mounting clip, or a screw assembly.

Figure 5-7. Package Exploded Cross-Sectional



The board designer can choose between several types of heat sinks to place on the 750CL. There are many commercially-available heat sinks that are appropriate for the 750CL provided by the vendors listed in *Table 5-5, 750CL Heat-Sink Vendors,* on page 57.

Table 5-5. 750CL Heat-Sink Vendors

Company Names and Addresses for Heat-Sink Vendors
Cool Polymers (formerly Chip Coolers, Inc.) 333 Strawberry Field Rd. Warwick, RI 02886 (888) 811-3787 http://coolpolymers.com
International Electronic Research Corporation (IERC) 413 North Moss Street Burbank, CA 91502 (818) 842-7277 http://www.ctscorp.com
Aavid Thermalloy 80 Commercial Street Concord, NH 03301 (603) 224-9888 http://www.aavid.com http://www.aavidthermalloy.com
Wakefield Thermal Solutions Inc. 33 Bridge Street Pellham, NH 03076 (603) 635-2800 http://www.wakefield.com

5.8.1 Minimum Heat Sink Requirements

The worst-case power dissipation (P_D) for the 750CL is shown in *Table 3-5, Power Consumption,* on page 24. A conservative thermal management design will provide sufficient cooling to maintain the junction temperature (T_J) of the 750CL below 105°C at maximum P_D and worst-case ambient temperature and airflow conditions.

Many factors affect the 750CL power dissipation, including V_{DD}, T_J, core frequency, process factors, and the code that is running on the processor. In general, P_D increases with increases in T_J, V_{DD}, core frequency, process variables, and the number of instructions executed per second.

For various reasons, a designer may determine that the power dissipation of the 750CL in their application will be less than the maximum value shown in this datasheet. Assuming a lower P_D will result in a thermal management system with less cooling capacity than would be required for the maximum P_D shown in the datasheet. In this case, the designer may decide to determine the actual maximum 750CL P_D in the particular application. Contact your IBM PowerPC field applications engineer for more information.

However, regardless of methodology, IBM only supports system designs that successfully maintain the maximum junction temperature within the datasheet limits. IBM also supports designs that rely on the maximum P_D values given in this datasheet and supply a cooling solution sufficient to dissipate that amount of power while keeping the maximum junction temperature below the maximum T_J.

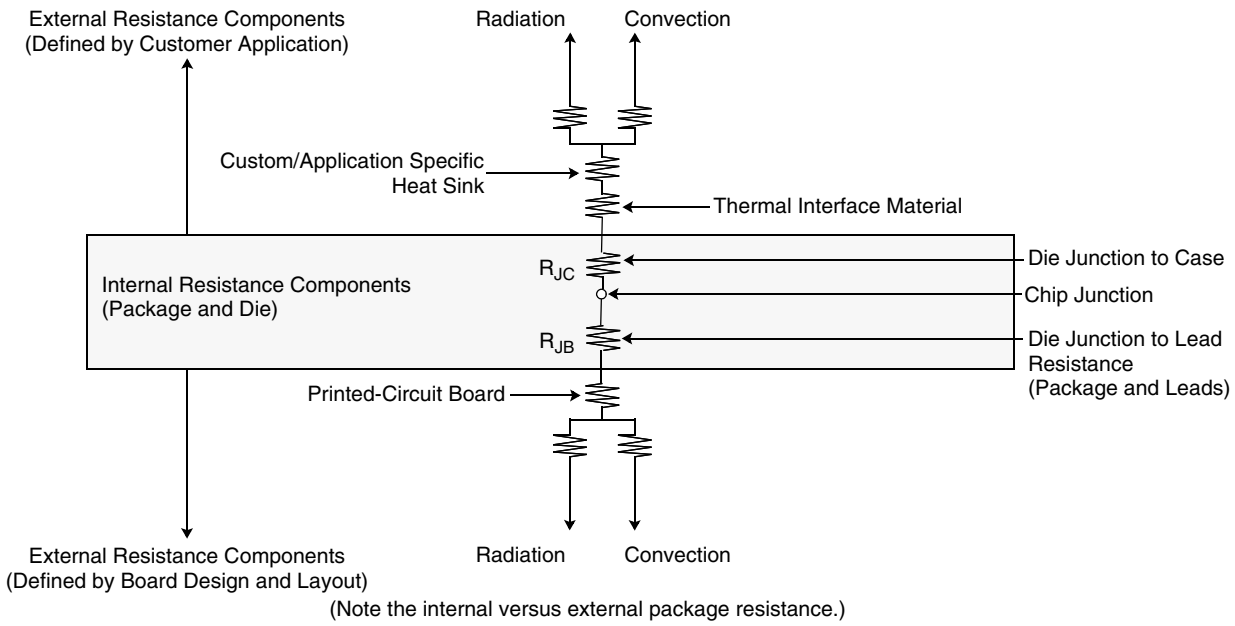
5.8.2 Internal Package Conduction Resistance

For the exposed-die packaging technology shown in *Table 3-3, Package Thermal Characteristics,* on page 22, the thermal paths illustrated in *Figure 5-8* are as follows:

- Die junction-to-case thermal resistance (primary thermal path), defined as the thermal resistance from the die junctions to the top surface of the package.
- Die junction-to-lead thermal resistance (not normally a significant thermal path), defined as the thermal resistance from the die junctions to the circuit board interface.
- Die junction-to-ambient thermal resistance (largely dependent on customer-supplied heat sink), defined as the sum total of all the thermally conductive components that comprise the end user's application. Ambient is further defined as the air temperature in the immediate vicinity of the thermally conductive components, including the contributions of surrounding heat sources.

Figure 5-8 is a thermal model, in schematic form, of the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 5-8. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



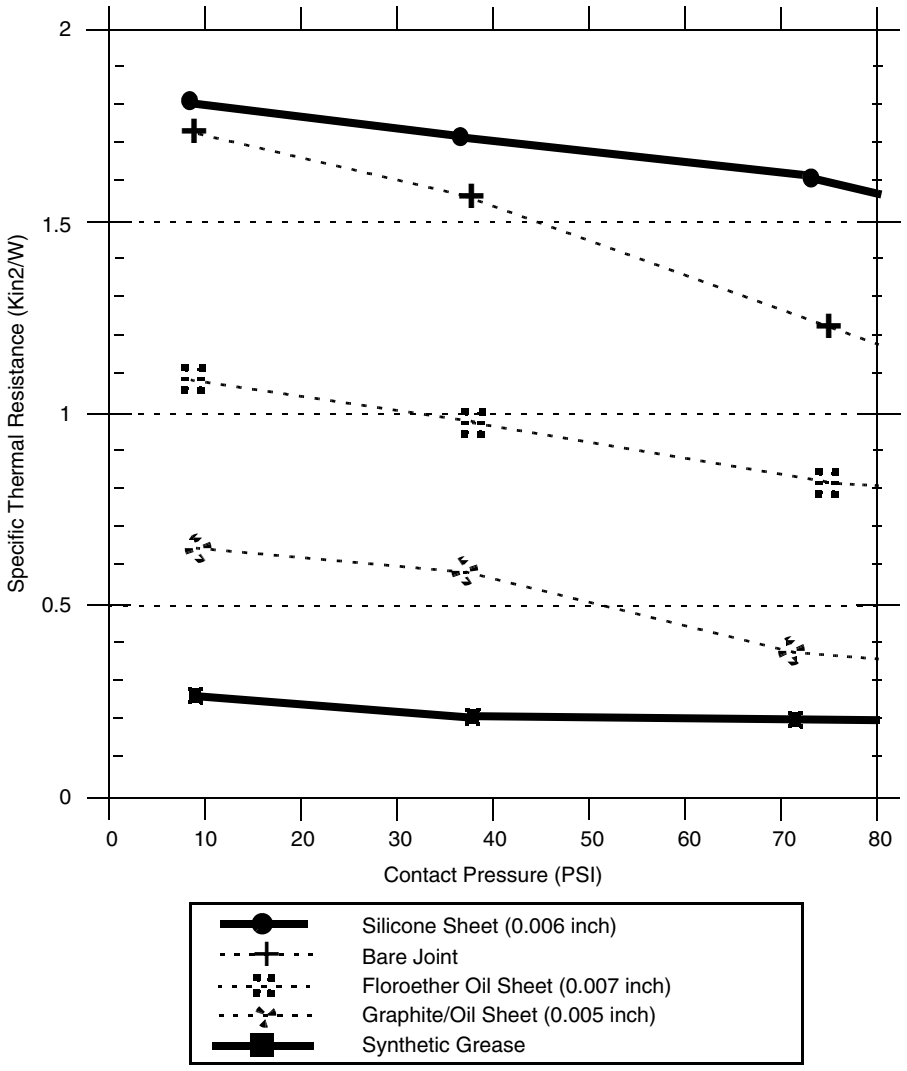
Heat generated in the chip is conducted through the silicon, then through the package to the top of the package, then through the heatsink attach material (or thermal interface material), and finally into the heat sink and the ambient air. Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat-sink conduction/convective thermal resistances are the dominant terms.

5.8.3 Adhesives and Thermal Interface Materials

A thermal interface material is required at the package die-surface-to-heat-sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by a mechanical means (not adhesive), *Figure 5-9* on page 60 shows an example of the thermal performance of three thin-sheet thermal-interface materials (silicon, graphite/oil, floroether oil), a bare joint, and a joint with synthetic grease, as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of synthetic grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the synthetic grease joint. Customers are advised to investigate alternative thermal interface materials to ensure the most reliable, efficient, and cost-effective thermal design.

An example of heat-sink attachment to the package by mechanical means is illustrated in *Figure 5-7, Package Exploded Cross-Sectional,* on page 56. In this case, the synthetic grease offers the best thermal performance considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors: thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so forth.

Figure 5-9. Thermal Performance of Select Thermal Interface Material



The board designer can choose between several types of thermal interfaces. Heat-sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the vendors shown in *Table 5-6*.

Table 5-6. 750CL Thermal Interface and Adhesive Materials Vendors

Company Names and Addresses for Thermal Interfaces and Adhesive Materials Vendors
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 0997 Midland, MI 48686-0997 (989) 496-4000 http://www.dowcorning.com/content/etronics
Chomerics, Inc. 77 Dragon Court Woburn, MA 01888-4850 (781) 935-4850 http://www.chomerics.com
Laird Technologies (formerly Thermagon, Inc.) 4707 Detroit Avenue Cleveland, OH 44102-2216 (888) 246-9050 http://www.lairdtech.com
Loctite Corporation 1001 Trout Brook Crossing Rocky Hill, CT 06067 (860) 571-5100 / (800) 562-8483 http://www.loctite.com
AI Technology 70 Washington Road Princeton, NJ 08550-1097 (609) 799-9388 http://www.aitechnology.com

Section 5.9 provides a heat-sink selection example using one of the commercially available heat sinks.

5.9 Heat-Sink Selection Example

In most cases, the thermal path through the package balls is not significant, and is not included in the heat sink calculations. Considering only the thermal path through the heat sink, the thermal equation is

$$T_J = Ta + Pd \times (\theta jc + \theta cs + \theta sa)$$

where:

T_J is the junction temperature.
Ta is the ambient temperature (that is, the temperature of the air at the heatsink).
Pd is the maximum power dissipated by the 750CL.
θjc is the thermal resistance from the junction to the case (the top surface of the package).
θcs is the thermal resistance from the case to the heatsink.
θsa is the thermal resistance from the heatsink to ambient.

In this example, let:

T_J = 105°C maximum
Ta = 50°C at heatsink = 35°C air inlet temperature plus 15°C internal temperature rise
Pd = 6 W maximum at 105°C
θjc = 2°C/W
θcs = 0.5°C/W
θsa = unknown

So

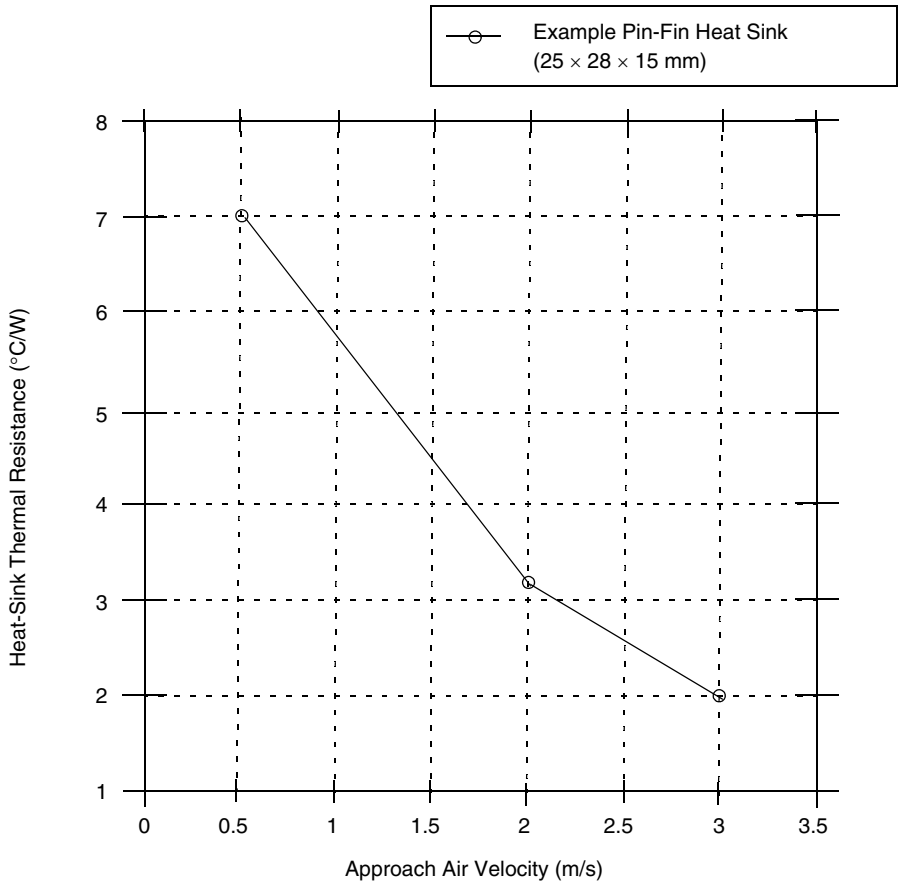
105°C = 50°C + 6 W(2 + 0.5 + x°C/W)

Thus

θsa ≤ 6.67°C/W

Airflow at the heatsink is a minimum of 1 m/s. Considering the heatsink of *Figure 5-10*, thermal resistance at 1 m/s airflow is less than 5.8°C/W, which satisfies the requirement with a reasonable engineering margin.

Figure 5-10. Example of a Pin-Fin Heat-Sink-to-Ambient Thermal Resistance versus Airflow Velocity



5.10 Operational and Design Considerations

5.10.1 Level Protection

A level protection feature is included in the 750CL. This feature prevents ambiguous floating reference voltages by pulling the respective signal line to the last valid or nearest valid state.

For example, if the input/output voltage level is closer to OV_{DD}, the circuit pulls the I/O level to OV_{DD}. If the I/O level is closer to GND, the I/O level is pulled low. This self-latching circuitry keeps the floating inputs defined and avoids meta-stability. In *Table 5-4, Input/Output Usage,* on page 51, these signals are defined as "keeper" in the "Level Protect" column. The keeper circuits are not intended to hold a net at a particular logic level, or to strongly hold a net at the current logic level. Strong noise can cause the net to switch.

The level protect circuitry provides no additional leakage current to the signal I/O; however, some amount of current must be applied to the keeper node to overcome the level protection latch. Any pullup or pulldown resistors should be 1k Ω or less to overcome the keeper current.

This feature allows the system designer to limit the number of resistors in the design and optimize placement and reduce costs.

Note: Having a keeper on the associated signal I/O does not replace a pullup or pulldown resistor that is needed by a separate device located on the 60x bus. The designer must supply any termination requirements for these separate devices, as defined in their specifications.

5.10.2 Configuring the Processor During Reset

Operating modes of the processor such as the data bus width, DRTRY mode, and so forth are selected when the processor exits reset mode (that is, when HRESET is deasserted). Specifically, selected pins are sampled when HRESET transitions to the de-asserted state and the sampled value determines the operating mode. The mode select pins and their descriptions follow.

Table 5-7. Summary of Mode Select

Mode	750CL
32-bit mode	Sample TLBISYNC to select High = 64-bit mode Low = 32-bit mode
Data retry mode	Selects DRTRY mode. Sample DRTRY to select. 0 at HRESET transition No DRTRY mode 1 at HRESET transition DRTRY mode DRTRY must be de-asserted once the processor is configured for no-drtry mode. This can be accomplished by driving DRTRY with a copy of HRESET.
Standard/extended precharge mode	QACK in a logical high state at the transition of HRESET from asserted to negated enables standard precharge mode, the recommended default. See *Section 5.10.3.1* for details.
I/O bus voltage (OV_{DD})	Continuously ground L2_TSTCLK to select 1.8 V bus operation. Continuously connect L2_TSTCLK to OV_{DD} to select 1.15 V bus mode.
PLL divider mode	PLL divider mode is selected by sensing the data bus write-only (DBWO) pin at the transition of HRESET from low to high. For normal operation, DBWO must be held low ('0') at the HRESET transition whenever noninteger processor-to-bus frequency ratios are selected (that is, 2.5, 3.5, 4.5, 5.5, 6.5, 7.5, 8.5, and 9.5). DBWO can be held either low or high (= OV_{DD}) for integer ratios.

5.10.3 64-Bit or 32-Bit Data Bus Mode

The 750CL typically operates in 64-bit data bus mode. Mode setting is determined by the state of the mode signal, TLBISYNC, at the transition of HRESET from its active to inactive state (low to high). If TLBISYNC is *high* when HRESET transitions from active to inactive, 64-bit mode is selected. If TLBISYNC is *low* when HRESET transitions from active to inactive, 32-bit mode is selected.

5.10.3.1 Precharge Duration Selection and Application

An extended precharge feature is available for the signals $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, and $\overline{\text{ARTRY}}$ in situations where the loading and net topology of these signals requires a longer precharge duration for the signals to attain a valid level.

The bus signals, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, and $\overline{\text{ARTRY}}$ require a precharge to the inactive state (bus high) before going to tristate. The precharge duration in standard precharge mode is approximately one half cycle, and should be used for systems with point-to-point topologies. Extended precharge mode increases the precharge duration to one cycle. This increase may be required for bus speeds approaching 200 MHz when bus loading is high.

$\overline{\text{QACK}}$ in a logical high state at the transition of $\overline{\text{HRESET}}$ from asserted to negated enables standard precharge mode in the 750CL. QACK in a logical low state at the transition of HRESET from asserted to negated enables extended precharge mode in the 750CL.

5.11 JTAG Test Access Port (TAP) Operation

750CL supports the IEEE 1149.1 standard, *IEEE Standard Test Access Port and Boundary-Scan Architecture*. The standard defines a 5-pin interface that is used to perform functions such as continuity testing between components on boards and system debug. Data is serially shifted into the processor through the TDI pin and shifted out of the processor through the TDO pin. The scan operations can be divided into two categories: instruction scan and data scan operations. The operations or modes are selected using the TMS pin. Finally, all scanning and mode selection is performed synchronously with respect to the clock pin, TCK.

This section details the IEEE 1149.1 operations supported by the 750CL processor and recommendations for system design to support system debug using the TAP interface. For additional details, see the IEEE 1149.1 document.

5.11.1 Interface Pins

Table 5-8 provides a brief description of the five dedicated pins of the test access port (TAP). These pins do not have an associated boundary scan cell.

Table 5-8. TAP Pins

Pin	Input/Output	Weak Pullup	Mandatory TAP Pin	Function
TDI	Input	Yes	Yes	Serial Scan input pin
TDO	Output	No	Yes	Serial Scan output pin
TMS	Input	Yes	Yes	TAP controller mode pin
TCK	Input	No	Yes	Scan clock
$\overline{\text{TRST}}$	Input	Yes	No	TAP controller reset

TRST is an optional pin, but it is required for 750CL to reset the TAP controller on a power-on reset (POR). The 1149.1 standard requires a weak pullup only on the TRST pin, but in the 750CL, weak pullups are provided to most TAP input pins such that the 750CL will function normally with the TAP pins unconnected. However, it is recommended to tie the TDI and TMS input pins high and TRST low when they are not in use for greater system reliability.

5.11.2 Supported IEEE 1149 JTAG Instructions and Data Registers

5.11.2.1 Instructions

750CL supports the three required JTAG instructions; Bypass, Sample/Preload, and Extest plus the optional HIGHZ and CLAMP JTAG instructions. The 8-bit hexadecimal encoding for these instructions is shown in *Table 5-9*. Hexadecimal encodings not included in the table are reserved for other functions.

JTAG instructions are scanned serially (least significant bit first) into an 8-bit TAP controller instruction register through the TDI pin. Consult the IEEE 1149.1 standard for details regarding loading the JTAG instructions using the TAP.

Table 5-9. Instruction Encodings

Instruction	Encoding	Description
EXTEST	x‘00’	JTAG extest instruction
SMPL_PLD	x‘C0’	JTAG sample/preload instruction
HIGHZ	x‘F0’	JTAG HIGHZ instruction
CLAMP	x‘F1’	JTAG CLAMP instruction
BYPASS	x‘FF’	JTAG bypass instruction

The instruction register output is forced to the Bypass instruction (all ones) if the TAP controller is in the Test_Logic_Reset state or if TRST is active**.**

5.11.2.2 Data Registers

750CL supports the Bypass and Boundary Scan data registers. When selected with the corresponding JTAG instruction (as shown in *Table 5-10*), the register is inserted between the TDI and TDO TAP pins and can be scanned when the TAP controlled is in “Shift-DR” state to control or observe 750CL input and output states. Consult the IEEE 1149.1 specification for details on manipulation of the data registers. An industry-standard boundary scan design language (BSDL) file is available for 750CL with specific information on the boundary scan latch size and organization. This document can be used to create card-level connectivity tests between components.

Table 5-10. JTAG Instructions

Data Register	Instruction	TAP State	Scan Clock	Data Register Length
Bypass register	Bypass	Shift-DR	TCK	1
Boundary scan register	Sample/preload or extest	Shift-DR	TCK	169

Bypass Register

The Bypass register is required by the IEEE 1149.1 standard. This is a single bit register that is used to bypass the 750CL This feature allows a shorter system data scan string when scanning an entire system board in which the 750CL boundary scan string is a part of a larger system data scan string.

Boundary Scan Register

The Boundary Scan register allows system board trace tests and access to the pins where physical access is difficult. Basically, a latch is placed on inputs to capture data, and a latch is placed on outputs to force data. Additional latches may be needed to configure bidirectional pins as either inputs or outputs and also to enable or disable tri-state outputs. All these latches, or boundary scan cells, are serially connected to comprise the boundary scan register.

Not all pins of the 750CL have an associated boundary scan cell. The five TAP pins and the dedicated test pins do not have a boundary scan cell.

An industry-standard BSDL file is available for the 750CL with specific information on the boundary scan register size and individual cell placement and function. This document can then be used to create card-level connectivity tests between components.

5.11.3 Recommendations to Support System Debug

The TAP interface also allows functions such as observation and control of 750CL general-purpose registers, cache contents, 60x bus cycles, and so forth, using the IBM RISCWatch debug tool. To simplify system debug, the following system design recommendations are offered to allow use of RISCWatch and other diagnostic tools.

$\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{TRST}}$ are signals used for RISCWatch to enable proper operation of the tool. Logical AND gates should be placed between these signals and the IBM PowerPC 750CL RISC microprocessor. See *Table 5-4, Input/Output Usage,* on page 51 and *Figure 5-6, IBM RISCWatch JTAG to HRESET, TRST, and SRESET Signal Connector,* on page 55 for more information.

5.11.3.1 Processor Debug System Enablement when Implementing Precharge Selection

System designers who want to use a processor debug system attached to the 750CL IEEE 1149.1 test access port (TAP) interface (such as the IBM RISCWatch debug system) should provide a method to assert QACK after the transition of HRESET. Debug systems use a “soft stop” feature to stop the processor, allow processor internal states to be read, and then a restart of the processor. A soft stop requires the system to be in a quiescent state before the processor can be queried for internal state values. This is accomplished by the assertion of a quiescent request (that is, QREQ is asserted) and subsequent acknowledgment (that is, QACK is asserted). Systems that do not use the doze, nap, and sleep power management features, and do not require the extended pre-charge feature, can drive the QACK pin with an inverted version of HRESET.

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Revision Log

Revision Date	Contents of Modification
October 16, 2009	Version 2.6 • Added information about the Application Conditions field (See *Section 1.3, Part Number Information,* on page 12).
December 2, 2008	Version 2.5 • Changed part designator A0 recommended V_{DD} range to 1.24 V (see *Section 1.3, Part Number Information,* on page 12). • Added nominal V_{DD} column (see *Section 1.3, Part Number Information,* on page 12). • Added information about reliability grade (see *Section 1.3, Part Number Information,* on page 12). • Added a note about V_{DD} values (see *Section 1.3, Part Number Information,* on page 12). • Added *Section 1.4, Reliability Information,* on page 12. • Added *Section 1.4.1, Package Reliability,* on page 13. • Added text about voltage sense pins (see *Section 3, Electrical and Thermal Characteristics,* on page 21). • Added a note about V_{DD} values (see *Table 3-1, Absolute Maximum Ratings,* on page 21). • Added power consumption information for IBMPPC750CLE73xx, IBMPPC750CLE80xx, IBMPPC750CLE90xx, and IBMPPC750CLEA0xx (see *Table 3-5, Power Consumption,* on page 24). • Added a note about V_{DD} values (see *Table 3-5, Power Consumption,* on page 24). • Removed notes about typical power and power dissipation (see *Table 3-5, Power Consumption,* on page 24). • Changed SYSCLK slew rate, single-ended values (see *Table 3-6, Clock AC Timing Specifications,* on page 25). • Added *Section 3.5.2, Following HRESET Deassertion,* on page 30.
May 29, 2007	Version 2.4 • Changed the reliability grade (see *Section 1.3, Part Number Information,* on page 12). • Changed the power consumption values for the 1000 MHz part (see *Table 3-5, Power Consumption,* on page 24).
March 5, 2007	Version 2.3 • Updated the list of PowerPC 750CL features (see *Section 1.1* on page 9). • Changed the Processor Version Register number (see *Table 1-1* on page 11). • Changed the part number information (see *Section 1.3* on page 12). • Updated the PowerPC 750CL Microprocessor Block Diagram (see *Table 2-1* on page 19). • Changed the description of the core power supply (see *Table 2-2* on page 20). • Added a note about ESD ratings (see *Table 3-1* on page 21). • Updated the recommended operating conditions (see *Table 3-2* on page 22). • Updated the DC electrical specifications (see *Table 3-4* on page 23). • Updated the power consumption table (see *Table 3-5* on page 24). • Updated the clock AC timing specifications (see *Table 3-6* on page 25). • Changed some values for AC timing reference levels (see *Table 3-7* on page 27). • Updated the 60x Bus Output AC Timing Specifications (see *Table 3-8* on page 31). • Updated the JTAG AC Timing Specifications (see *Table 3-9* on page 34). • Corrected the number of balls in the 750CL package (see *Section 4* on page 37). • Corrected a footnote (see *Table 4-1* on page 41). • Removed two footnotes (see *Table 5-1* on page 44). • Changed the description of the DBWO signal (see *Table 5-4* on page 51). • Corrected the list of 750CL heat-sink vendors (see *Table 5-5* on page 57). • Corrected the list of 750CL thermal interface and adhesive materials vendors (see *Table 5-6* on page 61). • Updated the Summary of Mode Select table (see *Table 5-7* on page 63).

Revision Date	Contents of Modification
October 5, 2006	Version 2.2—Preliminary updated version of the datasheet
September 30, 2006	Version 2.1—Preliminary updated version of the datasheet
August 20, 2006	Version 2.0—Preliminary version of the datasheet