TOSHIBA BiCD Integrated Circuit   Silicon Monolithic

TB62269FTAG

PWM method CLK-IN bipolar stepping motor driver

The TB62269FTAG is a PWM chopper type clock-in controlled motor driver for two-phase bipolar stepping motor.
Fabricated with the BiCD process, the TB62269FTAG is rated at 40 V/1.8 A .
The internal voltage regulator allows control of the motor with a single
VM power supply.

Features

- Bipolar stepping motor driver
- PWM controlled constant-current drive
- Clock input control
- Allows full, half, quarter ,1/8,1/16, and 1/32 step resolutions
- Low on-resistance of output stage by using BiCD process
- High Voltage and large current (For specification, please refer to absolute maximum ratings and operation ranges.)
- Thermal shutdown (TSD), over-current shutdown (ISD), and power-on reset (POR)
- Built-in regulator allows the TB62269FTAG to operate with only VM power supply.
- Able to customize chopping frequency by external resistance and capacitor.
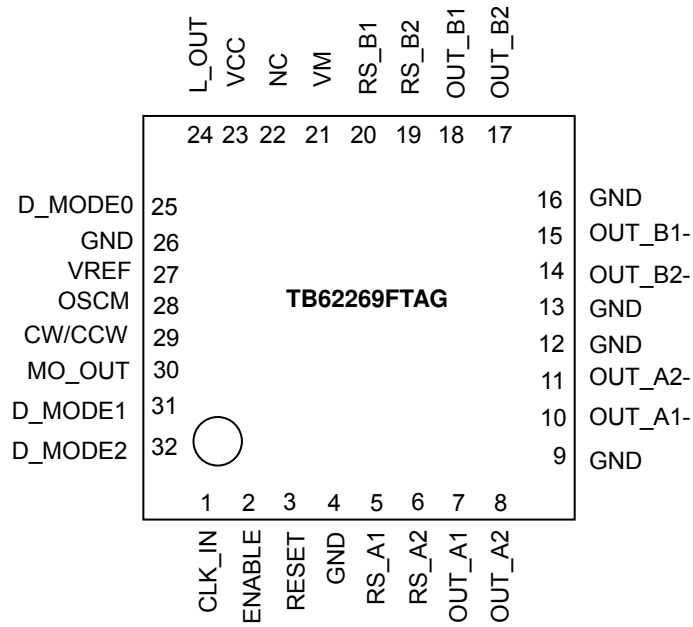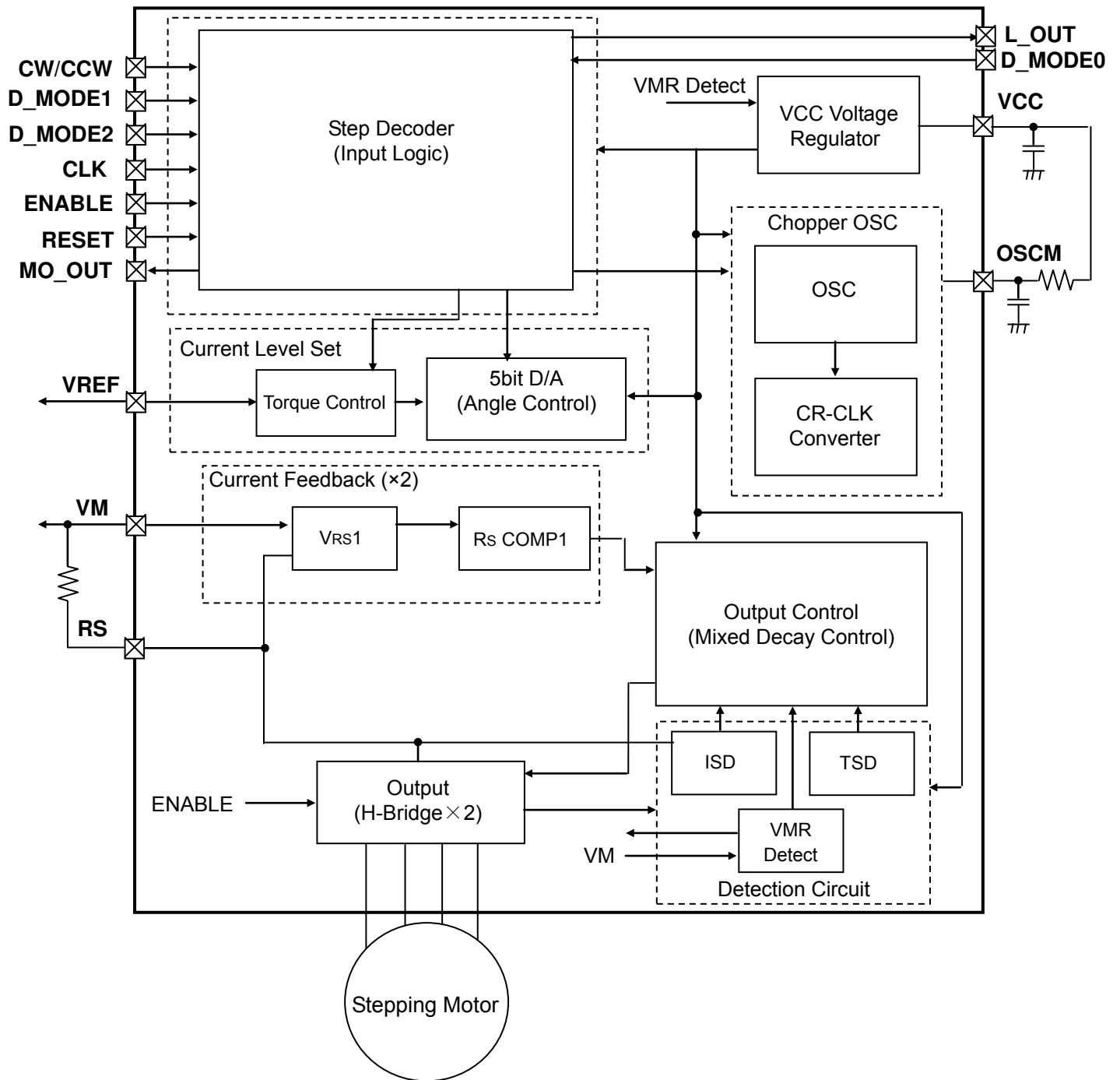- Packages: P-VQFN32-0505-0.50-004

P-VQFN32-0505-0.50-004
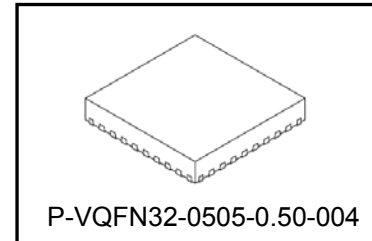
Weight: 0.11g (Typ.)

Note: Please be careful about thermal conditions during use.

1. Pin assignment

(Top View)

Pin	Name
24	L_OUT
23	VCC
22	NC
21	VM
20	RS_B1
19	RS_B2
18	OUT_B1
17	OUT_B2

TB62269FTAG

Pin	Name
25	D_MODE0
26	GND
27	VREF
28	OSCM
29	CW/CCW
30	MO_OUT
31	D_MODE1
32	D_MODE2

Pin	Name
16	GND
15	OUT_B1-
14	OUT_B2-
13	GND
12	GND
11	OUT_A2-
10	OUT_A1-
9	GND

Pin	Name
1	CLK_IN
2	ENABLE
3	RESET
4	GND
5	RS_A1
6	RS_A2
7	OUT_A1
8	OUT_A2

2. Block Diagram

Functional blocks, circuit, and constants etc. in the block diagram may be omitted or simplified for explanatory purposes.

Note: For GND wiring, we recommend that a heat sink should be grounded at all points, and the board should be grounded at only one GND pin for single point ground.
Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the TB62269FTAG may be permanently damaged.
Also, the utmost care should be taken for pattern designing and implementation of the TB62269FTAG since it has power supply pins (VM, RS, OUT, and GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the TB62269FTAG may be destroyed.
The logic input pins must also be wired correctly. Otherwise, the TB62269FTAG may be damaged owing to a current running through the IC that is larger than the specified current.

3. Pin Function
TB62269FTAG (QFN32)

Function explanation of terminal number 1 to 32

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	CLK_IN	An electrical angle leads on the rising edge of the clock input. A motor rotation count depends on the input frequency.	17	OUT_B2	B-channel output+
2	ENABLE	A, B-channel output enable (5V) OFF switching pin (GND)	18	OUT_B1	
3	RESET	Electric angle reset	19	RS_B2	A sensing resistance connection pin for a current value setting of B-channel output
4	GND	Logic ground	20	RS_B1	
5	RS_A1	A sensing resistance connection pin for a current value setting of A-channel output	21	VM	Monitoring pin of motor power supply
6	RS_A2		22	NC	No-connect
7	OUT_A1	A-channel output+	23	VCC	Monitoring pin for internal generation 5V bias
8	OUT_A2		24	L_OUT	Error detect signal output pin
9	GND	Power GND of A-channel	25	D_MODE0	Step resolution mode control 0
10	OUT_A1-	A-channel output-	26	GND	Logic ground
11	OUT_A2-		27	VREF	Bias pin for tuning the current level
12	GND	Power GND of A-channel	28	OSCM	Oscillator pin for PWM chopper
13	GND	Power GND of A-channel	29	CW/CCW	Motor rotation: forward/reverse
14	OUT_B2-	B-channel output-	30	MO_OUT	Electric angle monitor pin
15	OUT_B1-		31	D_MODE1	Step resolution mode control pin 1
16	GND	Power GND of B-channel	32	D_MODE2	Step resolution mode control pin 2

● Please use the pin of NC with Open.
● Please connect the pins with the same names, at the nearest point of the device.

4. Input equivalent circuit

TB62269FTAG
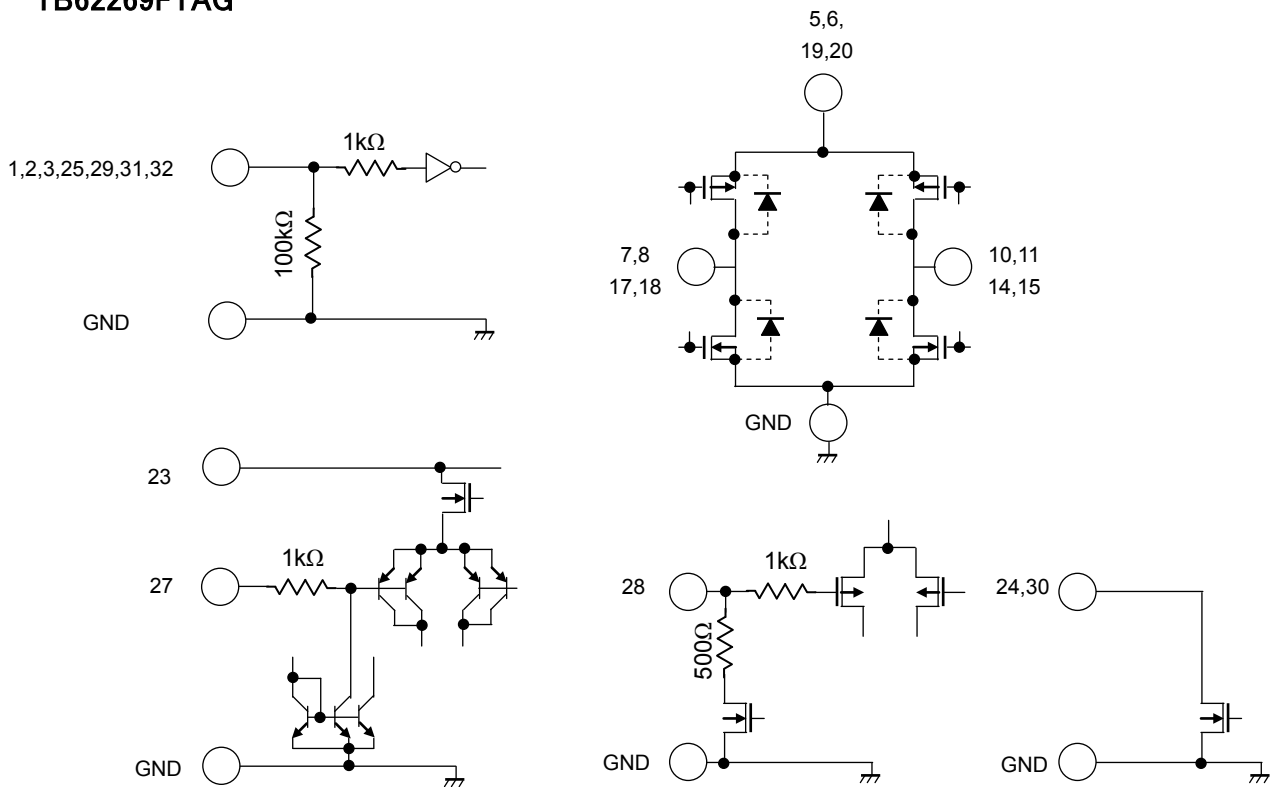
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin No	Pin name
1	CLK_IN
2	ENABLE
3	RESET
5,6	RS_A
7,8	OUT_A
10,11	OUT_A−
14,15	OUT_B−
17,18	OUT_B
19,20	RS_B
21	VM
23	VCC
24	L_OUT
25	D_MODE0
27	VREF
28	OSCM
29	CW/CCW
30	MO_OUT
31	D_MODE1
32	D_MODE2

5. CLK Function

The electrical angle leads one by one in the manner of the clocks. The clock signal is reflected to the electrical angle on the rising edge.

CLK Input	Function
Rise	The electrical angle leads one by one on the rising edge.
Fall	- (Remains at the same position.)

6. ENABLE Function

The ENABLE pin controls whether the current is allowed to flow through a given phase for a stepper motor drive. This pin selects whether the motor is stopped in OFF mode (high impedance state: Z) or activated. The pin must be fixed to Low at power-on or power-down.

ENABLE Input	Function
H	Output transistors are enabled (normal operation).
L	Output transistors are disabled (high impedance state: Z).

7. CW/CCW Function

The CW/CCW pin switches rotation direction of stepper motors.

CW/CCW Input	Function	OUT (+)	OUT (-)
H	Clock-wise	H	L
L	Counter clock-wise	L	H

8. Step resolution Mode Select Function

D_MODE0	D_MODE1	D_MODE2	Function
L	L	L	STANDBY MODE (OSCM stop, output transistors are disabled, full step mode, torque 100%)
L	L	H	Full step
L	H	L	Half step(a)
L	H	H	Quarter step
H	L	L	Half step(b)
H	L	H	1/8 step
H	H	L	1/16 step
H	H	H	1/32 step

It is recommended that D_MODE0, D_MODE1 and D_MODE2 are changed after setting RESET to Low in the state of an initial state (MO_OUT = Low).

9. RESET Function

| RESET Input	Function
L	Normal operation mode
H	The electrical angle is reset.

Phase currents when RESET is applied are as follows:
In this case, the terminal MO_OUT becomes Low.

Step resolution mode	A-channel current	B-channel current	Electric Angle
Full step	100%	100%	45°
Half step	100%	100%	45°
Quarter step	71%	71%	45°
1/8 step	71%	71%	45°
1/16 step	71%	71%	45°
1/32 step	71%	71%	45°

10. Output function of reset signal

When IC is stopped by applying Thermal shutdown(TSD) or Over-current shutdown(ISD), Low is output.
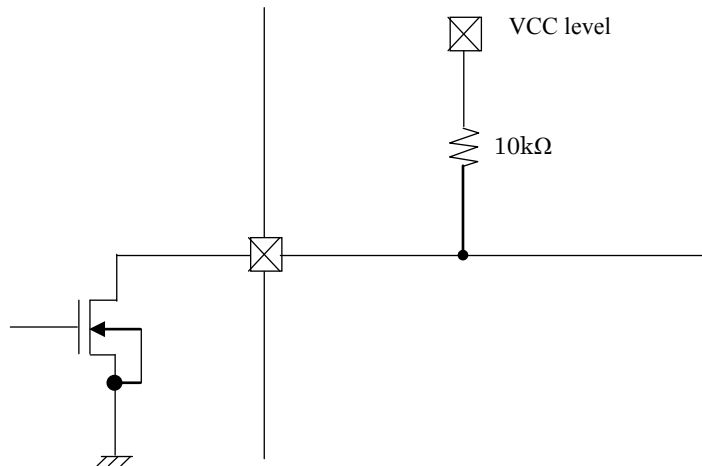
It is an open-drain output. When the output pin is pulled up with a resistor to power supply, Low is output (internal ON) at the time of Reset. Then High (internal Hi-Z) is output in normal operation (no-Reset).
Pull-up to VCC pin.

11. Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Motor power supply	V_M	40	V	
Motor output voltage	V_{OUT}	40	V	
Motor output current	I_{OUT}	1.8	A/phase	Note 1
Logic power supply	V_{CC}	6.0	V	When externally applied.
Digital input voltage	V_{IN}	6.0	V	
MO,L_OUT output voltage	V_{MO} ,V_{L_OUT}	6.0	V	
MO,L_OUT Inflow current	I_{MO} ,I_{L_OUT}	30.0	mA	
Power dissipation	P_D	1.3	W	Note 2
Operating temperature	T_{opr}	-20 to 85	°C	
Storage temperature	T_{str}	-55 to 150	°C	
Junction temperature	$T_{j(Max)}$	150	°C	

Note 1: As a guide, the maximum output current should be kept below 1.4A per phase. The maximum output current may be further limited in view of thermal considerations, depending on ambient temperature and board conditions.

Note 2: Stand-alone (Ta =25°C)
When Ta exceeds 25°C, it is necessary to do the derating with 10.4mW/°C.

Ta: Ambient temperature

Topr: Ambient temperature while the TB62269FTAG is active

Tj: Junction temperature while the TB62269FTAG is active. The maximum junction temperature is limited by the thermal shutdown (TSD) circuitry. It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, Tj (MAX), will not exceed 120°C.

Caution: Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The TB62269FTAG does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.

All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

12. Operation Ranges (Ta=0 to 85°C)

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Sensing resistance connection pin voltage	V_{RS}	0.0	±1.0	±1.5	V	VM terminal standard,(Note 2)
Motor power supply	V_M	10.0	24.0	38.0	V	
Motor output current	I_{OUT}	-	1.4	1.8	A	1 phase, (Note 1)
Logic input voltage	$V_{IN(H)}$	2.0	-	5.5	V	H-level of the logic
	$V_{IN(L)}$	-0.4	-	1.0	V	L-level of the logic
MO output pin voltage	V_{MO}, V_{L_OUT}	-	3.3	5.5	V	The voltage of pull-up direction
Clock input frequency	f_{CLK}	-	-	100	kHz	
Chopper frequency	f_{chop}	40	100	150	kHz	
V_{ref} reference voltage	V_{ref}	GND	-	3.6	V	

Note 1: Maximum current for actual usage may be limited by the operating circumstances such as operating conditions (step resolution mode, operating time, and so on), ambient temperature, and heat conditions (board condition and so on).

Note 2: Maximum voltage of V_{RS} must not be exceeded the absolute maximum rating.

13. Electrical Characteristics

13-1. Electrical Characteristics 1 (Ta = 25°C, VM = 24V, unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Logic input voltage		VIH	Logic input pins	2.0	-	5.0	V
		VIL		GND	-	0.8	
Input hysteresis voltage		$V_{IN(HYS)}$	Logic input pins (Note)	100	200	300	mV
Digital input current	High	$I_{IN(H)}$	V_{IN} = 5 V at the digital input pins under test	35	50	75	µA
	Low	$I_{IN(L)}$	V_{IN} = 0 V at the digital input pins under test	-	-	1.0	µA
MO output voltage	High	$V_{OH(MO)}$	I_{OH} = -24 mA when the output is High	2.4	-	-	V
	Low	$V_{OL(MO)}$	I_{OL} = 24 mA when the output is Low	-	-	0.5	V
Supply current		I_{M1}	Outputs open, In STANDBY mode	-	2.5	3.0	mA
		I_{M2}	Outputs open, ENABLE = Low	-	4.0	5.5	mA
		I_{M3}	Outputs open (full step)	-	5	7	mA
Output leakage current	High-side	I_{OH}	V_{RS} = V_M = 40 V, V_{OUT} = 0 V	-	-	1	µA
	Low-side	I_{OL}	V_{RS} = V_M = V_{OUT} = 40 V	1	-	-	µA
Output current difference between channels		ΔI_{OUT1}	Output current difference between channels	-5	0	5	%
Output current difference relative to the predetermined value		ΔI_{OUT2}	I_{OUT} = 1.0A	-5	0	5	%
R_S pin current		I_{RS}	V_{RS} = V_M = 24V, DMODE_0,1,2 = L ENABLE = L	0	-	27.0	µA
Drain-source ON-resistance of the output transistors (upper and lower sum)		$R_{ON(D-S)}$	I_{OUT} =1.0A, Tj = 25°C	-	0.8	1.2	Ω

Note: $V_{IN (L to H)}$ is defined as the V_{IN} voltage that causes the outputs (OUT_A1, OUT_A2, OUT_B1, and OUT_B2 pin) to change when a pin under test is gradually raised from 0 V. $V_{IN (H to L)}$ is defined as the V_{IN} voltage that causes the outputs (OUT_A1, OUT_A2, OUT_B1, and OUT_B2 pin) to change when the pin is then gradually lowered.
The difference between $V_{IN (L to H)}$ and $V_{IN (H to L)}$ is defined as the input hysteresis.

13-2. Electrical Characteristics 2 (Ta = 25°C, VM = 24V, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
V_{ref} input current	I_{ref}	V_{ref} = 3.0 V	-	0	1.0	µA
V_{ref} decay rate	V_{ref} (GAIN)	V_{ref} = 2.0 V	1/4.8	1/5.0	1/5.2	-
TSD threshold (Note 1))	T_jTSD		140	150	170	°C
VM recovery voltage	V_{MR}		7.0	8.0	9.0	V
Overcurrent trip threshold(Note 2)	ISD		2.0	3.0	4.0	A
Power-supply voltage for internal circuit operation	V_{CC}	I_{CC}=5.0mA	4.75	5.0	5.25	V

Note 1: Thermal shutdown (TSD) circuitry

When the junction temperature of the device reaches the threshold, the TSD circuitry is tripped, causing the internal reset circuitry to turn off the output transistors. The TSD circuitry is tripped at a temperature between 140°C (min) and 170°C (max). Once tripped, the TSD circuitry keeps the output transistors off until the TSD circuitry is released. The TSD status is released once the TB62269FTAG is rebooted or all the D_MODE pins (DMODE_1,2) are switched to Low (set to STANDBY mode). The TSD circuitry does not necessarily guarantee the complete safety of the device; therefore do not use the TSD circuitry actively.

Note 2: Overcurrent shutdown (ISD) circuitry

When the output current reaches the threshold, the ISD circuitry is tripped, causing the internal reset circuitry to turn off the output transistors. To prevent the ISD circuitry from being tripped owing to switching noise, it has a masking time of four CR oscillator cycles. Once tripped, it takes a maximum of four cycles to exit ISD mode and resume normal operation. The ISD circuitry remains active until all the D_MODE(D_MODE1,2) pins are switched to Low or the TB62269FTAG is rebooted. The TB62269FTAG remains in STANDBY mode while in ISD mode.

Note 3: When the power supply voltage (Vcc) for operating internal circuit is divided by the external resistor and used as Vref input voltage, the accuracy of the output current setting value becomes ±8% together with the Vcc output voltage accuracy and the Vref decay ratio accuracy.

Note 4: Even when the logic input signal is input under the condition that the VM voltage is not supplied, the electromotive force and the leakage current by the signal input are not generated. However, before VM is rebooted, logic input signal should be controlled not to let the motor operating by rebooting VM.

Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current is fed back to the power supply owing to the effect of the motor back-EMF.

If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the TB62269FTAG or other components will be damaged or fail owing to the motor back-EMF.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short circuit; they do not necessarily guarantee complete IC safety.

If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged owing to an output short circuit.

The ISD circuit is only intended to provide temporary protection against an output short circuit. If such a condition persists for a long time, the device may be damaged owing to overstress. Overcurrent conditions must be removed immediately by external hardware.

IC Mounting

Do not insert devices in the wrong orientation or incorrectly. Otherwise, it may cause device breakdown, damage and/or deterioration.

13-3. AC Electrical Characteristics (Ta = 25°C, VM = 24V, 6.8 mH/5.7Ω)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Logic input frequency		fLogic	OSC=1600 kHz	1.0	-	150	kHz
Width of minimum clock pulse	High	$T_{CLK(H)}$	-	300	-	-	ns
	Low	$T_{CLK(L)}$	-	250	-	-	
Output transistor Switching characteristic		tr	-	0.15	0.20	0.25	μs
		tf	-	0.12	0.15	0.18	
		tpLH(CLK)	CLK Signal to OUT	-	1.0	-	
		tpHL(CLK)	CLK Signal to OUT	-	1.5	-	
Blanking time for current spike prevention		tBLANK	Iout = 1.0A	450	700	950	ns
OSC_M oscillation frequency		fosc	C_{osc} = 270 pF, R_{osc} = 3.6 kΩ	1200	1600	2000	kHz
Chopper frequency range		fchop(Typ.)	Output operation (Iout = 1.0A)	40	100	150	kHz
Chopper setting frequency		fchop	Output operation (Iout = 1.0A) OSC = For 1600kHz	-	100	-	kHz
ISD masking time		tISD(Mask)	After ISD threshold is exceeded owing to an output short circuit to power or ground	-	4	-	CR-CLK
ISD on-time		tISD		-	-	8	

Timing Charts of Output Transistors Switching

Timing charts may be simplified for explanatory purposes.
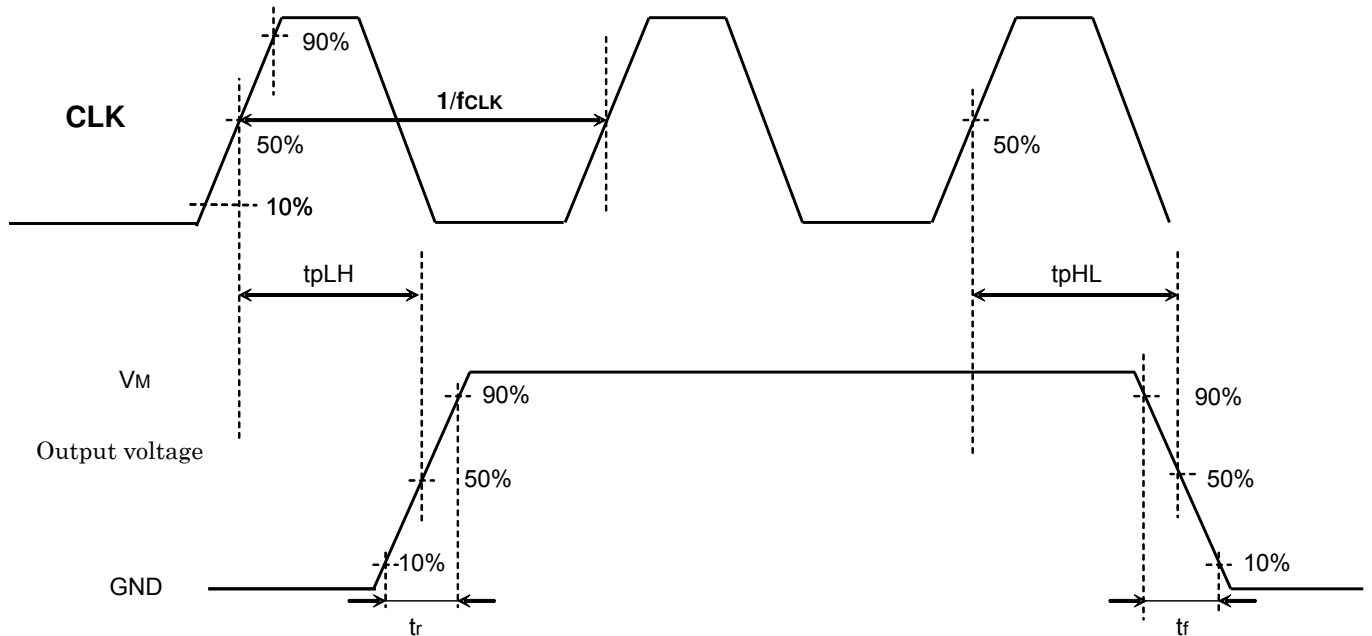
Figure 1 Timing Charts of Output Transistors Switching

14. Mixed Decay Mode /Detecting zero point

CR pin
Internal CLK
waveform

f_{chop}

DECAY MODE 1

37.5%
MIXED
DECAY
MODE

NF

Setting current

MDT

RNF

CHARGE MODE → NF: Reach setting current → SLOW MODE → MIXED DECAY TIMMING → FAST MODE → Monitoring current → (In case setting current > Outputting current) CHARGE MODE

Charge   **Slow**   **Fast**
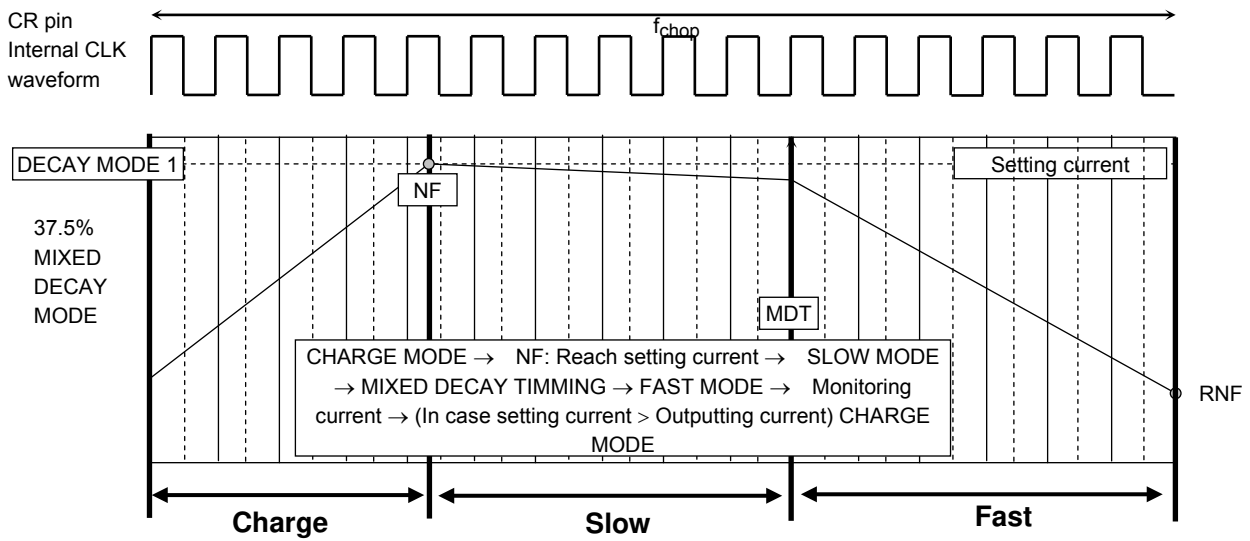
The NF point shows that the output current reaches the setting current value. The Charge time shows the difference value according to the characteristic(such as inductance or resistance) of step resolutions.

Charge   Slow   Fast

Note

Iout=0

Hi-Z
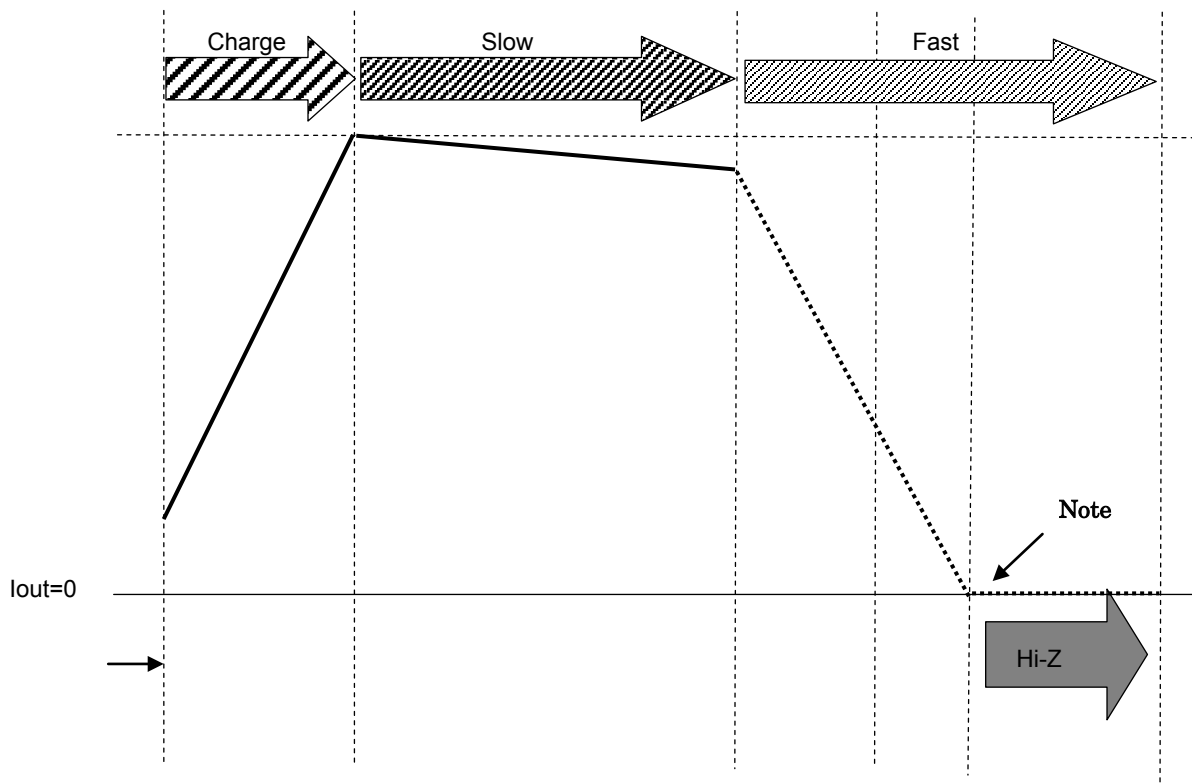
Note: When Iout reaches the 0A level, the output transistor will turn to "Hi-Z" status.

15. Output Transistor Operating Modes

Charge Mode
A current flows into the motor coil.

Slow Mode
A current circulates around the motor coil and this device.

Fast Mode
The energy of the motor coil is fed back to the power
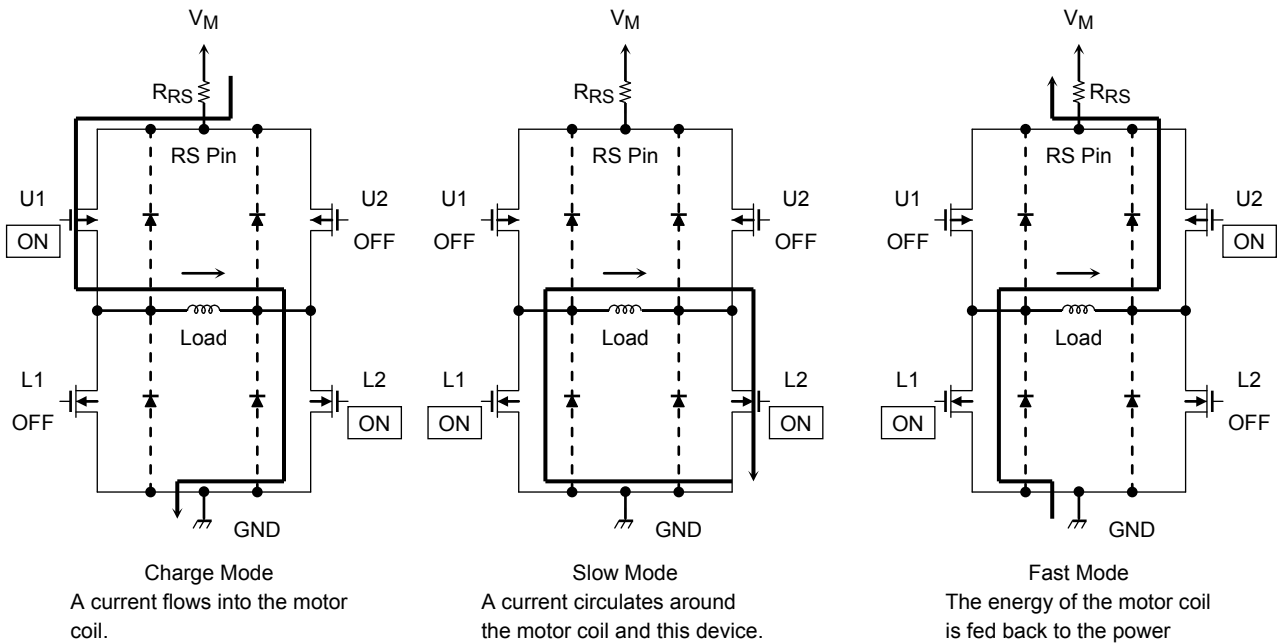
16. Output Transistor Operating Functions

CLK	U1	U2	L1	L2
Charge mode	ON	OFF	OFF	ON
Slow mode	OFF	OFF	ON	ON
Fast mode	OFF	ON	ON	OFF

Note: This table shows an example of when the current flows as indicated by the arrows in the figures shown above. If the current flows in the opposite direction, refer to the following table.

CLK	U1	U2	L1	L2
Charge mode	OFF	ON	ON	OFF
Slow mode	OFF	OFF	ON	ON
Fast mode	ON	OFF	OFF	ON

The TB62269FTAG switches among Charge, Slow-Decay and Fast-Decay modes automatically for constant-current control.

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

17. Calculation of the Setting Output Current

For PWM constant-current control, the TB62269FTAG uses a clock generated by the CR oscillator. The peak output current can be set via the current-sensing resistor (RS) and the reference voltage (V_{ref}), as follows:

$$Iout(Max) = Vref(gain) \times \frac{Vref(V)}{R_{RS}(\Omega)}$$

Vref(gain): Vref decay ratio is 1 / 5.0 (typ.).

Ex.): In case of 100% setting,

When Vref = 3.0 V, Torque = 100%, and RS = 0.51Ω,

constant current output of the motor (peak current) is calculated as follows;

I_{out} = 3.0V / 5.0 / 0.51Ω= 1.18 A.

18. Calculation of the OSCM oscillation frequency (chopper reference frequency)

OSCM oscillation frequency (fOSCM) and chopper frequency (fchop) are computable in the following expressions.

fOSCM=1/[0.56x{Cx(R1+500)}]......C, R1: External constant for OSCM (C=270pF, R1=3.6kΩ)

fchop = fOSCM / 16

Because the loss of the gate in IC rises, generation of heat grows though wavy reproducibility goes up because the pulsating flow of the current decreases when the chopper frequency is raised.

There is a possibility of the current pulsating flow increasing though a decrease in generation of heat can be expected by lowering the chopper frequency.
The thing set within the range of the frequency from 50 to about 100 kHz based on the frequency generally of about 70 kHz is recommended.

19. IC Power Consumption

The power consumed by the TB62269FTAG is approximately the sum of the following; 19-1 Power consumption of output transistors, and 19-2 Power consumption of logic block and IM domain.

19-1. Power consumption of output transistors using the R_{on} (upper + lower) value of 1.0Ω

The power of the output transistors is consumed by upper and lower H-bridge.

The power consumed by each H-bridge is given by:

$$P \text{ (out)} = \text{Iout (A)} \times \text{VDS (V)} = \text{Iout (A)}^2 \times \text{Ron (Ω)} \quad\text{...(1)}$$

In full step mode (in which two phases have a phase difference of 90°), the average power consumption in the output transistors is calculated as follows:

Ron = 1.0Ω, Iout (peak: Max) = 1.0 A, VM = 24 V
$$P \text{ (out)} = 2 \text{ (Tr)} \times 1.0 \text{ (A)}^2 \times 1.0 \text{(Ω)} \quad\text{...(2)}$$
$$= 2.0 \text{ (W)}$$

19-2. Power consumption of logic block and IM domain

The power consumption of logic block and the IM domain is calculated separately for normal operation and standby modes.

I (IM3) = 5 mA (typ.)   : Normal operation mode/1axis
I (IM2) = 3.5 mA (typ.)   : STANDBY mode

The output domain is connected to VM (24V). It consists of the digital logic connected to VM (24 V) and the network affected by the switching of the output transistors.

The total power consumed by IM can be estimated as:

$$P \text{ (IM)} = 24 \text{ (V)} \times 0.005 \text{ (A)} \quad\text{..(3)}$$
$$= 0.12 \text{ (W)}$$

19-3. Power consumption

Hence, the total power consumption of the TB62269FTAG is:

P = P (out) + P (IM) = 2.12 (W)

The STANDBY mode power consumption per axis is given by:

P (STANDBY mode) = 24 (V) × 0.0035 (A) = 0.084 (W)

Board design should be fully verified, taking thermal dissipation into consideration.

20. Step Resolution Drive

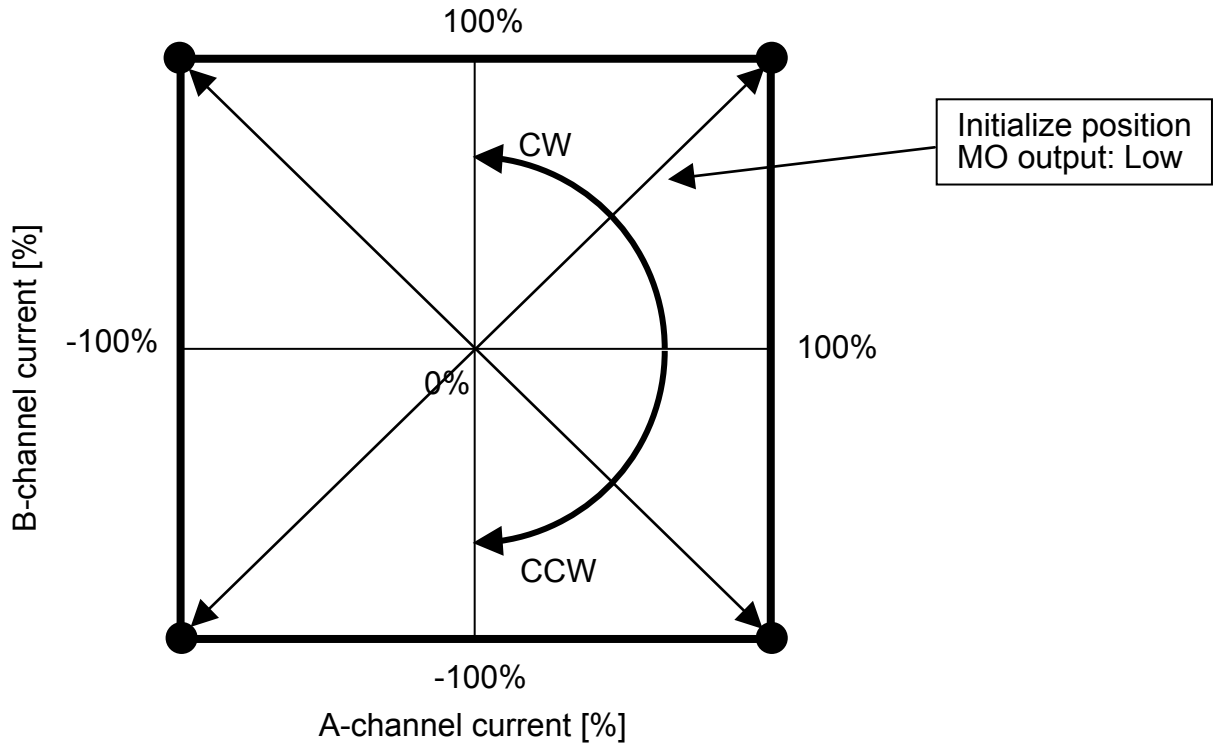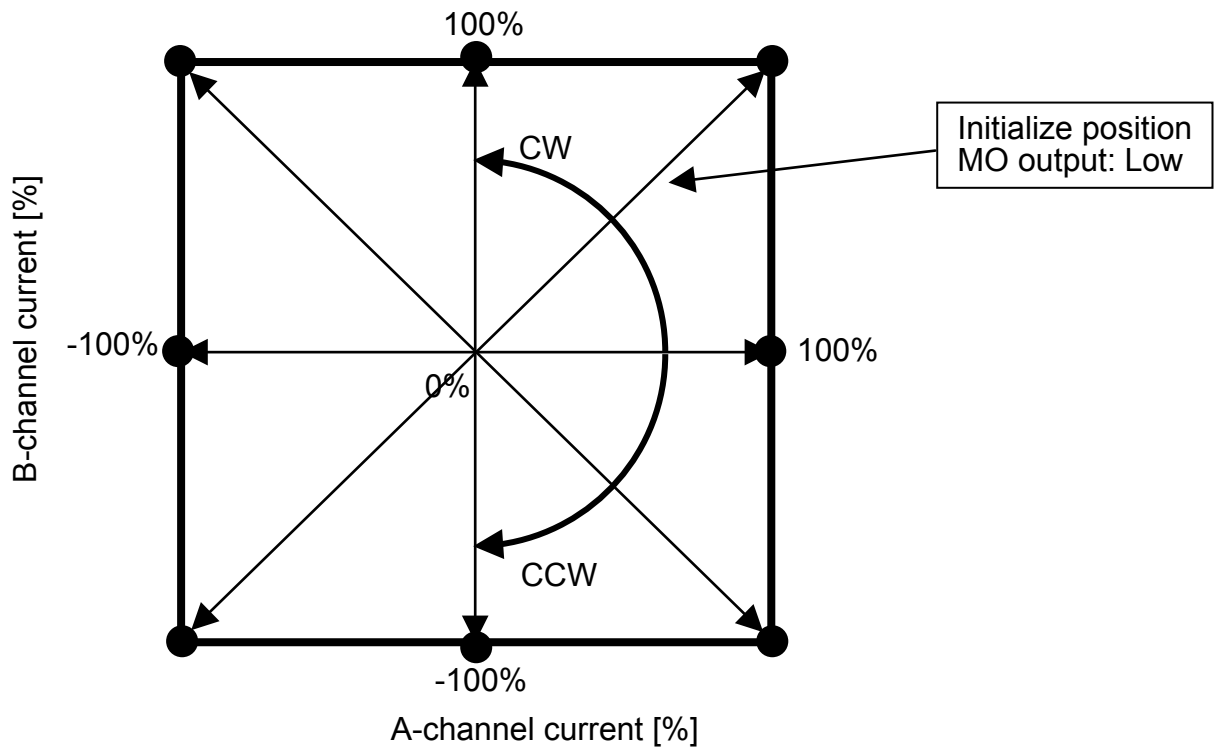|		
Clock Input		
Full step resolution	A ch	
	B ch	
	MO output	
Half step resolution	A ch	
	B ch	
	MO output	
Quarter step resolution	A ch	
	B ch	
	MO output	
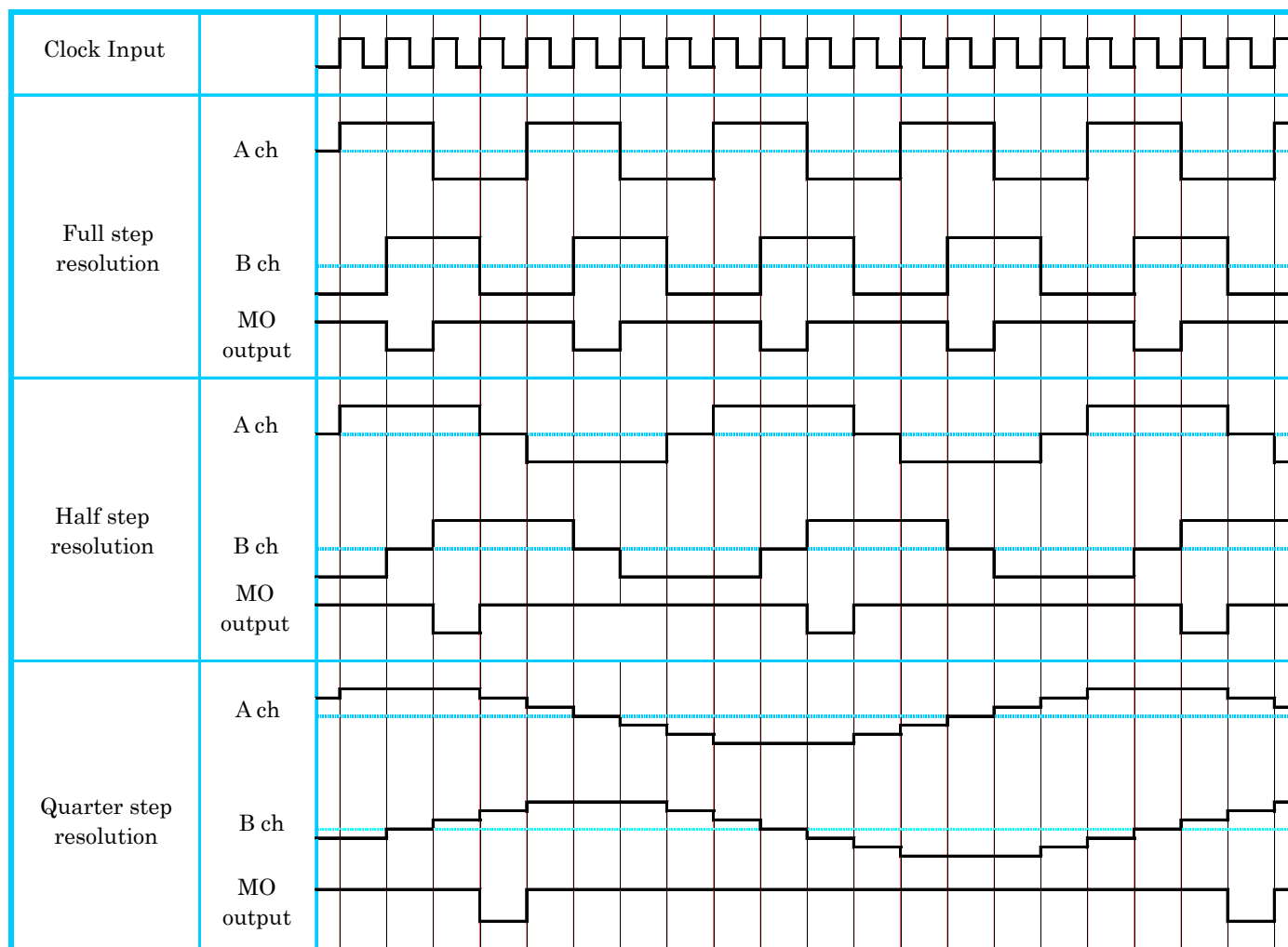
MO output is the waveform in the state of pull-up.

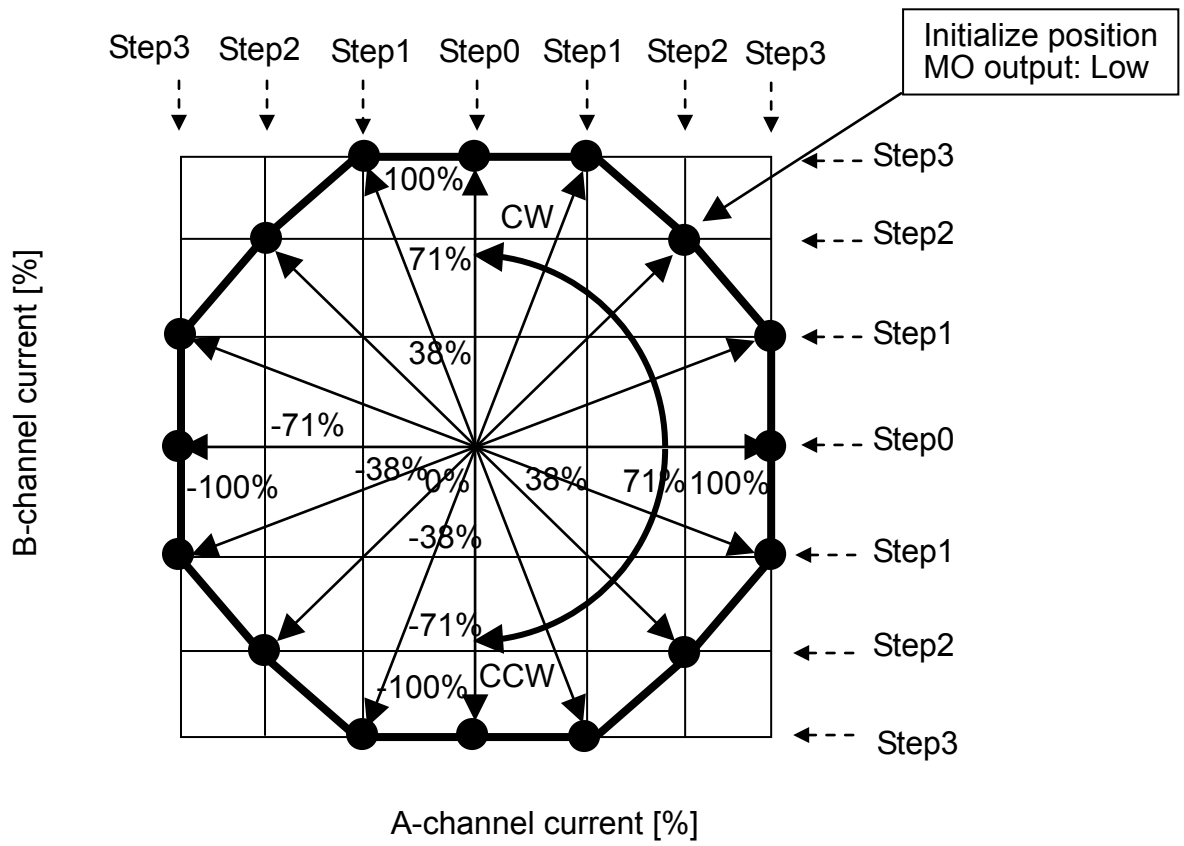## 21. Electrical Angle of Step Resolution Mode and Initialize Position
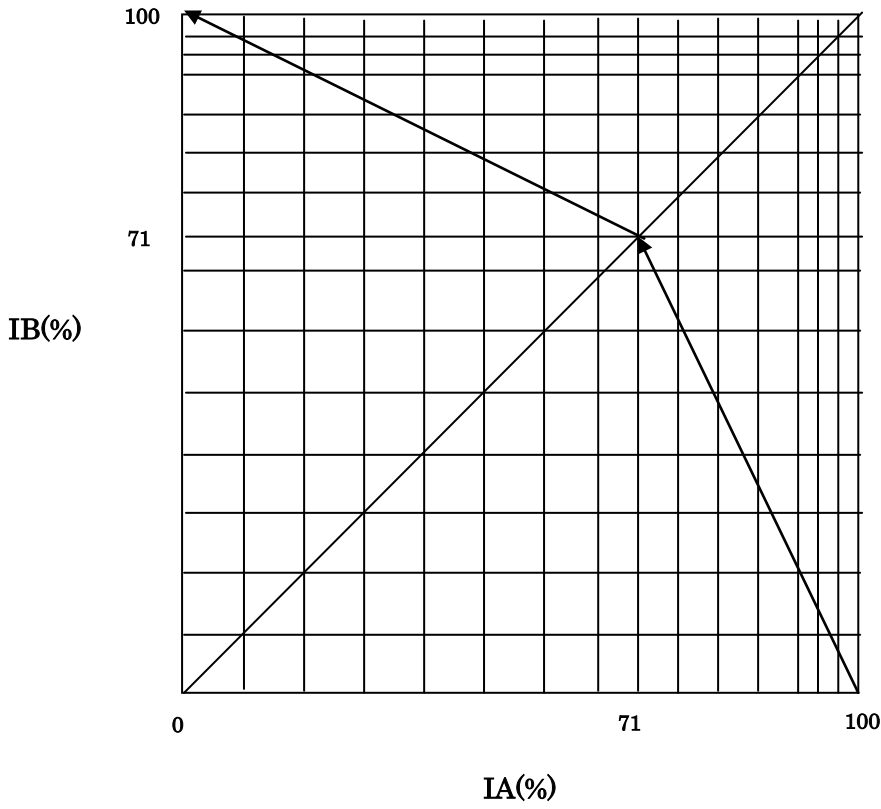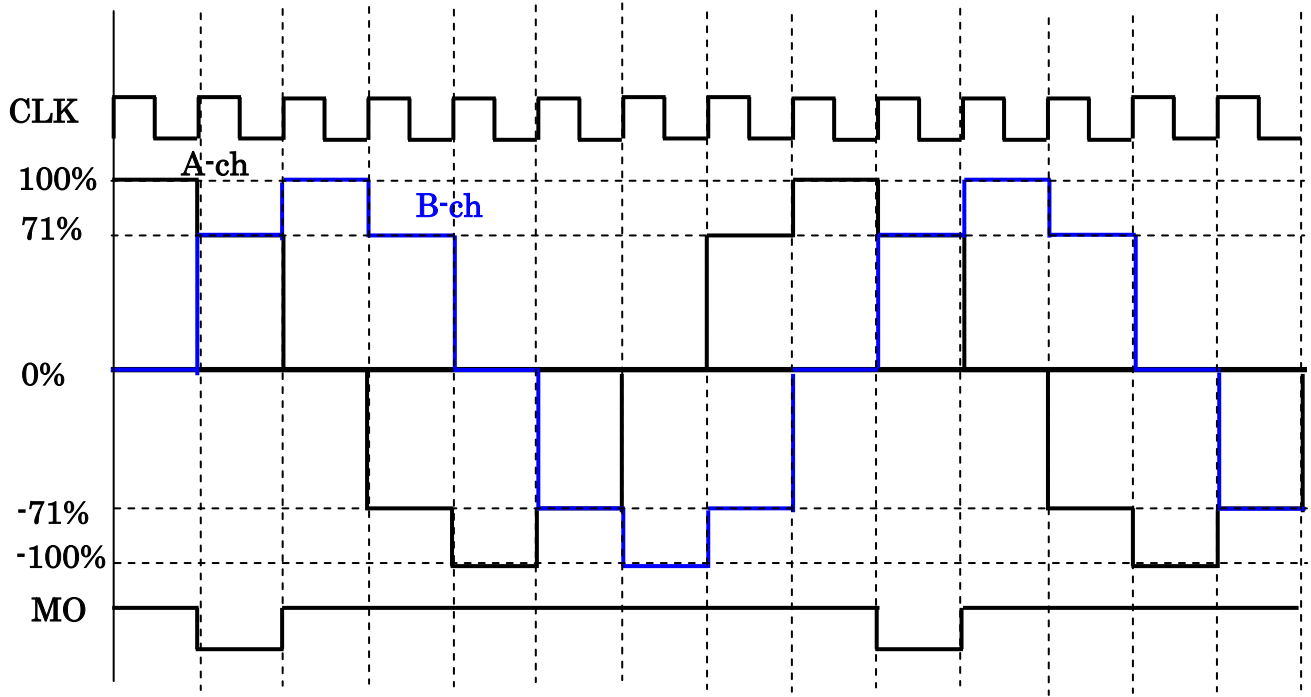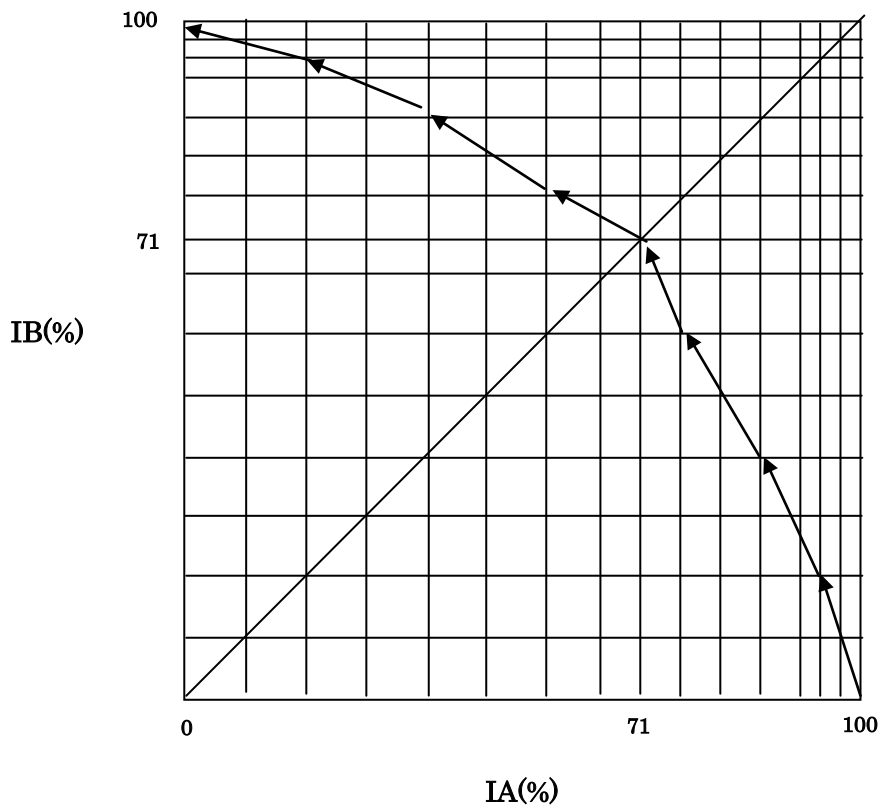
● **Full step resolution mode**

● **Half step resolution mode**

● **Quarter Step resolution mode**

A-channel current [%]

Half Step resolution (b)

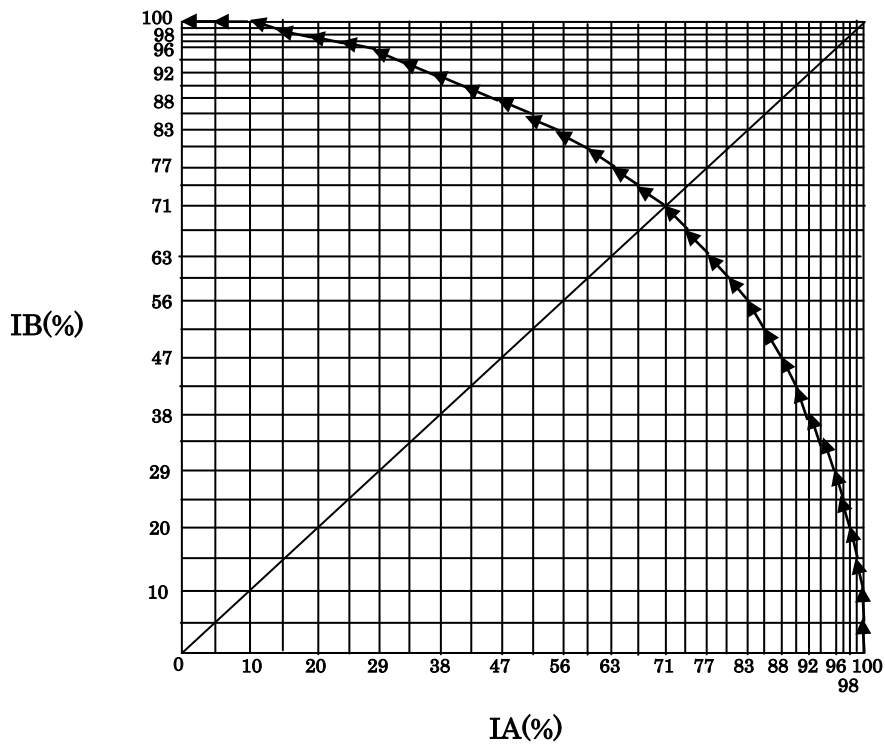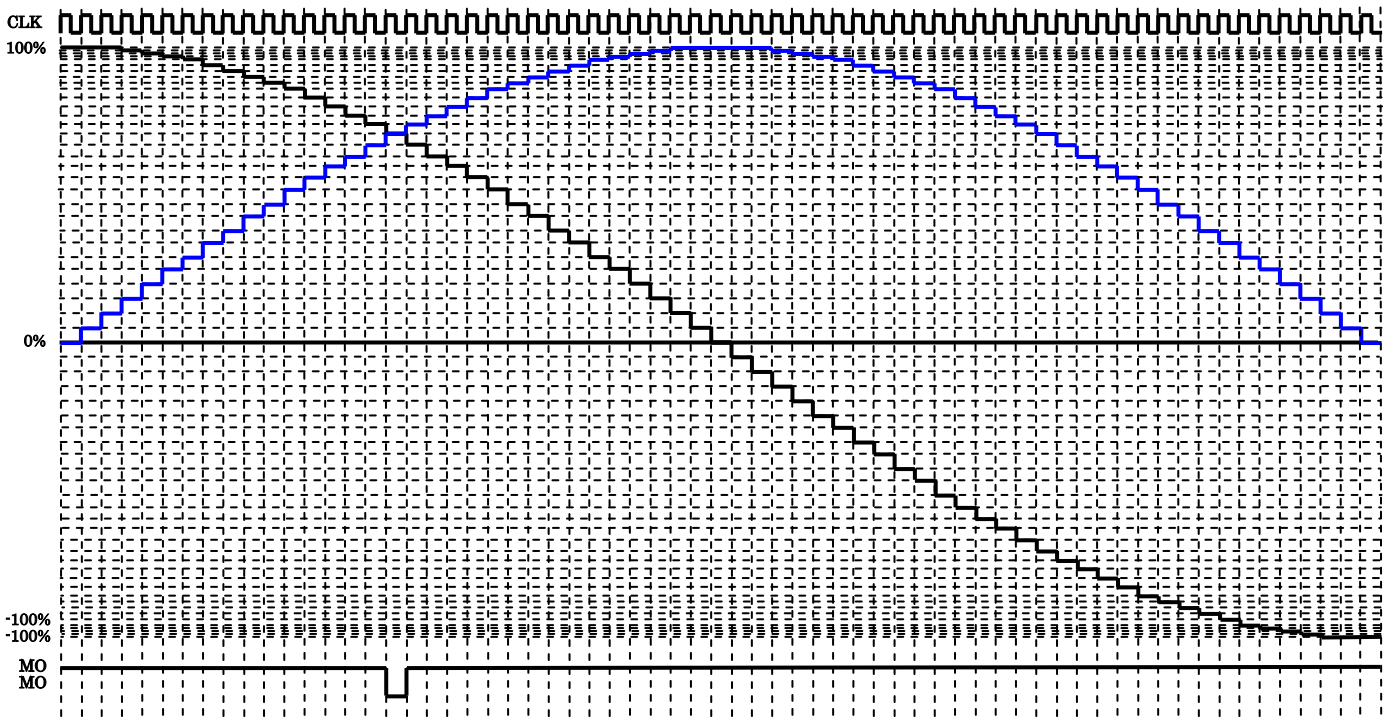**1/8 Step resolution**
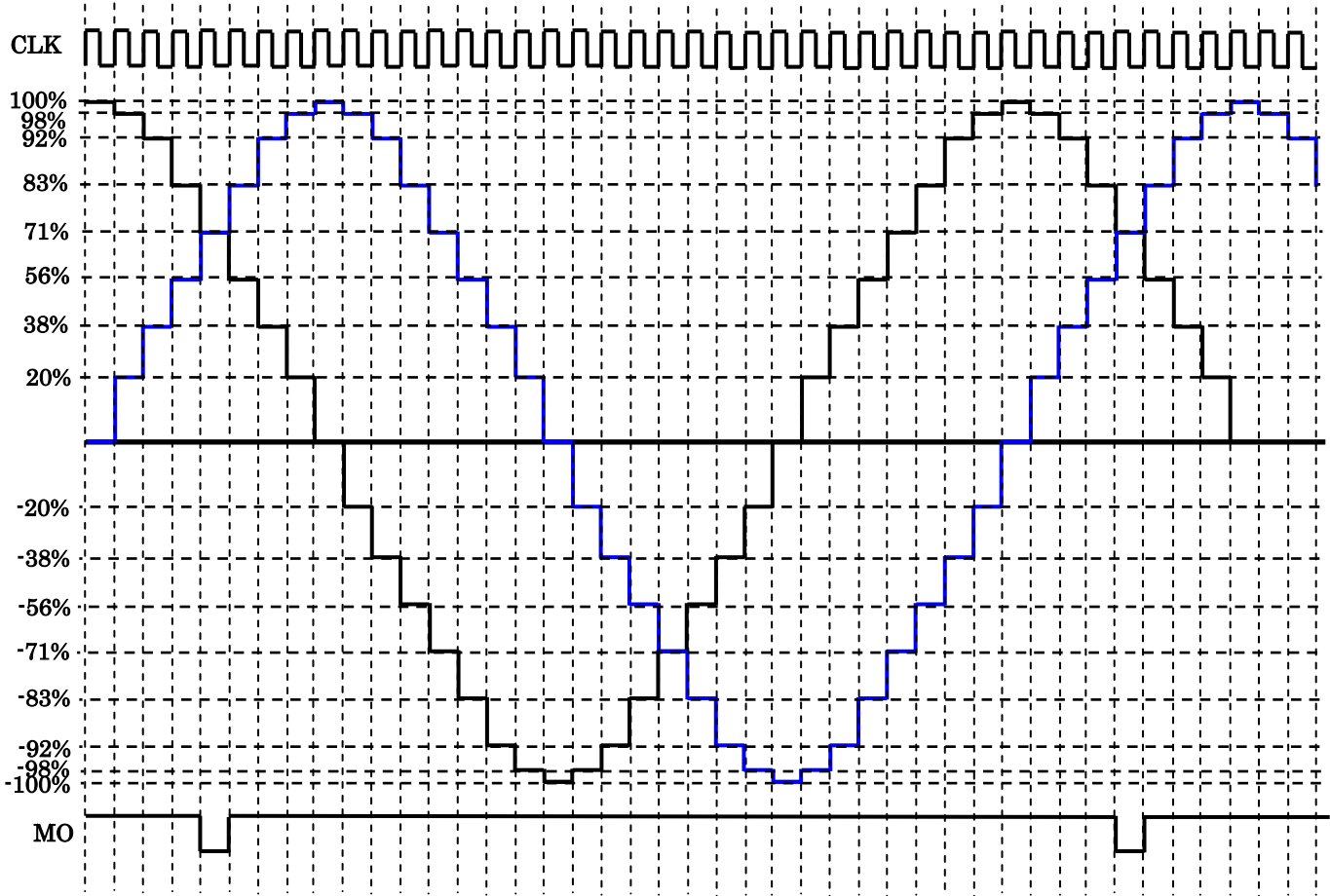
1/16 Step resolution
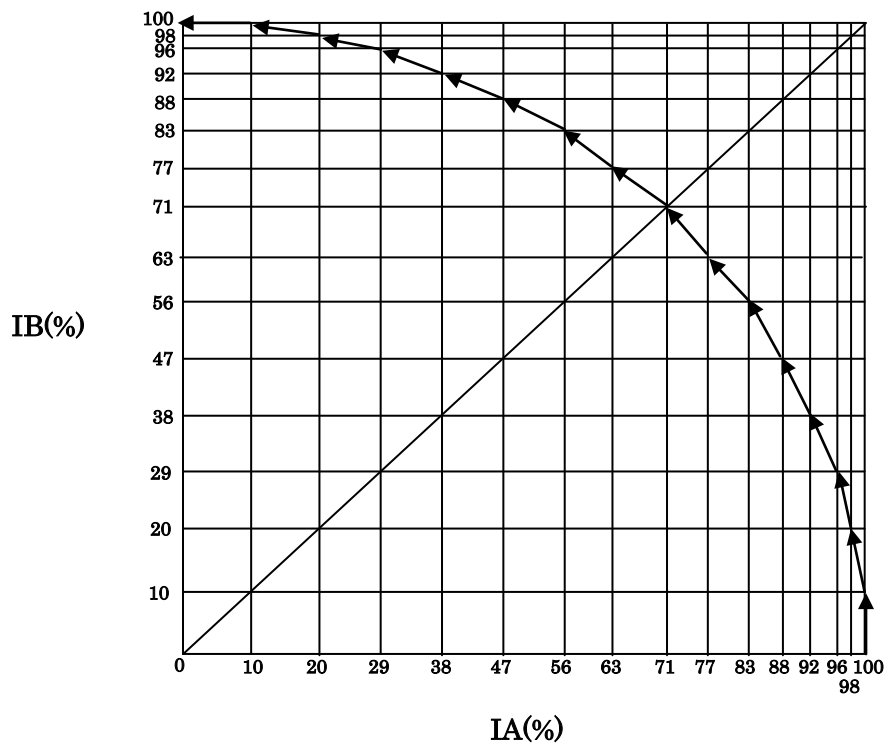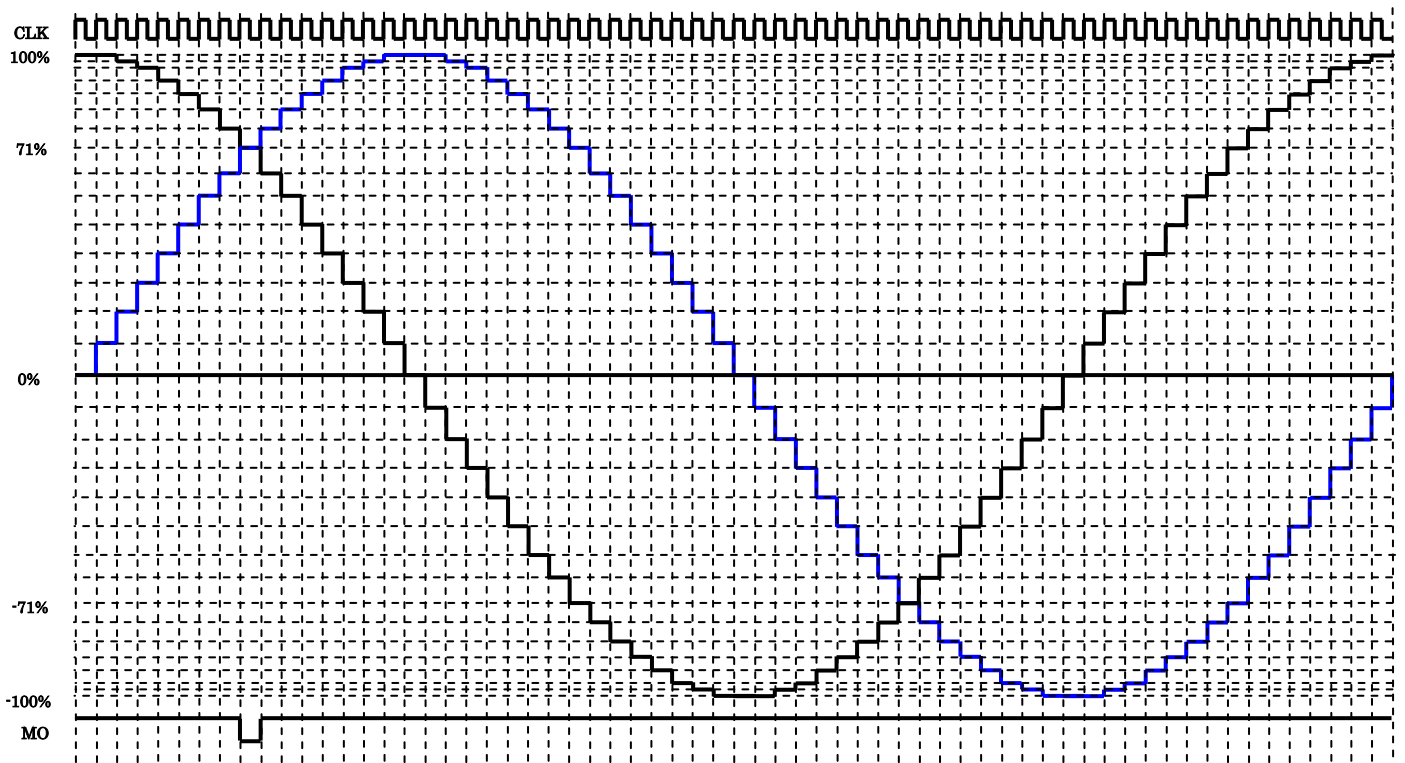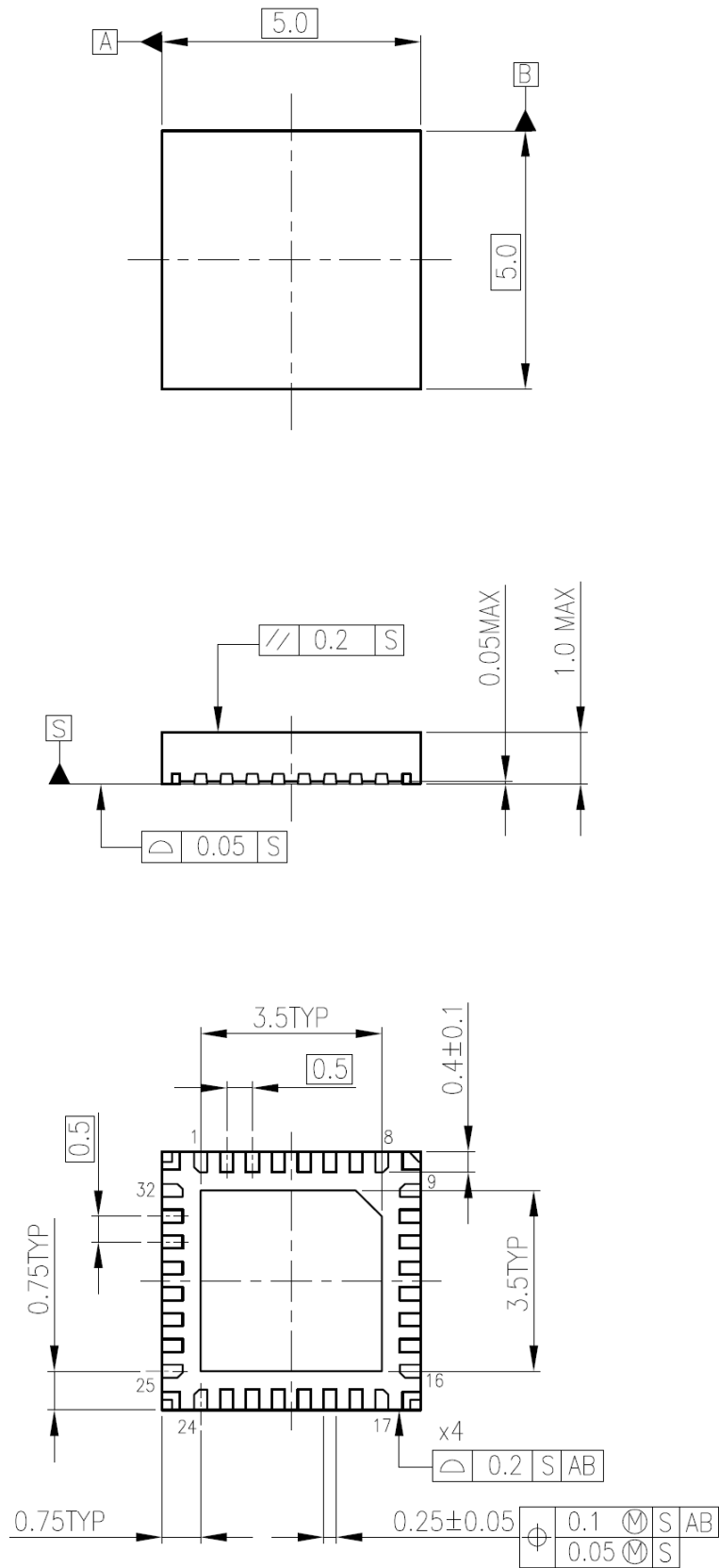
1/32 Step resolution

22. Package Dimensions

P-VQFN32-0505-0.50-004   Unit: mm

Notes on Contents

(1) Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

(2) Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

(3) Timing Charts
Timing charts may be simplified for explanatory purposes.

(4) Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

(5) Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
In addition, do not use any device inserted in the wrong orientation or incorrectly to which current is applied even just once.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

Overcurrent detection Circuit

Overcurrent detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the overcurrent detection circuits operate against the overcurrent, clear the overcurrent status immediately.

Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the overcurrent detection circuit to operate improperly or IC breakdown may occur before operation. In addition, depending on the method of use and usage conditions, if overcurrent continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over-temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the thermal shutdown circuit to operate improperly or IC breakdown to occur before operation.

Heat Radiation Design

When using an IC with large current flow such as power amp, regulator or driver, design the device so that heat is appropriately radiated, in order not to exceed the specified junction temperature (TJ) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, when designing the device, take into consideration the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor rotates in the reverse direction, stops or slows abruptly, current flows back to the motor's power supply owing to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond the absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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