

Precision Low Dropout Linear Controllers

FEATURES

- Precision 1% Reference
- Over-Current Sense Threshold Accurate to 5%
- Programmable Duty-Ratio Over-Current Protection
- 4.5 V to 36 V Operation
- 100mA Output Drive, Source, or Sink
- Under-Voltage Lockout

Additional Features of the UC2832 series:

- Adjustable Current Limit to Current Sense Ratio
- Separate +VIN terminal
- Programmable Driver Current Limit
- Access to VREF and E/A(+)
- Logic-Level Disable Input

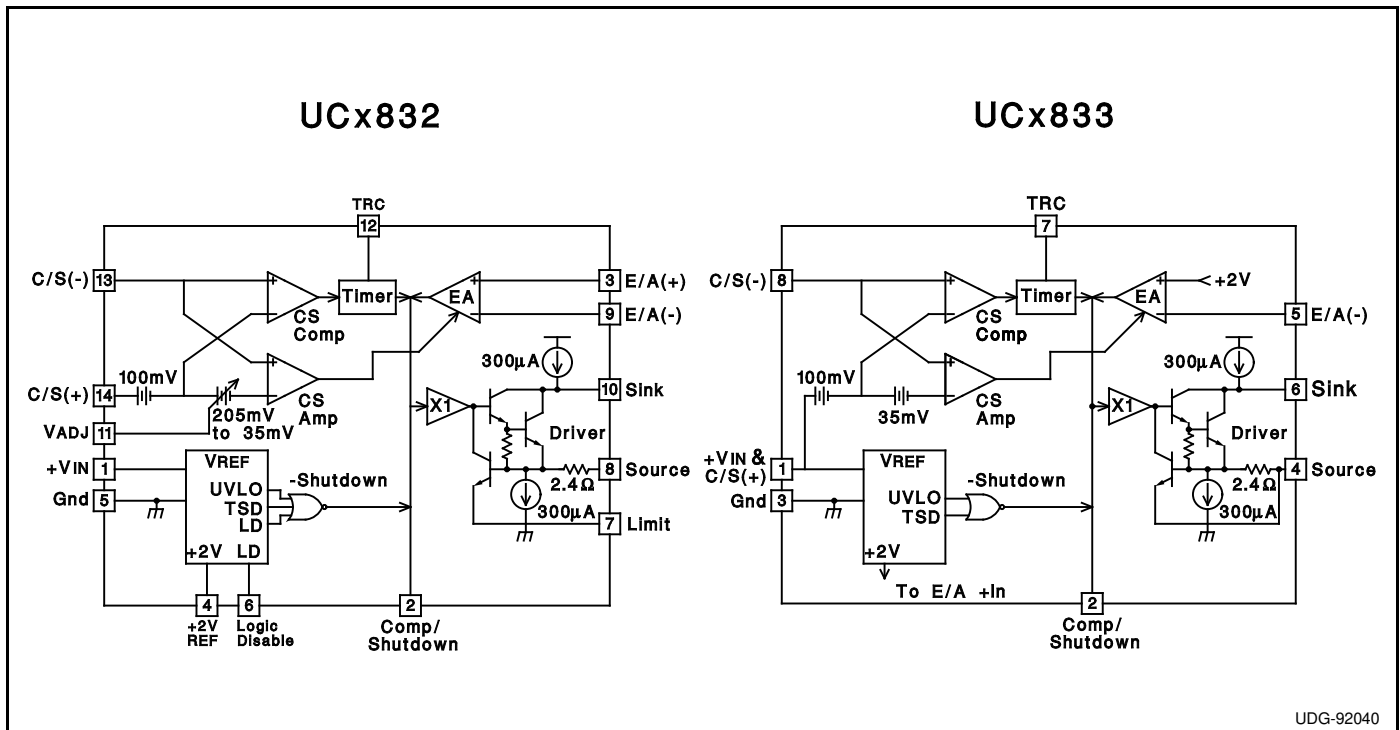
DESCRIPTION

The UC2832 and UC3833 series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the UCx832 to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

These IC's include a 2 Volt ($\pm 1\%$) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

The UC3833 family includes the basic functions of this design in a low-cost, 8-pin mini-dip package, while the UC2832 series provides added versatility with the availability of 14 pins. Packaging options include plastic (N suffix), or ceramic (J suffix). Specified operating temperature ranges are: commercial (0°C to 70°C), order UC3832/3 (N or J); and industrial (-40°C to 85°C), order UC2832/3 (N or J). Surface mount packaging is also available.

BLOCK DIAGRAMS



UDG-92040

ABSOLUTE MAXIMUM RATINGS

Supply Voltage +VIN	40V
Driver Output Current (Sink or Source)	450mA
Driver Sink to Source Voltage	40V
TRC Pin Voltage	-0.3V to 3.2V
Other Input Voltages	-0.3V to +VIN
Operating Junction Temperature (note 2)	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

Note 2: See Unitorde Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

UC2832

**DIL-14 (Top View)
J Or N Package**

**SOIC-16 (Top View)
DW Package**

**LCC-20 & PLCC-20
L & Q Package
(Top View)**

PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+VIN	2
Comp/Shutdown	3
E/A(+)	4
+2V REF	5
N/C	6
Gnd	7
Logic Disable	8
Limit	9
Source	10
N/C	11
E/A(-)	12
Sink	13
VADJ	14
N/C	15-17
Timer RC	18
Current Sense(-)	19
Current Sense(+)	20

UC3833

**DIL-8 (Top View)
J Or N Package**

**SOIC-16 (Top View)
DW Package**

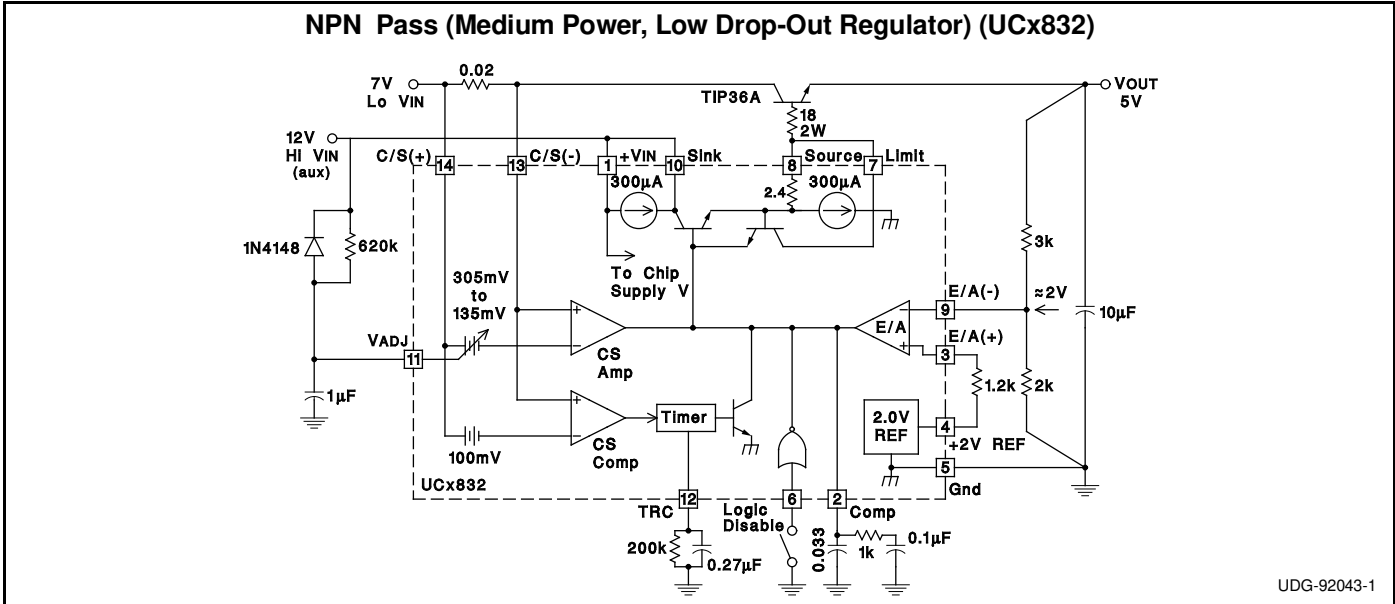
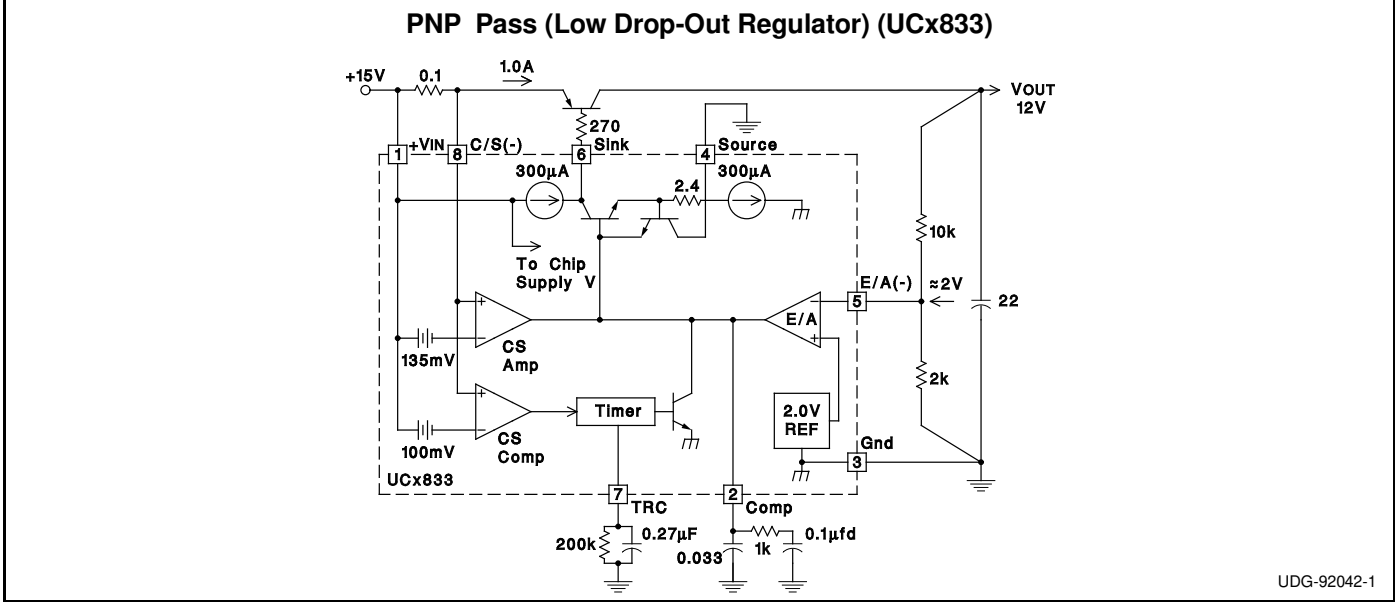
**LCC-20 & PLCC-20
L & Q Package
(Top View)**

PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN & C/S(+)	1
Comp/Shutdown	2
N/C	3
N/C	4
Gnd	5
N/C	6
N/C	7
Source	8
E/A(-)	9
Sink	10
N/C	11
N/C	12
N/C	13
Timer RC	14
Current Sense(-)	15
N/C	16
N/C	17
N/C	18-20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for
 $T_A = 0^\circ\text{C}$ to 70°C for the UC3832/3, -40°C to 85°C
for the UC2832/3, $+V_{IN} = 15\text{V}$, Driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	$+V_{IN} = 6\text{V}$		6.5	10	mA
	$+V_{IN} = 36\text{V}$		9.5	15	mA
	Logic Disable = 2 V (UCx832 only)		3.3		mA
Reference Section					
Output Voltage (Note 3)	$T_J = 25^\circ\text{C}$, $I_{DRIVER} = 10\text{mA}$	1.98	2.00	2.02	V
	over temperature, $I_{DRIVER} = 10\text{mA}$	1.96	2.00	2.04	V
Load Regulation (UCx832 only)	$I_o = 0$ to 10 m	-10	-5.0		mV
Line Regulation	$+V_{IN} = 4.5\text{V}$ to 36 V, $I_{DRIVER} = 10\text{m}$		0.033	0.5	mV/V
Under-Voltage Lockout Threshold			3.6	4.5	V
Logic Disable Input (UCx832 only)					
Threshold Voltage		1.3	1.4	1.5	V
Input Bias Current	Logic Disable = 0 V	-5.0	-1.0		μA
Current Sense Section					
Comparator Offset		95	100	105	mV
	Over Temperature	93	100	107	mV
Amplifier Offset (UCx833 only)		110	135	170	mV
Amplifier Offset (UCx832 only)	$V_{ADJ} = \text{Open}$	110	135	170	mV
	$V_{ADJ} = 1\text{V}$	180	235	290	mV
	$V_{ADJ} = 0\text{V}$	250	305	360	mV
Input Bias Current	$V_{CM} = +V_{IN}$	65	100	135	μA
Input Offset Current (UCx832 only)	$V_{CM} = +V_{IN}$	-10		10	μA
Amplifier CMRR (UCx832 only)	$V_{CM} = 4.1\text{V}$ to $+V_{IN} + 0.3$		80		dB
Transconductance	$I_{COMP} = \pm 100\mu\text{A}$		6		mS
V_{ADJ} Input Current (UCx832 only)	$V_{ADJ} = 0\text{V}$	-10	-1		μA
Timer					
Inactive Leakage Current	C/S(+) = C/S(-) = $+V_{IN}$; TRC pin = 2 V		0.25	1.0	μA
Active Pullup Current	C/S(+) = $+V_{IN}$, C/S(-) = $+V_{IN} - 0.4\text{V}$; TRC pin = 0 V	-345	-270	-175	μA
Duty Ratio (note 4)	ontime/period, $R_T = 200\text{k}$, $C_T = 0.27\mu\text{F}$		4.8		%
Period (notes 4,5)	ontime + offtime, $R_T = 200\text{k}$, $C_T = 0.27\mu\text{F}$		36		ms
Upper Trip Threshold (V_U)			1.8		V
Lower Trip Threshold (V_L)			0.9		V
Trip Threshold Ratio	V_U/V_L		2.0		V/V
Error Amplifier					
Input Offset Voltage (UCx832 only)	$V_{CM} = V_{COMP} = 2\text{V}$	-8.0		8.0	mV
Input Bias Current	$V_{CM} = V_{COMP} = 2\text{V}$	-4.5	-1.1		μA
Input Offset Current (UCx832 only)	$V_{CM} = V_{COMP} = 2\text{V}$	-1.5		1.5	μA
AVOL	$V_{COMP} = 1\text{V}$ to 13 V	50	70		dB
CMRR (UCx832 only)	$V_{CM} = 0\text{V}$ to $+V_{IN} - 3\text{V}$	60	80		dB
PSRR (UCx832 only)	$V_{CM} = 2\text{V}$, $+V_{IN} = 4.5\text{V}$ to 36		90		dB
Transconductance	$I_{COMP} = \pm 10\mu\text{A}$		43		mS
VOH	$I_{COMP} = 0$, Volts below $+V_{IN}$.95	1.3	V
VOL	$I_{COMP} = 0$.45	0.7	V
IOH	$V_{COMP} = 2\text{V}$	-700	-500	-100	μA

APPLICATION AND OPERATION INFORMATION (cont.)



Estimating Maximum Load Capacitance

For any power supply, the rate at which the total output capacitance can be charged depends on the maximum output current available and on the nature of the load. For a constant-current current-limited power supply, the output will come up if the load asks for less than the maximum available short-circuit limit current.

To guarantee recovery of a duty-ratio current-limited power supply from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time. The design value of ON time can be adjusted by changing the timing capacitor. Nominally, $T_{ON} = 0.693 \times 10k \times C_T$.

Typically, the IC regulates output current to a maximum of $I_{MAX} = K \times I_{TH}$, where I_{TH} is the timer trip-point current,

and
$$K = \frac{\text{Current Sense Amplifier Offset Voltage}}{100mA}$$

≈ 1.35 for UCx833, and is variable from 1.35 to 3.05 with VADJ for the UCx832.

For a worst-case constant-current load of value just less than I_{TH} , C_{MAX} can be estimated from:

$$C_{MAX} = ((K-1)I_{TH}) \left(\frac{T_{ON}}{V_{OUT}} \right),$$

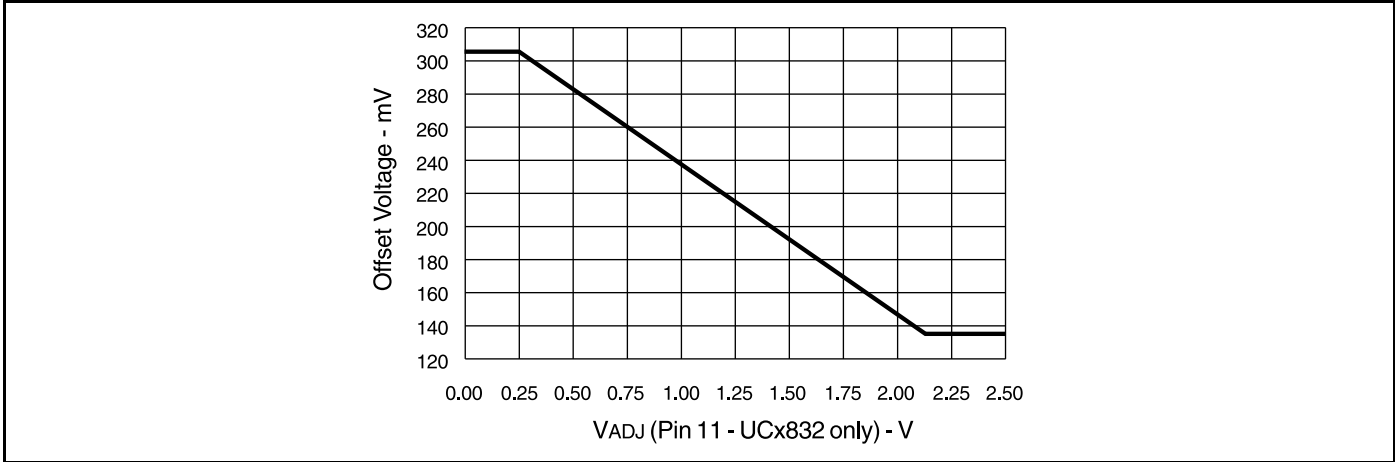
where V_{OUT} is the nominal regulator output voltage.

For a resistive load of value R_L , the value of C_{MAX} can be estimated from:

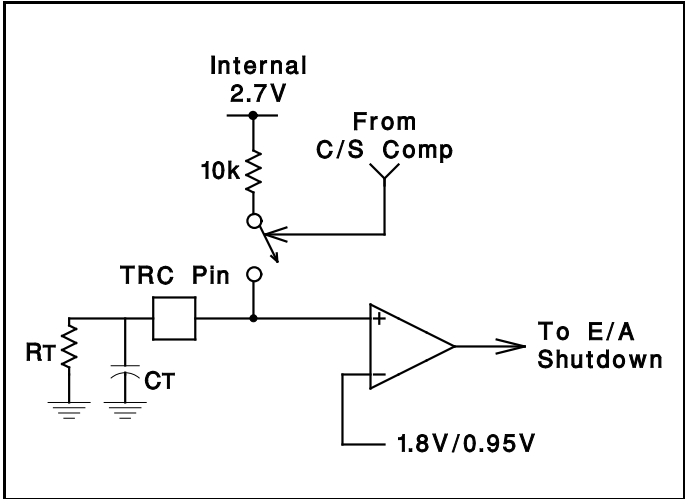
$$C_{MAX} = \frac{T_{ON}}{R_L} \cdot \frac{1}{\ln \left[\left(1 - \frac{V_{OUT}}{K \cdot I_{TH} \cdot R_L} \right)^{-1} \right]}$$

APPLICATION AND OPERATION INFORMATION (cont.)

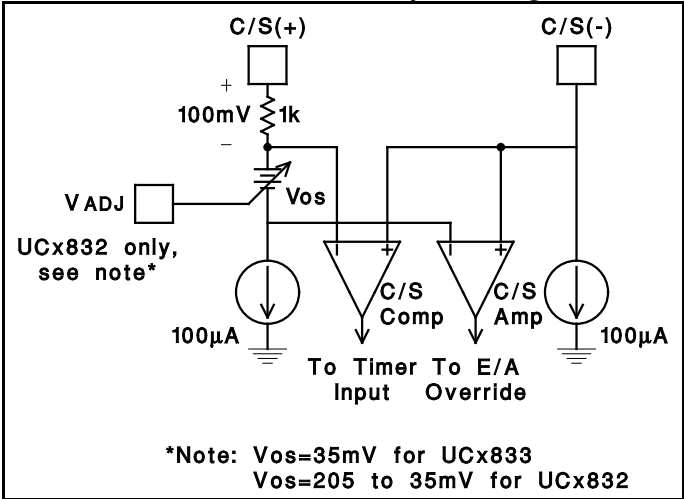
Current Sense Amplifier Offset Voltage vs VADJ



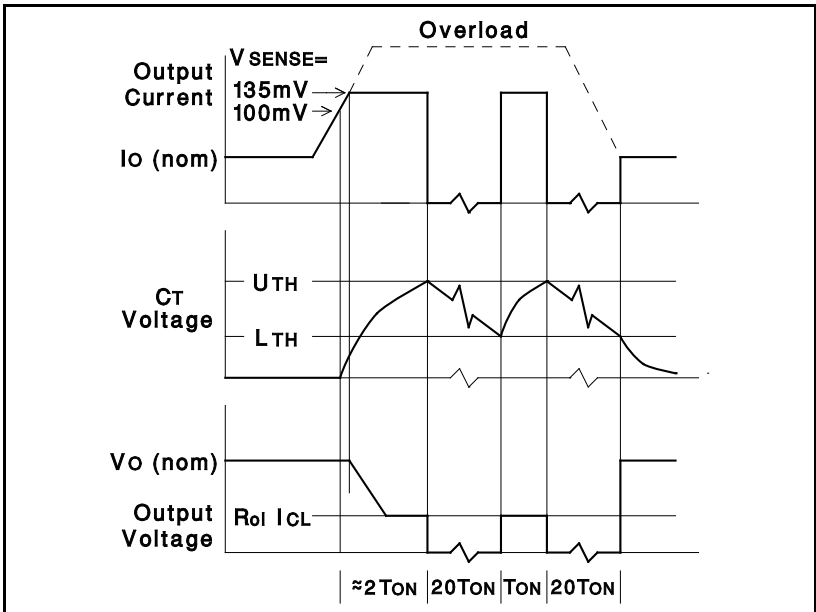
UCx832/33 Timer Function



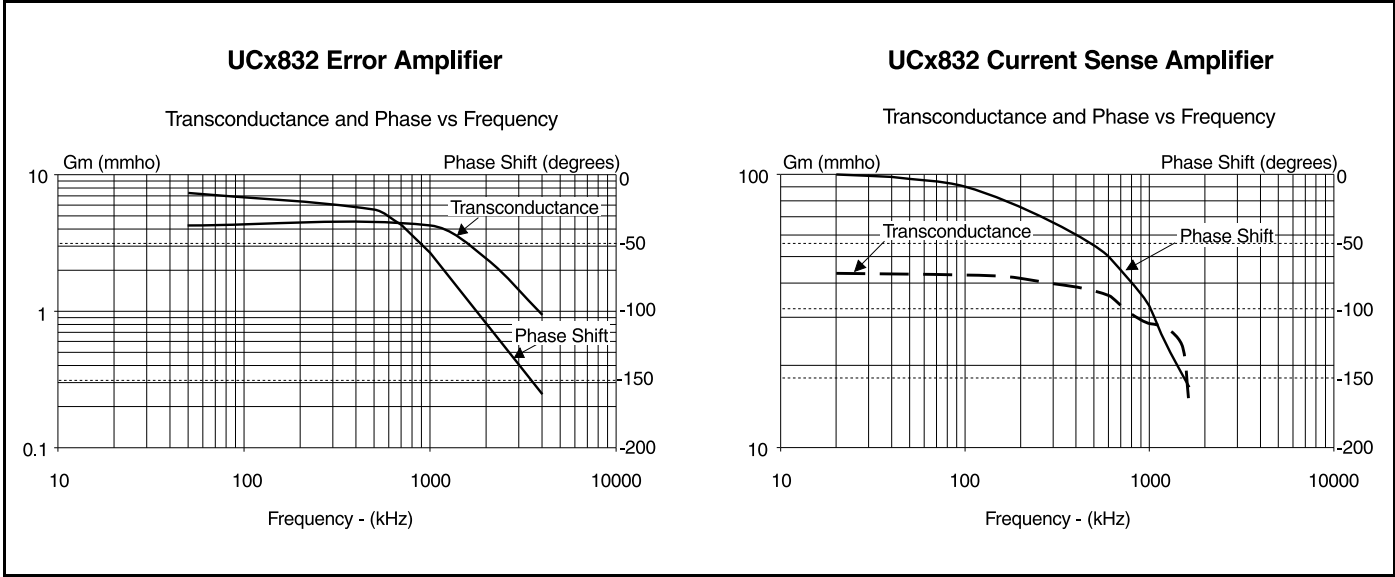
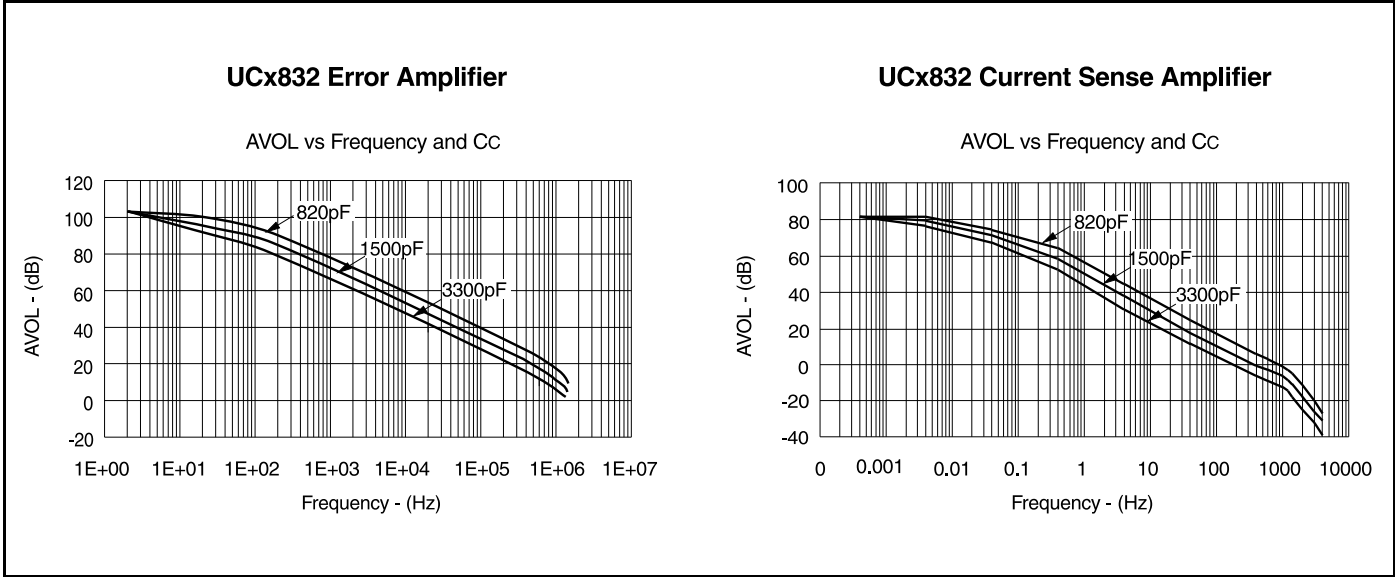
UCx832/33 Current Sense Input Configuration



Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.



APPLICATION AND OPERATION INFORMATION (cont.)



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9326501M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9326501M2A UC1832L/ 883B	Samples
5962-9326501MCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9326501MC A UC1832J/883B	Samples
5962-9326501V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9326501V2A UC1832L QMLV	Samples
5962-9326501VCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9326501VC A UC1832JQMLV	Samples
UC1832J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	UC1832J	Samples
UC1832J883B	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9326501MC A UC1832J/883B	Samples
UC1832L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9326501M2A UC1832L/ 883B	Samples
UC2832DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2832DW	Samples
UC2833DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2833DW	Samples
UC2833DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2833DW	Samples
UC2833DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2833DW	Samples
UC3832DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3832DW	Samples
UC3832DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3832DW	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3833DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3833DW	Samples
UC3833DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3833DW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC1832, UC1832-SP, UC2832, UC3832 :

- Catalog: [UC3832](#), [UC1832](#)
- Enhanced Product: [UC2832-EP](#)
- Military: [UC1832](#)
- Space: [UC1832-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2833DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3833DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

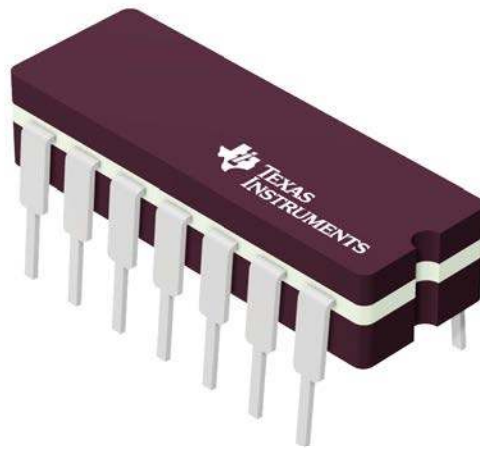


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2833DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3833DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

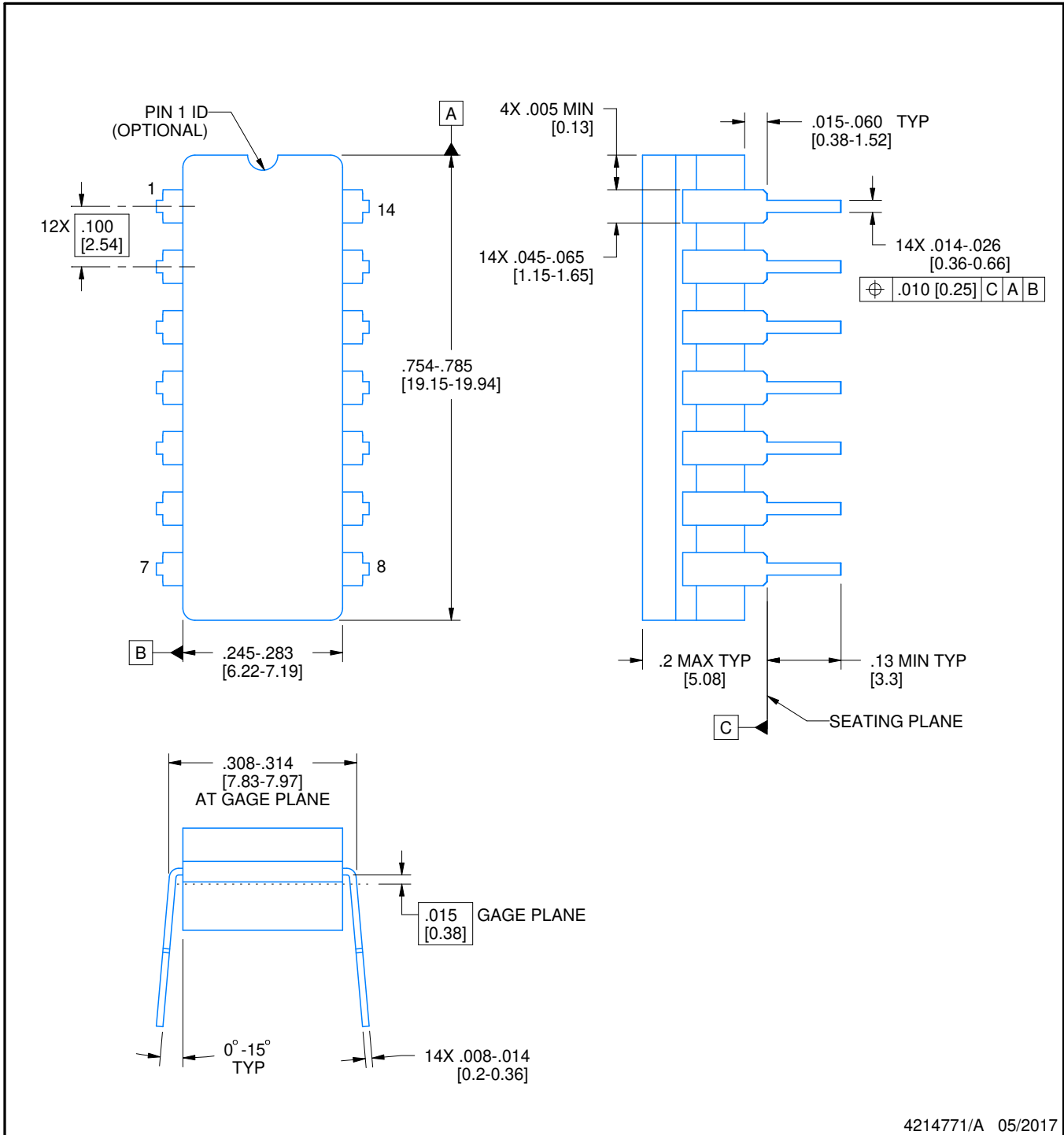
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PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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NOTES:

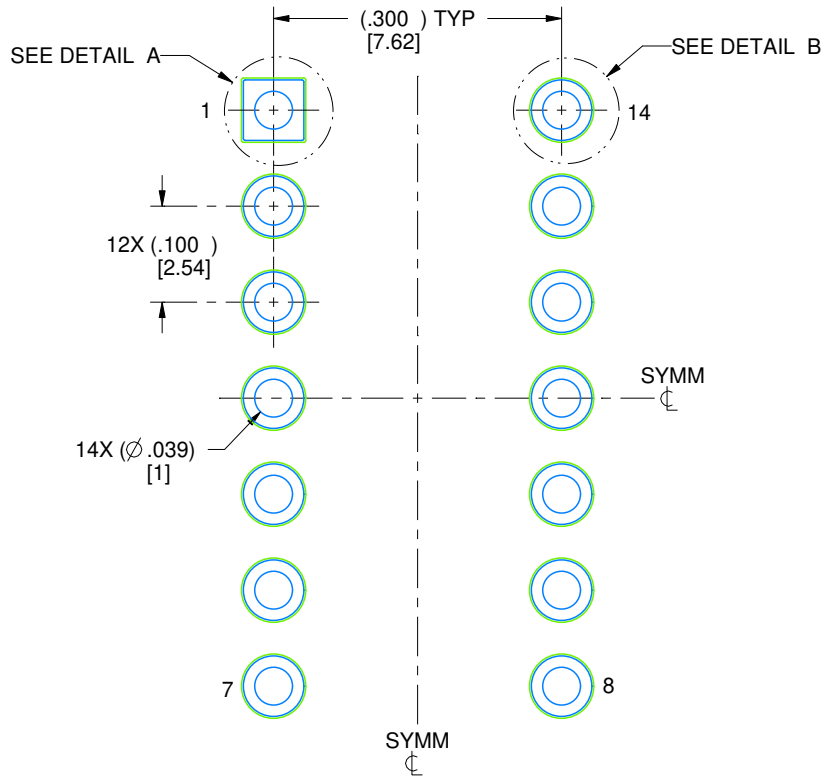
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

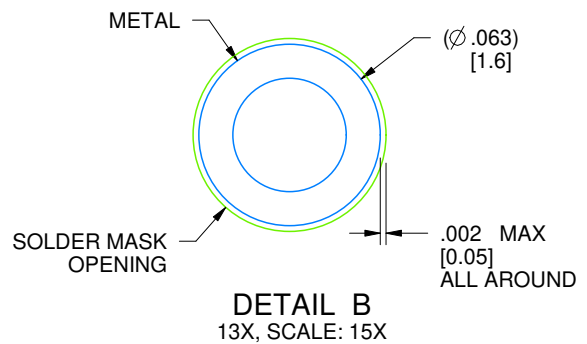
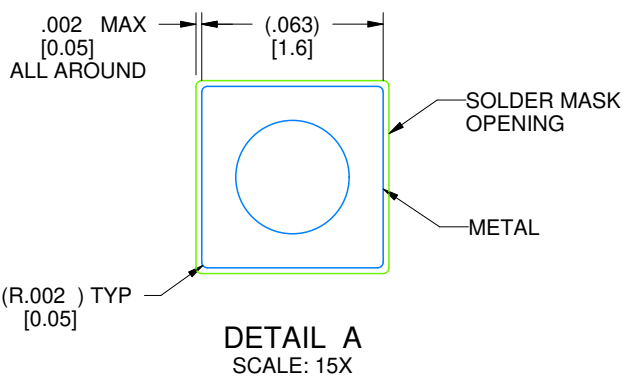
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

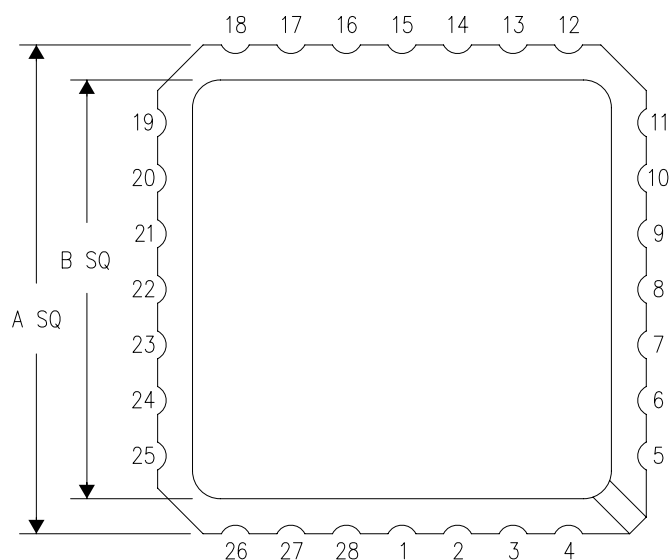


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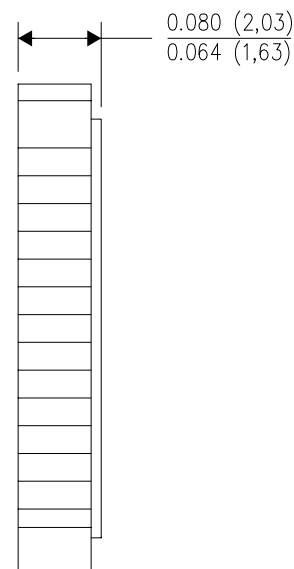
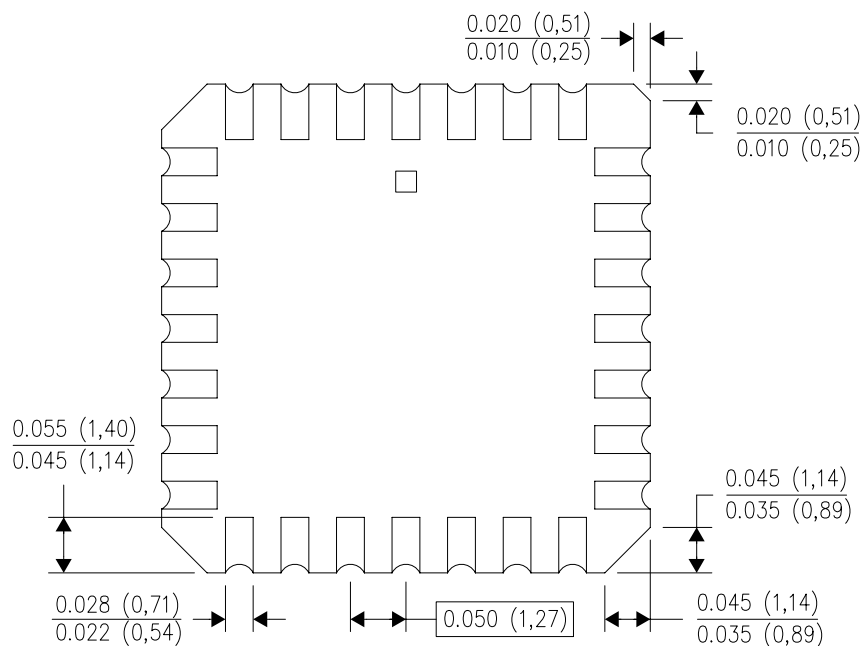
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

GENERIC PACKAGE VIEW

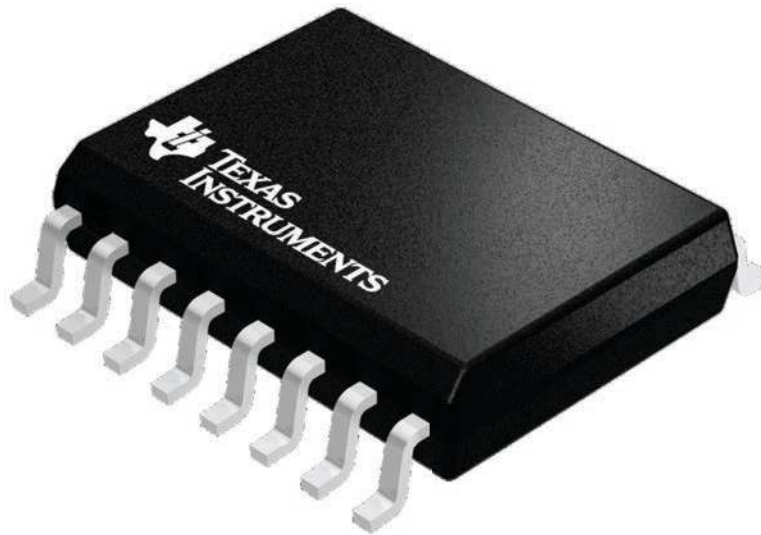
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



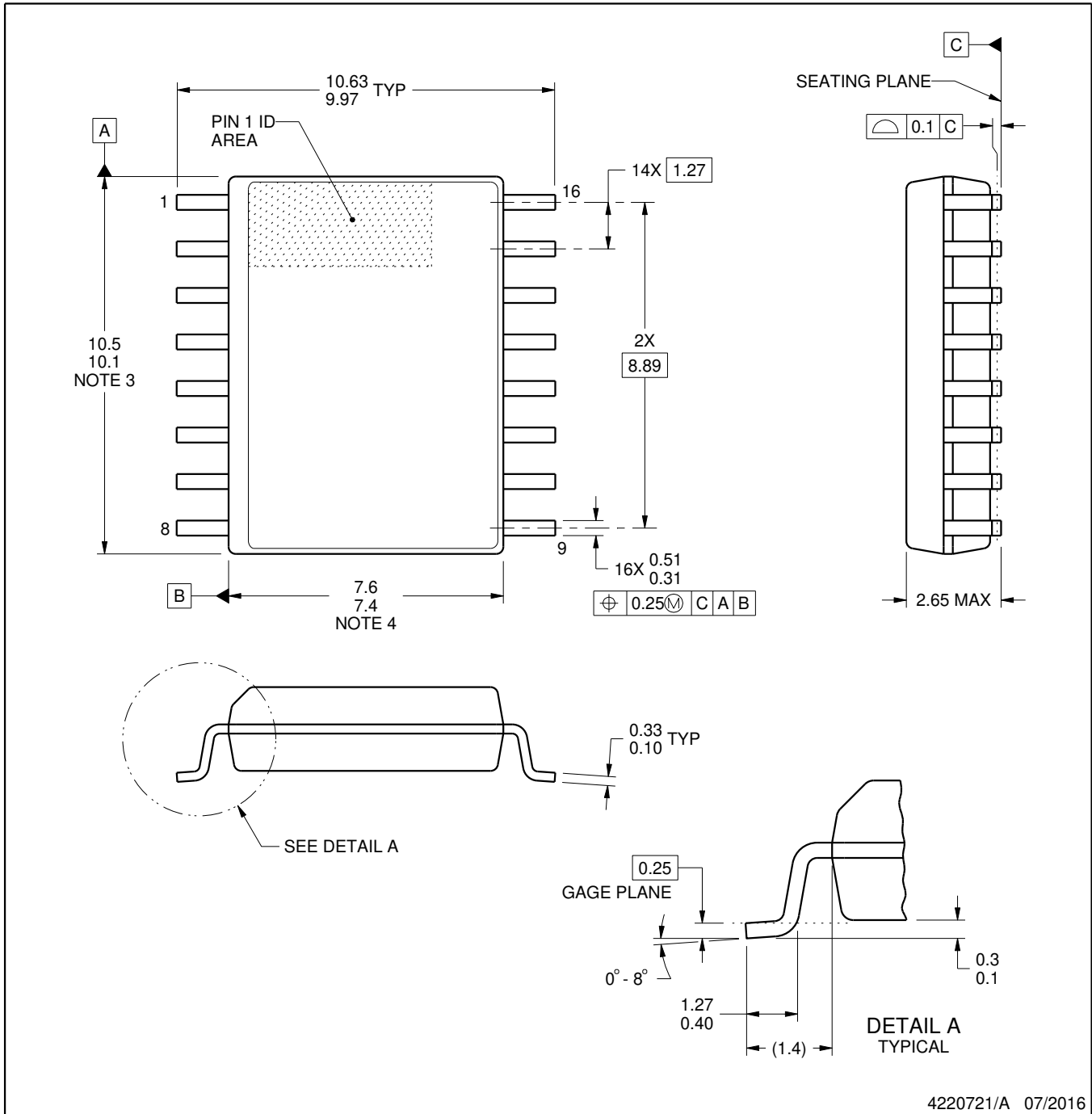
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DW0016A

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

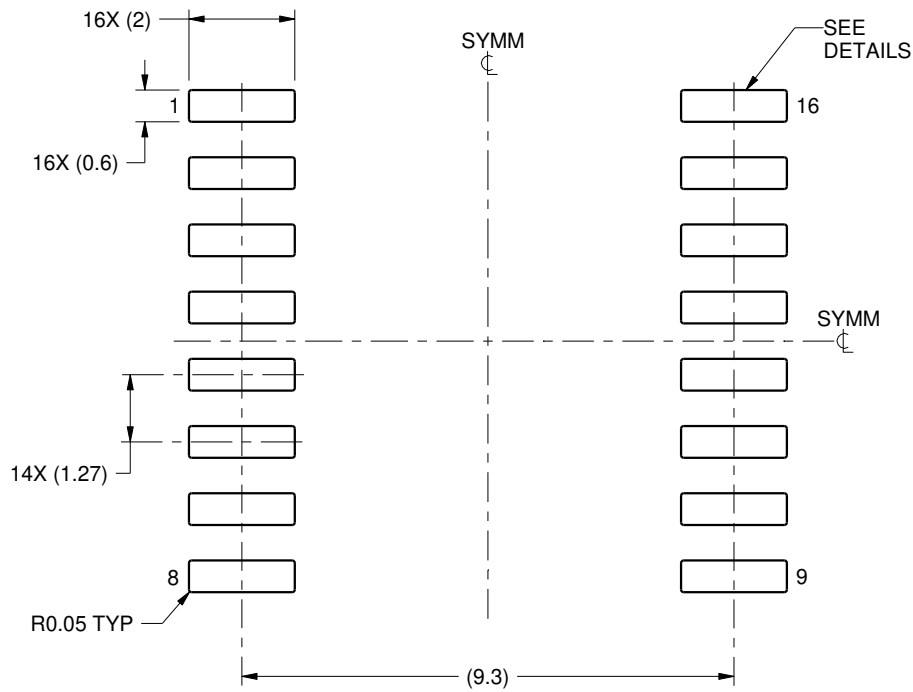
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

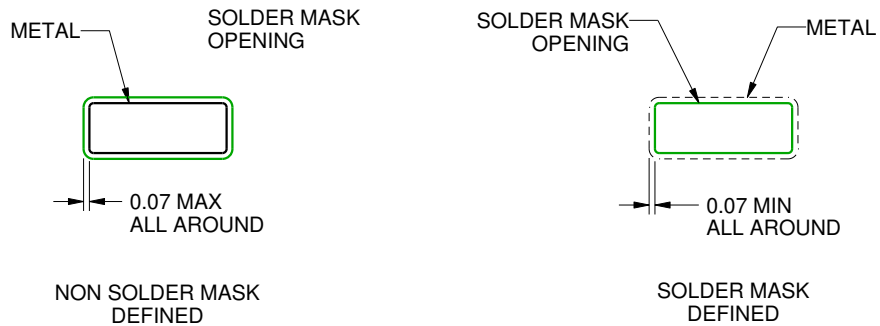
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

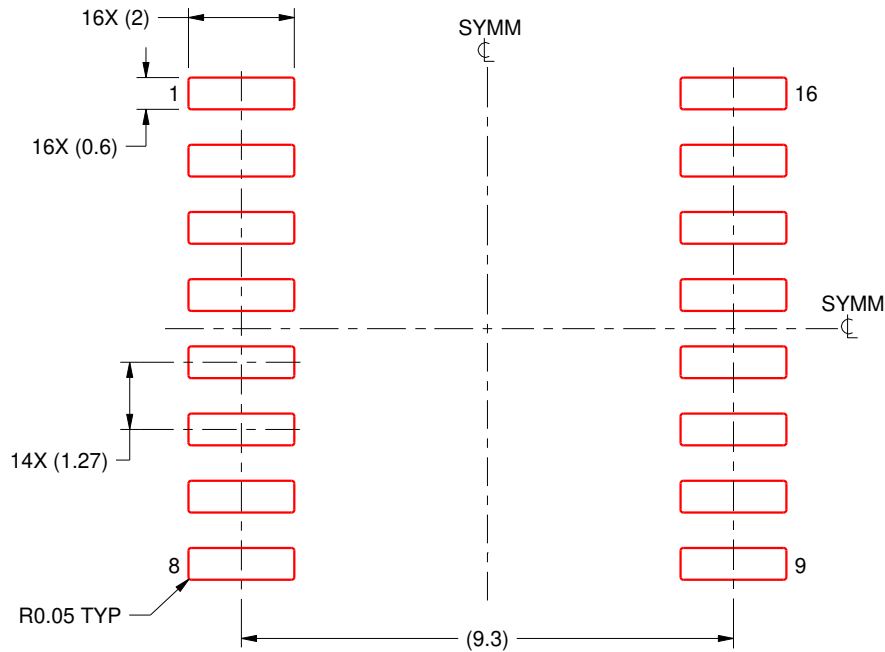
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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