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MM74HCT245 Octal 3-STATE Transceiver

General Description

The MM74HCT245 3-STATE bi-directional buffer utilizes advanced silicon-gate CMOS technology and is intended for two-way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption of CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device is TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The MM74HCT245 has one active low enable input (\bar{G}), and a direction control (DIR). When the DIR input is HIGH, data flows from the A inputs to the B outputs. When DIR is LOW, data flows from B to A.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

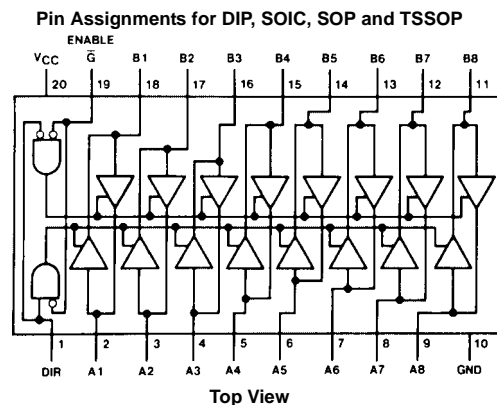
- TTL input compatible
- 3-STATE outputs for connection to system busses
- High output drive current: 6 mA (min)
- High speed: 16 ns typical propagation delay
- Low power: 80 μ A (74HCT Series)

Ordering Code:

Order Number	Package Number	Package Description
MM74HCT245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT245N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

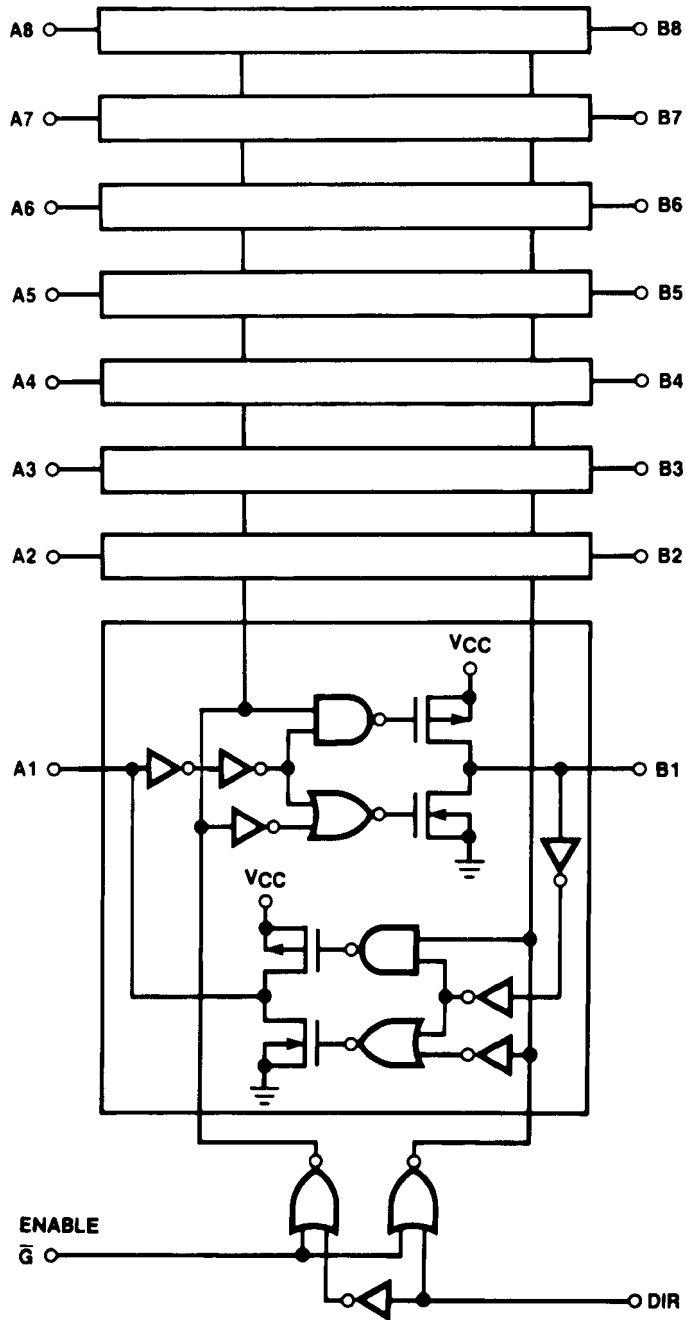


Truth Table

Control Inputs		Operation
\bar{G}	DIR	245
L	L	B data to A bus
L	H	A data to B bus
H	X	isolation

H = HIGH Level
L = LOW Level
X = Irrelevant

Logic Diagram



Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current,	± 35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	-40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.**Note 2:** Unless otherwise specified all voltages are referenced to ground.**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.**DC Electrical Characteristics** $(V_{CC} = 5V \pm 10\%$, unless otherwise specified.)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40$ to 85°C	$T_A = -55$ to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}	V_{CC}	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
		$ I_{OUT} = 20 \mu\text{A}$	4.2	3.98	3.84	3.7	V
		$ I_{OUT} = 6.0 \text{ mA}, V_{CC} = 4.5V$	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum LOW Level Voltage	$V_{IN} = V_{IH}$ or V_{IL}	0	0.1	0.1	0.1	V
		$ I_{OUT} = 20 \mu\text{A}$	0.2	0.26	0.33	0.4	V
		$ I_{OUT} = 6.0 \text{ mA}, V_{CC} = 4.5V$	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL} , Pin 1 or 19		± 0.1	± 1.0	± 1.0	μA
		$V_{OUT} = V_{CC}$ or GND $\bar{G} = V_{IH}$		± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$		8	80	160	μA
		$V_{IN} = 2.4V$ or $0.5V$ (Note 4)	0.6	1.0	1.3	1.5	mA

Note 4: Measured per input. All other inputs at V_{CC} or ground.

AC Electrical Characteristics

$V_{CC} = 5.0V$, $t_r = t_f = 6\text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 45\text{ pF}$	16	20	ns
t_{PZL} , t_{PZH}	Maximum Output Enable Time	$C_L = 45\text{ pF}$ $R_L = 1\text{ k}\Omega$	29	40	ns
t_{PLZ} , t_{PHZ}	Maximum Output Disable Time	$C_L = 5\text{ pF}$ $R_L = 1\text{ k}\Omega$	20	25	ns

AC Electrical Characteristics

$V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40\text{ to }85^\circ\text{C}$	$T_A = -55\text{ to }125^\circ\text{C}$	Units
			Typ	Guaranteed Limits			
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 50\text{ pF}$	17	23	29	34	ns
		$C_L = 150\text{ pF}$	24	30	38	45	ns
t_{PZL}	Maximum Output Enable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$	31	42	53	63	ns
t_{PZH}	Maximum Output Enable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$	23	33	41	49	ns
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$	21	30	38	45	ns
t_{THL} , t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50\text{ pF}$	8	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output/Input Capacitance		20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance	$\overline{G} = V_{CC}$ (Note 5)	7				pF
		$\overline{G} = \text{GND}$	100				pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



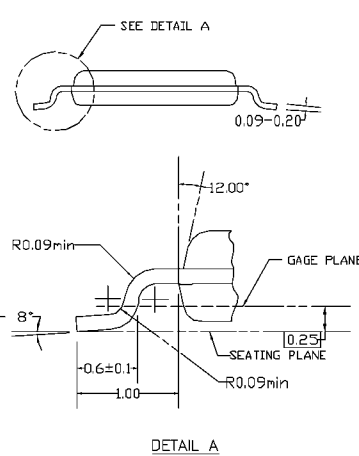
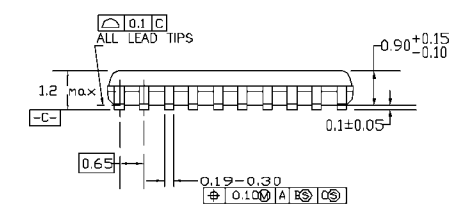
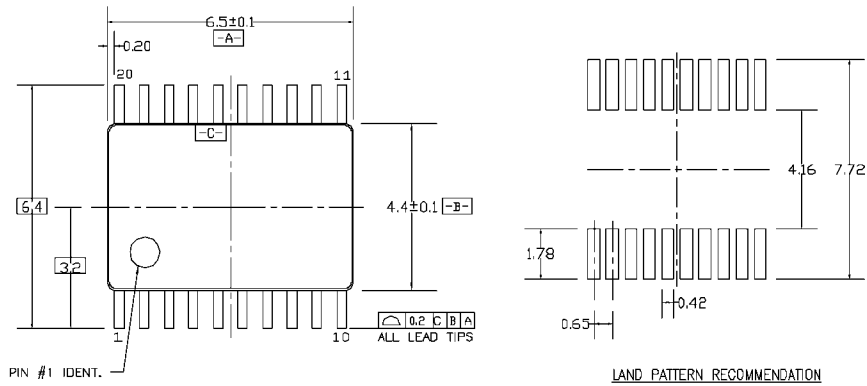
DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
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 - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

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