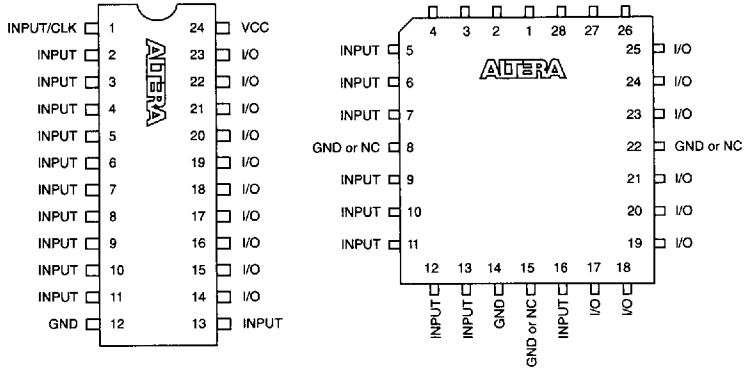
Features

- High-performance, 10-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 7.5 ns
  - Counter frequencies of up to 111.1 MHz
  - Pipelined data rates of up to 109.8 MHz
- 1.0-micron CMOS technology with EPROM configuration elements
- Programmable I/O architecture with 12 dedicated inputs and 10 I/O pins
- Up to 16 product terms per macrocell, with selectable output polarity and separate Output Enable
- Global asynchronous Reset and synchronous Preset product terms
- Industry-standard 22V10 architecture
- Enhanced version with superset Clock and feedback features (EP22V10E)
- Available in one-time-programmable (OTP) plastic packages (see Figure 19)
  - 24-pin plastic dual in-line package (PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

Figure 19. EP22V10 Package Outlines

Package outlines not drawn to scale.



24-Pin DIP

EP22V10
EP22V10E

28-Pin J-Lead

EP22V10
EP22V10E

Table 6 summarizes EP22V10 features.

Table 6. EP22V10 Device Features

Feature	EP22V10	EP22V10E
t_{PD}	7.5 ns	10 ns
Counter frequency	111.1 MHz	95.2 MHz
Pipeline data rates	109.8 MHz	100 MHz
Packages	24-pin PDIP 28-pin PLCC	24-pin CerDIP 24-pin PDIP 28-pin PLCC

General Description

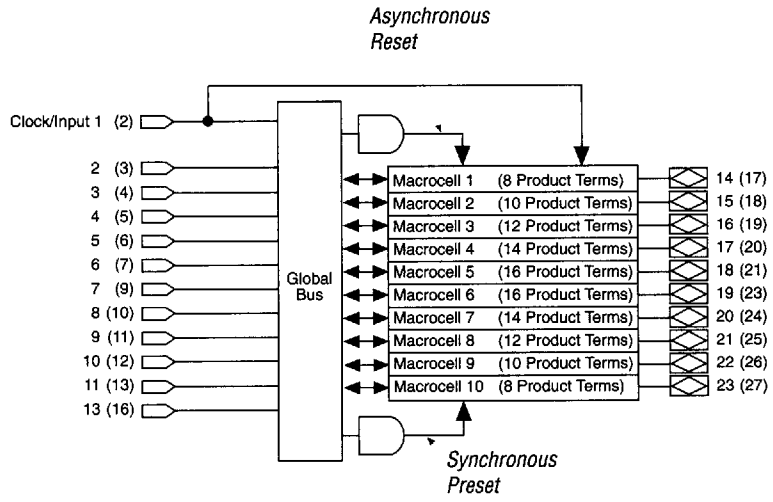
Altera's EP22V10 devices are high-performance, high-integration, general-purpose EPLDs that use 1.0-micron CMOS technology with EPROM configuration elements. These devices accommodate logic functions with up to 22 inputs and 10 I/O macrocells, including an average of 12 input product terms and a separate product term for Output Enable. The EP22V10 provides a high-speed, low-cost, low-power upgrade from PAL and GAL devices. Altera's EP22V10 devices are pin- and JEDEC File-compatible with industry-standard 22V10s. The EP22V10E offers an enhanced macrocell, including an inverted Clock option and an additional feedback path.

Functional Description

The EP22V10 is an optimized device featuring 10 macrocells, 12 dedicated input pins, and 10 I/O pins. Each I/O pin is associated with a macrocell (see Figure 20); all inputs and feedback signals, and their complements, are available to product terms. The product terms form a global bus that feeds each macrocell. Depending on its position, each macrocell can use from 8 to 16 product terms.

Figure 20. EP22V10 Block Diagram

Numbers in parentheses are for PLCC packages.



The EP22V10 architecture includes the following elements:

- Macrocells
- Register Reset and Preset
- Programmable Output Enable
- Power-on characteristics

Macrocells

Each EP22V10 macrocell can be programmed to function as an input, or as a combinatorial or registered output. Each combinatorial or registered output can be active-high or active-low.

EP22V10

The EP22V10 macrocell, shown in Figure 21, offers registered or combinatorial logic with active-high or active-low outputs. In EP22V10 devices, the output type determines the feedback type (if feedback is used); registered output dictates registered feedback, and combinatorial output dictates pin feedback. Because outputs may be programmed as either active-high or active-low on a macrocell-by-macrocell basis, the polarity of the output pin associated with the macrocell register is independent of the register itself.

Figure 21. EP22V10 Macrocell Architecture

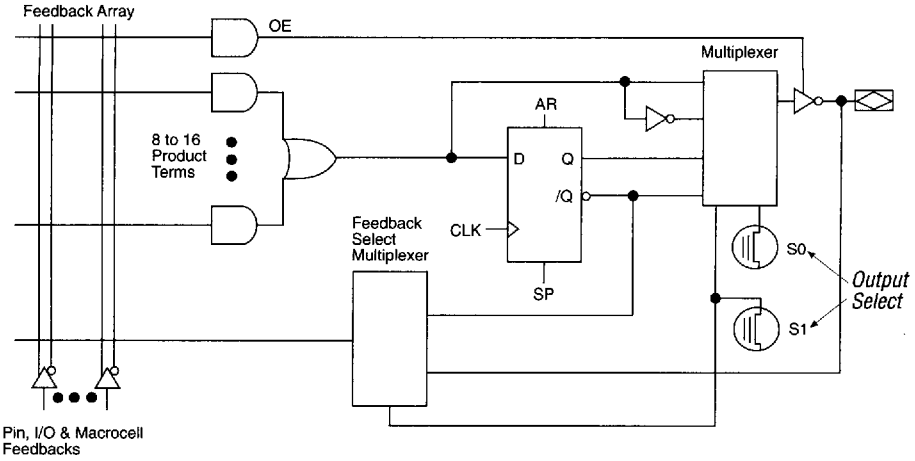


Table 7 lists the output configurations for EP22V10 device.

Table 7. EP22V10 Macrocell Configurations

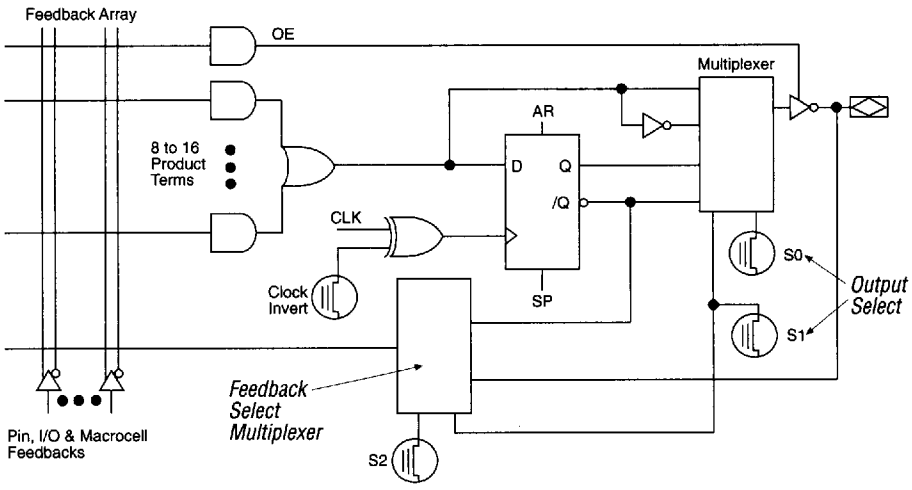
S1	S0	Output/Polarity	Feedback
0	0	Registered/active low	Registered
0	0	Registered/active high	Registered
1	0	Combinatorial/active low	Pin
1	1	Combinatorial/active high	Pin

Pin 1 can supply the Clock input (CLK) for the macrocell registers or be used as a generic input. The Output Enable (OE) for each macrocell is controlled by an independent, asynchronous product term in the array.

EP22V10E

The EP22V10E macrocell has an enhanced Clock and improved feedback selection. See Figure 22. In this macrocell, the Clock can be inverted using the attached XOR gate, allowing the macrocell flipflop to latch at the falling edge—rather than the rising edge—of the CLK input.

Figure 22. EP22V10E Macrocell Architecture



To further enhance the macrocell, an S2 switch has been added to the feedback select multiplexer. See Table 8 for feedback output configurations.

Table 8. EP22V10E Macrocell Configurations

S2	S1	S0	Output/Polarity	Feedback
0	0	0	Registered/active low	Registered
0	0	1	Registered/active high	Registered
0	1	0	Combinatorial/active low	Pin
0	1	1	Combinatorial/active high	Pin
1	0	0	Registered/active low	Pin
1	0	1	Registered/active high	Pin
1	1	0	Combinatorial/active low	Registered
1	1	1	Combinatorial/active high	Registered

All combinations of output and feedback are supported by the EP22V10E. A combinatorial signal can drive the macrocell, while a registered version of that signal is fed back into the device.

Register Reset & Preset

All EP22V10 macrocell registers can be preset or reset using global Preset and Reset product terms. The register Preset is synchronous and must meet the specified Clock setup time; the register Reset is asynchronous and has no Clock setup requirement. Output polarity is selected separately.

The global Preset signal is determined by a single product term originating from the feedback array. When the signal is asserted, the next Clock transition that triggers a macrocell register will set the register's Q outputs to a logic high. If post-register inversion is used (active-low output), the macrocell's pin will be set to a logic low.

Programmable Output Enable

Each macrocell's Output Enable can place the output in a high-impedance state (tri-state). This output buffer is controlled by a single asynchronous product term per macrocell.

Power-On Characteristics

All EP22V10 device inputs and outputs respond a maximum of 1 µs after V_{CC} power-up (V_{CC} = 4.75 V) or after a power-down/power-up sequence. Macrocells programmed as registers are set to a logic low; output polarity is selected separately.

JEDEC File & Pin Compatibility

EP22V10 devices are 100% pin-, function-, and JEDEC File-compatible with industry-standard 22V10 devices. JEDEC Files developed for standard 22V10 architectures can be used to program EP22V10 and EP22V10E devices. EP22V10E devices maintain JEDEC File compatibility if none of the device's superset features are used.

EP22V10 devices in 28-pin PLCC packages offer additional VCC and GND pins (1, 8, 15, and 22). Industry-standard 22V10 designs leave these pins as No Connects (NC).

Figure 23 shows the typical supply current (I_{CC}) versus frequency for EP22V10 devices.

Figure 23. EP22V10 I_{CC} vs. Frequency

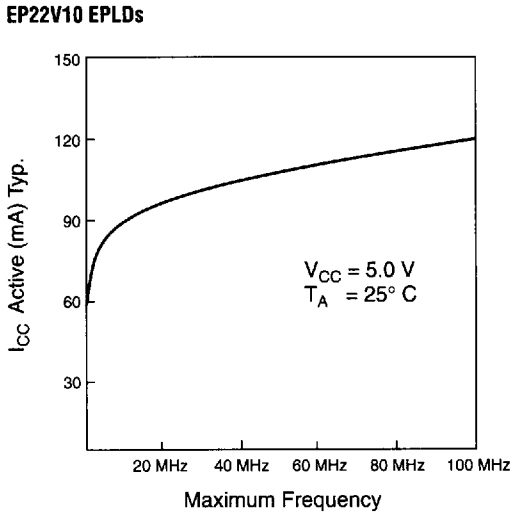
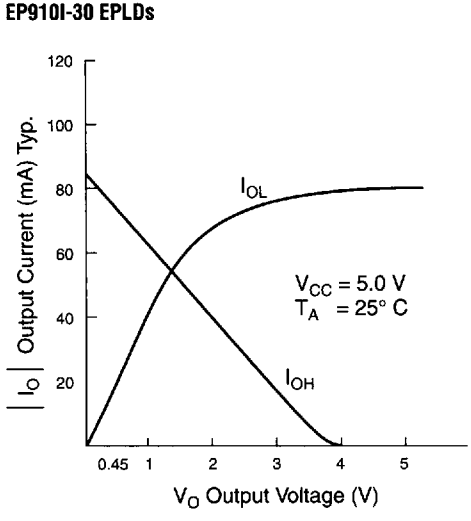


Figure 24 shows the output drive characteristics of EP22V10 I/O pins.

Figure 24. EP22V10 Output Drive Characteristics



Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	–2.0	7.0	V
V_I	DC input voltage	*Notes (2), (3)*	–0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature		–65	150	° C
T_{AMB}	Ambient temperature	*Note (4)*	–10	85	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	5.0-V operation	4.75	5.25	V
V_{IN}	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			5	ns
t_F	Input fall time			5	ns

DC Operating Conditions *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	*Note (2)*	–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4.0 mA DC, V_{CC} = Min.	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –100 µA, V_{CC} = Min.	V_{CC} – 0.3		V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA DC, V_{CC} = Min.		0.45	V
I_I	Input leakage current	V_{CC} = Max., GND < V_{IN} < V_{CC}		10	µA
I_{OZ}	Tri-state output leakage current	V_{CC} = Max., GND < V_{OUT} < V_{CC}		10	µA
I_{SC}	Output short-circuit current	V_{CC} = Max., V_{OUT} = 0.5 V, *Note (7)*		120	mA

Capacitance

			EP22V10 EP22V10E		
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{OUT}	I/O capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF
C_{CLK}	Clock pin capacitance, *Note (6)*	V_{IN} = 0 V, f = 1.0 MHz		17 (10)	pF

I_{CC} Supply Current *Note (8)*

			EP22V10 EP22V10E			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{CC3}	V_{CC} supply current	V_{CC} = Max., V_{IN} = V_{CC} or GND, no load, f_{IN} = 15 MHz, *Note (9)*		90	130	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.
(2) Voltage with respect to ground; all over- and undershoots due to system or tester noise are included.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no load conditions.
(4) Under bias. Extended temperature versions are also available.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(6) Value in parentheses is for EP22V10-7 device only.
(7) Test 1 output at a time; test duration should not exceed 1 second.
(8) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(9) Measured with device programmed as a 10-bit counter.

Combinatorial Mode AC Operating Conditions: EP22V10 & EP22V10E *Note (1)*

			EP22V10-7		EP22V10-10 EP22V10E-10		EP22V10-15 EP22V10E-15		EP22V10-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PD1}	Input to non-registered output, *Note (2)*	C1 = 50 pF		7.5		10		15		25	ns
t_{PD2}	I/O to non-registered output, *Note (2)*	C1 = 50 pF		7.5		10		15		25	ns
t_{PZX}	Input or I/O to output enable	C1 = 50 pF		9		10		15		25	ns
t_{PXZ}	Input or I/O to output disable	C1 = 5 pF		9		10		15		25	ns
t_{PCLR}	Input or I/O to asynchronous reset			10		15		20		20	ns

Register Mode Synchronous Clock AC Operating Conditions: EP22V10 & EP22V10E *Note (1)*

		EP22V10-7		EP22V10-10 EP22V10E-10		EP22V10-15 EP22V10E-15		EP22V10-25		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CNT1}	Maximum counter frequency, external feedback, *Note (3)*	111.1		95.2		64.5		35.7		MHz
f_{CNT2}	Maximum counter frequency, internal feedback, *Note (3)*	111.1		100		83.3		40		MHz
f_{MAX}	Maximum frequency (pipelined), no feedback	109.8		100		83.3		40		MHz
t_{SU}	Input or I/O setup time to global clock	3		3.5		7.5		14		ns
t_{SP}	Input or I/O setup time to synchronous preset	4.5		4.5		7.5		10.5		ns
t_{H}	Input or I/O hold time from global clock	0		0		0		0		ns
t_{CO1}	Global clock to output delay		6		7		8		14	ns
t_{CO2}	Global clock to output valid fed through combinatorial macrocell		13		16		18		30	ns
t_{CNT}	Minimum global clock period		13		10		12		25	ns
t_{CL}	Clock low time	4		4		5		10		ns
t_{CH}	Clock high time	4		4		5		10		ns
t_{CP}	Clock period	9.1		10		12		25		ns
t_{ARW}	Asynchronous reset pulse duration	4		4		5		5		ns
t_{ARR}	Asynchronous reset to global clock recovery time	7		7		9		10		ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) Measured with all outputs switching.

(3) Measured with device configured as a 10-bit counter.