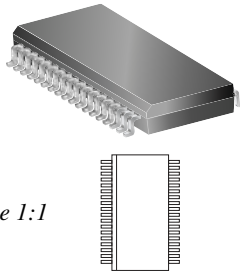


## 3-Phase Power MOSFET Controller for Automotive Applications

### Features and Benefits

- Drives wide range of N-channel MOSFETs in 3-phase bridges
- PFM boost converter for use with low-voltage battery supplies
- Internal LDO regulator for gate-driver supply
- Bootstrap circuits for high-side gate drivers
- Current monitor output
- Adjustable battery overvoltage detection
- Diagnostic outputs
- Motor lead short-to-battery, short-to-ground, and bridge-open protection
- Undervoltage protection
- $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$   $T_J$  operation
- Thermal shutdown

### Package 36-pin QSOP (LQ):



Approximate scale 1:1

### Description

The A3935 is designed specifically for automotive applications that require high-power motors. Each provides six high-current gate drive outputs capable of driving a wide range of N-channel power MOSFETs.

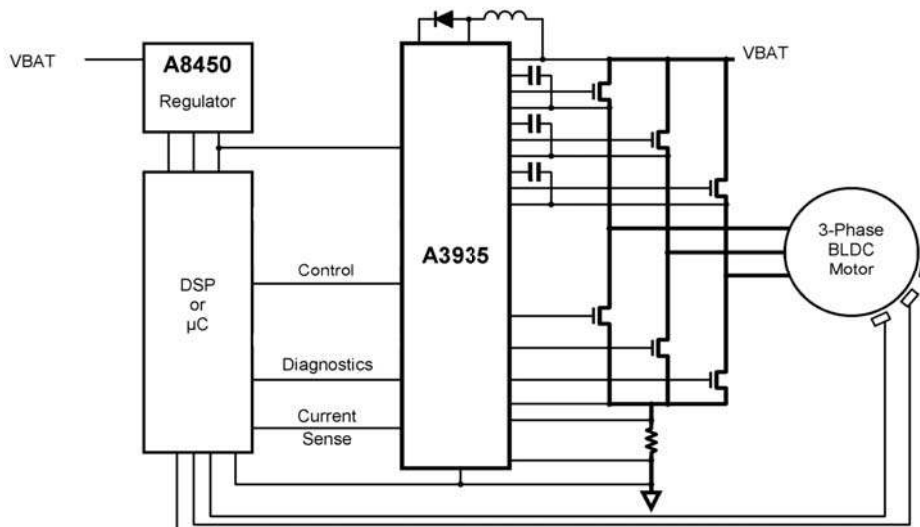
A requirement of automotive systems is steady operation over a varying battery input range. The A3935 integrates a pulse-frequency modulated boost converter to create a constant supply voltage for driving the external MOSFETs. Bootstrap capacitors are utilized to provide the above battery supply voltage required for N-channel FETs.

Direct control of each gate output is possible via six TTL-compatible inputs. A differential amplifier is integrated to allow accurate measurement of the current in the three-phase bridge.

Diagnostic outputs can be continuously monitored to protect the driver from short-to-battery, short-to-supply, bridge-open, and battery under/overvoltage conditions. Additional protection features include dead-time, VDD undervoltage, and thermal shutdown.

The A3935 is supplied in a 36-lead 0.8 mm pitch QSOP (package LQ, similar to SOICW). The lead (Pb) free variants (suffix -T) have 100% matte tin leadframe plating.

### Typical Application



### Selection Guide

Part Number	Pb-free	Packing	Terminals	Package
A3935KLQTR <sup>1</sup>	–	1500 pieces/reel	36	QSOP (similar to SOICW) surface mount
A3935KLQTR-T <sup>2</sup>	Yes			

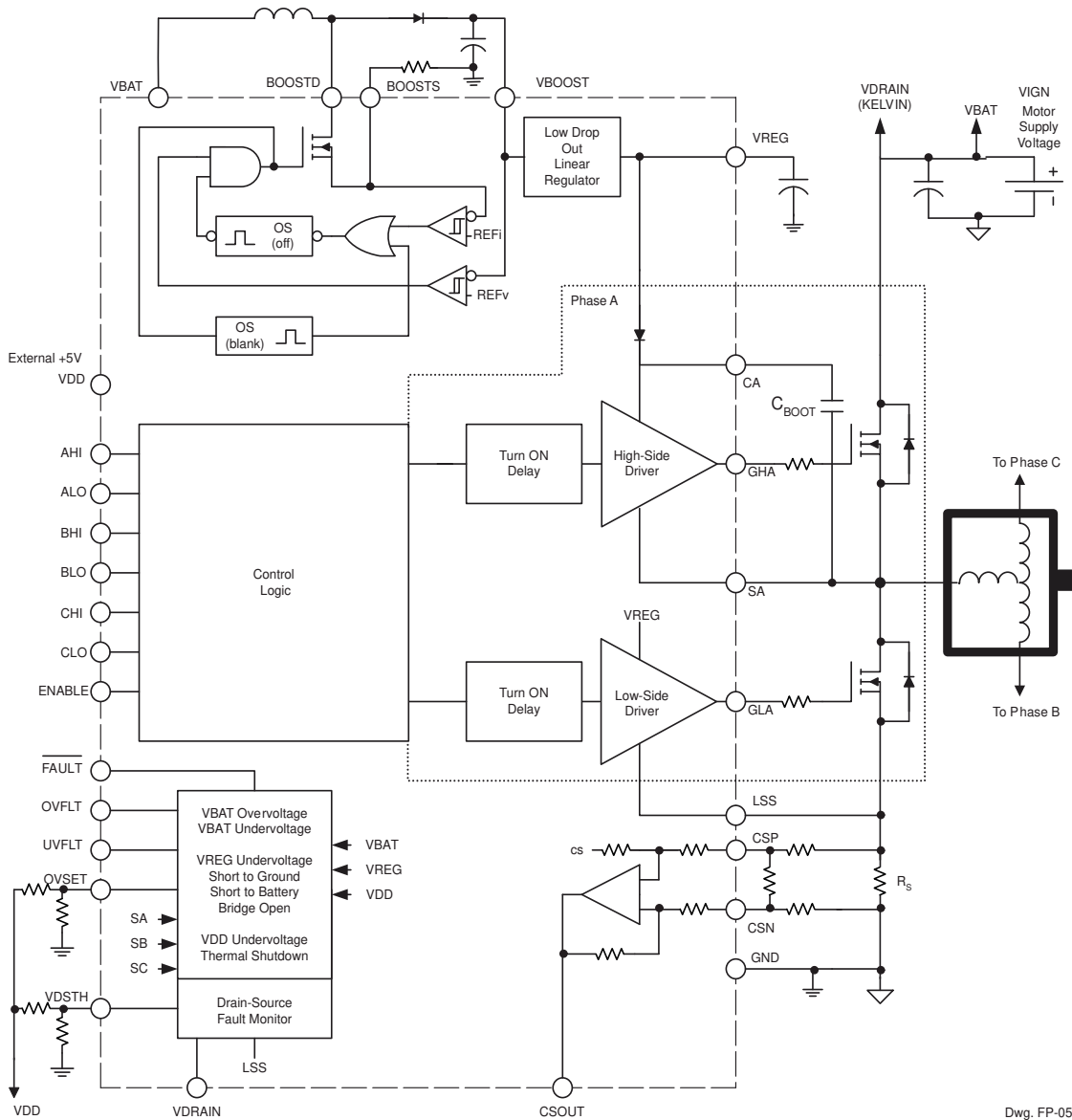
<sup>1</sup>Variant has been determined to be obsolete and is no longer in production. Status change: October 31, 2011.

<sup>2</sup>Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: October 31, 2011.

### Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Units
Load Supply Voltage	$V_{BAT}$	VBAT pin	–0.6 to 40	V
	$V_{DRAIN}$	VDRAIN pin		
	$V_{BOOST}$	VBOOST pin		
	$V_{BOOSTD}$	VBOOSTD pin		
Output Voltage Range	$V_{GHx}$	GHA, GHB, and GHC pins	–4 to 55	V
	$V_{Sx}$	SA, SB, and SC pins	–4 to 40	V
	$V_{GLx}$	GLA, GLB, and GLC pins	–4 to 16	V
	$V_{Cx}$	CA, CB, and CC pins	–0.6 to 55	V
Sense Circuit Voltage	$V_{CSx}$	CSN and CSP pins	–4 to 6.5	V
	$V_{LSS}$	LSS pin		
Logic Supply Voltage	$V_{DD}$	VDD pin	–0.3 to 6.5	V
Logic Input/Output	$V_{OVSET}$	OVSET pin		
	$V_{BOOSTS}$	BOOSTS pin		
	$V_{CSOUT}$	CSOUT pin		
	$V_{DSTH}$	VDSTH pin		
		remaining logic pins		
ESD Rating – Human Body Model		AEC-Q100-002; all pins	2.5	kV
ESD Rating – Charged Device Model		AEC-Q100-011; all pins	1050	V
Operating Temperature	$T_A$	Range K	–40 to 135	°C
Junction Temperature*	$T_{J(max)}$	Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.	150	°C
Storage Temperature Range	$T_{stg}$		–55 to 150	°C

Functional Block Diagram



Dwg. FP-053

**ELECTRICAL CHARACTERISTICS** at  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $V_{\text{BAT}} = 7$  to  $16$  V,  $V_{\text{DD}} = 4.75$  to  $5.25$  V, **ENABLE** = 22.5 kHz, 50% duty cycle, two phases active; unless otherwise noted

Characteristics	Symbol	Conditions	Min.	Typ <sup>1</sup> .	Max.	Units
<b>Power Supply</b>						
$V_{\text{DD}}$ Supply Current	$I_{\text{DD}}$	All logic inputs = 0 V	–	–	7.0	mA
$V_{\text{BAT}}$ Supply Current	$I_{\text{BAT}}$	All logic inputs = 0 V	–	–	3.0	mA
Battery Voltage Operating Range	$V_{\text{BAT}}$		7.0	–	40	V
Bootstrap Diode Forward Voltage	$V_{\text{DBOOT}}$	$I_{\text{DBOOT}} = -I_{\text{Cx}} = 10$ mA, $V_{\text{DBOOT}} = V_{\text{REG}} - V_{\text{Cx}}$	0.8	–	2.0	V
		$I_{\text{DBOOT}} = -I_{\text{Cx}} = 100$ mA	1.5	–	2.3	V
Bootstrap Diode Resistance	$r_{\text{DBOOT}}$	$r_{\text{DBOOT}}(100 \text{ mA}) = (V_{\text{DBOOT}}(150 \text{ mA}) - V_{\text{DBOOT}}(50 \text{ mA})) / 100 \text{ mA}$	2.5	–	7.5	$\Omega$
Bootstrap Diode Current Limit <sup>2</sup>	$I_{\text{DM}}$	$3 \text{ V} < V_{\text{REG}} - V_{\text{Cx}} < 12 \text{ V}$	–150	–	–1150	mA
Bootstrap Quiescent Current	$I_{\text{Cx}}$	$V_{\text{Cx}} = 40$ V, <b>GHx</b> = ON	10	–	30	$\mu\text{A}$
Bootstrap Refresh Time	$t_{\text{refresh}}$	$V_{\text{Sx}}$ = low, to guarantee $\Delta V = +0.5$ V refresh of 0.47 $\mu\text{F}$ Bootstrap Capacitor, <b>CBOOT</b> , to $V_{\text{Cx}} - V_{\text{Sx}} = +10$ V	–	–	2.0	$\mu\text{s}$
VREG Output Voltage <sup>3</sup>	$V_{\text{REG}}$	$V_{\text{BAT}} = 7$ to $40$ V, $V_{\text{BOOST}}$ from Boost Regulator	12.7	–	14	V
VREG Dropout Voltage <sup>4</sup>	$V_{\text{REGDO}}$	$V_{\text{REGDO}} = V_{\text{BOOST}} - V_{\text{REG}}$ , $I_{\text{REG}} = 40$ mA	–	0.9	–	V
Gate Drive Average Supply Current	$I_{\text{REG}}$	No external dc load at VREG, $C_{\text{REG}} = 10$ $\mu\text{F}$	–	–	40	mA
VREG Input Bias Current	$I_{\text{REGbias}}$	Current into $V_{\text{BOOST}}$ , <b>ENABLE</b> = 0	–	–	4.0	mA
<b>Boost Supply</b>						
VBOOST Output Voltage Limit	$V_{\text{BOOSTM}}$	$V_{\text{BAT}} = 7$ V	14.9	–	16.3	V
VBOOST Output Voltage Limit Hysteresis	$\Delta V_{\text{BOOSTM}}$		35	–	180	mV
Boost Switch On Resistance	$r_{\text{DS(on)}}$	$I_{\text{BOOSTD}} < 300$ mA	–	1.4	3.3	$\Omega$
Boost Switch Maximum Current	$I_{\text{BOOSTSW}}$		–	–	300	mA
Boost Current Limit Threshold Voltage	$V_{\text{Bl(th)}}$	Increasing $V_{\text{BOOSTS}}$	0.45	–	0.55	V
Off Time	$t_{\text{off}}$		3.0	–	8.0	$\mu\text{s}$
Blanking Time	$t_{\text{blank}}$		100	–	220	ns
<b>Control Logic</b>						
Logic Input Voltage	$V_{\text{I(1)}}$	Minimum high level input for logic 1	2.0	–	–	V
	$V_{\text{I(0)}}$	Maximum low level input for logic 0	–	–	0.8	V
Logic Input Current	$I_{\text{I(1)}}$	$V_{\text{I}} = V_{\text{DD}}$	–	–	500	$\mu\text{A}$
	$I_{\text{I(0)}}$	$V_{\text{I}} = 0.8$ V	50	–	–	$\mu\text{A}$
Logic Input Hysteresis	$V_{\text{Ihys}}$		100	–	300	mV
Logic Output High Voltage	$V_{\text{O(H)}}$	$I_{\text{O(H)}} = -800$ $\mu\text{A}$	$V_{\text{DD}} - 0.8$	–	–	V
Logic Output Low Voltage	$V_{\text{O(L)}}$	$I_{\text{O(L)}} = 1.6$ mA	–	–	0.4	V
<b>Gate Drives, GHx (internal source, or upper, switch stages)<sup>5</sup></b>						
Output High Voltage	$V_{\text{DSL(H)}}$	<b>GHx</b> : $I_{\text{xU}} = -10$ mA, $V_{\text{Sx}} = 0$	$V_{\text{REG}} - 2.26$	–	$V_{\text{REG}}$	V
		<b>GLx</b> : $I_{\text{xU}} = -10$ mA, $V_{\text{LSS}} = 0$	$V_{\text{REG}} - 0.26$	–	$V_{\text{REG}}$	V
Source Current (pulsed)	$I_{\text{xU}}$	$V_{\text{SDU}} = 10$ V, $T_J = 25^\circ\text{C}$	–	800	–	mA
		$V_{\text{SDU}} = 10$ V, $T_J = 135^\circ\text{C}$	400	–	–	mA
Source On Resistance	$r_{\text{SDU(on)}}$	$I_{\text{xU}} = -150$ mA, $T_J = 25^\circ\text{C}$	4.0	–	10	$\Omega$
		$I_{\text{xU}} = -150$ mA, $T_J = 135^\circ\text{C}$	7.0	–	15	$\Omega$

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**ELECTRICAL CHARACTERISTICS (continued) at  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $V_{\text{BAT}} = 7$  to  $16\text{ V}$ ,  $V_{\text{DD}} = 4.75$  to  $5.25\text{ V}$ ,  
**ENABLE = 22.5 kHz, 50% duty cycle, two phases active; unless otherwise noted****

Characteristics	Symbol	Conditions	Min.	Typ <sup>1</sup> .	Max.	Units
<b>Gate Drives, GLx (internal sink or lower switch stages)<sup>6</sup></b>						
Sink Current (pulsed)	$I_{\text{xL}}$	$V_{\text{DSL}} = 10\text{ V}$ , $T_J = 25^\circ\text{C}$	–	850	–	mA
		$V_{\text{DSL}} = 10\text{ V}$ , $T_J = 135^\circ\text{C}$	550	–	–	mA
Sink On Resistance	$r_{\text{DSL(on)}}$	$I_{\text{xL}} = 150\text{ mA}$ , $T_J = 25^\circ\text{C}$	1.8	–	6.0	$\Omega$
		$I_{\text{xL}} = 150\text{ mA}$ , $T_J = 135^\circ\text{C}$	3.0	–	7.5	$\Omega$
<b>Gate Drives, GHx, GLx (General)<sup>5,6</sup></b>						
Propagation Delay, Logic only	$t_{\text{pd}}$	Logic input to unloaded GHx, GLx	–	–	150	ns
Output Skew Time	$t_{\text{sk(o)}}$	Grouped by edge, phase-to-phase	–	–	50	ns
Dead Time (shoot-through prevention)	$t_{\text{dead}}$	Between GHx, GLx transitions of same phase	75	–	180	ns
<b>Sense Amplifier</b>						
Input Bias Current <sup>2</sup>	$I_{\text{bias}}$	CSP = CSN = 0 V	–180	–	–360	$\mu\text{A}$
Input Offset Current <sup>2</sup>	$I_{\text{IO}}$	CSP = CSN = 0 V	–	–	$\pm 35$	$\mu\text{A}$
Input Resistance	$r_i$	CSP with respect to GND	–	80	–	k $\Omega$
		CSN with respect to GND	–	4.0	–	k $\Omega$
Diff. Input Operating Voltage	$V_{\text{ID}}$	$V_{\text{ID}} = \text{CSP} - \text{CSN}$ , $-1.3\text{ V} < \text{CSP}, \text{N} < 4\text{ V}$	–	–	$\pm 200$	mV
Output Offset Voltage	$V_{\text{OO}}$	CSP = CSN = 0 V	77	250	450	mV
Output Offset Voltage Drift	$\Delta V_{\text{OO}}$	CSP = CSN = 0 V	–	100	–	$\mu\text{V}/^\circ\text{C}$
Input Common Mode Operating Range	$V_{\text{IC}}$	CSP = CSN	–1.5	–	4.0	V
Voltage Gain	$A_V$	$V_{\text{ID}} = 40$ to $200\text{ mV}$	18.6	19.2	19.8	V/V
Low Output Voltage Error	$E_V$	$V_{\text{ID}} = 0$ to $40\text{ mV}$ , $V_O = (19.2 \times V_{\text{ID}}) + V_O + E_V$	–	–	$\pm 25$	mV
DC Common Mode Attenuation	$A_{\text{VC}}$	CSP = CSN = $200\text{ mV}$	28	–	–	dB
Output Resistance	$r_O$	$V_{\text{CSOUT}} = 2.0\text{ V}$	–	8.0	–	$\Omega$
Output Dynamic Range	$V_{\text{CSOUT}}$	$I_{\text{CSOUT}} = -100\ \mu\text{A}$ at top rail, $100\ \mu\text{A}$ at bottom rail	0.075	–	$V_{\text{DD}} - 0.25$	V
Output Current, Sink	$I_{\text{sink}}$	$V_{\text{CSOUT}} = 2.5\text{ V}$	20	–	–	mA
Output Current, Source <sup>2</sup>	$I_{\text{source}}$	$V_{\text{CSOUT}} = 2.5\text{ V}$	–1.0	–	–	mA
VDD Supply Ripple Rejection	$\text{PSRR}_{\text{VDD}}$	CSP = CSN = GND, frequency = 0 to 1 MHz	20	–	–	dB
VREG Supply Ripple Rejection	$\text{PSRR}_{\text{VREG}}$	CSP = CSN = GND, frequency = 0 to 300 kHz	45	–	–	dB
Small Signal 3 dB Bandwidth	$\text{BW}_{\text{f3db}}$	10 mV input	–	1.6	–	MHz
AC Common Mode Attenuation	$A_{\text{VC(ac)}}$	$V_{\text{cm}} = 250\text{ mV(pp)}$ , frequency = 0 to 800 kHz	26	–	–	dB
Output Slew Rate (positive or negative)	SR	200 mV step input, measured at 10/90% points	10	–	–	V/ $\mu\text{s}$
<b>Fault Logic</b>						
VDD Undervoltage	$V_{\text{DD(uv)}}$	Decreasing $V_{\text{DD}}$	3.8	–	4.3	V
VDD Undervoltage Hysteresis	$\Delta V_{\text{DD(uv)}}$	$V_{\text{DD(recovery)}} - V_{\text{DD(uv)}}$	100	–	300	mV
OVSET Operating Voltage Range	$V_{\text{SET(ov)}}$		0	–	$V_{\text{DD}}$	V
OVSET Calibrated Voltage Range	$V_{\text{SET(ov)cal}}$		0	–	2.5	V
OVSET Input Current Range <sup>2</sup>	$I_{\text{SET(ov)}}$		–1.0	–	1.0	$\mu\text{A}$
VBAT Overvoltage Range	$V_{\text{BAT(ov)}}$	$0\text{ V} < V_{\text{SET(ov)}} < 2.5\text{ V}$	19.4	–	40	V
		Increasing $V_{\text{BAT}}$ , $V_{\text{SET(ov)}} = 0\text{ V}$	19.4	22.4	25.4	V
VBAT Overvoltage Hysteresis	$\Delta V_{\text{BAT(ov)}}$	Percent of $V_{\text{BAT(ov)}}$ value set by $V_{\text{SET(ov)}}$	9.0	–	15	%

Continued on the next page...

**ELECTRICAL CHARACTERISTICS (continued) at  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $V_{\text{BAT}} = 7$  to  $16$  V,  $V_{\text{DD}} = 4.75$  to  $5.25$  V,  $\text{ENABLE} = 22.5$  kHz, 50% duty cycle, two phases active; unless otherwise noted**

Characteristics	Symbol	Conditions	Min.	Typ <sup>1</sup> .	Max.	Units
VBAT Overvoltage Gain Constant	$K_{\text{BAT(ov)}}$	$V_{\text{BAT(ov)}} = (K_{\text{BAT(ov)}} \times V_{\text{SET(ov)}}) + V_{\text{BAT(ov)(0)}}$ ; $V_{\text{BAT(ov)(0)}}$ at $V_{\text{SET(ov)}} = 0$	–	12	–	V/V
VBAT Undervoltage	$V_{\text{BAT(uv)}}$	Decreasing $V_{\text{BAT}}$	5.0	5.25	5.5	V
VBAT Undervoltage Hysteresis	$V_{\text{BAT(uv)}}$	Percent of $V_{\text{BAT(uv)}}$	8.0	–	12	%
VREG Undervoltage	$V_{\text{REG(uv)}}$	Decreasing $V_{\text{REG}}$	9.9	–	11.1	V
VDSTH Input Range	$V_{\text{DSTH}}$		0.5	–	3.0	V
VDSTH Input Current	$I_{\text{DSTH}}$	$V_{\text{DSTH}} > 0.8$ V	40	–	100	$\mu\text{A}$
Short-to-Ground Threshold	$V_{\text{STG(th)}}$	With a high-side driver on, as $V_{\text{SX}}$ decreases, $V_{\text{DRAIN}} - V_{\text{SX}} > V_{\text{STG}}$ causes a fault	$V_{\text{DSTH}} - 0.3$	–	$V_{\text{DSTH}} + 0.2$	V
Short-to-Battery Threshold	$V_{\text{STB(th)}}$	With a low-side driver on, as $V_{\text{SX}}$ increases, $V_{\text{SX}} - V_{\text{LSS}} > V_{\text{STB}}$ causes a fault	$V_{\text{DSTH}} - 0.3$	–	$V_{\text{DSTH}} + 0.2$	V
VDRAIN-Open Bridge Operating Range	$V_{\text{DRAIN}}$	$7 \text{ V} < V_{\text{BAT}} < 40 \text{ V}$	–0.3	–	$V_{\text{BAT}} + 2.0$	V
VDRAIN-Open Bridge Current	$I_{\text{VDRAIN}}$	$7 \text{ V} < V_{\text{BAT}} < 40 \text{ V}$	0	–	1.0	mA
VDRAIN /Open Bridge Threshold Voltage	$V_{\text{BDGO(th)}}$	If $V_{\text{DRAIN}} < V_{\text{BDGO}}$ then a bridge fault occurs	1.0	–	3.0	V
Thermal Shut Down Temperature	$T_J$		160	170	180	$^\circ\text{C}$
Thermal Shutdown Hysteresis	$\Delta T_J$		7.0	10	13	$^\circ\text{C}$

<sup>1</sup>Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

<sup>2</sup>Negative current is defined as coming out of (sourcing) the specified device terminal.

<sup>3</sup>For  $V_{\text{BOOSTM}} < V_{\text{BOOST}} < 40$  V power dissipation in the  $V_{\text{REG}}$  LDO increases. Observe  $T_J < 150^\circ\text{C}$  limit.

<sup>4</sup>With  $V_{\text{BOOST}}$  decreasing, dropout voltage measured at  $V_{\text{REG}} = V_{\text{REG(ref)}} - 200$  mV where  $V_{\text{REG(ref)}} = V_{\text{REG}}$  at  $V_{\text{BOOST}} = 16$  V.

<sup>5</sup>For GHX:  $V_{\text{SDU}} = V_{\text{CX}} - V_{\text{GHx}}$ ,  $V_{\text{DSL}} = V_{\text{GHx}} - V_{\text{SX}}$ ,  $V_{\text{DSL(H)}} = V_{\text{CX}} - V_{\text{SDU}} - V_{\text{SX}}$ .

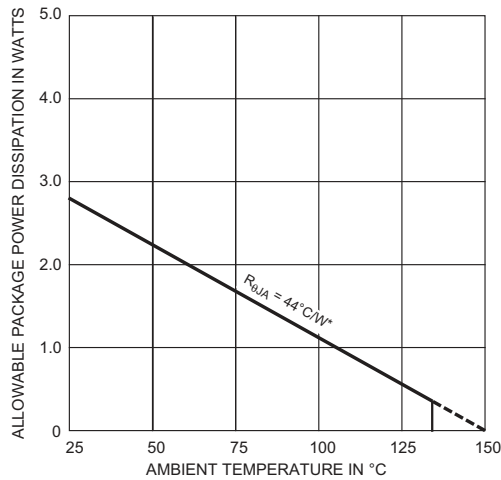
<sup>6</sup>For GLX:  $V_{\text{SDU}} = V_{\text{REG}} - V_{\text{GLx}}$ ,  $V_{\text{DSL}} = V_{\text{GLx}} - V_{\text{LSS}}$ ,  $V_{\text{DSL(H)}} = V_{\text{REG}} - V_{\text{SDU}} - V_{\text{LSS}}$ .

**Thermal Characteristics**

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB, based on JEDEC standard	44	$^{\circ}C/W$

\*Additional thermal information available on Allegro Web site.

**Power Dissipation versus Ambient Temperature**



## Terminal Descriptions

**AHI, BHI, and CHI.** Direct control of high-side gate outputs GHA, GHB, and GHC. Logic 1 drives the gate on. Logic 0 pulls the gate down, turning off the external power MOSFET. Internally pulled down when the terminal is open.

**ALO, BLO, and CLO.** Direct control of low-side gate outputs GHA, GHB, and GHC. Logic 1 drives the gate on. Logic 0 pulls the gate down, turning off the external power MOSFET. Internally pulled down when the terminal is open.

**BOOSTD.** Boost converter switch drain connection.

**BOOSTS.** Boost converter switch source connection.

**CA, CB, and CC.** High-side connection for the bootstrap capacitors, CBOOT<sub>x</sub>, positive supply for high-side gate drive. The bootstrap capacitor is charged to  $V_{REG}$  when the output S<sub>x</sub> terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for N-channel power MOSFETs.

**CSN.** Input for current-sense differential amplifier, on the inverting, negative side. Kelvin connection for the ground side of the current-sense resistor, RSENSE.

**CSOUT.** Amplifier output voltage proportional to the current sensed across an external low-value resistor placed in the ground side of the power MOSFET bridge.

**CSP.** Input for current-sense differential amplifier, on the non-inverting, positive side. Connected to the positive side of the sense resistor, RSENSE.

**ENABLE.** Logic 0 disables the gate control signals and switches off all the gate drivers (low) causing a coast condition. Can be used in conjunction with the gate inputs to PWM (pulse wave modulate) the load current. Internally pulled down when the terminal is open.

**FAULT.** Diagnostic logic output signal. When low, indicates that one or more fault conditions have occurred.

**GHA, GHB, and GHC.** High-side gate drive outputs for N-channel MOSFET drivers. External series gate resistors can control the slew rate seen at the power driver gate, thereby controlling the  $di/dt$  and  $dv/dt$  of S<sub>x</sub> outputs.

**GLA, GLB, and GLC.** Low-side gate drive outputs for external, N-channel MOSFET drivers. External series gate resistors can control slew rate.

**GND.** Ground, or negative, side of VDD and VBAT supplies.

**LSS.** Low-side gate driver return. Connects to the common sources on the low sides of the power MOSFET bridge.

**OVFLT.** Logic 1 indicates that the  $V_{BAT}$  level exceeded the VBAT overvoltage trip point set by the OVSET level. It will recover after exceeding a hysteresis below that maximum value. Normally, it has a high-impedance state. If OVFLT and UVFLT are both in high-impedance state; then, at least, a thermal shutdown or VDD undervoltage has occurred.

**OVSET.** A positive dc level that controls the VBAT overvoltage trip point. Usually, set by a precision resistor divider network between VDD and GND, but can be held grounded for a preset value. When this terminal is open, it sets an unspecified but high overvoltage trip point.

**SA, SB, and SC.** Directly connected to the motor terminals, these terminals sense the voltages switched across the load and are connected to the negative side of the bootstrap capacitors, CBOOT<sub>x</sub>. Also, are the negative supply connection for the floating high-side drivers.

**UVFLT.** Logic 1 indicates that the  $V_{BAT}$  level is below its minimum value. It will recover after exceeding a hysteresis above that minimum value. Has a high-impedance state. If UVFLT and OVFLT are both in high-impedance state; then, at least, a thermal shutdown or VDD undervoltage has occurred.

**VBAT.** Battery voltage. Positive input. usually connected to the motor voltage supply.

**VBOOST.** Boost converter output, 16 V nominal, is also the input to the regulator for VREG. Has internal boost-current and boost-voltage control loops. In high-voltage systems is approximately one diode drop below  $V_{BAT}$ .

**VDD.** Logic supply, +5 V nominal.

**VDRAIN.** Kelvin connection for drain-to-source voltage monitor. Connected to the high-side drains of the MOSFET bridge. High impedance when this terminal is open, and registers as a short-to-ground fault on all motor phases.

**VDSTH.** A positive dc level that sets the drain-to-source monitor threshold voltage. Internally pulled down when this terminal is open.

**VREG.** High-side gate driver supply, 13.5 V nominal. Has low-voltage dropout (LDO) feature.



## Functional Description

**Motor Lead Protection.** A fault detection circuit monitors the voltage across the drain-to-source of the external MOSFETs. A fault is asserted low on the output terminal, **FAULT**, if the drain-to-source voltage of any MOSFET that is instructed to turn on is greater than the voltage applied to the  $V_{DSTH}$  input terminal. When a high-side switch is turned on, the voltage from  $V_{DRAIN}$  to the appropriate motor phase output,  $V_{SX}$ , is examined. If the motor lead is shorted to ground before the high-side is turned on, the measured voltage will exceed the threshold and the **FAULT** terminal will go low. Similarly, when a low-side MOSFET is turned on, the differential voltage between the motor phase (drain) and the LSS terminal (source) is monitored.  $V_{DSTH}$  is set by a resistor divider to  $V_{DD}$ .

The  $V_{DRAIN}$  is intended to be a Kelvin connection for the high-side, drain-to-source monitor circuit. Voltage drops across the power bus are eliminated by connecting an isolated PCB trace from the  $V_{DRAIN}$  terminal to the drain of the MOSFET bridge. This allows improved accuracy in setting the  $V_{DSTH}$  threshold voltage. The low-side, drain-to-source monitor uses the LSS terminal, rather than  $V_{DRAIN}$ , for comparison with  $V_{DSTH}$ . The A3935 just reports these motor faults.

**Fault Outputs.** Transient faults on any of the fault outputs are to be expected during switching, and will not disable the gate drive outputs. External circuitry or controller logic must determine if the faults represent a hazardous condition.

**FAULT.** This terminal will go active low when any of the following conditions occur:

- $V_{BAT}$  overvoltage
- $V_{BAT}$  undervoltage
- $V_{REG}$  undervoltage
- Motor lead short-to-ground
- Motor lead short-to-supply or short-to-battery
- Bridge (or  $V_{DRAIN}$ ) open
- $V_{DD}$  undervoltage
- Thermal shut down

**OVFLT.** Asserts high when a  $V_{BAT}$  overvoltage fault occurs and resets low after a recovery hysteresis. It has a high-impedance state when a thermal shutdown or  $V_{DD}$  undervoltage occurs. The voltage at the OVSET terminal,  $V_{OVSET}$ , controls the  $V_{BAT}$  overvoltage set point  $V_{BAT(ov)}$ , as follows:

$$V_{BAT(ov)} = (A_{BAT(ov)} \times V_{SET(ov)}) + V_{BAT(ov)(0)}$$

where  $A_{BAT(ov)}$  is the gain (12) and  $V_{BAT(ov)(0)}$  is the value of  $V_{BAT(ov)}$  when  $V_{SET(ov)} = 0$  ( $V_{BAT(ov)} \approx 22.4$ ). For the above formula to be valid, all variables must be in range and below the maximum operating specification.

**UVFLT.** Asserts high when a  $V_{BAT}$  undervoltage fault occurs and resets low after exceeding a recovery hysteresis. It has a high-impedance state when a thermal shut down or  $V_{DD}$  undervoltage occurs. OVFLT and UVFLT are mutually exclusive by definition.

**Current Sensing.** A current-sense amplifier is provided to allow system monitoring of the load current. The differential amplifier inputs are intended to be Kelvin-connected across a low-value sense resistor or current shunt. The output voltage is represented by:

$$V_{CSOUT} = (I_{LOAD} \times A_V \times R_{SENSE}) + V_{OS}$$

where  $V_{OS}$  is the output voltage calibrated at zero load current and  $A_V$  is the differential amplifier gain of about 19.2. If either the CSP or CSN pin is open, the CSOUT pin will go to its maximum positive level.

**Shut Down.** If a fault occurs because of excessive junction temperature or undervoltage on  $V_{DD}$  or  $V_{BAT}$ , all gate driver outputs are driven low until the fault condition is removed. In addition, the boost supply switch and VREG are turned off until those undervoltages and junction temperatures recover.

**Boost Supply.**  $V_{BOOST}$  is controlled by an inner current-control loop, and by an outer voltage-feedback loop. The current-control loop turns off the boost switch for 5  $\mu$ s whenever the voltage across the boost current-sense resistor exceeds 500 mV. A diode reverse-recovery current flows through the sense resistor whenever the boost switch turns on, which could result in turning off the switch again if not for the blanking-time circuit. Adjustment of this external sense resistor determines the maximum current in the inductor. Whenever  $V_{BOOST}$  exceeds the predefined threshold, 16 V nominal the boost switch is inhibited.

Input Logic Table

Input			Output		Mode of Operation
ENABLE	xLO	xHI	GLx	GHx	
0	Don't Care	Don't Care	0	0	All gate drive outputs low
1	0	0	0	0	Both gate drive outputs low
1	0	1	0	1	High-side on
1	1	0	1	0	Low-side on
1	1	1	0	0	XOR circuitry prevents shoot-through

Fault Response Table

Operating Conditions		Fault Output			Regulator State		Driver Output	
Fault Mode	ENABLE	FAULT	OVFLT	UVFLT	Boost	V <sub>REG</sub>	GHx	GLx
No Fault	Don't Care	1	0	0	ON	ON	a	a
Short-to-Battery	1 <sup>b</sup>	0	0	0	ON	ON	a	a
Short-to-Ground	1 <sup>c</sup>	0	0	0	ON	ON	a	a
Bridge (VDRAIN) Fault	1 <sup>d</sup>	0	0	0	ON	ON	a	a
VREG Undervoltage	Don't Care	0	0	0	ON	ON	a	a
VBAT Overvoltage	Don't Care	0	1	0	OFF <sup>e</sup>	ON	a	a
VBAT Undervoltage <sup>f</sup>	Don't Care	0	0	1	OFF	OFF	0	0
VDD Undervoltage <sup>f</sup>	Don't Care	0	High Z	High Z	OFF	OFF	0	0
Thermal Shut Down <sup>f</sup>	Don't Care	0	High Z	High Z	OFF	OFF	0	0

<sup>a</sup>Determined by input states: xLO, xHI, and ENABLE. See Input Logic table.

<sup>b</sup>Short-to-battery can only be detected when the corresponding GLx = 1. This fault is not detected when ENABLE = 0.

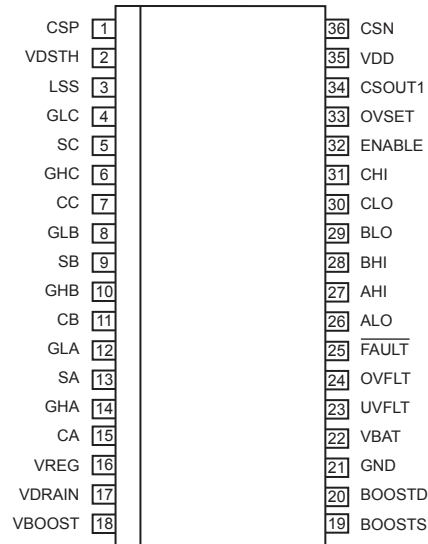
<sup>c</sup>Short-to-ground can only be detected when the corresponding GHx = 1. This fault is not detected when ENABLE = 0.

<sup>d</sup>Bridge fault appears as a short-to-ground fault on all motor phases. This fault is not detected when ENABLE = 0.

<sup>e</sup>Off only because  $V_{BOOST} \approx V_{BAT}$ , which is above the voltage threshold of the Boost regulator voltage control loop.

<sup>f</sup>These faults are not only reported, but also action is taken by the internal logic to protect the A3935 and the system.

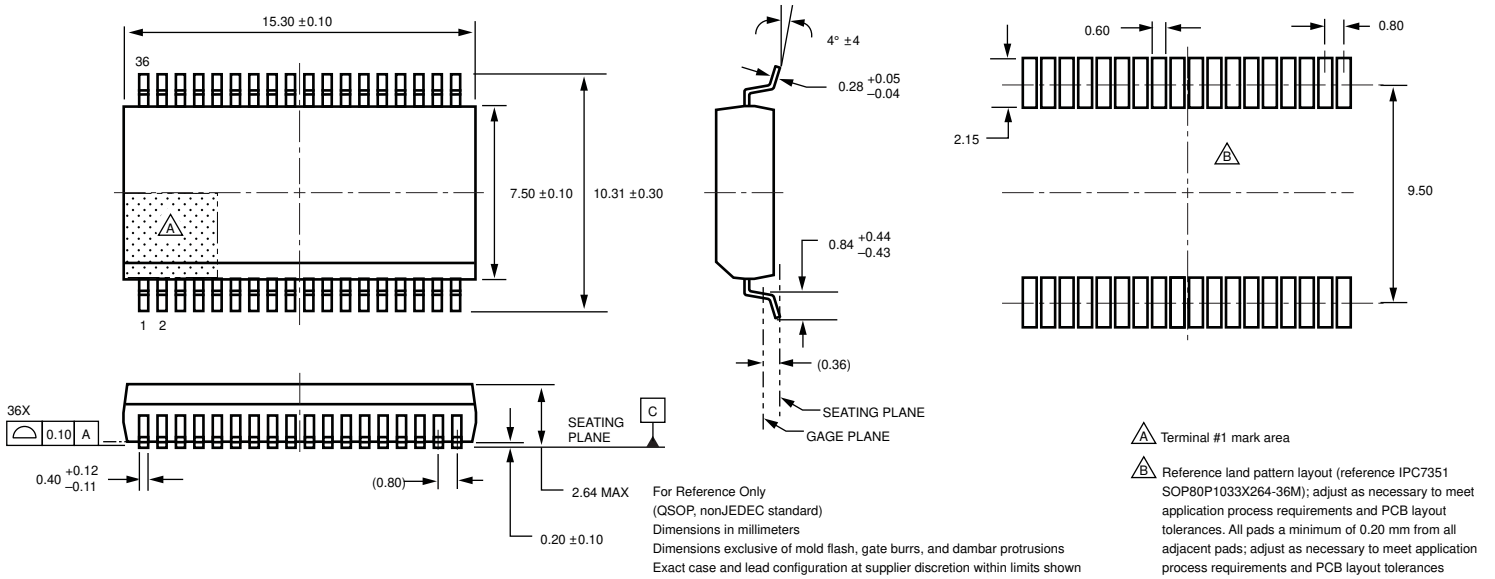
### Pin-out Diagram



### Terminal List

Number	Name	Function	Number	Name	Function
1	CSP	Current-sense input, positive-side	19	BOOSTS	Boost switch, source
2	VDSTH	DC input, drain-to-source monitor threshold voltage	20	BOOSTD	Boost switch, drain
3	LSS	Gate-drive source return, low-side	21	GND	Ground, dc supply returns, negative
4	GLC	Gate-drive C output, low-side	22	VBAT	Battery supply, positive
5	SC	Load phase C input	23	UVFLT	VBAT undervoltage fault output
6	GHC	Gate-drive C output, high-side	24	OVFLT	VBAT overvoltage fault output
7	CC	Bootstrap capacitor C	25	FAULT	Active-low fault output, primary
8	GLB	Gate-drive B output, low-side	26	ALO	Gate control input A, low-side
9	SB	Load phase B input	27	AHI	Gate control input A, high-side
10	GHB	Gate-drive B output, high-side	28	BHI	Gate control input B, high-side
11	CB	Bootstrap capacitor B	29	BLO	Gate control input B, low-side
12	GLA	Gate-drive A output, low-side	30	CLO	Gate control input C, low-side
13	SA	Load phase A input	31	CHI	Gate control input C, high-side
14	GHA	Gate-drive A output, high-side	32	ENABLE	Gate output enable
15	CA	Bootstrap capacitor A	33	OVSET	DC input, overvoltage threshold setting for VBAT
16	VREG	Gate drive supply, positive	34	CSOUT	Current-sense amplifier output
17	VDRAIN	Kelvin connection to MOSFET high-side drains	35	VDD	Logic supply, nominally +5 V
18	VBOOST	Boost supply output	36	CSN	Current-sense input, negative-side

Package LQ, 36-pin QSOP



**Revision History**

Revision	Revision Date	Description of Revision
Rev. J	October 31, 2011	Update product availability

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