36 V, Low Noise, Zero Drift Op Amp

Data Sheet

ADA4523-1

FEATURES

- Supply voltage range: 4.5 V to 36 V
- Offset voltage: ±4 µV maximum at 5 V
- Offset voltage drift: 0.01 µV/°C maximum at 5 V
- Input noise
  - Voltage: 88 nV p-p from 0.1 Hz to 10 Hz typical
  - Spectral density voltage: 4.2 nV/√Hz typical at 1 kHz
- Rail-to-rail output
- Unity-gain stable
- GBP: 5 MHz typical
- Slew rate: 1.8 V/µs typical falling
- PSRR: 168 dB typical at V_S = 4.5 V to 36 V
- Open-loop voltage gain: 160 dB typical at V_{OUT} = −14.75 V to +14.75 V, R_L = 10 kΩ, V_S = 30 V
- CMRR: 160 dB typical at V_{CM} = −15.1 V to +13.5 V, V_S = 30 V
- Integrated EMI filters
- Shutdown mode
- Ground sense
- Available in 8-lead SOIC, 8-lead MSOP, and 8-lead LFCSP

APPLICATIONS

- High resolution data acquisition
- Reference buffering
- Test and measurement
- Electronic scales
- Thermocouple amplifiers
- Strain gages
- Low-side current sense

GENERAL DESCRIPTION

The ADA4523-1 is a high voltage, low noise, zero drift op amp that offers precision dc performance over a wide supply range of 4.5 V to 36 V. Offset voltage and 1/f noise are suppressed, allowing this op amp to achieve a maximum offset voltage of ±4 µV and a 0.1 Hz to 10 Hz input noise voltage of 88 nV p-p typical. The self calibrating circuitry of the ADA4523-1 results in low offset voltage drift with temperature (0.01 µV/°C maximum) and zero drift over time. Additionally, the ADA4523-1 uses on-chip filtering to achieve high immunity to electromagnetic interference (EMI).

Wide supply range, combined with low noise, low offset, 168 dB power supply rejection ratio (PSRR), and 160 dB common-mode rejection ratio (CMRR), make the ADA4523-1 well suited for high dynamic range test, measurement, and instrumentation systems.

TYPICAL APPLICATION DIAGRAM

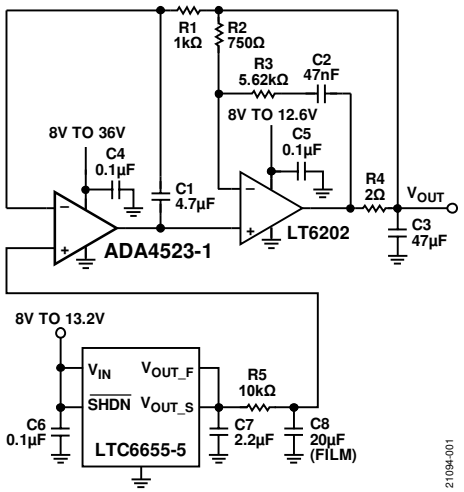

Figure 1. Precision Filtering Voltage Reference Buffer

The ADA4523-1 provides a rail-to-rail output swing and an input common-mode range that includes the V^- rail (V^- – 0.1 V to V^+ – 1.5 V).

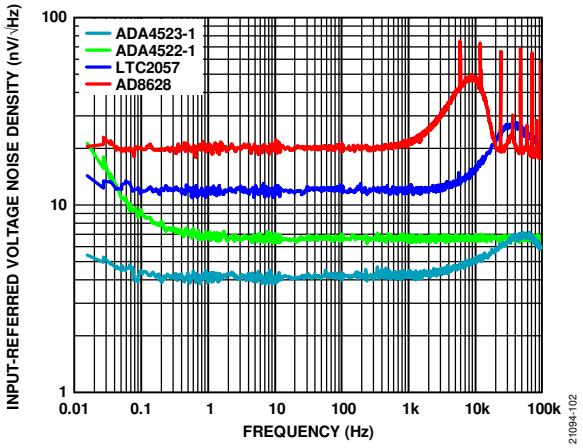

Figure 2. Input-Referred Voltage Noise Density vs. Frequency, Zero Drift Amplifier Family Comparison

COMPANION PRODUCTS

- Voltage References: LTC6655 and ADR4525
- Low Noise High Speed Amplifier: LT6202
- ADC: LTC2500-32
- Low Noise, Low Dropout Regulators: LT3093 and LT3042

Additional companion products for the ADA4523-1 can be found in the Related Products section.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

4/2020—Revision 0: Initial Version

SPECIFICATIONS

5 V ELECTRICAL CHARACTERISTICS

T_A = 25°C, supply voltage (V_S) = ±2.5 V (V^+ = +2.5 V and V^- = −2.5 V), and common-mode voltage (V_{CM}) = output voltage (V_{OUT}) = 0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}			±0.5	±4	µV
		−40°C ≤ T_A ≤ +125°C			±5	µV
Offset Voltage Drift[1]	TCV_{OS}	−40°C ≤ T_A ≤ +125°C			0.01	µV/°C
Input Bias Current[2]	I_B			100	300	pA
		−40°C ≤ T_A ≤ +125°C			600	pA
Input Offset Current[2]	I_{OS}			200	600	pA
		−40°C ≤ T_A ≤ +125°C			800	pA
Input Voltage Range	IVR	−40°C ≤ T_A ≤ +125°C	−2.6		+1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.6 V to +1 V	124	146		dB
		V_{CM} = −2.5 V to +1 V, −40°C ≤ T_A ≤ +125°C	124			
Input Resistance	R_{IN}					
Differential				47		kΩ
Common Mode				100		GΩ
Input Capacitance	C_{IN}					
Differential				13		pF
Common Mode				20		pF
Open-Loop Voltage Gain	A_V	V_{OUT} = −2.3 V to +2.3 V, load resistance (R_L) = 1 kΩ	125	150		dB
		−40°C ≤ T_A ≤ +125°C	125			dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing Low	V_{OL}	V_{OL} = V_{OUT} − V^-				
		No load		12	20	mV
		No load, −40°C ≤ T_A ≤ +125°C			30	mV
		Sink current (I_{SINK}) = 1 mA		52	75	mV
		I_{SINK} = 1 mA, −40°C ≤ T_A ≤ +125°C			100	mV
		I_{SINK} = 5 mA		215	300	mV
		I_{SINK} = 5 mA, −40°C ≤ T_A ≤ +125°C			400	mV
Output Voltage Swing High	V_{OH}	V_{OH} = V^+ − V_{OUT}				
		No load		1.3	10	mV
		No load, −40°C ≤ T_A ≤ +125°C			20	mV
		Source current (I_{SOURCE}) = 1 mA		22	40	mV
		I_{SOURCE} = 1 mA, −40°C ≤ T_A ≤ +125°C			55	mV
		I_{SOURCE} = 5 mA		106	150	mV
		I_{SOURCE} = 5 mA, −40°C ≤ T_A ≤ +125°C			200	mV
Short-Circuit Current	I_{SC}	Sourcing	+25	+36		mA
		Sinking	−25	−30		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 36 V	140	168		dB
		−40°C ≤ T_A ≤ +125°C	140			dB
Supply Current per Amplifier	I_S			4.5	4.8	mA
		−40°C ≤ T_A ≤ +125°C			6	mA
Shutdown Amplifier Current				4.5	6	µA
		−40°C ≤ T_A ≤ +125°C			7.5	µA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			5		MHz
Slew Rate						
Rising	SR_{RISE}	G = −1, R_L = 10 kΩ		1.85		V/µs
Falling	SR_{FALL}	G = −1, R_L = 10 kΩ		1.8		V/µs
Internal Chopping Frequency	f_C			330		kHz
INPUT NOISE						
Spectral Density						
Current	i_n	1 kHz		1		pA/√Hz
Voltage	e_n	1 kHz		4.2		nV/√Hz
Voltage	$e_{n\ P-P}$	0.1 Hz to 10 Hz		88		nV p-p
	$e_{n\ RMS}$	0.1 Hz to 10 Hz		13.3		nV rms
SHUTDOWN CHARACTERISTICS		−40°C ≤ T_A ≤ +125°C				
Shutdown Threshold ($\overline{SD}$ − SDCOM)						
Low	V_{SDL}				0.8	V
High	V_{SDH}		2			V
SDCOM Voltage Range			−2.5		+0.15	V
$\overline{SD}$ Current	$I_{\overline{SD}}$	$V_{\overline{SD}} - V_{SDCOM}$ = 0 V	−1.5	−0.5		µA
SDCOM Current	I_{SDCOM}	$V_{\overline{SD}} - V_{SDCOM}$ = 0 V		3	6	µA

[1] These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing. V_{OS} is measured to a limit determined by the test equipment capabilities.
[2] The input bias current and input offset current are measured using an equivalent source impedance of 100 MΩ || 51 pF.

30 V ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15 V (V^+ = +15 V and V^- = −15 V), and V_{CM} = V_{OUT} = 0 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT AND DC CHARACTERISTICS						
Offset Voltage[1]	V_{OS}			±0.5	±5	µV
		−40°C ≤ T_A ≤ +125°C			±7	µV
Offset Voltage Drift[1]	TCV_{OS}	−40°C ≤ T_A ≤ +125°C			±0.02	µV/°C
Input Bias Current[2]	I_B			125	300	pA
		−40°C ≤ T_A ≤ +125°C			600	pA
Input Offset Current[2]	I_{OS}			250	600	pA
		−40°C ≤ T_A ≤ +125°C			800	pA
Input Voltage Range	IVR	−40°C ≤ T_A ≤ +125°C	−15.1		+13.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −15.1 V to +13.5 V	140	160		dB
		V_{CM} = −15 V to +13.5 V, −40°C ≤ T_A ≤ +125°C	140			
Input Resistance	R_{IN}					
Differential				47		kΩ
Common Mode				100		GΩ
Input Capacitance	C_{IN}					
Differential				13		pF
Common Mode				20		pF
Open-Loop Voltage Gain	A_V	V_{OUT} = −14.75 V to +14.75 V, R_L = 10 kΩ	140	160		dB
		−40°C ≤ T_A ≤ +125°C	140			dB
OUTPUT CHARACTERISTICS						
Output Low Voltage Swing	V_{OL}	V_{OL} = V_{OUT} − V^-				
		No load		12	20	mV
		No load, −40°C ≤ T_A ≤ +125°C			30	mV
		I_{SINK} = 1 mA		50	75	mV
		I_{SINK} = 1 mA, −40°C ≤ T_A ≤ +125°C			100	mV
		I_{SINK} = 5 mA		215	300	mV
		I_{SINK} = 5 mA, −40°C ≤ T_A ≤ +125°C			400	mV
Output High Voltage Swing	V_{OH}	V_{OH} = V^+ − V_{OUT}				
		No load		2.5	10	mV
		No load, −40°C ≤ T_A ≤ +125°C			20	mV
		I_{SOURCE} = 1 mA		25	40	mV
		I_{SOURCE} = 1 mA, −40°C ≤ T_A ≤ +125°C			55	mV
		I_{SOURCE} = 5 mA		110	150	mV
		I_{SOURCE} = 5 mA, −40°C ≤ T_A ≤ +125°C			200	mV
Short-Circuit Current	I_{SC}	Sourcing	+25/	+36/		mA
		Sinking	−25	−30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 36 V	140	168		dB
		−40°C ≤ T_A ≤ +125°C	140			dB
Supply Current per Amplifier	Is			4.5	5	mA
		−40°C ≤ T_A ≤ +125°C			6	mA
Shutdown Amplifier Current				10	15	µA
		−40°C ≤ T_A ≤ +125°C			20	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Gain Bandwidth Product				5		MHz
Slew Rate						
Rising	SR_{RISE}	A_V = −1, R_L = 10 kΩ		1.85		V/µs
Falling	SR_{FALL}	A_V = −1, R_L = 10 kΩ		1.8		V/µs
Internal Chopping Frequency	f_C			330		kHz
EMI Rejection Ratio +IN	EMIRR	Input voltage (V_{IN}) = −10 dBm peak, frequency (f) = 400 MHz		80		dB
		V_{IN} = −10 dBm peak, f = 900 MHz		140		dB
		V_{IN} = −10 dBm peak, f = 1800 MHz		90		dB
		V_{IN} = −10 dBm peak, f = 2400 MHz		94		dB
INPUT NOISE						
Spectral Density						
Current	i_n	1 kHz		1		pA/√Hz
Voltage	e_n	1 kHz		4.2		nV/√Hz
Voltage	$e_{n\ P-P}$	0.1 Hz to 10 Hz		88		nV p-p
	$e_{n\ RMS}$	0.1 Hz to 10 Hz		13.3		nV rms
SHUTDOWN CHARACTERISTICS		−40°C ≤ T_A ≤ +125°C				
Shutdown Threshold ($\overline{SD}$ – SDCOM)						
Low	V_{SDL}				0.8	V
High	V_{SDH}		2			V
SDCOM Voltage Range			−15		+12.65	V
$\overline{SD}$ Current	$I_{\overline{SD}}$	$V_{\overline{SD}}$ – V_{SDCOM} = 0 V	−1.5	−0.5		µA
SDCOM Current	I_{SDCOM}	$V_{\overline{SD}}$ – V_{SDCOM} = 0 V		3	6	µA

[1] These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing. V_{OS} is measured to a limit determined by the test equipment capabilities.
[2] The input bias current and input offset current are measured using an equivalent source impedance of 100 MΩ || 51 pF.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V^+ to V^-	40 V
Input Voltage	
+IN and −IN[1]	V^- − 0.3 V to V^+ + 0.3 V
$\overline{SD}$ and SDCOM	V^- − 0.3 V to V^+ + 0.3 V
Input Current	
+IN and −IN[1]	±10 mA
$\overline{SD}$ and SDCOM	±10 mA
Output Short-Circuit Duration[2]	Indefinite
Temperature Range	
Operating	−40°C to +125°C
Junction	−65°C to +150°C
Storage	−65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	4.0 kV
Field Induced Charge Device Model (FICDM)[3]	2.0 kV

[1] Limit the input current to less than 10 mA. The input voltage must not exceed 300 mV beyond the power supply. These limits are set by the ESD protection structures at the input pins.

[2] A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

[3] JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient, thermal resistance.

θ_{JC} is the junction to case, thermal resistance. For θ_{JC} on the exposed pad package, such as CP-8-29, heat sink applies to the package bottom exposed pad only.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
R-8	120	39	°C/W
RM-8	163	40	°C/W
CP-8-29	43	5.5	°C/W

[1] Measured with JEDEC 4-layer high effective thermal conductivity board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

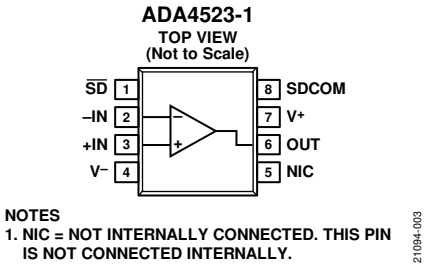


Figure 3. 8-Lead SOIC_N Pin Configuration

Table 5. 8-Lead SOIC_N Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{SD}$	Shutdown Control Pin.
2	–IN	Inverting Input of the Amplifier.
3	+IN	Noninverting Input of the Amplifier.
4	V^-	Negative Power Supply.
5	NIC	Not Internally Connected. This pin is not connected internally.
6	OUT	Amplifier Output.
7	V^+	Positive Power Supply.
8	SDCOM	Reference Voltage for $\overline{SD}$.

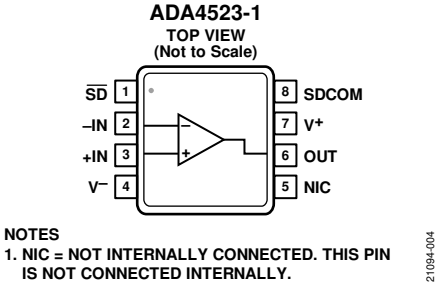


Figure 4. 8-Lead MSOP Pin Configuration

Table 6. 8-Lead MSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{SD}$	Shutdown Control Pin.
2	–IN	Inverting Input of the Amplifier.
3	+IN	Noninverting Input of the Amplifier.
4	V^-	Negative Power Supply.
5	NIC	Not Internally Connected. This pin is not connected internally.
6	OUT	Amplifier Output.
7	V^+	Positive Power Supply.
8	SDCOM	Reference Voltage for $\overline{SD}$.

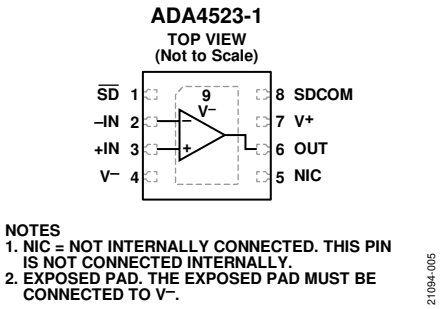


Figure 5. 8-Lead LFCSP Pin Configuration

Table 7. 8-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{SD}$	Shutdown Control Pin.
2	–IN	Inverting Input of the Amplifier.
3	+IN	Noninverting Input of the Amplifier.
4	V^-	Negative Power Supply.
5	NIC	Not Internally Connected. This pin is not connected internally.
6	OUT	Amplifier Output.
7	V^+	Positive Power Supply.
8	SDCOM	Reference Voltage for $\overline{SD}$.
9	EPAD	Exposed Pad. The exposed pad must be connected to V^-.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

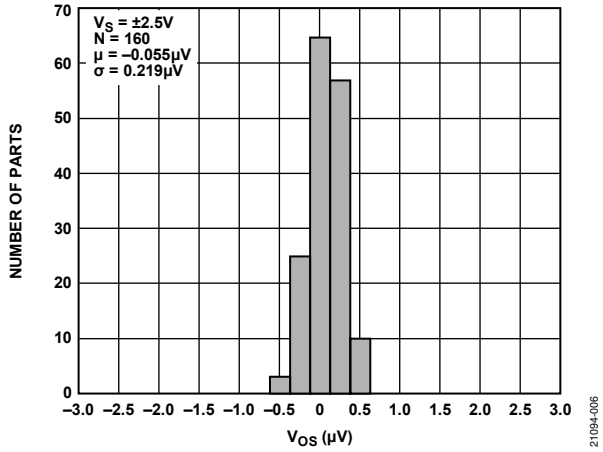


Figure 6. Input Offset Voltage (V_{OS}) Distribution, V_S = ±2.5 V
(N Is Total Number of Amplifiers, μ is Mean, and σ is Standard Deviation)

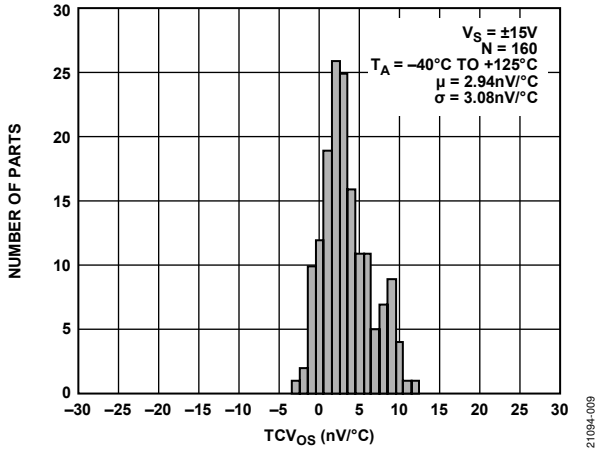


Figure 9. TCV_{OS} Distribution, V_S = ±15 V

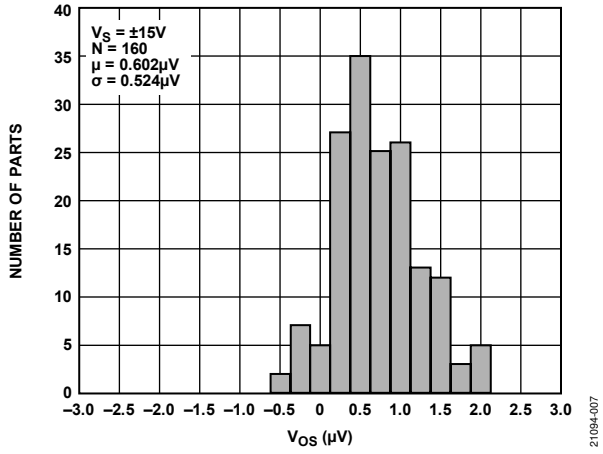


Figure 7. V_{OS} Distribution, V_S = ±15 V

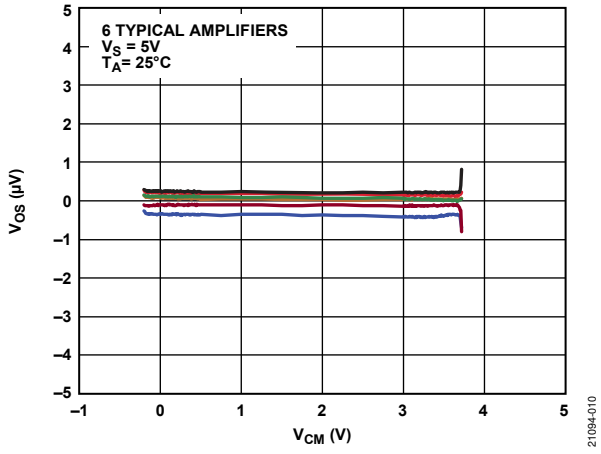


Figure 10. V_{OS} vs. V_{CM}, V_S = 5 V

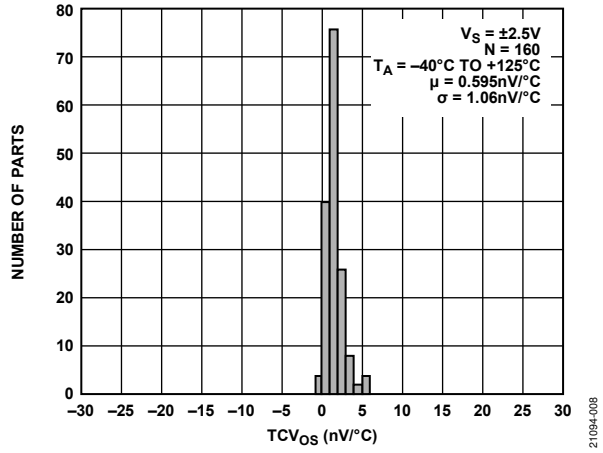


Figure 8. Input Offset Drift (TCV_{OS}) Distribution, V_S = ±2.5 V

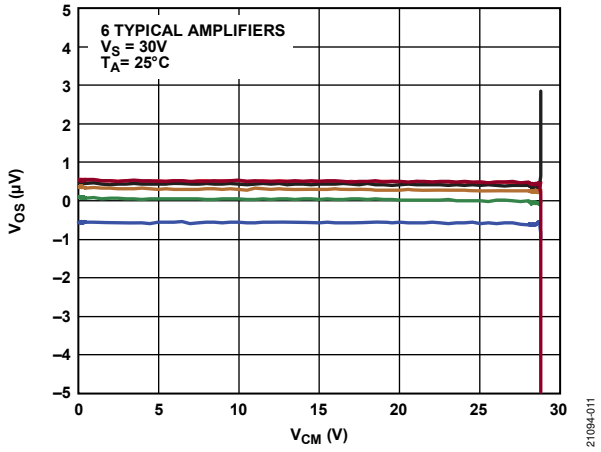


Figure 11. V_{OS} vs. V_{CM}, V_S = 30 V

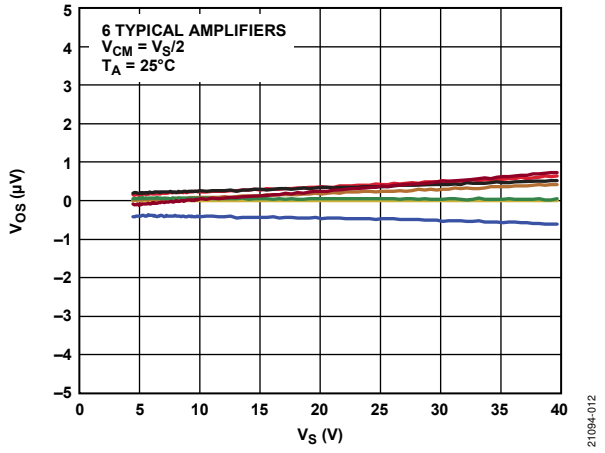


Figure 12. V_{OS} vs. V_S

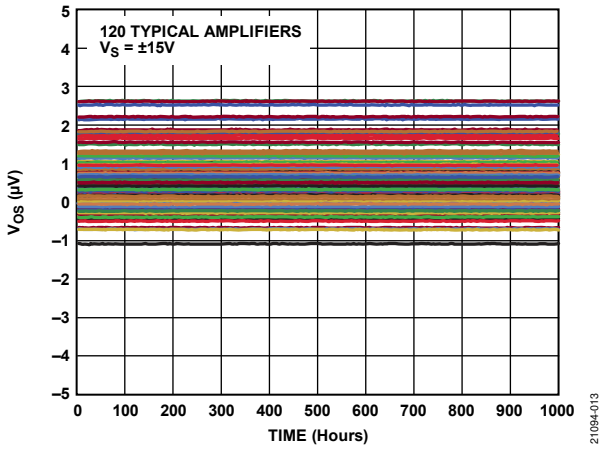


Figure 13. V_{OS} Long Term Drift

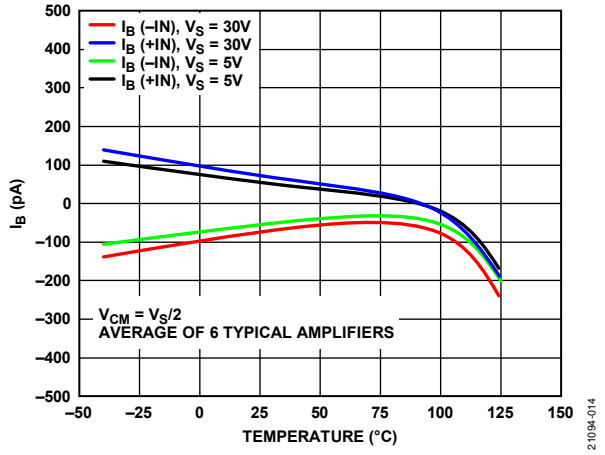


Figure 14. I_B vs. Temperature

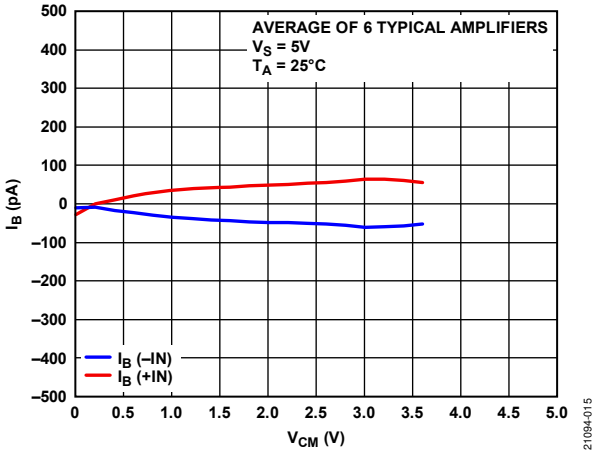


Figure 15. I_B vs. V_{CM}, V_S = 5 V

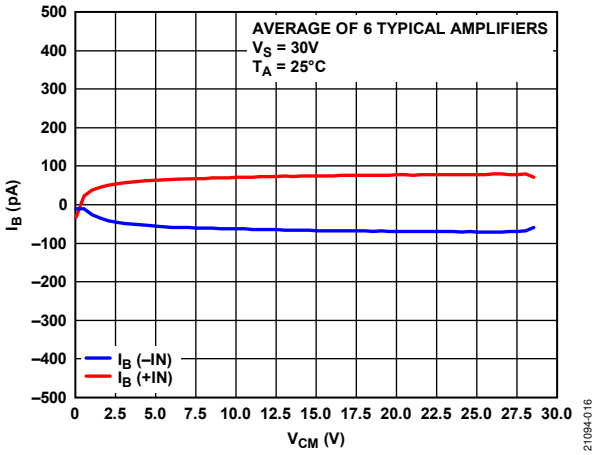


Figure 16. I_B vs. V_{CM}, V_S = 30 V

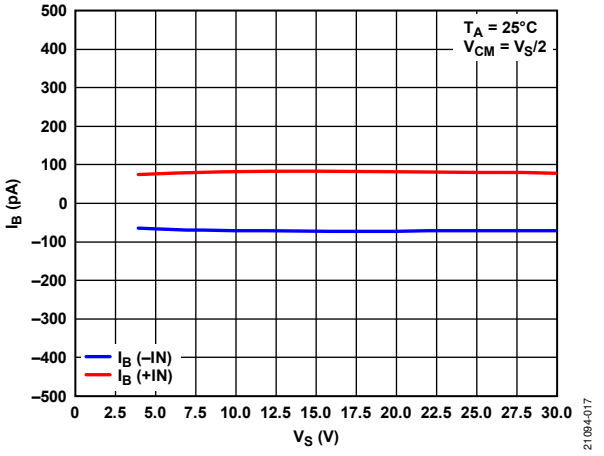


Figure 17. I_B vs. V_S

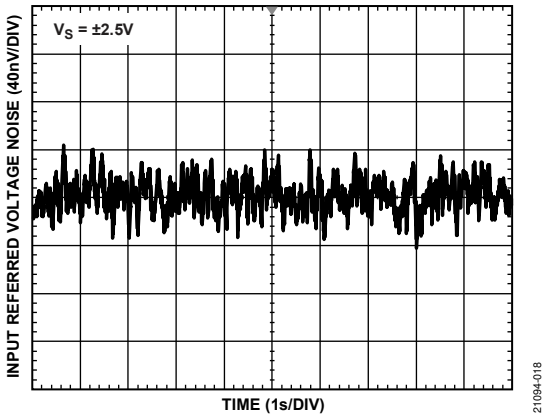


Figure 18. 0.1 Hz to 10 Hz, Input Referred Voltage Noise, V_S = ±2.5 V

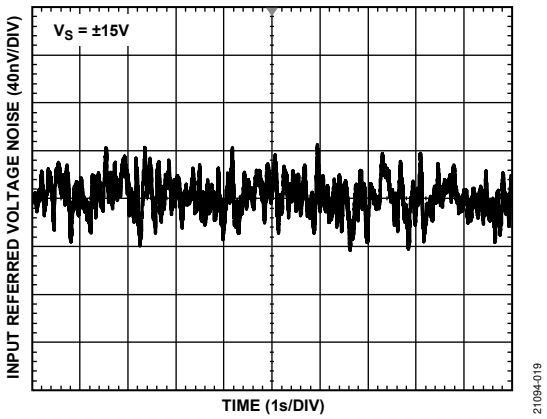


Figure 19. 0.1 Hz to 10 Hz, Input Referred Voltage Noise, V_S = ±15 V

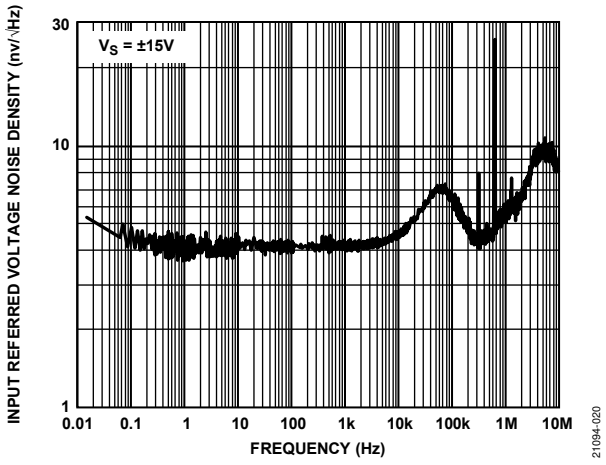


Figure 20. Input Referred Voltage Noise Density vs. Frequency, V_S = ±15 V

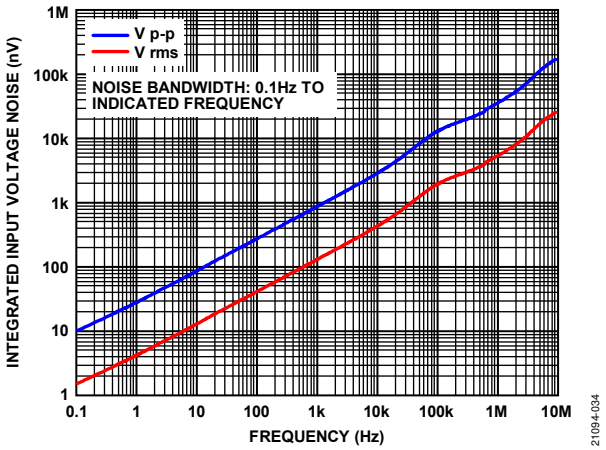


Figure 21. Integrated Input Voltage Noise vs. Frequency

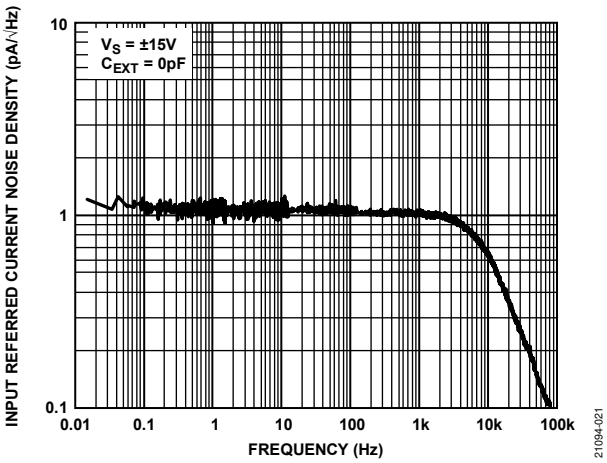


Figure 22. Input Referred Current Noise Density vs. Frequency (C_{EXT} Is the External Capacitance)

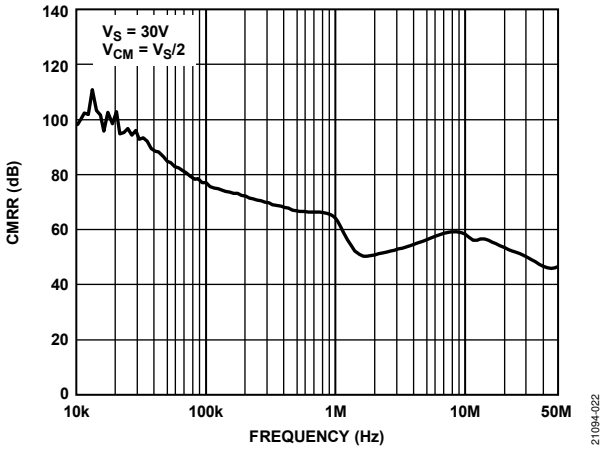


Figure 23. CMRR vs. Frequency

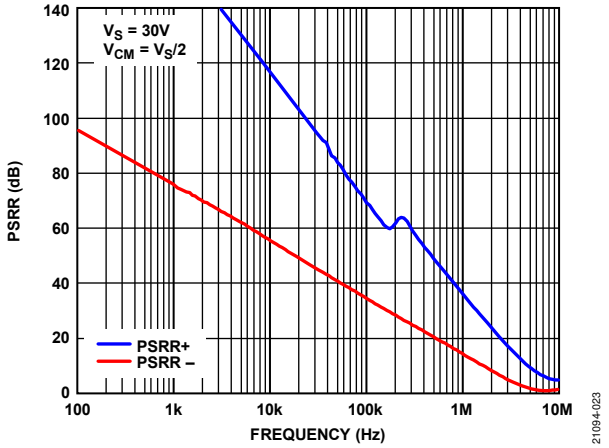


Figure 24. PSRR vs. Frequency

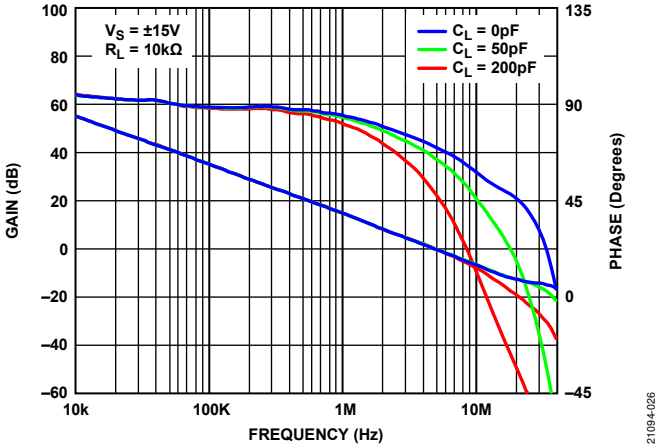


Figure 27. Gain and Phase vs. Frequency, V_S = ±15 V

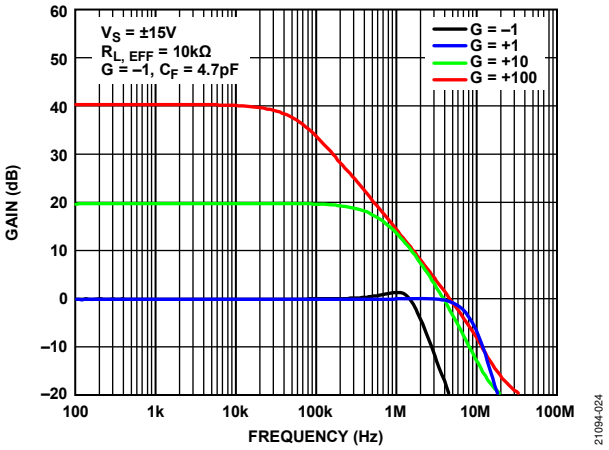


Figure 25. Closed-Loop Gain vs. Frequency (C_F Is the Feedback Capacitor and $R_{L, EFF}$ Is the Effective Load Resistance)

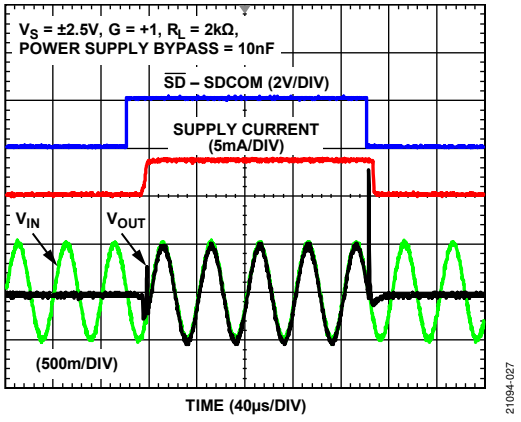


Figure 28. Shutdown Transient with Sinusoid Input, V_S = ±2.5 V

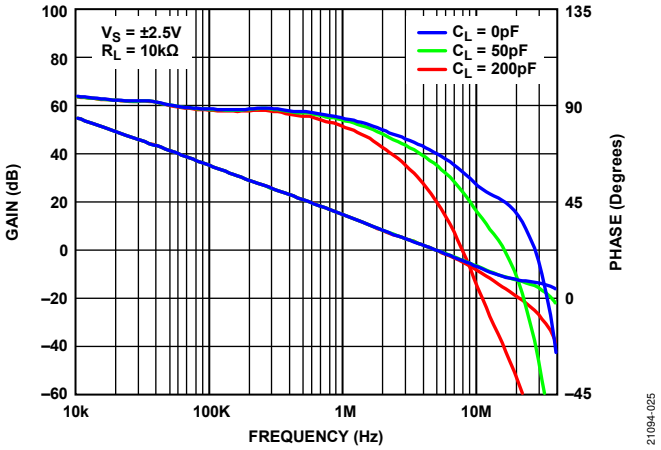


Figure 26. Gain and Phase vs. Frequency, V_S = ±2.5 V (C_L Is the Load Capacitance)

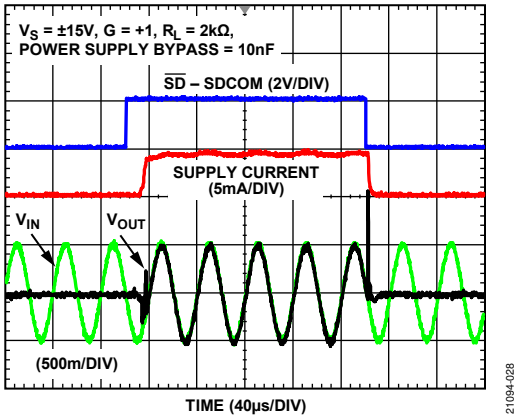


Figure 29. Shutdown Transient with Sinusoid Input, V_S = ±15 V

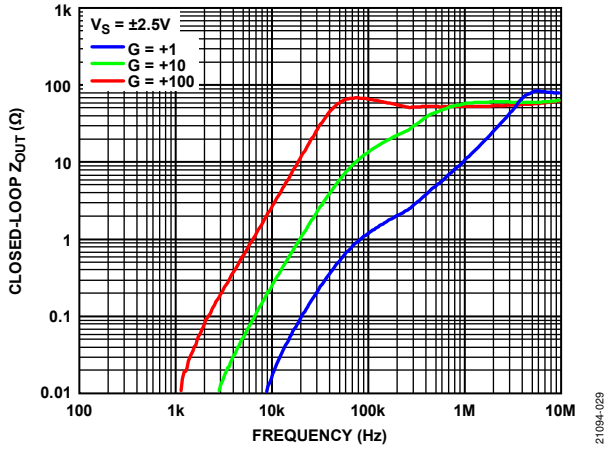


Figure 30. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency, V_S = ±2.5 V

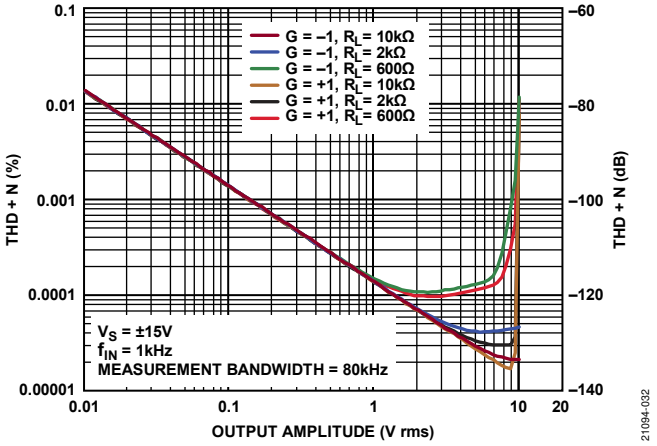


Figure 33. Total Harmonic Distortion plus Noise (THD + N) vs. Output Amplitude (f_{IN} Is the Input Frequency)

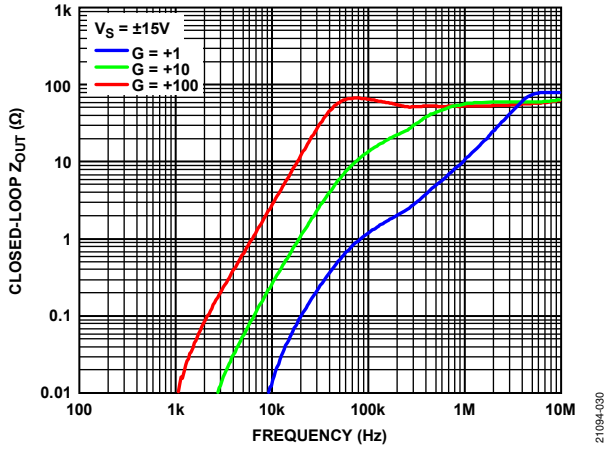


Figure 31. Closed-Loop Z_{OUT} vs. Frequency, V_S =±15 V

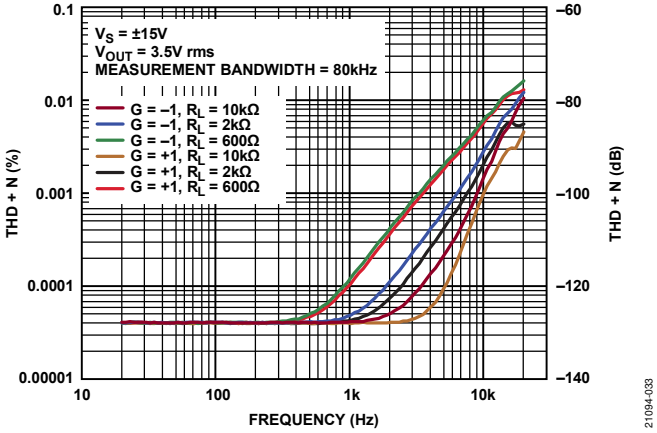


Figure 34. THD + N vs. Frequency

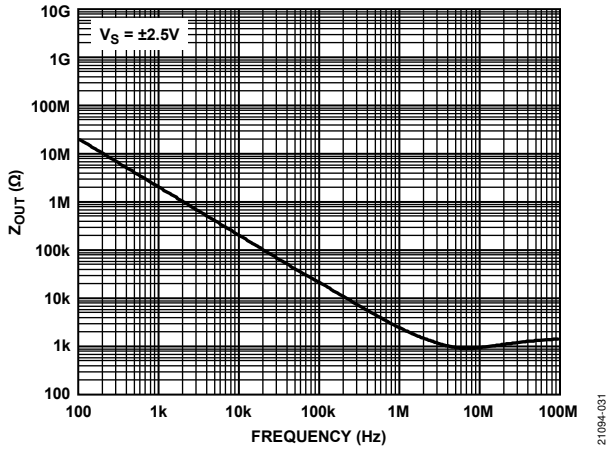


Figure 32. Z_{OUT} vs. Frequency in Shutdown

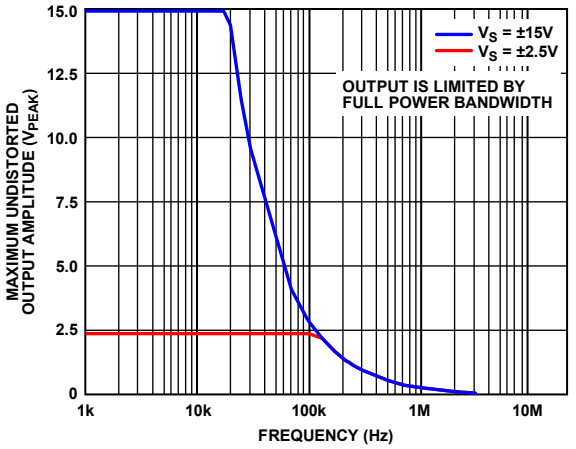


Figure 35. Maximum Undistorted Output Amplitude vs. Frequency

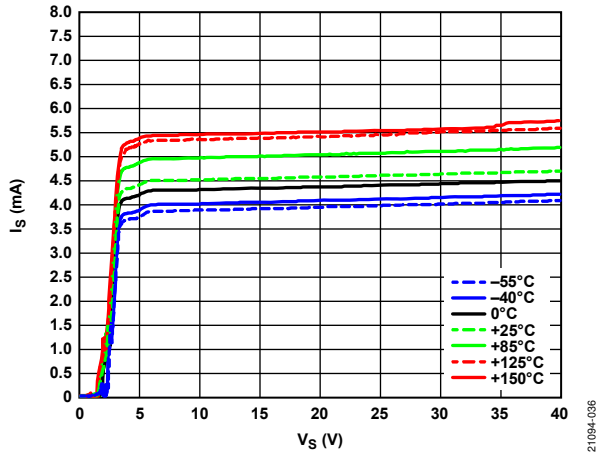


Figure 36. I_S vs. V_S for Various Temperatures

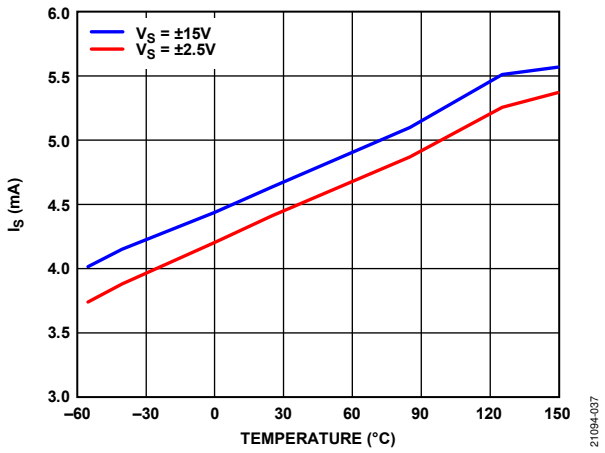


Figure 37. I_S vs. Temperature

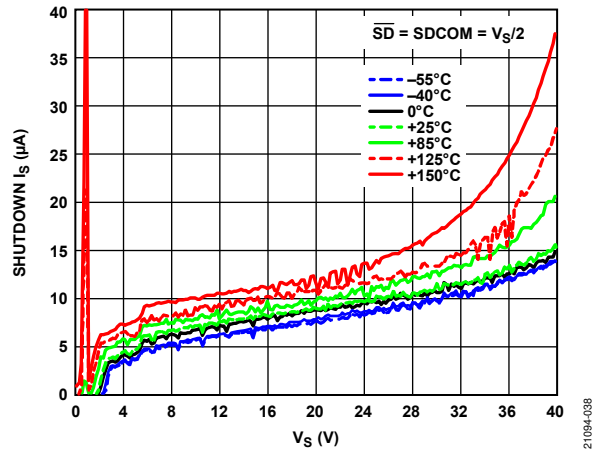


Figure 38. Shutdown I_S vs. V_S for Various Temperatures

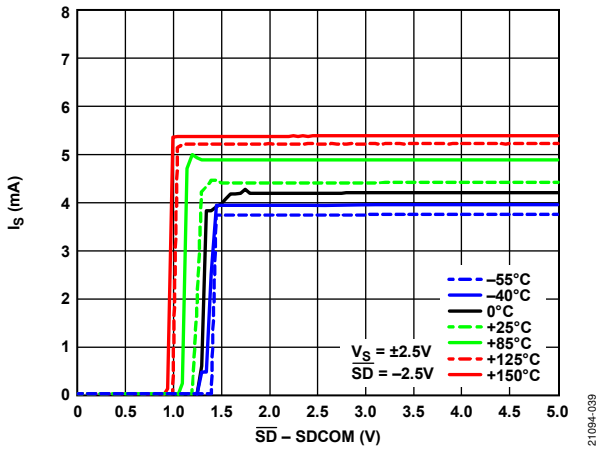


Figure 39. I_S vs. $\overline{SD}$ – SDCOM Voltage for Various Temperatures, V_S = ±2.5 V

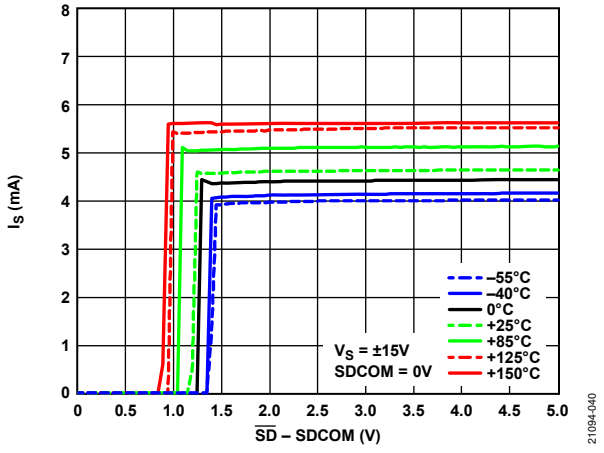


Figure 40. I_S vs. $\overline{SD}$ – SDCOM Voltage for Various Temperatures, V_S = ±15 V

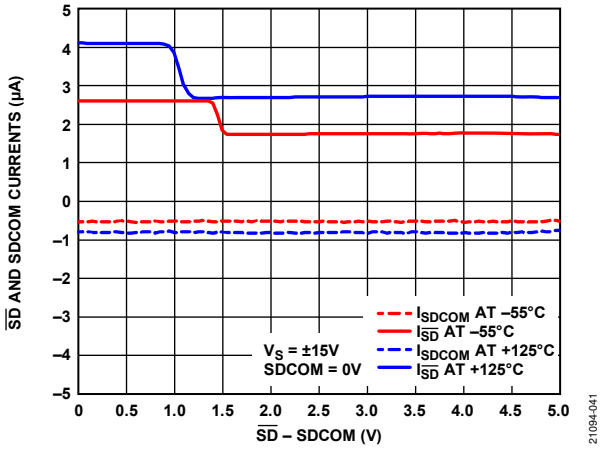


Figure 41. $\overline{SD}$ and SDCOM Currents vs. $\overline{SD}$ – SDCOM Voltage

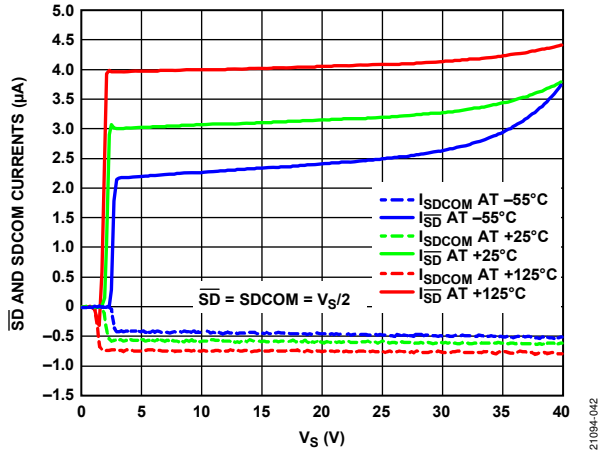


Figure 42. $\overline{SD}$ and SDCOM Currents vs. V_S

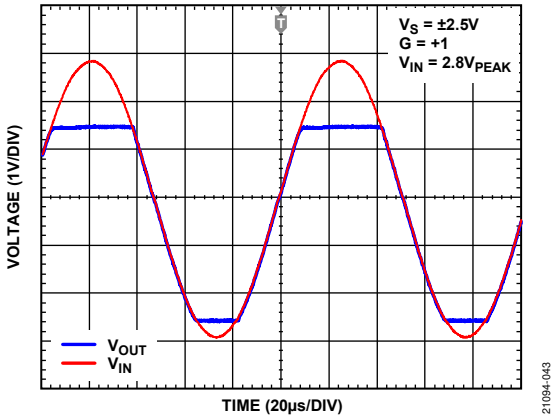


Figure 43. No Phase Reversal

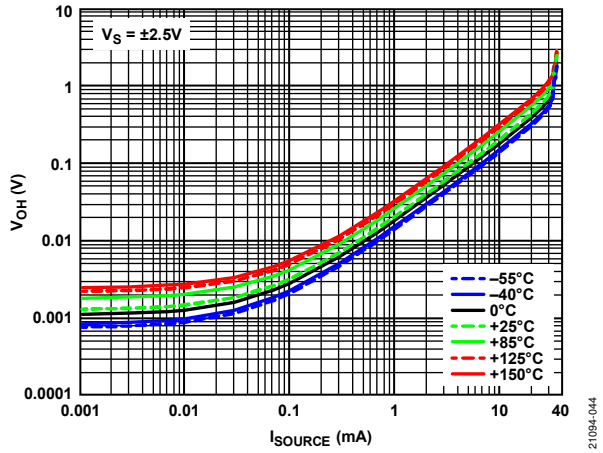


Figure 44. V_{OH} vs. I_{SOURCE} for Various Temperatures, V_S = ±2.5 V

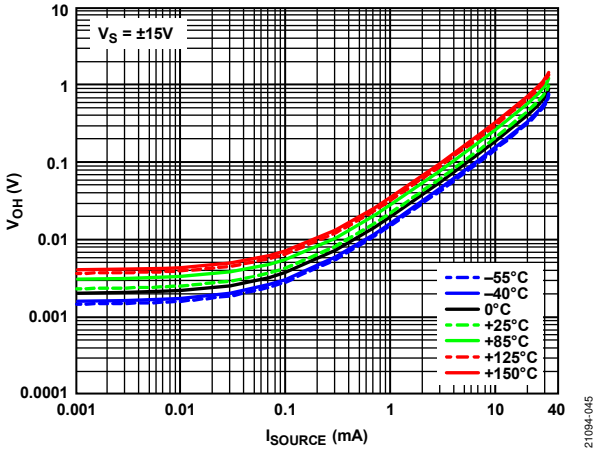


Figure 45. V_{OH} vs. I_{SOURCE} for Various Temperatures, V_S = ±15 V

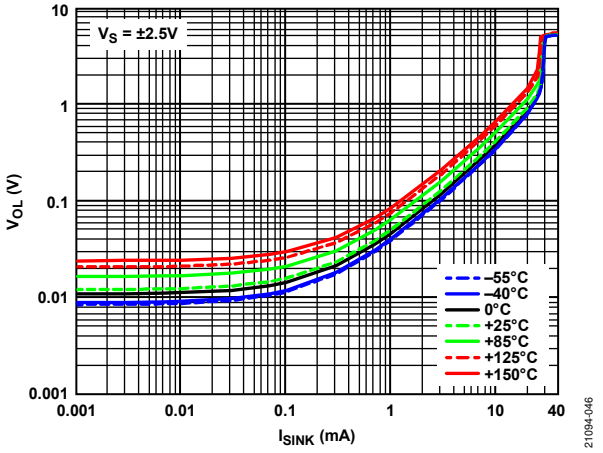


Figure 46. V_{OL} vs. I_{SINK} for Various Temperatures, V_S = ±2.5 V

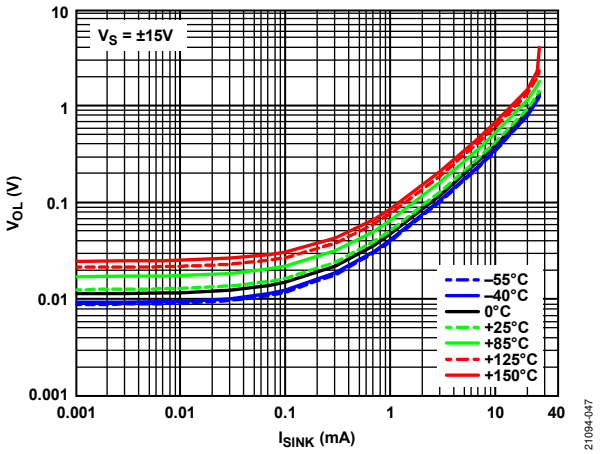


Figure 47. V_{OL} vs. I_{SINK} for Various Temperatures, V_S = ±15 V

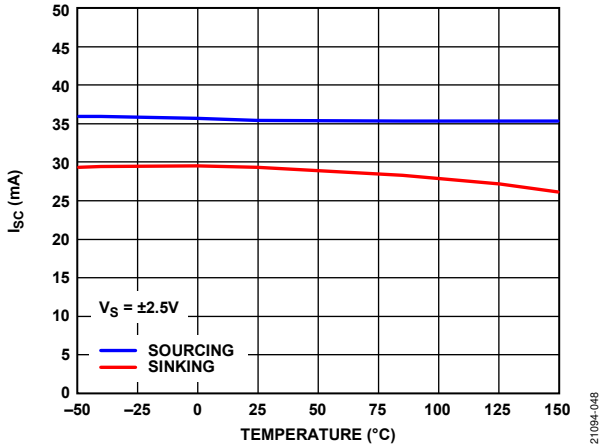


Figure 48. I_{SC} vs. Temperature, V_S = ±2.5 V

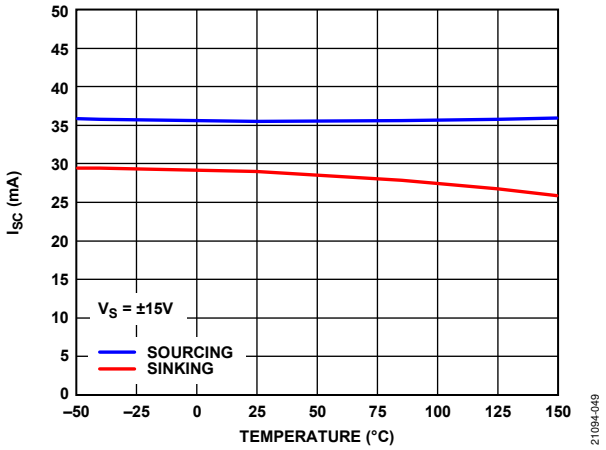


Figure 49. I_{SC} vs. Temperature, V_S = ±15 V

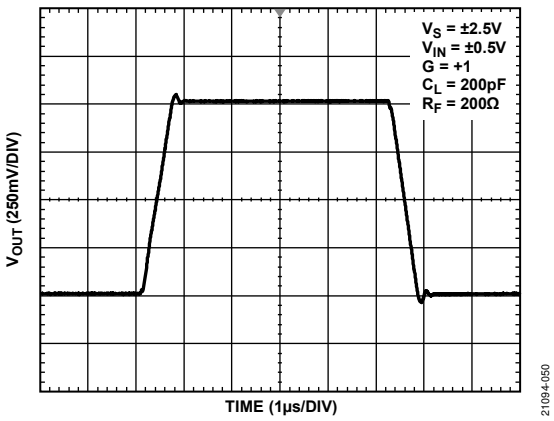


Figure 50. Large Signal Response, V_S = ±2.5 V

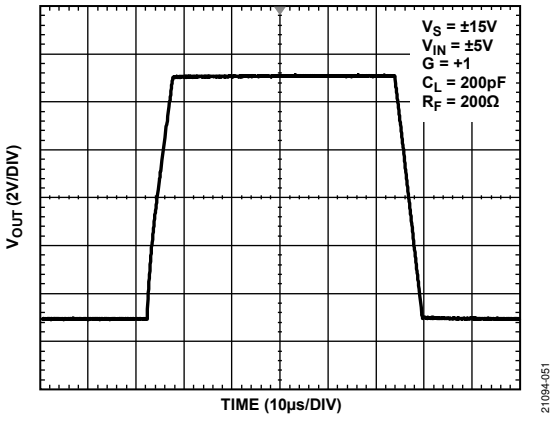


Figure 51. Large Signal Response, V_S = ±15 V

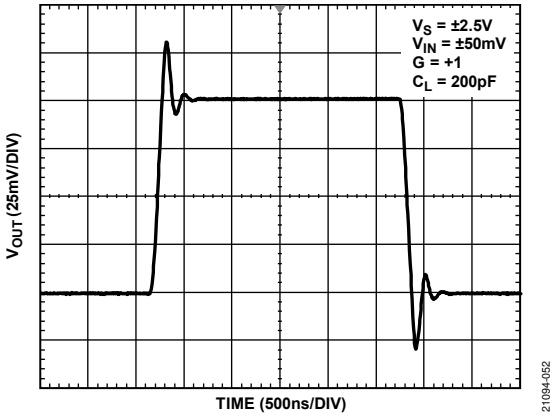


Figure 52. Small Signal Response, V_S = ±2.5 V

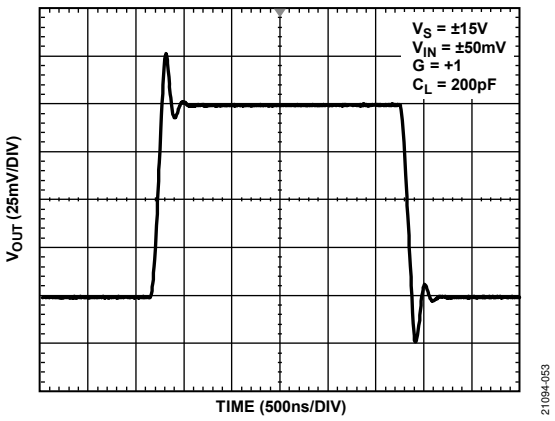


Figure 53. Small Signal Response, V_S = ±15 V

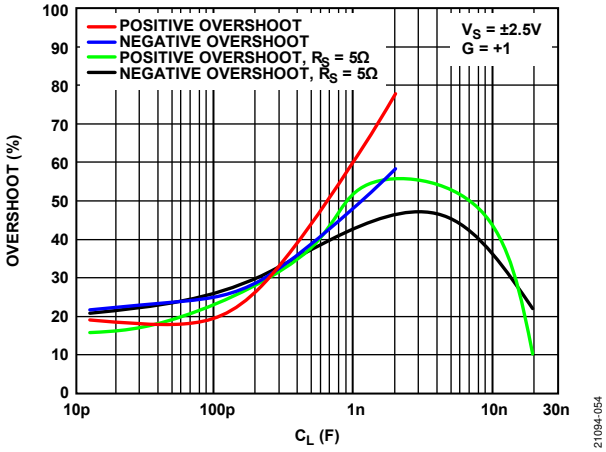


Figure 54. Small Signal Overshoot vs. C_L, V_S = ±2.5 V

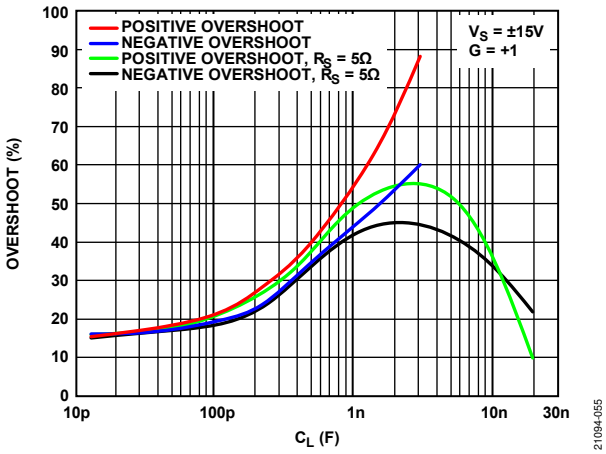


Figure 55. Small Signal Overshoot vs. C_L, V_S = ±15 V

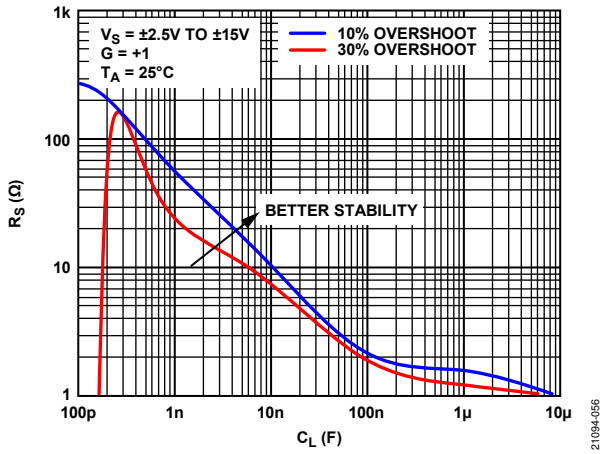


Figure 56. Output Series Resistance (R_S) vs. C_L and Overshoot

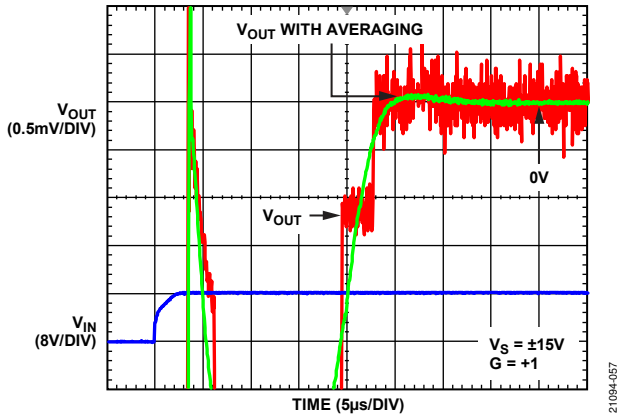


Figure 57. Large Signal Positive Settling Transient

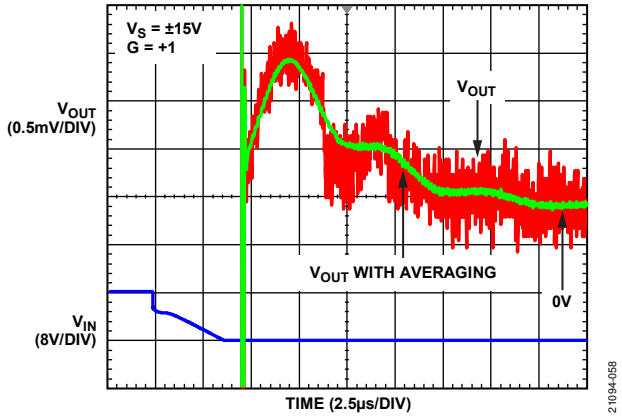


Figure 58. Large Signal Negative Settling Transient

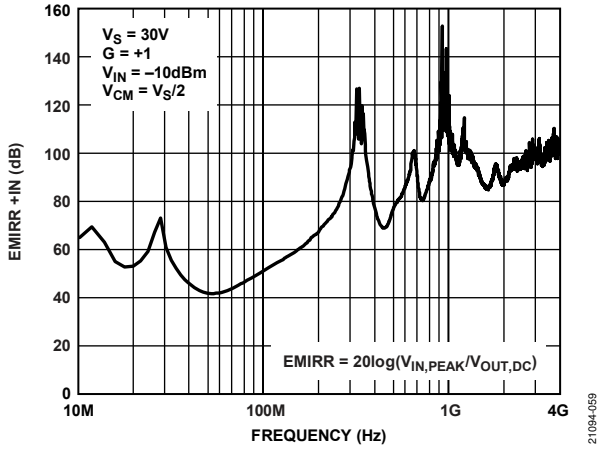


Figure 59. EMI Rejection Ratio (EMIRR) +IN vs. Frequency ($V_{IN, PEAK}$ Is the Peak Input Voltage and $V_{OUT, DC}$ Is the DC Output Voltage)

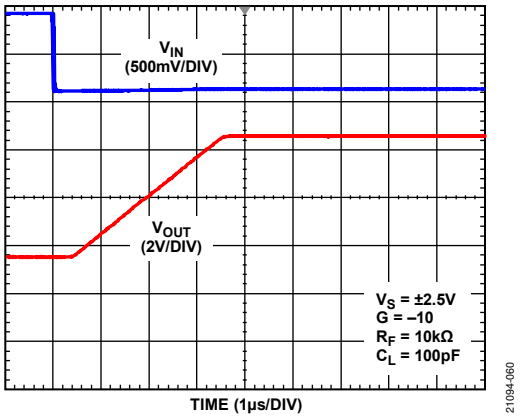


Figure 60. Negative Output Overload Recovery, V_S = ±2.5 V

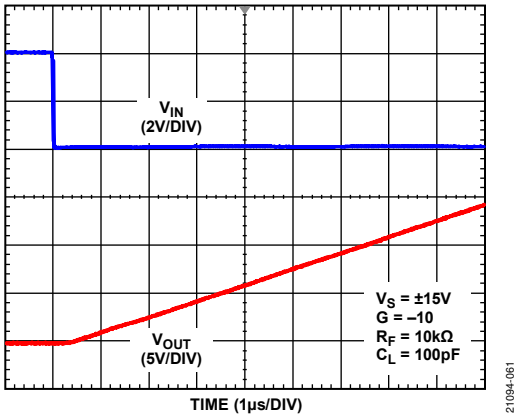


Figure 61. Negative Output Overload Recovery, V_S = ±15 V

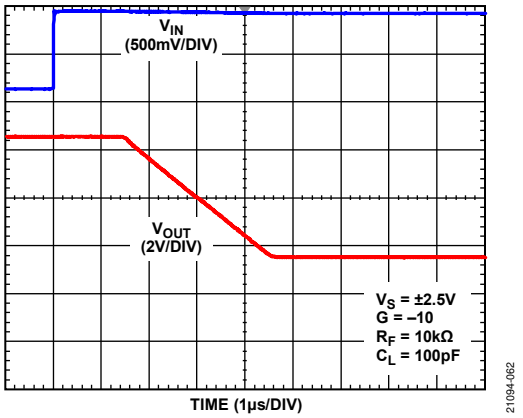


Figure 62. Positive Output Overload Recovery, V_S = ±2.5 V

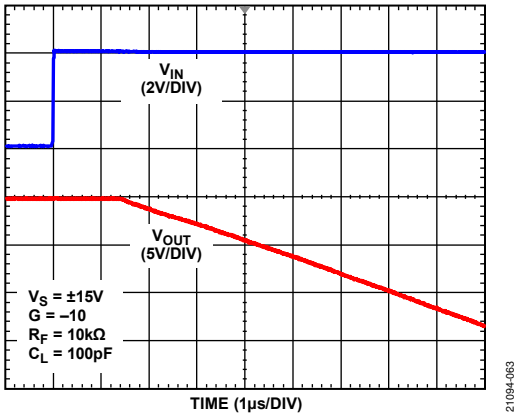


Figure 63. Positive Output Overload Recovery, V_S = ±15 V

THEORY OF OPERATION

The block diagram and clamp circuits are shown in Figure 64.

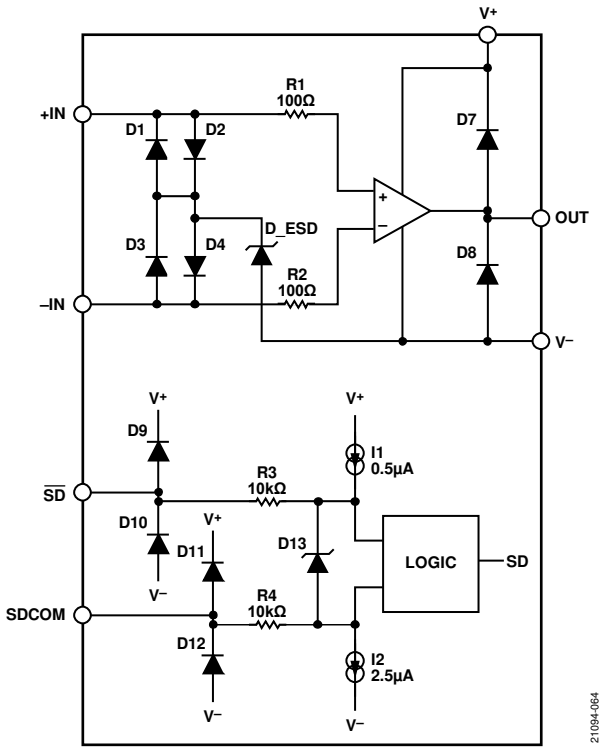


Figure 64. Block Diagram and Clamp Circuits (SD Is the Internal Shutdown)

INPUT VOLTAGE NOISE

Chopper stabilized amplifiers, such as the ADA4523-1, achieve low offset and 1/f noise by heterodyning dc and flicker noise to higher frequencies. In a typical chopper stabilized amplifier, this process results in idle tones at the chopping frequency and its odd harmonics.

The ADA4523-1 uses circuitry to suppress these spurious artifacts to below the offset voltage. The typical ripple magnitude at the 330 kHz chopping frequency is less than 1 µV rms.

The input voltage noise spectral density of the ADA4523-1 is shown in Figure 20. If lower noise is required, see Figure 75 in the Applications Information section.

INPUT CURRENT NOISE

For applications with high source impedances, input current noise can be a significant contributor to the total output noise. For this reason, it is important to consider noise current interaction with circuit elements placed at the inputs of the amplifier.

The input current noise spectral density of the ADA4523-1 is shown in Figure 22 and as measured by the circuit in Figure 65, with a shunt capacitance (C_{EXT}) = 0 pF. The characteristic curve shows no 1/f behavior. As with all zero drift amplifiers, there is a significant current noise component at the offset nulling frequency, which is discussed further in the Input Bias Current section.

It is important to note that the current noise is not equal to $2qI_B$, where q is the charge of an electron, 1.6×10^{-19} Coulombs. This formula is relevant for base current in bipolar transistors and diode currents. However, for most chopper and autozero amplifiers with switched inputs, the dominant current noise mechanism is not shot noise.

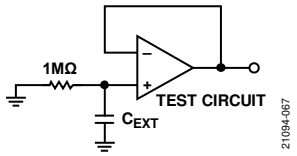


Figure 65. Input Current Noise Spectrum Test Circuit

INPUT BIAS CURRENT

The input bias current of the ADA4523-1 comprises two different currents, leakage and charge injection. Leakage current increases with temperature, while the charge injection current from the switching input remains relatively constant with temperature. The composite of these two currents over temperature is shown in Figure 14.

How the various input bias currents behave and contribute to error depends on the nature of the source impedance. For the input bias currents specified in Table 1 and Table 2, the source impedances are high value resistors bypassed with C_{EXT}, in the same configuration as shown in Figure 65. Figure 66 shows the effective dc error as an input referred current error (output dc voltage error divided by gain and then by the source resistance) as a function of C_{EXT}. Note that the effective dc error decreases as the capacitance increases. The added C_{EXT} also reduces the input referred current noise density as shown in Figure 67.

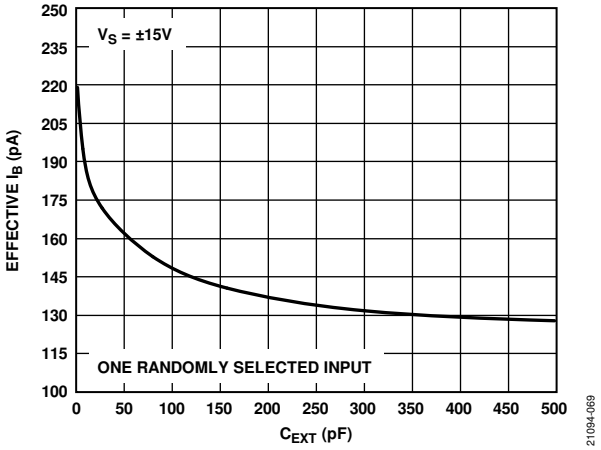


Figure 66. Effective I_B vs. C_{EXT}

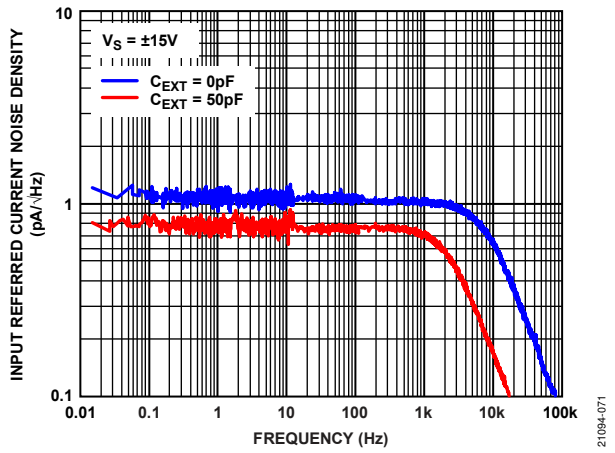


Figure 67. Input Referred Current Noise Density vs. Frequency for C_{EXT} = 0 pF and C_{EXT} = 50 pF

Another function of the input capacitance is to reduce the effects of charge injection. The charge injection-based current has frequency components at the 330 kHz chopping frequency and its harmonics. In the time domain, these frequency components appear as current pulses (appearing at regular intervals related to the chopping frequency). When these small current pulses interact with source impedances or gain setting resistors, the resulting voltage spikes are amplified by the closed-loop gain.

For higher source impedances, this may cause the 330 kHz chopping frequency to be visible in the output spectrum, which is known as clock feedthrough. To prevent excessive clock feedthrough, keep the gain setting resistors and source impedances as low as possible. When dc highly resistive source impedance is required, the capacitor across the source impedance reduces the ac impedance, reducing the amplitude of the input voltage spikes. Another way to reduce clock injection effects is to bandwidth limit after the op amp output.

Injection currents from the two inputs are of equal magnitude but opposite direction. Therefore, when chopping behavior is the predominant source of I_B, the effects of I_B on the offset voltage cannot be canceled by placing matched impedances at both inputs.

Above 50°C, ESD protection diode leakage current begins to dominate the input bias current and continues to increase exponentially at elevated temperatures. The input bias cancellation circuit of the ADA4523-1 minimizes this temperature driven growth of the leakage current to keep the input bias current low over all temperatures. Unlike injection current, leakage currents are in the same direction for both inputs. Therefore, the output error due to leakage current may be mitigated by matching the source impedances seen by the two inputs. If the source impedance matching technique is employed to cancel the effect of the leakage currents, at less than 50°C, there is an offset voltage error of $2I_B \times R$ due to the charge injection currents. For example, if I_B = 100 pA and R = 10 kΩ, the error is 2 µV.

THERMOCOUPLE EFFECTS

To achieve accuracy on the microvolt level, consider thermocouple effects. Any connection of dissimilar metals forms a thermoelectric junction and generates a small temperature dependent voltage, which is known as the Seebeck effect. These thermal electric magnetic fields (EMFs) can be the dominant error source in low drift circuits.

Connectors, switches, relay contacts, sockets, resistors, and solders are all candidates for significant thermal EMF generation. Even junctions of copper wire from different manufacturers can generate thermal EMFs of 200 nV/°C, which is over 10 times the maximum drift specification of the ADA4523-1. Figure 68 and Figure 69 illustrate the potential magnitude of these voltages and their sensitivity to temperature.

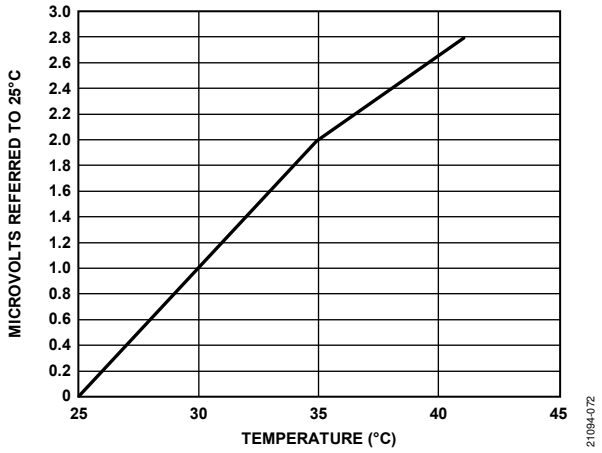


Figure 68. Thermal EMF Generated by the Junction of Two Copper Wires from Different Manufacturers

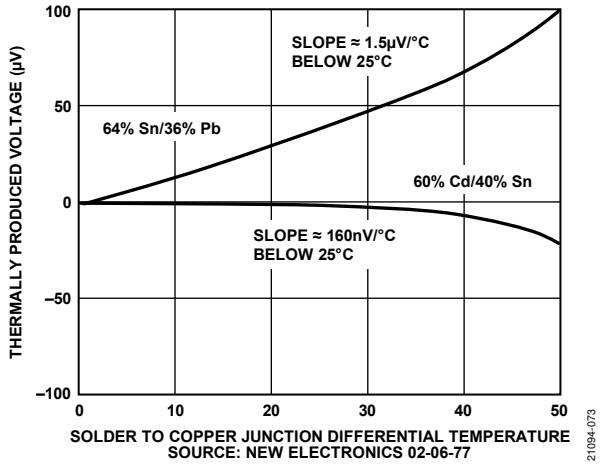


Figure 69. Solder Copper Thermal EMFs

To minimize thermocouple induced errors, attention must be given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the input signal path of the op amp and to avoid connectors, sockets, switches, and relays whenever possible. If such components are required, select these components for low thermal EMF characteristics. Furthermore, match the number, type, and layout of junctions for both inputs with respect to thermal gradients on the circuit board, which can involve deliberately introducing dummy junctions to offset unavoidable junctions.

Air currents can also lead to thermal gradients and cause significant noise in measurement systems. It is important to prevent airflow across sensitive circuits because doing so often reduces thermocouple noise substantially.

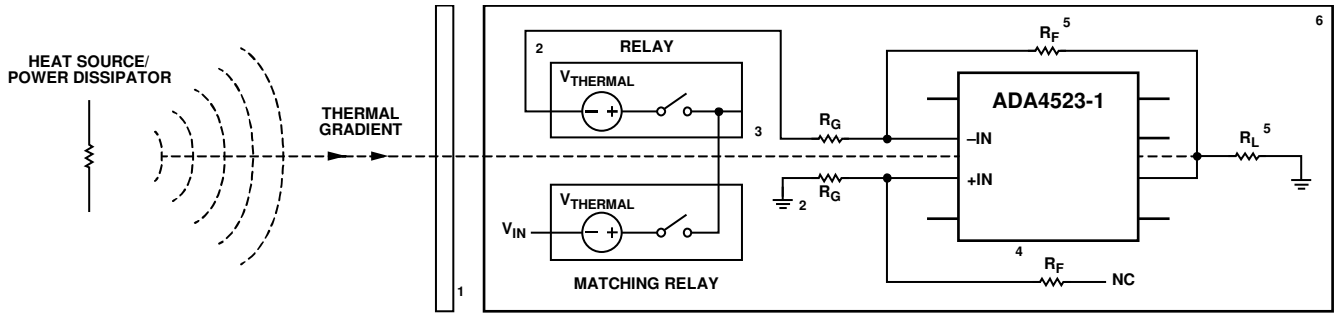
A summary of techniques is shown in Figure 70.

POWER DISSIPATION

Because the ADA4523-1 can operate at a 36 V total supply, take care with respect to power dissipation in the amplifier. When driving heavy loads at high voltages, use the θ_{JA} of the package to estimate the resulting die temperature rise and ensure that the resulting junction temperature does not exceed specified limits. In addition, consider PCB metallization and heat sinking when high power dissipation is expected.

The ADA4523-1 LFCSP features lower package thermal resistances compared to its standard counterparts. The LFCSP exposed pad facilitates heat sinking. The exposed bottom pad must be soldered to the PCB, and due to its internal connection to V^-, connecting the exposed pad to V^- is a requirement. For more efficient heat sinking, it is recommended that the exposed pad have as much PCB metal connected to the pad as reasonably available.

Thermal information for the ADA4523-1 packages can be found in the Thermal Resistance section.



[1]CUT SLOTS IN PCB FOR THERMAL ISOLATION.
[2]INTRODUCE DUMMY JUNCTIONS AND COMPONENTS TO OFFSET UNAVOIDABLE JUNCTIONS OR CANCEL THERMAL EMFS.
[3]ALIGN INPUTS SYMMETRICALLY WITH RESPECT TO THERMAL GRADIENTS.
[4]INTRODUCE DUMMY TRACES AND COMPONENTS FOR SYMMETRICAL THERMAL HEAT SINKING.
[5]LOADS AND FEEDBACK CAN DISSIPATE POWER AND GENERATE THERMAL GRADIENTS. BE AWARE OF THEIR THERMAL EFFECTS.
[6]COVER CIRCUIT TO PREVENT AIR CURRENTS FROM CREATING THERMAL GRADIENTS.

Figure 70. Techniques for Minimizing Thermocouple Induced Errors

ELECTRICAL OVERSTRESS AND INPUT PROTECTION

Do not exceed the absolute maximum ratings. Avoid driving the input and output pins beyond the rails, especially at supply voltages approaching 40 V. The inputs of the ADA4523-1 are internally protected by ESD diodes and an ESD clamp (see Figure 64). When the inputs are driven above and/or below the supply rail, the inputs draw substantial input currents, as shown in Figure 71.

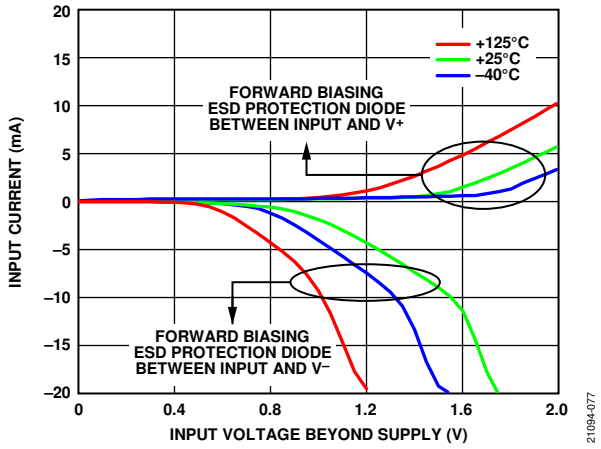


Figure 71. Input Current vs. Input Voltage Beyond Supply, ESD Protection Diode Forward Bias Voltage

If a large differential input voltage is imposed between +IN and –IN, the resulting input bias current is as shown in Figure 72. Note that the +IN and –IN bias currents are asymmetrical due to the input ESD clamp structure of the ADA4523-1. Some additional current is sourced from the supply when a large input voltage separates +IN from –IN, and this current then exits the device through –IN.

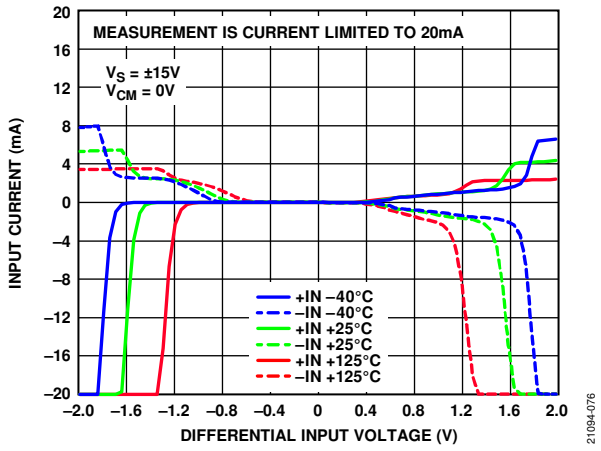


Figure 72. Input Current vs. Differential Input Voltage for +IN and –IN and Various Temperatures

If overvoltage conditions cannot be prevented, a resistor in series (R_{IN}) with the threatened pin can limit fault current, $I_{OVERLOAD}$, to below the absolute maximum rating and reduce the possibility of device damage (see Figure 73).

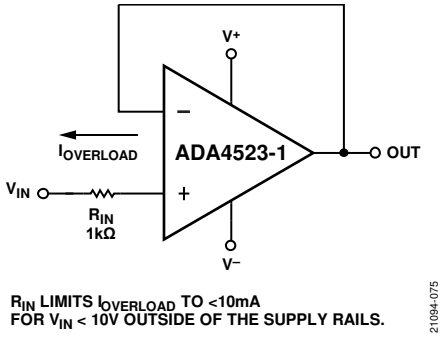


Figure 73. Using a Resistor to Limit the Input Current

Keep the current-limit resistance low enough to not add noise and error voltages from interaction with the input bias currents. Resistances ≤1 kΩ do not significantly impact noise or precision. See Figure 71 and Figure 72 for the characteristics of the internal ESD diodes to help determine the appropriate value of the resistor.

In harsh environments, reliability can be enhanced further with protection circuitry. The circuit shown in Figure 74 uses low leakage diodes (Nexperia BAV199) to protect the input. R2 protects the external diodes, and R1 limits the current that may flow through the internal diodes. In this circuit, R1 can be small because the applied voltage is already reduced by the external protection diodes.

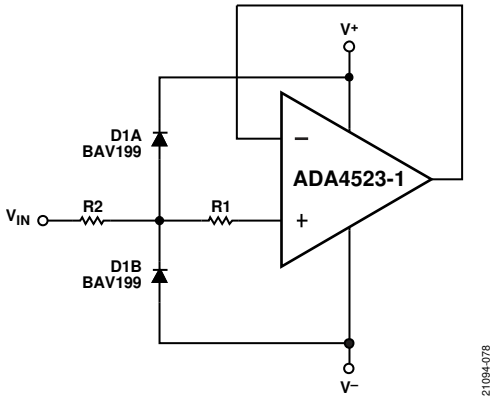


Figure 74. Input Protection Circuit Using External Diodes

In high temperature applications where the leakage currents of the internal ESD diodes dominate the input bias current, the circuit can benefit from adding an input bias cancellation resistor in the feedback path.

SHUTDOWN MODE

The ADA4523-1 features a shutdown mode for low power applications. In the off state, both amplifiers are shut off and draw less than 20 µA (maximum over temperature) of supply current per amplifier. In addition, in the off stage, both outputs present high impedances to external circuitry.

Keep in mind that during the off state, even with the amplifier output in high impedance, the output can still modulate by the input signal through the input differential clamp and the feedback resistor. (See Figure 64 for the location of the differential clamp.) In addition, depending on the resistor values, significant current can still be drawn from the input source.

Shutdown control is accomplished using the separate logic $\overline{SD}$ reference voltage input (SDCOM) and the shutdown pin ($\overline{SD}$). This method allows low voltage digital control logic to operate independently of the high voltage supply rails of the op amp. A summary of the shutdown control logic and operating ranges is shown in Table 8 and Table 9.

Table 8. Shutdown Control Logic

Shutdown Pin Condition	Amplifier State
$\overline{SD}$ = float, SDCOM = float	On
$\overline{SD}$ − SDCOM ≥ 2 V	On
$\overline{SD}$ − SDCOM ≤ 0.8 V	Off

Table 9. Operating Voltage Range for Shutdown Pins

Mnemonic	Minimum	Maximum
$\overline{SD}$ − SDCOM	−0.2 V	+5.2 V
SDCOM	V^-	V^+ − 2.35 V
$\overline{SD}$	V^-	V^+

If the shutdown feature is not required, leave $\overline{SD}$ and SDCOM floating. Internal circuitry automatically keeps the amplifier in the on state.

For operation in noisy environments, adding a capacitor between $\overline{SD}$ and SDCOM is recommended to prevent noise from changing the shutdown state.

When there is a danger of $\overline{SD}$ and SDCOM pulling beyond the supply rails, adding resistance in series with the shutdown pins is recommended to limit current.

APPLICATIONS INFORMATION

PARALLELING CHOPPERS TO IMPROVE NOISE

By using multiple amplifiers in parallel, voltage noise can be reduced at the cost of higher current noise because the voltage noise sources in each of the amplifiers are uncorrelated, while the input signal at each amplifier is correlated. The power of the correlated signal is multiplied by N, while the power of the uncorrelated noise is multiplied by √N. The net effect is a $\sqrt{N}$ improvement in signal-to-noise ratio.

The resulting overall input current of the paralleled amplifiers is the sum of the input currents of each of the amplifiers, and the current noise scales accordingly.

When the current noise of an amplifier is far smaller than its voltage noise, as is the case with ADA4523-1, and the current noise does not pass through large impedances, trading higher current noise for lower voltage noise can be advantageous.

The overall gain of the circuit depicted in Figure 75 is

$$A_V = (R2/R1 + 1) \times (R4/R3 + 1)$$

If N is the number of paralleled amplifiers, the resulting change in input referred noise due to paralleling is

0.1 Hz to 10 Hz *Noise* = 88 nV p-p/$\sqrt{N}$

$e_n = (4.2 \text{ nV}/\sqrt{\text{Hz}})/\sqrt{N}$

$i_n = \sqrt{N} \times 1 \text{ pA}/\sqrt{\text{Hz}}$

$I_B = N \times 300 \text{ pA}$ (maximum at 25°C)

For the example of N = 4, as shown in Figure 75, the exact results are the following:

0.1 Hz to 10 Hz *Noise* = 44 nV p-p

$e_n = 2.1 \text{ nV}/\sqrt{\text{Hz}}$

$i_n = 2 \text{ pA}/\sqrt{\text{Hz}}$

$I_B = 300 \text{ pA}$ (maximum at 25°C)

R5 in Figure 75 must be a few hundred ohms to isolate the individual amplifier outputs without contributing significantly to noise or I_B induced error.

The choice of output amplifier is important for headroom, precision, and noise concerns as well. In Figure 75, the 60 V headroom of the LTC2057HV allows a wide signal swing, and its zero-drift input does not add significant offset.

If enough gain is taken in the parallel amplifier stage for the input signal of the LTC2057HV to be large compared to its own input noise voltage of 11 nV/√Hz, the effect of the noise of the LTC2057HV is reduced in the overall output. To minimize the noise contribution of the output amplifier, choose the first stage gain of (R2/R1 + 1) to be far larger than √N as well.

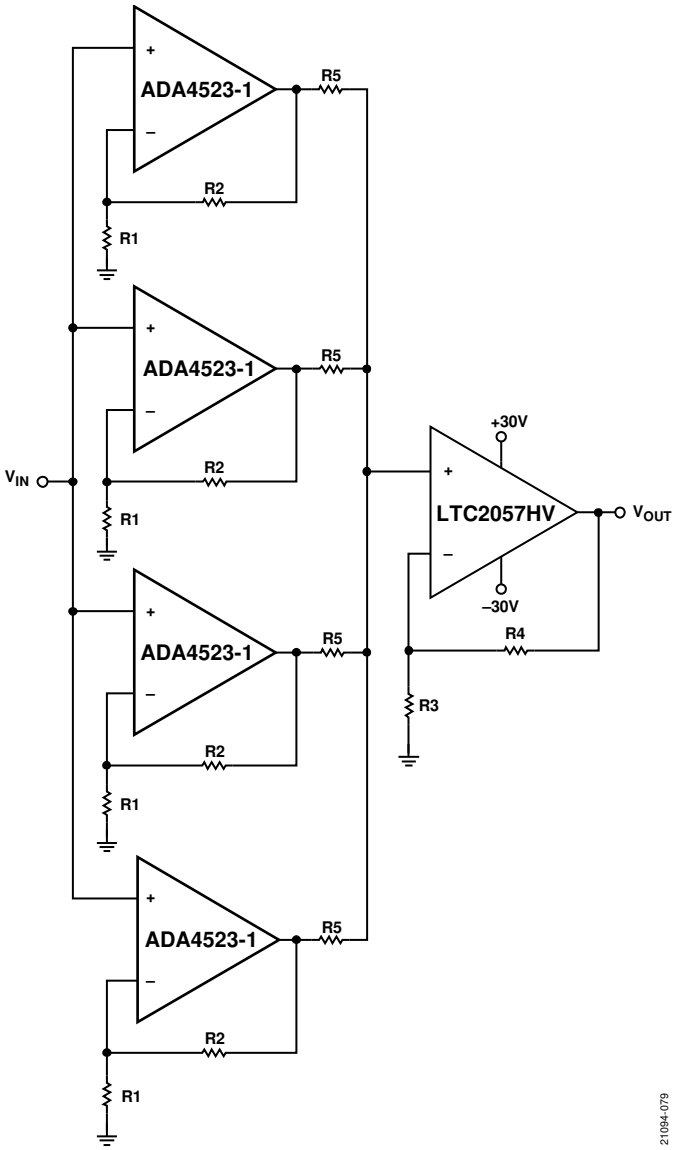


Figure 75. Paralleling Choppers to Improve Noise

SOLDER PAD LAYOUTS

The recommended solder pad layouts for the 8-lead SOIC_N, 8-lead MSOP, and 8-lead LFCSP are shown in Figure 76, Figure 77, and Figure 78, respectively. Drawings are not to scale. All dimensions are given in millimeters or millimeters/(inches).

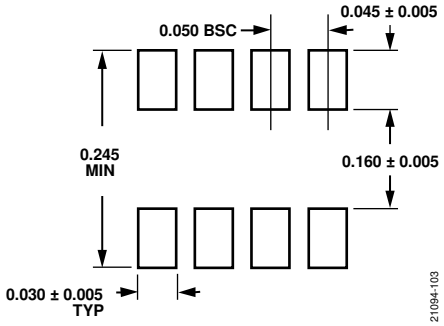


Figure 76. R-8 (8-Lead SOIC) Recommended Solder Pad Layout

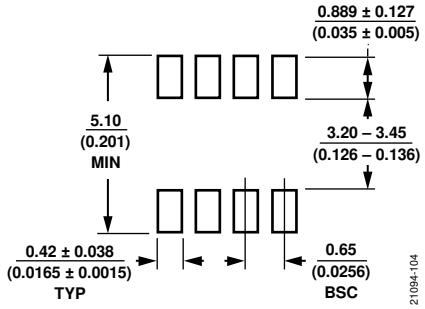


Figure 77. RM-8 (8-Lead MSOP) Recommended Solder Pad Layout

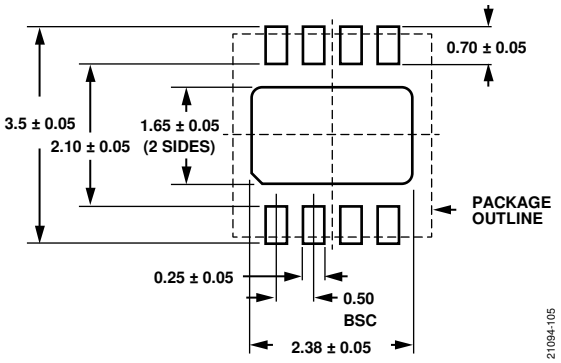


Figure 78. CP-8-29 (8-Lead LFCSP) Recommended Solder Pad Layout, Apply Solder Mask to Areas That Are Not Soldered

TYPICAL APPLICATION CIRCUIT AND TRANSFER FUNCTION

Figure 79 shows the low-side current sense amplifier circuit.

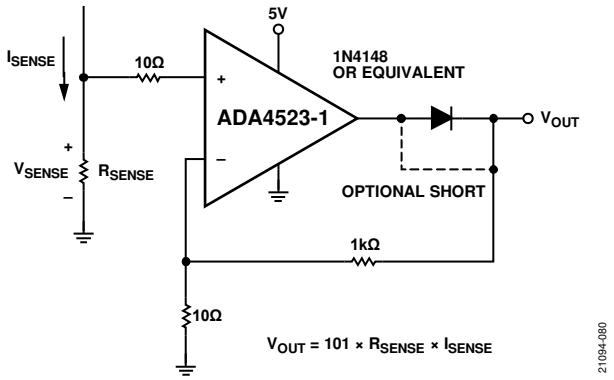


Figure 79. Low-Side Current Sense Amplifier Circuit (I_{SENSE} Is the Sense Current, V_{SENSE} Is the Sense Voltage Produced by I_{SENSE}, and R_{SENSE} Is the Sense Resistance)

Figure 80 shows the low-side current sense amplifier transfer function.

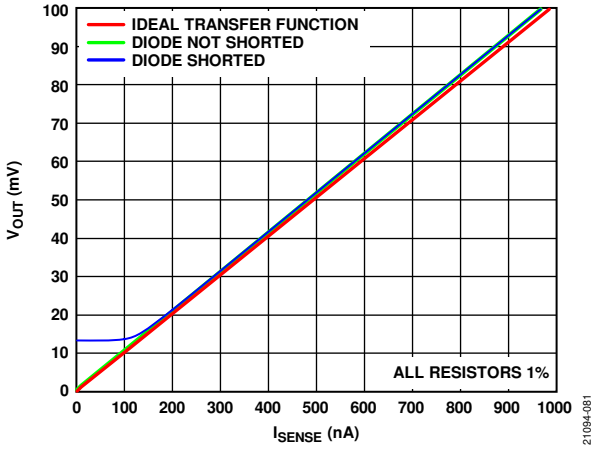


Figure 80. Low-Side Current Sense Amplifier Transfer Function, R_{SENSE} = 1 kΩ

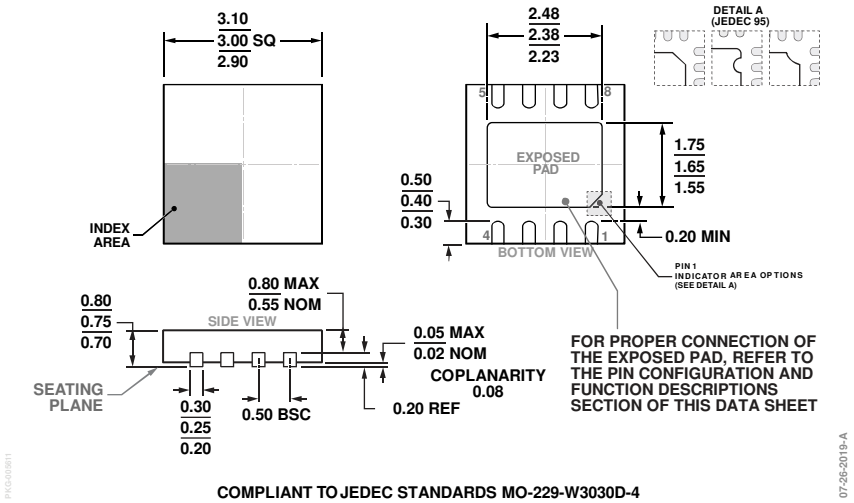
RELATED PRODUCTS

Table 10. Zero-Drift Op Amp Products

Device(s)	e_n at 1 kHz	GBP (MHz)	V_S Range (V)	I_S per Amp (mA)	Function
ADA4523-1	4.2 nV/√Hz	5	4.5 to 36	4.5	Rail-to-rail output (RRO)
ADA4528-1/ADA4528-2	5.6 nV/√Hz	3.4	2.2 to 5.5	1.5	Single or dual, rail to rail input output (RRIO)
ADA4522-1/ADA4522-2/ ADA4522-4	5.8 nV/√Hz	2.7	4.5 to 55	0.9	Single, dual, or quad, RRO, electro-magnetic interference (EMI) filter
LTC2058	9 nV/√Hz	2.5	4.75 to 36	0.95	Dual, RRO, shutdown
LTC2057HV	11 nV/√Hz	1.5	4.75 to 60	1	RRO, shutdown
ADA4254	17 nV/√Hz	1.8 for G = 1 V/V	10 to 56	See Note 1[1]	High voltage, low power, programmable gain instrumentation amplifier
AD8628/AD8629/AD8630	22 nV/√Hz	2.5	2.7 to 5.5	1.0	Single-supply, AEC-Q100, RRIO
LTC2050HV	1.5 µV p-p[2]	3	2.7 to 12	1.5	RRO, enhanced product grade available (−55°C to +150°C)
LTC2051/LTC2052	1.5 µV p-p[2]	3	2.7 to 12	1.5	Dual or quad, RRO
LTC2053-SYNC	2.5 µV p-p[2]	0.2	2.7 to 11	0.85	In-amp, resistor programmable, RRIO, external clock sync

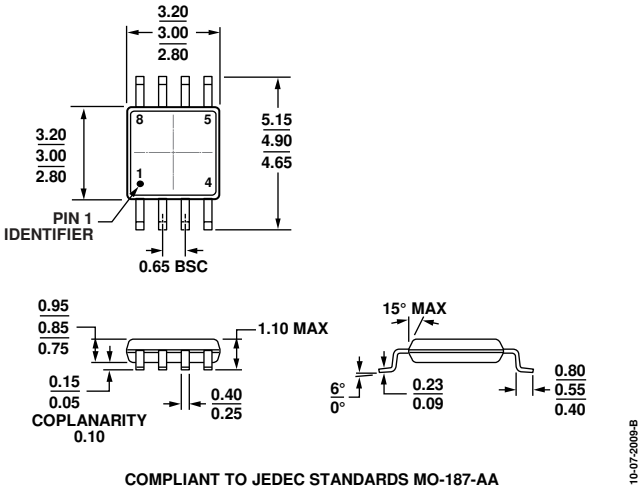
[1] The supply current for the ADA4254 is specified for each of the independent supplies, VDDH, VSSH, DVDD, and AVDD. Typical supply current values are I_{VDDH} = 600 µA, I_{VSSH} = 780 µA, I_{DVDD} = 150 µA, and I_{AVDD} = 980 µA.
[2] Integrated input voltage noise from 0.01 Hz to 10 Hz is given instead of input voltage noise density at 1 kHz.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-229-W3030D-4

Figure 81. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-29)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 82. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

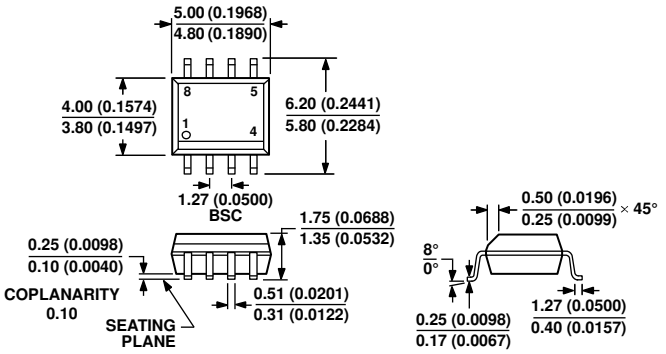


Figure 83. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADA4523-1BCPZ	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-29	Y77
ADA4523-1BCPZ-RL7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-29	Y77
ADA4523-1BRMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y77
ADA4523-1BRMZ-RL7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y77
ADA4523-1BRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4523-1BRZ-RL7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

[1] Z = RoHS Compliant Part.