

MC74ACT640

Octal 3-State Inverting Transceiver

The MC74ACT640 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus \bar{A} to bus B when $T/\bar{R} = \text{HIGH}$, or from bus \bar{B} to bus A when $T/\bar{R} = \text{LOW}$. The enable input can be used to disable the device so the buses are effectively isolated.

Features

- Bidirectional Data Path
- A and B Outputs Sink 24 mA/Source -24 mA
- TTL Compatible Inputs
- These are Pb-Free Devices

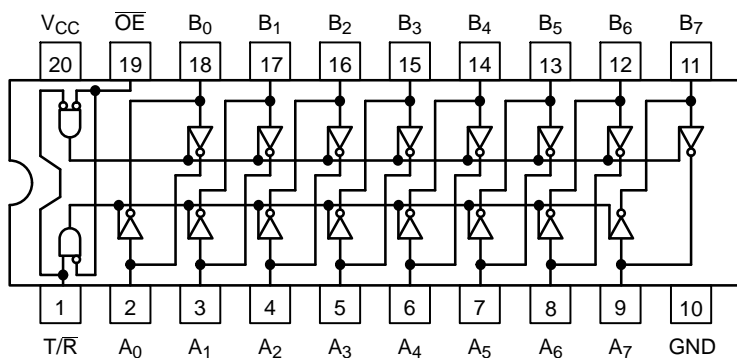


Figure 1. Pinout: 20-Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

| PIN | FUNCTION |
|--------------------------------|----------------------------------|
| A ₀ -A ₇ | Side A Inputs or 3-State Outputs |
| $\bar{O}E$ | Output Enable Input |
| T/ \bar{R} | Transmit/Receive Input |
| B ₀ -B ₇ | Side B Inputs or 3-State Outputs |

TRUTH TABLE

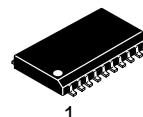
| OE | T/ \bar{R} | Applied Inputs | Valid Direction I/P \rightarrow O/P | Output |
|----|--------------|----------------|---------------------------------------|--------|
| H | X | X | X | X |
| L | H | H | \bar{A} to B | L |
| L | H | L | \bar{A} to B | H |
| L | L | H | \bar{B} to A | L |
| L | L | L | \bar{B} to A | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



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SOIC-20W
DW SUFFIX
CASE 751D

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 5 of this data sheet.

MC74ACT640

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit | |
|----------------------|---|--|---------------------------|----|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V | |
| V _{IN} | DC Input Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V | |
| V _{OUT} | DC Output Voltage (Referenced to GND) (Note 1) | -0.5 to V _{CC} +0.5 | V | |
| I _{IK} | DC Input Diode Current | ±20 | mA | |
| I _{OK} | DC Output Diode Current | ±50 | mA | |
| I _{OUT} | DC Output Sink/Source Current | ±50 | mA | |
| I _{CC} | DC Supply Current, per Output Pin | ±50 | mA | |
| I _{GND} | DC Ground Current, per Output Pin | ±100 | mA | |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C | |
| T _L | Lead temperature, 1 mm from Case for 10 Seconds | 260 | °C | |
| T _J | Junction Temperature Under Bias | 140 | °C | |
| θ _{JA} | Thermal Resistance (Note 2) | 65.8 | °C/W | |
| MSL | Moisture Sensitivity | Level 1 | | |
| F _R | Flammability Rating | Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in | | |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5) | > 2000 > 200 > 1000 | V |
| I _{Latchup} | Latchup Performance | Above V _{CC} and Below GND at 85°C (Note 6) | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{OUT} absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Unit | |
|------------------------------------|--|-------------------------|-----|-----------------|------|------|
| V _{CC} | DC Input Voltage (Referenced to GND) | 4.5 | | 5.5 | V | |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | | V _{CC} | V | |
| T _A | Operating Temperature, All Package Types | -40 | 25 | +85 | °C | |
| t _r , t _f | Input Rise and Fall Time (Note 8) | | | | | |
| | | V _{CC} = 4.5 V | 0 | 10 | 10 | ns/V |
| | | V _{CC} = 5.5 V | 0 | 8.0 | 8.0 | |
| I _{OH} | Output Current – High | | | -24 | mA | |
| I _{OL} | Output Current – Low | | | 24 | mA | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
8. V_{in} from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -40°C to +85°C | Unit | Conditions |
|--------------------------------------|--|------------------------|------------------------|-------------------|---------------------------------|----------|---|
| | | | Typ | Guaranteed Limits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | I _{OUT} = -50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | | 3.86 | 3.76 | V | *V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA |
| | | 5.5 | | 4.86 | 4.76 | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | I _{OUT} = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | | 0.36 | 0.44 | V | *V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA |
| | | 5.5 | | 0.36 | 0.44 | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | V _I = V _{CC} , GND |
| ΔI _{CCT} | Additional Max. I _{CC} /Input | 5.5 | 0.6 | | 1.5 | mA | V _I = V _{CC} - 2.1 V |
| I _{OZ} | Maximum 3-State Current | 5.5 | | ±0.5 | ±5.0 | μA | V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND |
| I _{OLD} I _{OHD} | †Minimum Dynamic Output Current | 5.5 5.5 | | | 75 -75 | mA mA | V _{OLD} = 1.65 V Max |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80 | μA | V _{IN} = V _{CC} or GND |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS t_r = t_f = 3.0 ns (For Figures and Waveforms, See Figures 2 and 3.)

| Symbol | Parameter | V _{CC} (V) | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Unit |
|------------------|--|------------------------|--|------|---|------|------|
| | | | Min | Max | Min | Max | |
| t _{PLH} | Propagation Delay An to Bn or Bn to An | 5.0 | 1.5 | 8.0 | 1.0 | 8.5 | ns |
| t _{PHL} | Propagation Delay An to Bn or Bn to An | 5.0 | 1.5 | 8.0 | 1.0 | 9.0 | ns |
| t _{PZH} | Output Enable Time \overline{OE} to An or Bn | 5.0 | 1.5 | 10.0 | 1.0 | 11.0 | ns |
| t _{PZL} | Output Enable Time \overline{OE} to An or Bn | 5.0 | 1.5 | 10.0 | 1.0 | 11.0 | ns |
| t _{PHZ} | Output Disable Time T/R or \overline{OE} to An or Bn | 5.0 | 1.5 | 10.0 | 1.0 | 11.0 | ns |
| t _{PLZ} | Output Disable Time T/R or \overline{OE} to An or Bn | 5.0 | 1.5 | 10.0 | 1.0 | 11.0 | ns |

*Voltage Range 5.0 V is 5.0 V ±0.5 V

CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|------------------|-------------------------------|-----------|------|-------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.0 V |
| C _{I/O} | Input/Output Capacitance | 15 | pF | V _{CC} = 5.0 V |
| C _{PD} | Power Dissipation Capacitance | 45 | pF | V _{CC} = 5.0 V |

MC74ACT640

SWITCHING WAVEFORMS

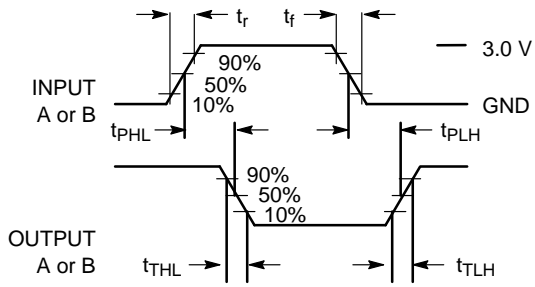


Figure 2.

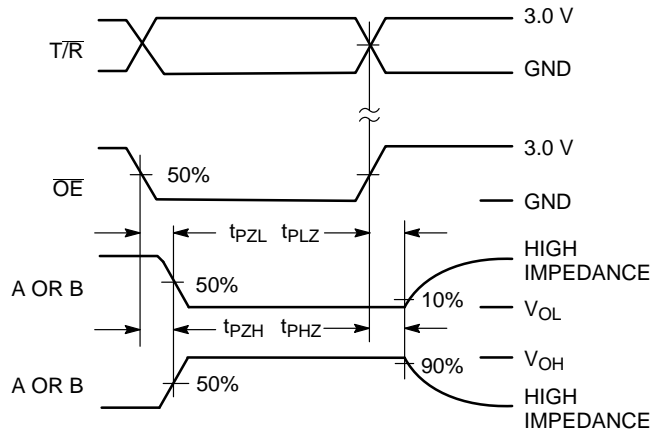
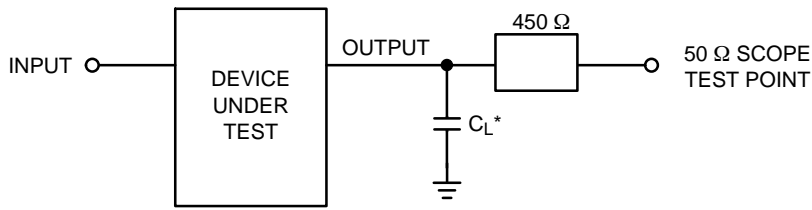


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

MC74ACT640

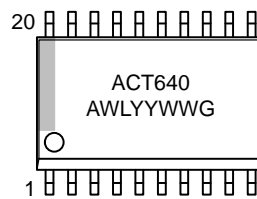
ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|----------------------|--------------------|
| MC74ACT640DWG | SOIC-20 (Pb-Free) | 38 Units / Rail |
| MC74ACT640DWR2G | SOIC-20 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

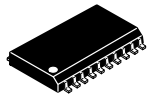
MARKING DIAGRAMS

SOIC-20W



- A = Assembly Location
- WL = Wafer Lot
- YY, Y = Year
- WW = Work Week
- G = Pb-Free Package

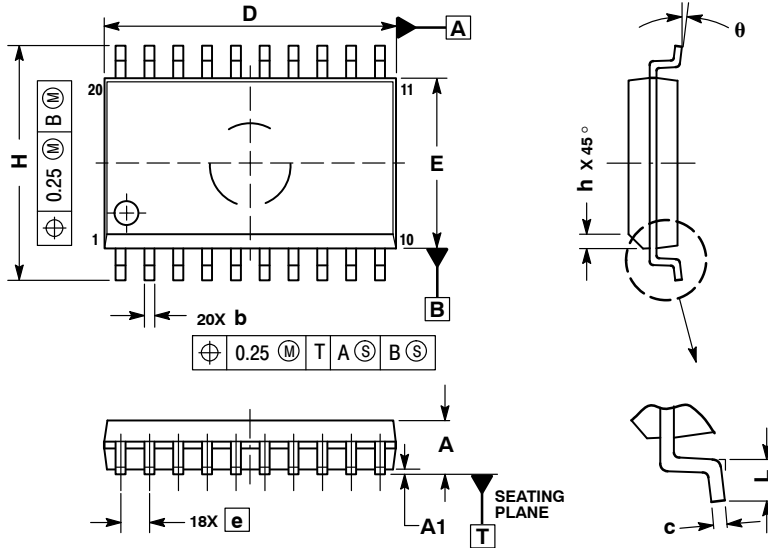
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

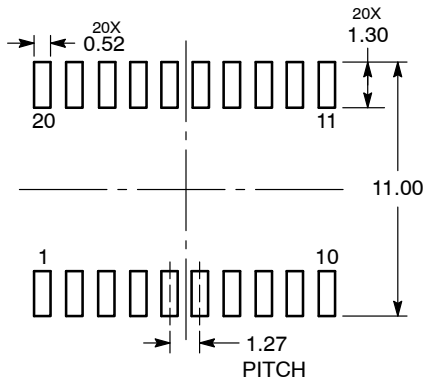


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

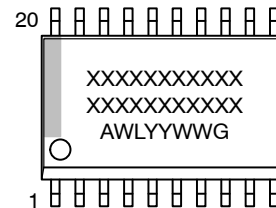
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|-------------|--|
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