INT-A-PAK™ "Half-Bridge" (Ultrafast Speed IGBT), 100 A

INT-A-PAK

FEATURES

- Generation 4 IGBT technology
- Ultrafast: Optimized for high speed 8 kHz to 40 kHz in hard switching, > 200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED® antiparallel diodes with ultrasoft recovery
- Industry standard package
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

PRODUCT SUMMARY	
V_{CES}	1200 V
I_C DC	182 A
$V_{CE(on)}$ at 100 A, 25 °C	2.25 V

BENEFITS

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, welding
- Lower EMI, requires less snubbing

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Collector to emitter voltage	V_{CES}		1200	V
Continuous collector current	I_C	T_C = 25 °C	182	A
		T_C = 93 °C	100	
Pulsed collector current	I_{CM}	Repetitive rating; V_{GE} = 20 V, pulse width limited by maximum junction temperature	200	
Peak switching current See fig. 17	I_{LM}		200	
Peak diode forward current	I_{FM}		200	
Gate to emitter voltage	V_{GE}		± 20	V
RMS isolation voltage	V_{ISOL}	Any terminal to case, t = 1 minute	2500	
Maximum power dissipation	P_D	T_C = 25 °C	520	W
		T_C = 85 °C	270	
Operating junction temperature range	T_J		- 40 to + 150	°C
Storage temperature range	T_{Stg}		- 40 to + 125	

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Collector to emitter breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0 V, I_C = 1 mA	1200	-	-	V
Collector to emitter voltage	$V_{CE(on)}$	V_{GE} = 15 V, I_C = 100 A	-	2.25	3	
		V_{GE} = 15 V, I_C = 100 A, T_J = 125 °C	-	2	2.4	
Gate threshold voltage	$V_{GE(th)}$	I_C = 1.25 mA	3.0	4.4	6.0	
Temperature coefficient of threshold voltage	$\Delta V_{GE(th)}/\Delta T_J$	$V_{CE} = V_{GE}$, I_C = 1.25 mA	-	- 12	-	mV/°C
Forward transconductance	g_{fe}	V_{CE} = 25 V, I_C = 100 A Pulse width 50 µs, single shot	-	136	-	S
Collector to emitter leaking current	I_{CES}	V_{GE} = 0 V, V_{CE} = 1200 V	-	0.03	1.0	mA
		V_{GE} = 0 V, V_{CE} = 1200 V, T_J = 125 °C	-	4.2	10	
Maximum diode forward voltage	V_{FM}	V_{GE} = 0 V, I_F = 100 A	-	3.3	4.0	V
		V_{GE} = 0 V, I_F = 100 A, T_J = 125 °C	-	3.2	3.8	
Gate to emitter leakage current	I_{GES}	V_{GE} = ± 20 V	-	-	250	nA

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Total gate charge (turn-on)	Q_g	V_{CC} = 400 V I_C = 124 A	-	830	1245	nC
Gate to emitter charge (turn-on)	Q_{ge}		-	140	210	
Gate to collector charge (turn-on)	Q_{gc}		-	275	412	
Turn-on delay time	$t_{d(on)}$	R_{g1} = 15 Ω R_{g2} = 0 Ω I_C = 100 A V_{CC} = 720 V V_{GE} = ± 15 V T_J = 25 °C	-	570	-	ns
Rise time	t_r		-	85	-	
Turn-off delay time	$t_{d(off)}$		-	581	-	
Fall time	t_f		-	276	-	
Turn-on switching energy	E_{on}		-	7.6	-	mJ
Turn-off switching energy	E_{off} (1)		-	6.8	-	
Total switching energy	E_{ts} (1)		-	14.4	-	
Turn-on delay time	$t_{d(on)}$	R_{g1} = 15 Ω R_{g2} = 0 Ω I_C = 100 A V_{CC} = 720 V V_{GE} = ± 15 V T_J = 125 °C	-	571	-	ns
Rise time	t_r		-	89	-	
Turn-off delay time	$t_{d(off)}$		-	606	-	
Fall time	t_f		-	649	-	
Turn-on switching energy	E_{on}		-	10	-	mJ
Turn-off switching energy	E_{off} (1)		-	16	-	
Total switching energy	E_{ts} (1)		-	26	45	
Input capacitance	C_{ies}	V_{GE} = 0 V V_{CC} = 30 V f = 1 MHz	-	18 672	-	pF
Output capacitance	C_{oes}		-	830	-	
Reverse transfer capacitance	C_{res}		-	161	-	
Diode reverse recovery time	t_{rr}	I_C = 100 A R_{g1} = 15 Ω R_{g2} = 0 Ω V_{CC} = 720 V dI/dt = 1300 A/µs	-	149	-	ns
Diode peak reverse current	I_{rr}		-	104	-	A
Diode recovery charge	Q_{rr}		-	7664	-	nC
Diode peak rate of fall of recovery during t_b	$dI_{(rec)M}/dt$		-	1916	-	A/µs

Note

(1) Repetitive rating; V_{GE} = 20 V, pulse width limited by maximum junction temperature

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER		**SYMBOL**	**TEST CONDITIONS**	**TYP.**	**MAX.**	**UNITS**
Thermal resistance, junction to case	IGBT	R_{thJC}		-	0.24	°C/W
	Diode			-	0.35	
Thermal resistance, case to sink per module		R_{thCS}		0.1	-	
Mounting torque	case to heatsink			-	4.0	Nm
	case to terminal 1, 2 and 3		For screws M5 x 0.8	-	3.0	
Weight of module				200	-	g

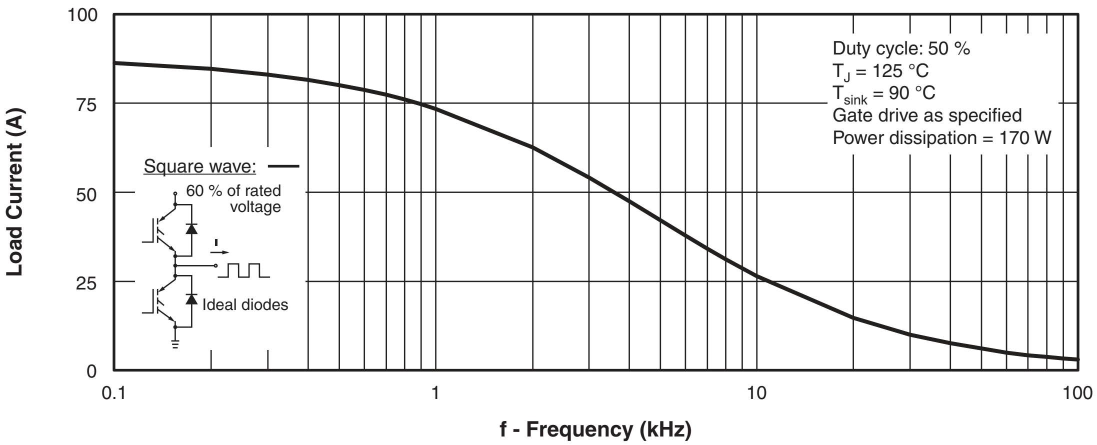


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of Fundamental)

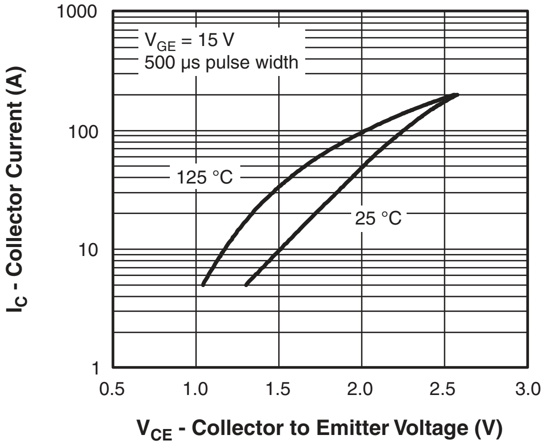


Fig. 2 - Typical Output Characteristics

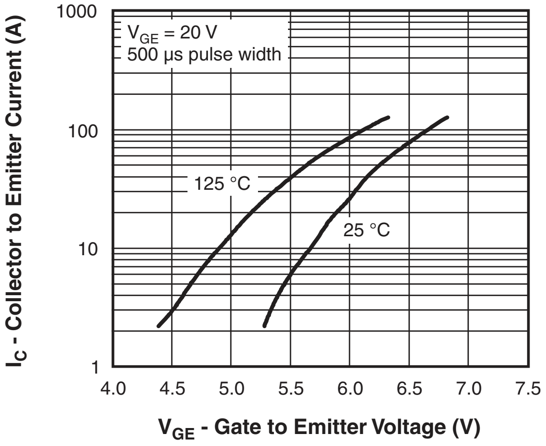


Fig. 3 - Typical Transfer Characteristics

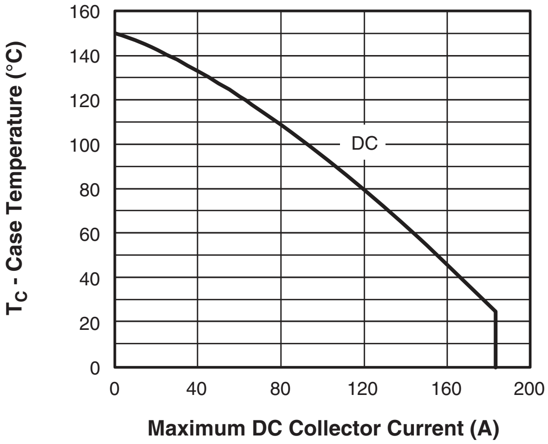


Fig. 4 - Case Temperature vs. Maximum Collector Current

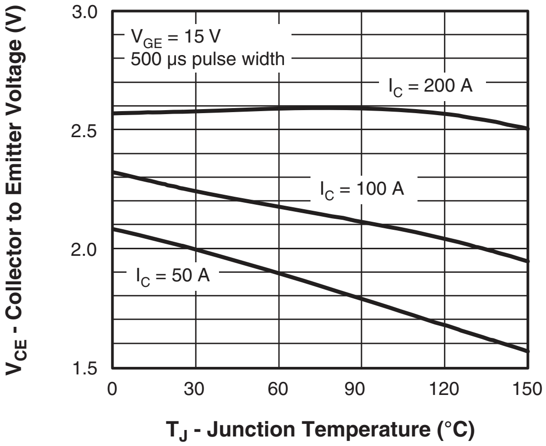


Fig. 5 - Typical Collector to Emitter Voltage vs. Junction Temperature

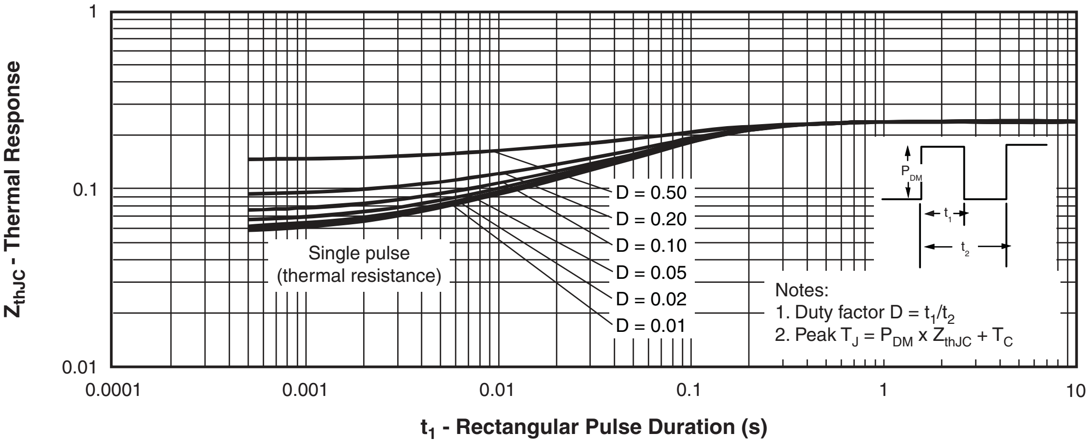


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction to Case

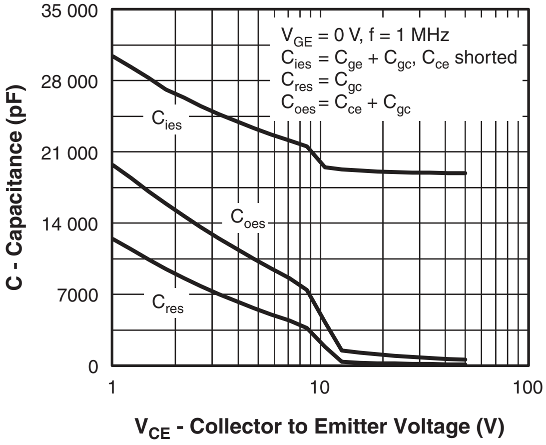


Fig. 7 - Typical Capacitance vs. Collector to Emitter Voltage

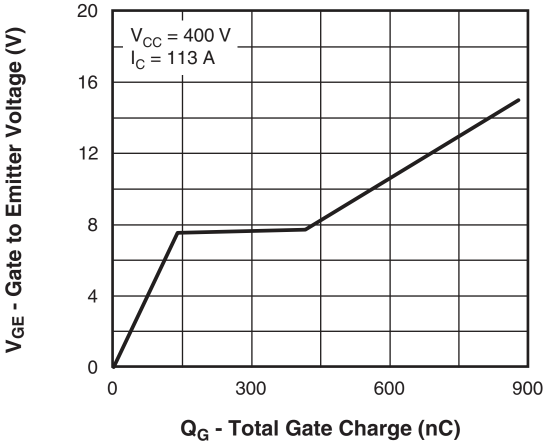


Fig. 8 - Typical Gate Charge vs. Gate to Emitter Voltage

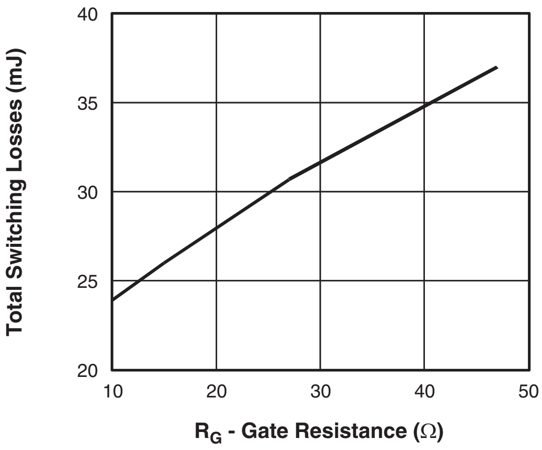


Fig. 9 - Typical Switching Losses vs. Gate Resistance

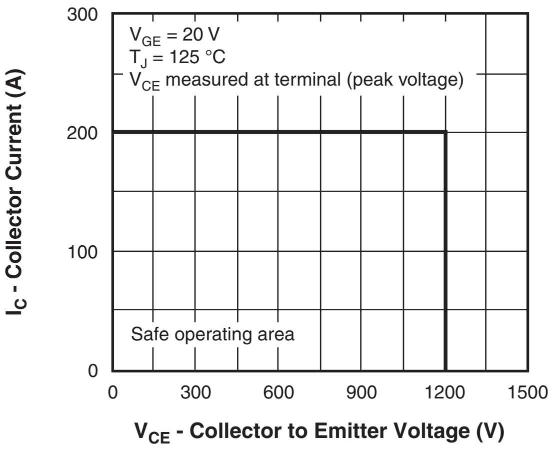


Fig. 12 - Reverse Bias SOA

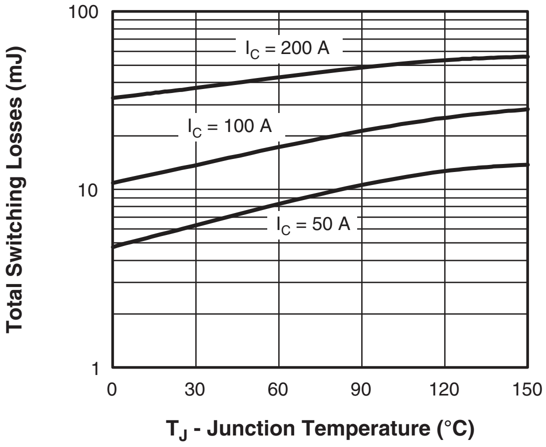


Fig. 10 - Typical Switching Losses vs. Junction Temperature

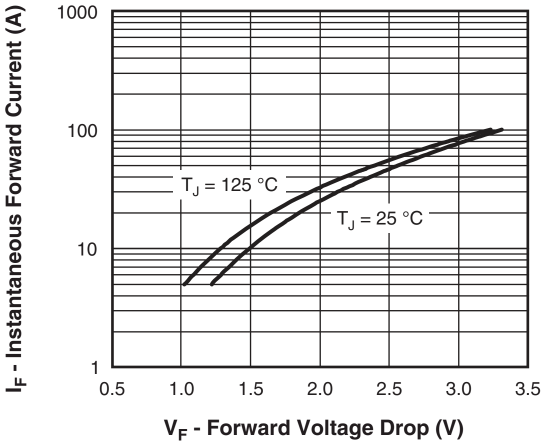


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

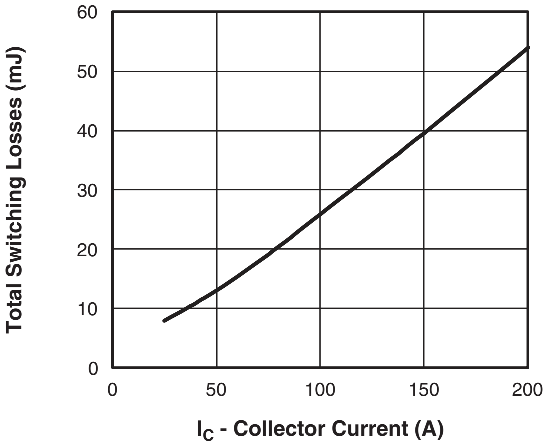


Fig. 11 - Typical Switching Losses vs. Collector Current

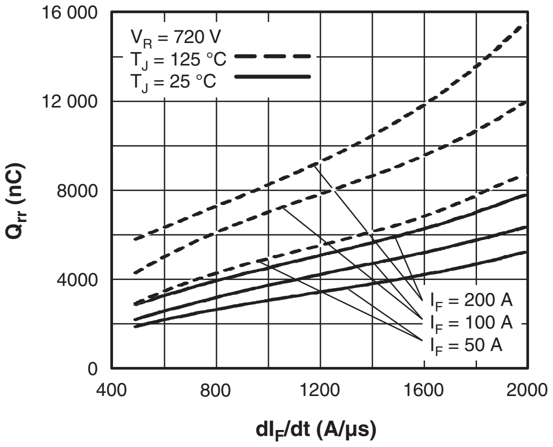


Fig. 14 - Typical Stored Charge vs. dI_F/dt

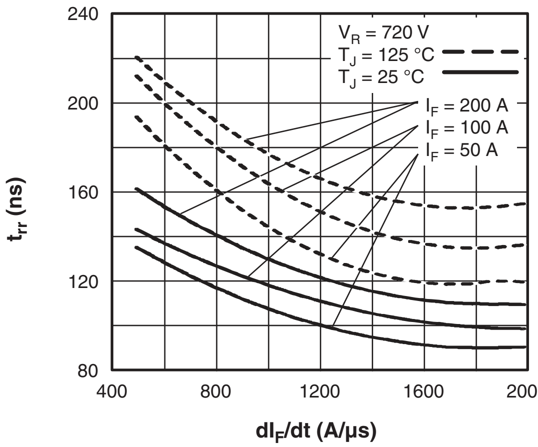


Fig. 15 - Typical Reverse Recovery Time vs. dI_F/dt

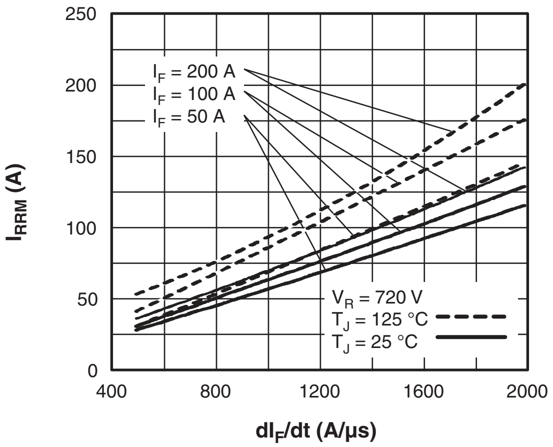


Fig. 16 - Typical Recovery Current vs. dI_F/dt

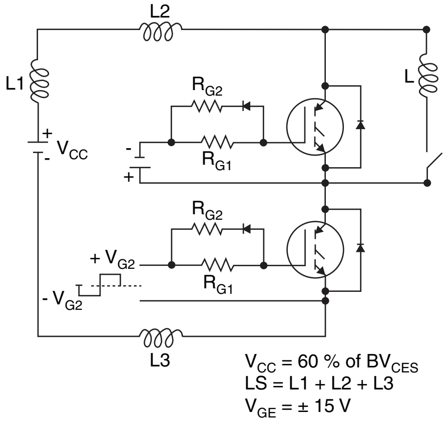


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

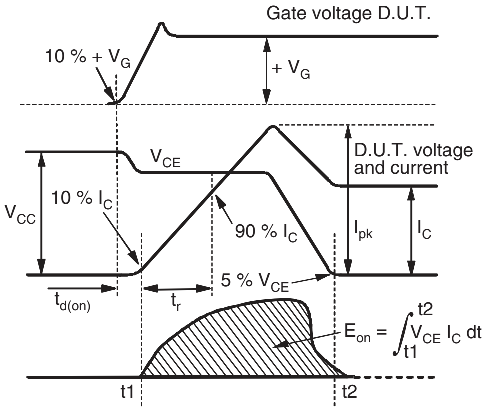


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

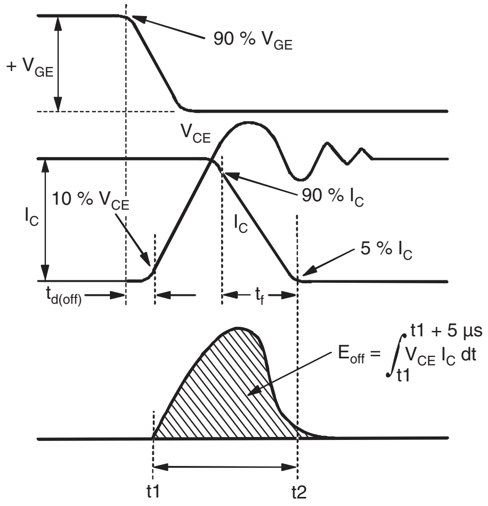


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

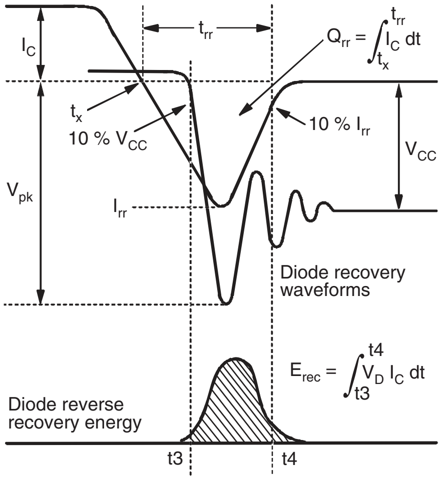


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

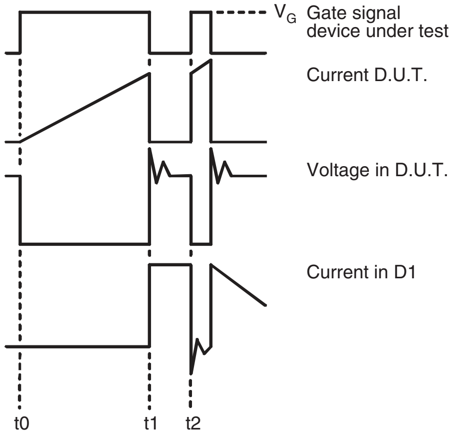
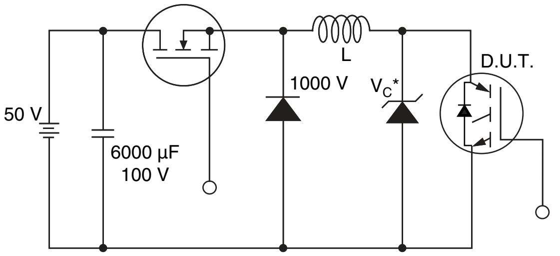


Fig. 17e - Macro Waveforms for Figure 18a's Test Circuit



* Driver same type as D.U.T.; V_C = 80 % of V_{CE} (max)

Note: Due to the 50 V power supply, pulse width and inductor will increase to obtain rated I_d

Fig. 18 - Clamped Inductive Load Test Circuit

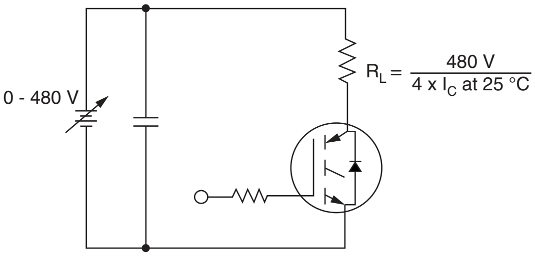


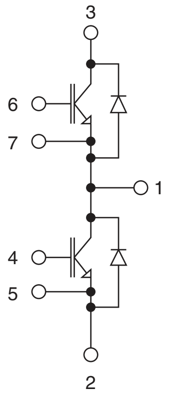
Fig. 19 - Pulsed Collector Current Test Circuit

ORDERING INFORMATION TABLE

Device code	VS-	G	A	100	T	S	120	U	PbF
	①	②	③	④	⑤	⑥	⑦	⑧	⑨

1 - Vishay Semiconductors product
2 - Insulated gate bipolar transistor (IGBT)
3 - Generation 4, IGBT silicon, DBC construction
4 - Current rating (100 = 100 A)
5 - Circuit configuration (T = Half-bridge)
6 - Package indicator (INT-A-PAK)
7 - Voltage rating (120 = 1200 V)
8 - Speed/type (U = Ultrafast)
9 - PbF = Lead (Pb)-free

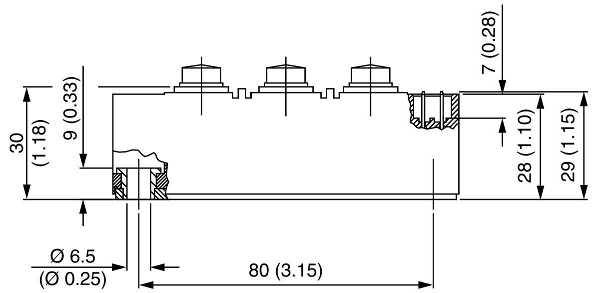
CIRCUIT CONFIGURATION

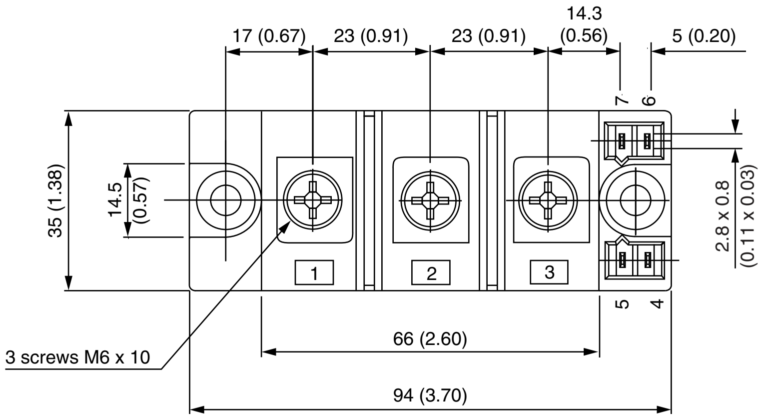


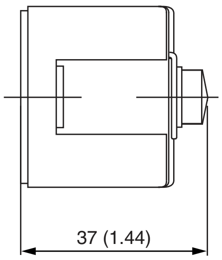
LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95173

INT-A-PAK IGBT

DIMENSIONS in millimeters (inches)







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