576Mb (x9, x18, x36) Common I/O RLDRAM® 2 Memory

JANUARY 2020

FEATURES

- 400MHz DDR operation (800Mb/s/pin data rate)
- 28.8Gb/s peak bandwidth (x36 at 400 MHz clock frequency)
- Reduced cycle time (15ns at 400MHz)
- 32ms refresh (16K refresh for each bank; 128K refresh command must be issued in total each 32ms)
- 8 internal banks
- Non-multiplexed addresses (address multiplexing option available)
- SRAM-type interface
- Programmable READ latency (RL), row cycle time, and burst sequence length
- Balanced READ and WRITE latencies in order to optimize data bus utilization
- Data mask signals (DM) to mask signal of WRITE data; DM is sampled on both edges of DK.
- Differential input clocks (CK, CK#)
- Differential input data clocks (DKx, DKx#)
- On-die DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- HSTL I/O (1.5V or 1.8V nominal)
- 25-60Ω matched impedance outputs
- 2.5V V_{EXT}, 1.8V V_{DD}, 1.5V or 1.8V V_{DDQ} I/O
- On-die termination (ODT) R_{TT}
- IEEE 1149.1 compliant JTAG boundary scan
- Operating temperature:
  Commercial
  (T_C = 0° to +95°C; T_A = 0°C to +70°C),
  Industrial
  (T_C = -40°C to +95°C; T_A = -40°C to +85°C)

OPTIONS

- Package:
  - 144-ball WBGA (lead-free)
- Configuration:
  - 64Mx9
  - 32Mx18
  - 16Mx36
- Clock Cycle Timing:

Speed Grade	-25E	-25	-33	-5	Unit
t_{RC}	15	20	20	20	ns
t_{CK}	2.5	2.5	3.3	5	ns

1 Package Ball out and Description

1.1 576Mb (64Mx9) Common I/O BGA Ball-out (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DNU[3]	DNU[3]	VSSQ					VSSQ	DQ0	DNU[3]	VDD
C	VTT	DNU[3]	DNU[3]	VDDQ					VDDQ	DQ1	DNU[3]	VTT
D	A22[1]	DNU[3]	DNU[3]	VSSQ					VSSQ	QK0#	QK0	VSS
E	A21	DNU[3]	DNU[3]	VDDQ					VDDQ	DQ2	DNU[3]	A20
F	A5	DNU[3]	DNU[3]	VSSQ					VSSQ	DQ3	DNU[3]	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	BA2	A9	VSS	VSS					VSS	VSS	A4	A3
J	NF[2]	NF[2]	VDD	VDD					VDD	VDD	BA0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	BA1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DNU[3]	DNU[3]	VSSQ					VSSQ	DQ4	DNU[3]	A19
P	A15	DNU[3]	DNU[3]	VDDQ					VDDQ	DQ5	DNU[3]	DM
R	VSS	DNU[3]	DNU[3]	VSSQ					VSSQ	DQ6	DNU[3]	VSS
T	VTT	DNU[3]	DNU[3]	VDDQ					VDDQ	DQ7	DNU[3]	VTT
U	VDD	DNU[3]	DNU[3]	VSSQ					VSSQ	DQ8	DNU[3]	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

Symbol	Description	Ball count
VDD	Supply voltage	16
VSS	Ground	16
VDDQ	DQ power supply	8
VSSQ	DQ Ground	12
VEXT	Supply voltage	4
VREF	Reference voltage	2
VTT	Termination voltage	4
A*	Address - A0-22	23
BA*	Banks - BA0-2	3
DQ*	I/O	9
DK*	Input data clock(Differential inputs)	2
QK*	Output data clocks(outputs)	2
CK*	Input clocks (CK, CK#)	2
DM	Input data mask	1
CS#,WE#,REF#	Command control pins	3
ZQ	External impedance (25–60Ω)	1
QVLD	Data valid	1
DNU,NF	Do not use, No function	31
T*	JTAG - TCK,TMS,TDO,TDI	4
Total		144

Notes:
1. Reserved for future use. This signal is not connected.
2. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to GND.
3. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND. Note that if ODT is enabled, these pins are High-Z.

1.2 576Mb (32Mx18) Common I/O BGA Ball-out (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DNU[4]	DQ4	VSSQ					VSSQ	DQ0	DNU[4]	VDD
C	VTT	DNU[4]	DQ5	VDDQ					VDDQ	DQ1	DNU[4]	VTT
D	A22[1]	DNU[4]	DQ6	VSSQ					VSSQ	QK0#	QK0	VSS
E	A21[2]	DNU[4]	DQ7	VDDQ					VDDQ	DQ2	DNU[4]	A20
F	A5	DNU[4]	DQ8	VSSQ					VSSQ	DQ3	DNU[4]	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	BA2	A9	VSS	VSS					VSS	VSS	A4	A3
J	NF[3]	NF[3]	VDD	VDD					VDD	VDD	BA0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	BA1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DNU[4]	DQ14	VSSQ					VSSQ	DQ9	DNU[4]	A19
P	A15	DNU[4]	DQ15	VDDQ					VDDQ	DQ10	DNU[4]	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	DQ11	DNU[4]	VSS
T	VTT	DNU[4]	DQ16	VDDQ					VDDQ	DQ12	DNU[4]	VTT
U	VDD	DNU[4]	DQ17	VSSQ					VSSQ	DQ13	DNU[4]	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

Symbol	Description	Ball count
VDD	Supply voltage	16
VSS	Ground	16
VDDQ	DQ power supply	8
VSSQ	DQ Ground	12
VEXT	Supply voltage	4
VREF	Reference voltage	2
VTT	Termination voltage	4
A*	Address - A0-22	23
BA*	Banks - BA0-2	3
DQ*	I/O	18
DK*	Input data clock(Differential inputs)	2
QK*	Output data clocks(outputs)	4
CK*	Input clocks (CK, CK#)	2
DM	Input data mask	1
CS#,WE#,REF#	Command control pins	3
ZQ	External impedance (25–60Ω)	1
QVLD	Data valid	1
DNU,NF	Do not use, No function	20
T*	JTAG - TCK,TMS,TDO,TDI	4
Total		144

Notes:
1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.
3. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to GND.
4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND. Note that if ODT is enabled, these pins are High-Z.

1.3 576Mb (16Mx36) Common I/O BGA Ball-out (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DQ8	DQ9	VSSQ					VSSQ	DQ1	DQ0	VDD
C	VTT	DQ10	DQ11	VDDQ					VDDQ	DQ3	DQ2	VTT
D	A22[1]	DQ12	DQ13	VSSQ					VSSQ	QK0#	QK0	VSS
E	A21[2]	DQ14	DQ15	VDDQ					VDDQ	DQ5	DQ4	A20[2]
F	A5	DQ16	DQ17	VSSQ					VSSQ	DQ7	DQ6	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	BA2	A9	VSS	VSS					VSS	VSS	A4	A3
J	DK0	DK0#	VDD	VDD					VDD	VDD	BA0	CK
K	DK1	DK1#	VDD	VDD					VDD	VDD	BA1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DQ24	DQ25	VSSQ					VSSQ	DQ35	DQ34	A19
P	A15	DQ22	DQ23	VDDQ					VDDQ	DQ33	DQ32	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	DQ31	DQ30	VSS
T	VTT	DQ20	DQ21	VDDQ					VDDQ	DQ29	DQ28	VTT
U	VDD	DQ18	DQ19	VSSQ					VSSQ	DQ27	DQ26	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

Symbol	Description	Ball count
VDD	Supply voltage	16
VSS	Ground	16
VDDQ	DQ power supply	8
VSSQ	DQ Ground	12
VEXT	Supply voltage	4
VREF	Reference voltage	2
VTT	Termination voltage	4
A*	Address - A0-22	23
BA*	Banks - BA0-2	3
DQ*	I/O	36
DK*	Input data clock(Differential inputs)	4
QK*	Output data clocks(outputs)	4
CK*	Input clocks (CK, CK#)	2
DM	Input data mask	1
CS#,WE#,REF#	Command control pins	3
ZQ	External impedance (25–60Ω)	1
QVLD	Data valid	1
DNU	Do not use	0
T*	JTAG - TCK,TMS,TDO,TDI	4
Total		144

Notes:
1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.

1.4 Ball Descriptions

Symbol	Type	Description
A*	Input	Address inputs: Defines the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK.
BA*	Input	Bank address inputs: Selects to which internal bank a command is being applied to.
CK, CK#	Input	Input clock: CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip select: CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
DQ*	I/O	Data input: The DQ signals form the data bus. During READ commands, the data is referenced to both edges of QK*. During WRITE commands, the data is sampled at both edges of DK.
DK*, DK*#	Input	Input data clock: DK* and DK*# are the differential input data clocks. All input data is referenced to both edges of DK*. DK*# is ideally 180 degrees out of phase with DK*. For the x36 device, DQ0–DQ17 are referenced to DK0 and DK0# and DQ18–DQ35 are referenced to DK1 and DK1#. For the x9 and x18 devices, all DQ* are referenced to DK and DK#. All DK* and DK*# pins must always be supplied to the device.
DM	Input	Input data mask: The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM is sampled on both edges of DK (DK1 for the x36 configuration). Tie signal to ground if not used.
TCK	Input	IEEE 1149.1 clock input: This ball must be tied to V_{SS} if the JTAG function is not used.
TMS,TDI	Input	IEEE 1149.1 test inputs: These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	Command inputs: Sampled at the positive edge of CK, WE# and REF# define (together with CS#) the command to be executed.
V_{REF}	Input	Input reference voltage: Nominally $V_{DDQ}/2$. Provides a reference voltage for the input buffers.
ZQ	I/O	External impedance (25–60Ω): This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 × RQ, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode.
QK*, QK*#	Output	Output data clocks: QK* and QK*# are opposite polarity, output data clocks. They are free running, and during READs, are edge-aligned with data output from the memory. QK*# is ideally 180 degrees out of phase with QK*. For the x36 device, QK0 and QK0# are aligned with DQ0-DQ17, and QK1 and QK1# are aligned with DQ18-DQ35. For the x18 device, QK0 and QK0# are aligned with DQ0-DQ8, while QK1 and QK1# are aligned with Q9-Q17. For the x9 device, all DQs are aligned with QK0 and QK0#.
QVLD	Output	Data valid: The QVLD pin indicates valid output data. QVLD is edge-aligned with QK* and QK*#.
TDO	Output	IEEE 1149.1 test output: JTAG output. This ball may be left as no connect if the JTAG function is not used.
V_{DD}	Supply	Power supply: Nominally, 1.8V.
V_{DDQ}	Supply	DQ power supply: Nominally, 1.5V or 1.8V. Isolated on the device for improved noise immunity.
V_{EXT}	Supply	Power supply: Nominally, 2.5V.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground: Isolated on the device for improved noise immunity.
V_{TT}	Supply	Power supply: Isolated termination supply. Nominally, $V_{DDQ}/2$.
A22	-	Reserved for future use: This signal is not connected and can be connected to ground.
DNU	-	Do not use: These balls may be connected to ground. Note that if ODT is enabled, these pins are High-Z.
NF	-	No function: These balls can be connected to ground.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Item	Min	Max	Units
I/O Voltage	– 0.3	V_{DDQ} + 0.3	V
Voltage on V_{EXT} supply relative to V_{SS}	– 0.3	+ 2.8	V
Voltage on V_{DD} supply relative to V_{SS}	– 0.3	+ 2.1	V
Voltage on V_{DDQ} supply relative to V_{SS}	– 0.3	+ 2.1	V

Note: Stress greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.2 DC Electrical Characteristics and Operating Conditions

Description	Conditions	Symbol	Min	Max	Units	Notes
Supply voltage		V_{EXT}	2.38	2.63	V	
Supply voltage		V_{DD}	1.7	1.9	V	2
Isolated output buffer supply		V_{DDQ}	1.4	VDD	V	2,3
Reference voltage		V_{REF}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	4,5,6
Termination voltage		V_{TT}	0.95 x V_{REF}	1.05 x V_{REF}	V	7,8
Input high voltage		V_{IH}	V_{REF} + 0.1	V_{DDQ} + 0.3	V	2
Input low voltage		V_{IL}	V_{SSQ} – 0.3	V_{REF} – 0.1	V	2
Output high current	V_{OH} = V_{DDQ}/2	I_{OH}	(V_{DDQ}/2)/ (1.15 x RQ/5)	(V_{DDQ}/2)/ (0.85 x RQ/5)	A	9, 10, 11
Output low current	V_{OL} = V_{DDQ}/2	I_{OL}	(V_{DDQ}/2)/ (1.15 x RQ/5)	(V_{DDQ}/2)/ (0.85 x RQ/5)	A	9, 10, 11
Clock input leakage current	0V ≤ V_{IN} ≤ V_{DD}	I_{LC}	– 5	5	µA	
Input leakage current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	– 5	5	µA	
Output leakage current	0V ≤ V_{IN} ≤ V_{DDQ}	I_{LO}	– 5	5	µA	
Reference voltage current		I_{REF}	– 5	5	µA	

Notes:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} (AC) ≤ V_{DD} + 0.7V for t ≤ t_{CK}/2. Undershoot: V_{IL} (AC) ≥ –0.5V for t ≤ t_{CK}/2. During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals may not have pulse widths less than t_{CK}/2 or operate at frequencies exceeding t_{CK} (MAX).
3. V_{DDQ} can be set to a nominal 1.5V ± 0.1V or 1.8V ± 0.1V supply.
4. Typically the value of V_{REF} is expected to be 0.5 x V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
5. Peak-to-peak AC noise on V_{REF} must not exceed ±2 percent V_{REF} (DC).
6. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from V_{DDQ}/2, V_{REF} is allowed ±2 percent V_{DDQ}/2 for DC error and an additional ±2 percent V_{DDQ}/2 for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. On-die termination may be selected using mode register A9 (for non-multiplexed address mode) or Ax9 (for multiplexed address mode). A resistance R_{TT} from each data input signal to the nearest V_{TT} can be enabled. R_{TT} = 125–185Ω at 95°C T_C.
9. I_{OH} and I_{OL} are defined as absolute values and are measured at V_{DDQ} /2. I_{OH} flows from the device, I_{OL} flows into the device.
10. If MRS bit A8 or Ax8 is 0, use RQ = 250Ω in the equation in lieu of presence of an external impedance matched resistor.

2.3 Capacitance (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Test Conditions	Min	Max	Units
Address / Control Input capacitance	C_{IN}	V_{IN}=0V	1.5	2.5	pF
I/O, Output, Other capacitance (DQ, DM, QK, QVLD)	C_{IO}	V_{IO}=0V	3.5	5.0	pF
Clock Input capacitance	C_{CLK}	V_{CLK}=0V	2.0	3.0	pF
JTAG pins	C_J	V_J=0V	2.0	5.0	pF

Note. These parameters are not 100% tested and capacitance is not tested on ZQ pin.

2.4 Operating Conditions and Maximum Limits

Description	Condition	Symbol	-25E	-25	-33	-5	units
Standby current	t_{CK} = idle; All banks idle; No inputs toggling	ISB1(V_{DD}) x9/x18	53	48	48	48	mA
		ISB1(V_{DD}) x36	53	48	48	48	
		ISB1(V_{EXT})	5	5	5	5	
Active standby current	CS# =1; No commands; Bank address incremented and half address/data change once every 4 clock cycles	ISB2(V_{DD}) x9/x18	293	288	233	189	mA
		ISB2(V_{DD}) x36	293	288	233	189	
		ISB2(V_{EXT})	5	5	5	5	
Operational current	BL=2; Sequential bank access; Bank transitions once every t_{RC}; Half address transitions once every t_{RC}; Read followed by write sequence; continuous data during WRITE commands	IDD1(V_{DD}) x9/x18	380	348	305	255	mA
		IDD1(V_{DD}) x36	400	374	343	292	
		IDD1(V_{EXT})	15	15	13	13	
	BL = 4; Sequential bank access; Bank transitions once every t_{RC}; Half address transitions once every tRC; Read followed by write sequence; Continuous data during WRITE commands	IDD2(V_{DD}) x9/x18	400	362	319	269	mA
		IDD2(V_{DD}) x36	425	418	389	339	
		IDD2(V_{EXT})	15	15	13	13	
	BL = 8; Sequential bank access; Bank transitions once every t_{RC}; half address transitions once every tRC; Read followed by write sequence; continuous data during WRITE commands	IDD3 (V_{DD}) x9/x18	430	408	368	286	mA
		IDD3 (V_{DD}) x36	540	460	425	425	
		IDD3(V_{EXT})	20	20	18	18	
Burst refresh current	Eight-bank cyclic refresh; Continuous address/data; Command bus remains in refresh for all eight banks	IREF1(V_{DD}) x9/x18	790	785	615	430	mA
		IREF1(V_{DD}) x36	915	785	615	430	
		IREF1(V_{EXT})	80	80	70	70	
Distributed refresh current	Single-bank refresh; Sequential bank access; Half address transitions once every t_{RC}, continuous data	IREF2(V_{DD}) x9/x18	330	325	267	221	mA
		IREF2(V_{DD}) x36	390	326	281	227	
		IREF2(V_{EXT})	20	20	18	18	
Operating burst write current	BL=2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; measurement is taken during continuous WRITE	IDD2W(V_{DD}) x9/x18	980	970	819	597	mA
		IDD2W(V_{DD}) x36	1105	990	914	676	
		IDD2W(V_{EXT})	50	50	40	40	
	BL=4; Cyclic bank access; Half of address bits change every 2 clock cycles; Continuous data; Measurement is taken during continuous WRITE	IDD4W(V_{DD}) x9/x18	785	779	609	439	mA
		IDD4W(V_{DD}) x36	887	882	790	567	
		IDD4W(V_{EXT})	30	30	25	25	
	BL=8; Cyclic bank access; Half of address bits change every 4 clock cycles; continuous data; Measurement is taken during continuous WRITE	IDD8W(V_{DD}) x9/x18	675	668	525	364	mA
		IDD8W(V_{DD}) x36	755	750	580	580	
		IDD8W(V_{EXT})	30	30	25	25	
Operating burst read current	BL=2; Cyclic bank access; Half of address bits change every clock cycle; Measurement is taken during continuous READ	IDD2R(V_{DD}) x9/x18	940	935	735	525	mA
		IDD2R(V_{DD}) x36	995	990	795	565	
		IDD2R(V_{EXT})	50	50	40	40	
	BL=4; Cyclic bank access; Half of address bits change every clock cycle; Measurement is taken during continuous READ	IDD4R(V_{DD}) x9/x18	685	680	525	380	mA
		IDD4R(V_{DD}) x36	735	730	660	455	
		IDD4R(V_{EXT})	30	30	25	25	
	BL=8; Cyclic bank access; Half of address bits change every clock cycle; Measurement is taken during continuous READ	IDD8R(V_{DD}) x9/x18	575	570	450	310	mA
		IDD8R(V_{DD}) x36	665	660	505	505	
		IDD8R(V_{EXT})	30	30	25	25	

Notes:
1) IDD specifications are tested after the device is properly initialized. +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, +2.38V ≤ V_{EXT} ≤ +2.63V, +1.4V ≤ V_{DDQ} ≤ V_{DD}, V_{REF} = V_{DDQ}/2.
2) t_{CK} = t_{DK} = MIN, t_{RC} = MIN.
3) Definitions for IDD conditions:
   a. LOW is defined as V_{IN} ≤ V_{IL}(AC) MAX.
   b. HIGH is defined as V_{IN} ≥ V_{IH}(AC) MIN.
   c. Stable is defined as inputs remaining at a HIGH or LOW level.
   d. Floating is defined as inputs at V_{REF} = V_{DDQ}/2.
   e. Continuous data is defined as half the D or Q signals changing between HIGH and LOW every half clock cycle (twice per clock).
   f. Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
   g. Sequential bank access is defined as the bank address incrementing by one every t_{RC}.
   h. Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
4) CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
5) IDD parameters are specified with ODT disabled.
6) Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
7) IDD tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#). Parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

2.5 Recommended AC Operating Conditions

(+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input HIGH voltage	V_{IH}(AC)	V_{REF} + 0.2	-	V
Input LOW voltage	V_{IL}(AC)	-	V_{REF} – 0.2	V

Notes:
1. Overshoot: V_{IH} (AC) ≤ V_{DDQ} + 0.7V for t ≤ t_{CK}/2
2. Undershoot: V_{IL} (AC) ≥ – 0.5V for t ≤ t_{CK}/2
3. Control input signals may not have pulse widths less than t_{CKH}(MIN) or operate at cycle rates less than t_{CK}(MIN.).

2.6 Temperature and Thermal Impedance

Temperature Limits

Parameter	Symbol	Min	Max	Units
Reliability junction temperature [1]	T_J	0	+110	°C
Operating junction temperature [2]	T_J	0	+100	°C
Operating case temperature [3]	T_C	0	+95	°C

Notes:
1. Temperatures greater than 110°C may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or above this is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the part.
2. Junction temperature depends upon cycle time, loading, ambient temperature, and airflow.
3. MAX operating case temperature; T_C is measured in the center of the package. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.

Thermal Resistance

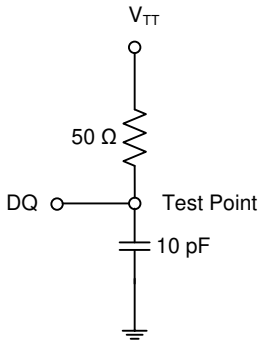
Package	Substrate	Theta-ja (Airflow = 0m/s)	Theta-ja (Airflow = 1m/s)	Theta-ja (Airflow = 2m/s)	Theta-jc	Unit
144-ball FBGA	**4-layer**	**20.6**	**19.1**	**17.2**	**2.4**	**C/W**

2.7 AC Electrical Characteristics [1, 2, 3, 4]

Description	Symbol	-25E (2.5ns @t_{RC}=15ns)		-25 (2.5ns @t_{RC}=20ns)		-33 (3.3ns @t_{RC}=20ns)		-5 (5ns @t_{RC}=20ns)		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Input clock cycle time	t_{CK}	2.5	5.7	2.5	5.7	3.3	5.7	5.0	5.7	ns
Input data clock cycle time	t_{DK}	tCK	–	tCK	–	tCK	–	tCK	–	ns
Clock jitter: period [5, 6]	t_{JITPER}	–150	150	–150	150	–200	200	–250	250	ps
Clock jitter: cycle-to-cycle	t_{JITCC}	–	300	–	300	–	400	–	500	ps
Clock HIGH time	t_{CKH}/t_{DKH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
Clock LOW time	t_{CKL}/t_{DKL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
Clock to input data clock	t_{CKDK}	–0.45	0.5	–0.45	0.5	–0.45	1.2	–0.3	1.5	ns
Mode register set cycle time to any command	t_{MRSC}	6	–	6	–	6	–	6	–	t_{CK}
Address/command and input setup time	t_{AS}/t_{CS}	0.4	–	0.4	–	0.5	–	0.8	–	ns
Data-in and data mask to DK setup time	t_{DS}	0.25	–	0.25	–	0.3	–	0.4	–	ns
Address/command and input hold time	t_{AH}/t_{CH}	0.4	–	0.4	–	0.5	–	0.8	–	ns
Data-in and data mask to DK hold time	t_{DH}	0.25	–	0.25	–	0.3	–	0.4	–	ns
Output data clock HIGH time	t_{QKH}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CKH}
Output data clock LOW time	t_{QKL}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CKL}
Half-clock period	t_{QHP}	MIN(t_{QKH}, t_{QKL})	–	MIN(t_{QKH}, t_{QKL})	–	MIN(t_{QKH}, t_{QKL})	–	MIN(t_{QKH}, t_{QKL})	–	
QK edge to clock edge skew	t_{CKQK}	–0.25	0.25	–0.25	0.25	–0.3	0.3	–0.5	0.5	ns
QK edge to output data edge [7]	t_{QKQ0}, t_{QKQ1}	–0.2	0.2	–0.2	0.2	–0.25	0.25	–0.3	0.3	ns
QK edge to any output data edge [8]	t_{QKQ}	–0.3	0.3	–0.3	0.3	–0.35	0.35	–0.4	0.4	ns
QK edge to QVLD	t_{QKVLD}	–0.3	0.3	–0.3	0.3	–0.35	0.35	–0.4	0.4	ns
Data valid window	t_{DVW}	t_{QHP} - (t_{QKQx} [MAX] + |t_{QKQx} [MIN]|)	–	t_{QHP} - (t_{QKQx} [MAX] + |t_{QKQx} [MIN]|)	–	t_{QHP} - (t_{QKQx} [MAX] + |t_{QKQx} [MIN]|)	–	t_{QHP} - (t_{QKQx} [MAX] + |t_{QKQx} [MIN]|)	–	
Average periodic refresh interval [9]	t_{REFI}	–	0.24	–	0.24	–	0.24	–	0.24	µs

Notes:

1. All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V_{REF} of the command, address, and data signals.
2. Outputs measured with equivalent load:



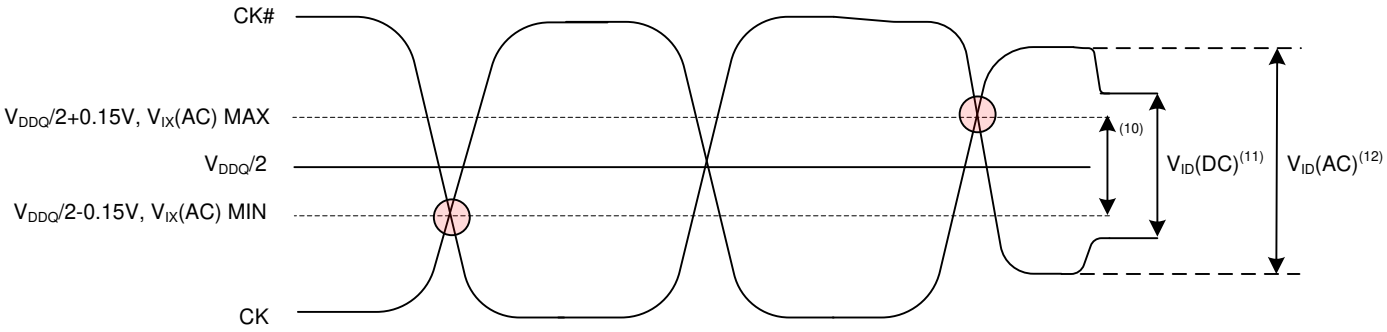
3. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
4. AC timing may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. Frequency drift is not allowed.
7. For a x36 device, DQ0-DQ17 is referenced to t_{QKQ0} and DQ18-DQ35 is referenced to t_{QKQ1}. For a x18 device, DQ0-DQ8 is referenced to t_{QKQ0} and DQ9-DQ17 is referenced to t_{QKQ1}. For a x9 device, t_{QKQ0} is referenced to DQ0-DQ8.
8. t_{QKQ} takes into account the skew between any QK*x* and any Q.
9. To improve efficiency, eight AREF commands (one for each bank) can be posted to the memory on consecutive cycles at periodic intervals of 1.95µs.

2.8 Clock Input Conditions

Differential Input Clock Operating Conditions

Parameter	Symbol	Min	Max	Units	Notes
Clock Input Voltage Level	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Clock Input Differential Voltage Level	V_{ID}(DC)	0.2	V_{DDQ}+0.6	V	8
Clock Input Differential Voltage Level	V_{ID}(AC)	0.4	V_{DDQ}+0.6	V	8
Clock Input Crossing Point Voltage Level	V_{IX}(AC)	V_{DDQ}/2-0.15	V_{DDQ}/2+0.15	V	9

Clock Input Example



Notes:

1. DKx and DKx# have the same requirements as CK and CK#.
2. All voltages referenced to V_{SS}.
3. Tests for AC timing, IDD and electrical AC and DC characteristics may be conducted at normal reference/supply voltage levels; but the related specifications and device operations are tested for the full voltage range specified.
4. AC timing and IDD tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or the crossing point for CK/CK#), and parameters specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. The AC and DC input level specifications are as defined in the HSTL Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above[below] the DC input LOW[HIGH] level).
6. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signal other than CK/CK# is V_{REF}.
7. CK and CK# input slew rate must be ≥ 2V/ns (≥ 4V/ns if measured differentially).
8. V_{ID} is the magnitude of the difference between the input level on CK and input level on CK#.
9. The value of V_{IX} is expected to equal V_{DDQ}/2 of the transmitting device and must track variations in the DC level of the same.
10. CK and CK# must cross within the region.
11. CK and CK# must meet at least V_{ID}(DC) (MIN.) when static and centered on V_{DDQ}/2.
12. Minimum peak-to-peak swing.

3 Functional Descriptions

3.1 Power-up and Initialization (1)

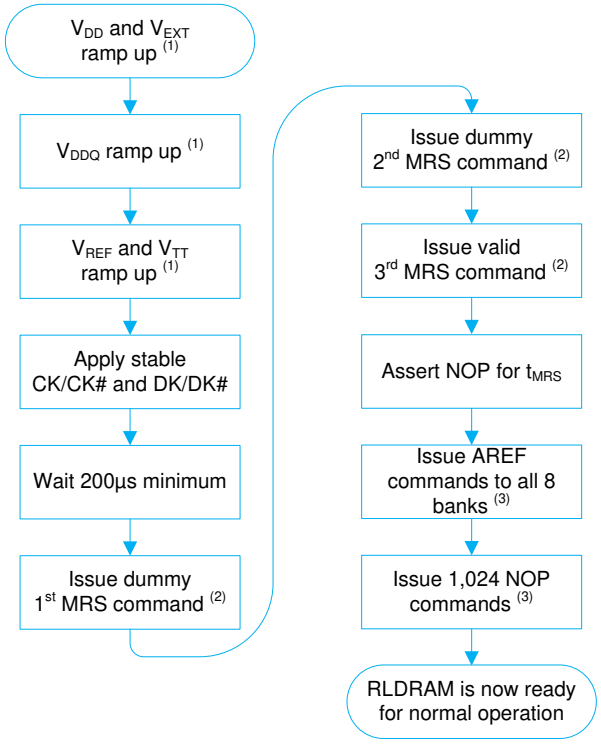
The RLDRAM® 2 Memory must be powered-up and initialized using the specific steps listed below:

1. Apply power by ramping up supply voltages V_{EXT}, V_{DD}, V_{DDQ}, V_{REF}, and V_{TT}. Apply V_{DD} and V_{EXT} before or at the same time as V_{DDQ} (2). Power-up sequence begins when both V_{DD} and V_{EXT} approach their nominal levels. Afterwards, apply V_{DDQ} before or at the same time as V_{REF} and V_{TT}. Once the supply voltages are stable, clock inputs CK/CK# and DK/DK# can be applied. Register NOP commands to the control pins to avoid issuing unwanted commands to the device.
2. Keep applying stable conditions for a minimum of 200 µs.
3. Register at least three consecutive MRS commands consisting of two or more dummy MRS commands and one valid MRS command. Timing parameter t_{MRSC} is not required to be met during these consecutive MRS commands but asserting a LOW logic to the address signals is recommended.
4. t_{MRSC} timing delay after the valid MRS command, Auto Refresh commands to all 8 banks and 1,024 NOP commands must be issued prior to normal operation. The Auto Refresh commands to the 8 banks can be issued in any order with respect to the 1,024 NOP commands. Please note that the tRC timing parameter must be met between an Auto Refresh command and a valid command in the same bank.
5. The device is now ready for normal operation.

Notes:

1. Operational procedure other than the one listed above may result in undefined operations and may permanently damage the device.
2. V_{DDQ} can be applied before V_{DD} but will result in all DQ data pin, DM, and output pins to go logic HIGH (instead of tri-state) and will remain HIGH until the V_{DD} is the same level as V_{DDQ}. This method is not recommended to avoid bus conflicts during the power-up.

3.2 Power-up and Initialization Flowchart

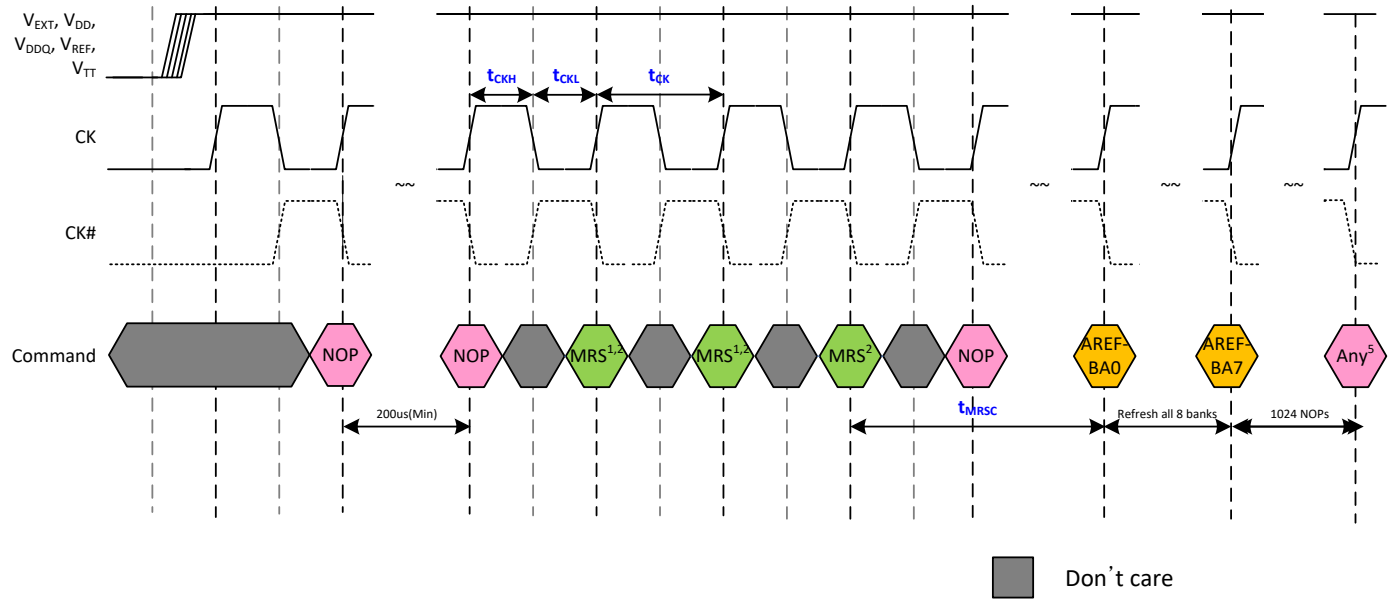


Notes:

1. The supply voltages can be ramped up simultaneously.
2. The dummy and valid MRS commands must be issued in consecutive clock cycles. At least two dummy MRS commands are required. It is recommended to assert a LOW logic on the address signals during the dummy MRS commands.
3. The Auto Refresh commands can be issued in any order with respect to the 1,024 NOP commands. However, timing parameter t_{RC} must be met before issuing any valid command in a bank after an AREF command to the same bank has been issued.

3.3 Power-up and Initialization Timing Diagram

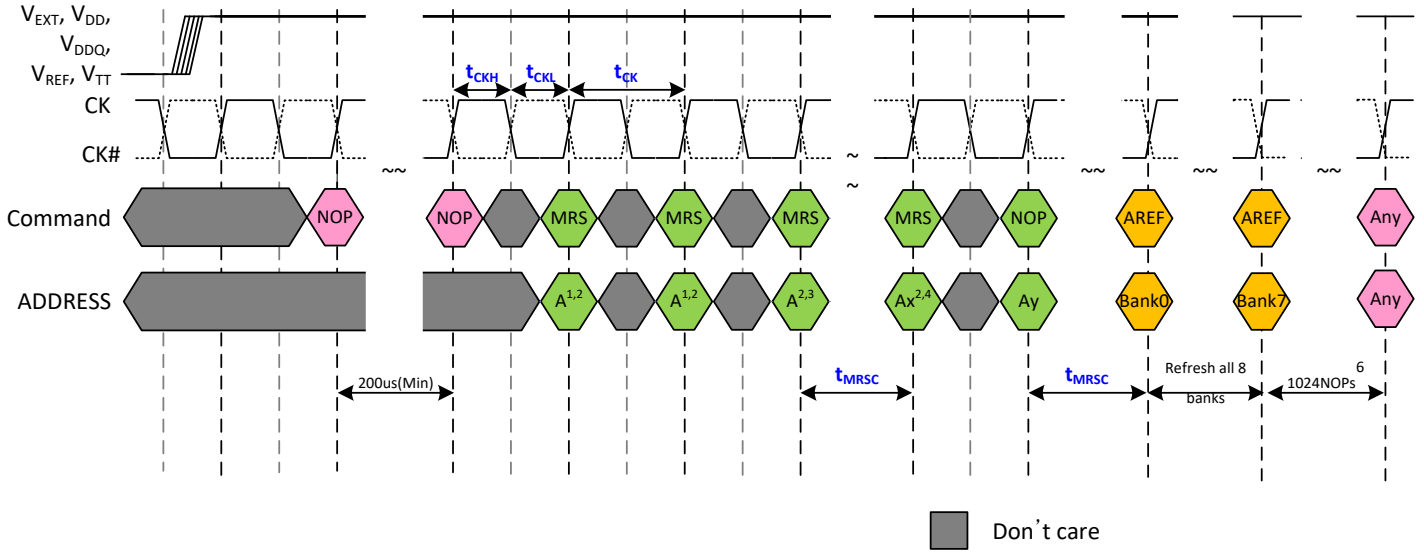
Non-multiplexed Address Mode



Notes:

1. It is recommended that the address input signals be driven LOW during the dummy MRS commands.
2. A10–A17 must be LOW.
3. DLL must be reset if t_{CK} or V_{DD} are changed.
4. CK and CK# must be separated at all times to prevent invalid commands from being issued.
5. The Auto Refresh commands can be issued in any order with respect to the 1,024 NOP commands. However, timing parameter t_{RC} must be met before issuing any valid command in a bank after an AREF command to the same bank has been issued.

Multiplexed Address Mode

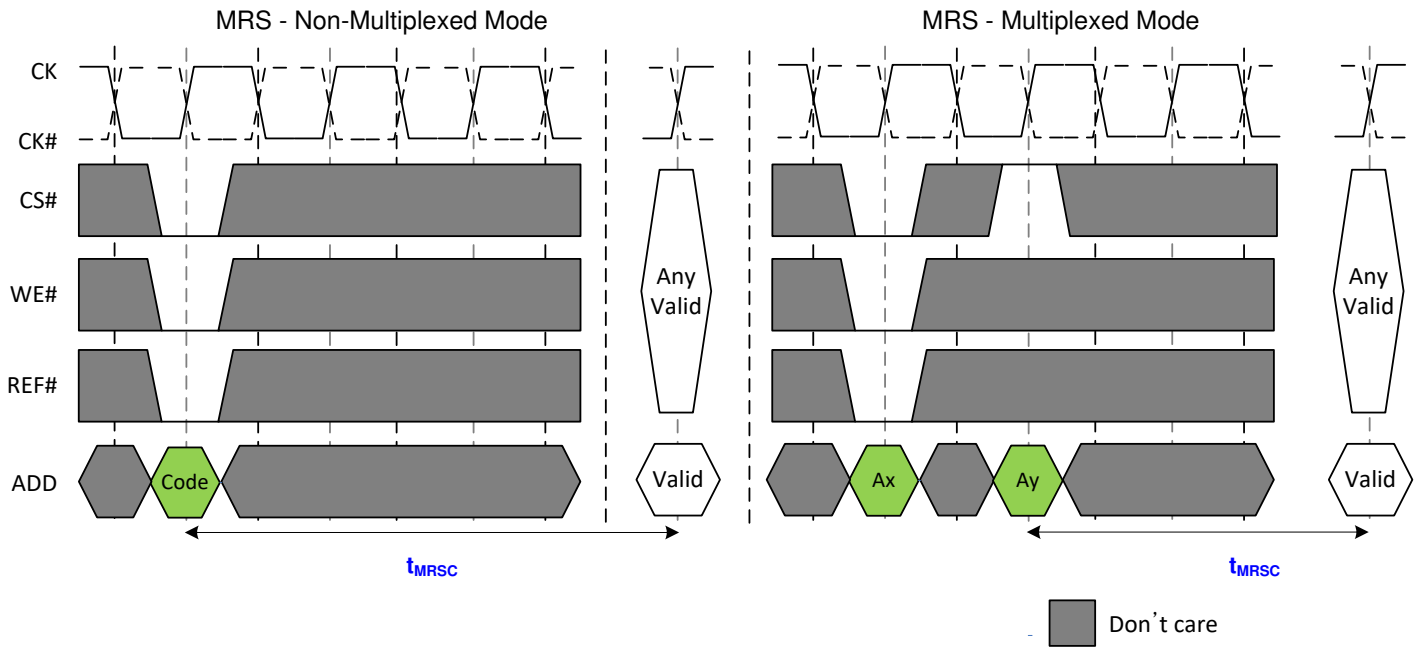


Notes:

1. It is recommended that the address input signals be driven LOW during the dummy MRS commands.
2. A10–A18 must be LOW.
3. Set address A5 HIGH. This enables the part to enter multiplexed address mode when in moon-multiplexed mode operation. Multiplexed address mode can also be entered at some later time by issuing an MRS command with A5 HIGH. Once address bit A5 is set HIGH, tMRSC must be satisfied before the two cycle multiplexed mode MRS command is issued.
4. Address A5 must be set HIGH. This and the following step set the desired mode register once the memory is in multiplexed address mode.

5. CK and CK# must be separated at all times to prevent invalid commands from being issued.
6. The Auto Refresh commands can be issued in any order with respect to the 1,024 NOP commands. However, timing parameter t_{RC} must be met before issuing any valid command (Any) in a bank after an AREF command to the same bank has been issued.

3.4 Mode Register Setting and Features



Note: The MRS command can only be issued when all banks are idle and no bursts are in progress.

The Mode Register Set command stores the data for controlling the various operating modes of the memory using address inputs A0-A17 as mode registers. During the MRS command, the cycle time and the read/write latency of the memory can be selected from different configurations. The MRS command also programs the memory to operate in either Multiplexed Address Mode or Non-multiplexed Address Mode. In addition, several features can be enabled using the MRS command. These are the DLL, Drive Impedance Matching, and On-Die Termination (ODT). t_{MRSC} must be met before any command can be issued. t_{MRSC} is measured like the picture above in both Multiplexed and Non-multiplexed mode.

Mode Register Diagram (Non-multiplexed Address Mode)

Address Field	Mode Register	
A10-17	M10-17	0 [1]
A9	M9	ODT
A8	M8	IM
A7	M7	DLL
A6	M6	NA [2]
A5	M5	AM
A4	M4	BL
A3	M3	
A2	M2	Config
A1	M1	
A0	M0	

A9	On-Die Termination
0	Off (Default)
1	On

A8	Drive Impedance
0	Internal 50Ω [5] (Default)
1	External(ZQ)

A7	DLL Reset
0	DLL reset [4] (Default)
1	DLL enable

A5	Address MUX
0	Non-multiplexed (Default)
1	Multiplexed

A4	A3	Burst Length(BL)
0	0	2 (Default)
0	1	4
1	0	8
1	1	Reserved

			Read/Write Latency and Cycle Time Configuration [6]				Valid Frequency Range
A2	A1	A0	Configuration	tRC(tCK)	tRL(tCK)	tWL(tCK)	(MHz)
0	0	0	1 [3] (Default)	4	4	5	266-175
0	0	1	1 [3]	4	4	5	266-175
0	1	0	2	6	6	7	400-175
0	1	1	3	8	8	9	533-175 [8]
1	0	0	4 [3,7]	3	3	4	200-175
1	0	1	5	5	5	6	333-175
1	1	0	Reserved	n/a	n/a	n/a	n/a
1	1	1	Reserved	n/a	n/a	n/a	n/a

Notes:
1. A10-A17 must be set to zero; A18-An are "Don't cares."
2. A6 not used in MRS.
3. BL = 8 is not available.
4. DLL RESET turns the DLL off.
5. ±30 % temperature variation.
6. t_{RC} < 20ns in any configuration is only available with -25E and -18 speed grades.
7. The minimum tRC is typically 3 cycles, except in the case of a WRITE followed by a READ to the same bank. In this instance the minimum t_{RC} is 4 cycles.
8. tCK must be met to use this configuration. For tCK values, please refer to AC Electrical Characteristics table.

Mode Register Diagram (Multiplexed Address Mode)

Ax	Ay	Mode Register	
A10-18	A10-18	M10-18	0 [1]
A9		M9	ODT
A8		M8	IM
	A9	M7	DLL
	A8	M6	NA [5]
A5		M5	AM
A4		M4	BL
A3		M3	
	A4	M2	Config
	A3	M1	
A0		M0	

A9	On-Die Termination
0	Off (Default)
1	On

A8	Drive Impedance
0	Internal 50Ω [6] (Default)
1	External(ZQ)

A7	DLL Reset
0	DLL reset [4] (Default)
1	DLL enable

A5	Address MUX
0	Non-multiplexed (Default)
1	Multiplexed

A4	A3	Burst Length(BL)
0	0	2 (Default)
0	1	4
1	0	8
1	1	Reserved

			Read/Write Latency and Cycle Time Configuration [8]				Valid Frequency
Ay4	Ay3	Ax0	Configuration	tRC(tCK)	tRL(tCK)	tWL(tCK)	Range (MHz)
0	0	0	1 [2] (Default)	4	5	6	266-175
0	0	1	1 [2]	4	5	6	266-175
0	1	0	2	6	7	8	400-175
0	1	1	3	8	9	10	533-175 [10]
1	0	0	4 [2,9]	3	4	5	200-175
1	0	1	5	5	6	7	333-175
1	1	0	Reserved	n/a	n/a	n/a	n/a
1	1	1	Reserved	n/a	n/a	n/a	n/a

Notes:
1. A10-A18 must be set to zero; A18-An are "Don't cares."
2. BL = 8 is not available.
3. ±30 % temperature variation.
4. DLL RESET turns the DLL off.
5. Ay = 8 is not used in MRS.
6. BA0-BA2 are "Don't care."
7. Addresses A0, A3, A4, A5, A8, and A9 must be set as shown in order to activate the mode register in the multiplexed address mode.
8. t_{RC} < 20ns in any configuration is only available with -25E speed grade.
9. The minimum t_{RC} is typically 3 cycles, except in the case of a WRITE followed by a READ to the same bank. In this instance the minimum t_{RC} is 4 cycles.
10. tCK must be met to use this configuration. For tCK values, please refer to the AC Electrical Characteristics table.

3.5 Mode Register Bit Description

Configuration

The cycle time and read/write latency can be configured from the different options shown in the Mode Register Diagram. In order to maximize data bus utilization, the WRITE latency is equal to READ latency plus one. The read and write latencies are increased by one clock cycle during multiplexed address mode compared to non-multiplexed mode.

Burst Length

The burst length of the read and write accesses to memory can be selected from three different options: 2, 4, and 8. Changes in the burst length affect the width of the address bus and is shown in the *Burst Length and Address Width Table*. The data written during a prior burst length setting is not guaranteed to be accurate when the burst length of the device is changed.

Burst Length and Address Width Table

Burst Length	576Mb Address Bus		
	x9	x18	x36
2	A0-A21	A0-A20	A0-A19
4	A0-A20	A0-A19	A0-A18
8	A0-A19	A0-A18	A0-A17

DLL Reset

The default setting for this option is LOW, whereby the DLL is disabled. Once the mode register for this feature is set HIGH, 1024 cycles (5µs at 200 MHz) are needed before a READ command can be issued. This time allows the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{CKQK} parameter. A reset of the DLL is necessary if t_{CK} or V_{DD} is changed after the DLL has already been enabled. To reset the DLL, an MRS command must be issued where the DLL Reset Mode Register is set LOW. After waiting t_{MRSC}, a subsequent MRS command should be issued whereby the DLL Reset Mode Register is set HIGH. 1024 clock cycles are then needed before a READ command is issued.

Drive Impedance Matching

The RLDRAM® 2 Memory is equipped with programmable impedance output buffers. The purpose of the programmable impedance output buffers is to allow the user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and V_{SS}. The value of the resistor must be five times the desired impedance. For example, a 300Ω resistor is required for an output impedance of 60Ω. The range of RQ is 125–300Ω, which guarantees output impedance in the range of 25–60Ω (within 15 percent). Output impedance updates may be required because over time variations may occur in supply voltage and temperature. When the external drive impedance is enabled in the MRS, the device will periodically sample the value of RQ. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update. When the Drive Impedance Mode Register is set LOW during the MRS command, the memory provides an internal impedance at the output buffer of 50Ω (±30% with temperature variation). This impedance is also periodically sampled and adjusted to compensate for variation in supply voltage and temperature.

Address Multiplexing

Although the RLDRAM® 2 Memory is capable of accepting all the addresses in a single rising clock edge, this memory can be programmed to operate in multiplexed address mode, which is very similar to a traditional DRAM. In multiplexed address mode, the address can be sent to the memory in two parts within two consecutive rising clock edges. This minimizes the number of address signal connections between the controller and the memory by reducing the address bus to a maximum of only 11 lines. Since the memory requires two clock cycles to read and write the data, data bus efficiency is affected when operating in continuous burst mode with a burst length of 2 setting. Bank addresses are provided to the memory at the same time as the WRITE and READ commands together with the first address part, Ax. The second address part, Ay, is then issued to the memory on the next rising clock edge. AREF commands only require the bank address. Since AREF commands do not need a second consecutive clock for address latching, they may be issued on consecutive clocks.

Address Mapping in Multiplexed Address Mode

Data Width	Burst Length	Address											
		Ball	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
x36	2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
X18	2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
X9	2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	A21	A6	A7	A19	A11	A12	A16	A15
	4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15

Note: X = Don't Care.

On-Die Termination (ODT)

If the ODT is enabled, the DQs and DM are terminated to V_{TT} with a resistance R_{TT}. The command, address, QVLD, and clock signals are not terminated. Figure 3.1 shows the equivalent circuit of a DQ receiver with ODT. The ODT function is dynamically switched off when a DQ begins to drive after a READ command is issued. Similarly, ODT is designed to switch on at the DQs after the memory has issued the last piece of data. The DM pin will always be terminated.

ODT DC Parameters Table

Description	Symbol	Min	Max	Units	Notes
Termination Voltage	V_{TT}	0.95 x V_{REF}	1.05 x V_{REF}	V	1, 2
On-die termination	R_{TT}	125	185	Ω	3

Notes:

1. All voltages referenced to V_{SS} (GND).
2. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
3. The R_{TT} value is measured at 95°C T_C.

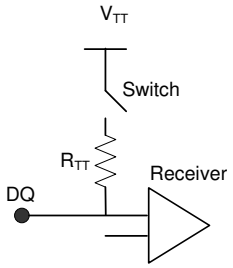


Figure 3.1 ODT Equivalent Circuit

3.6 Deselect/No Operation (DESL/NOP)

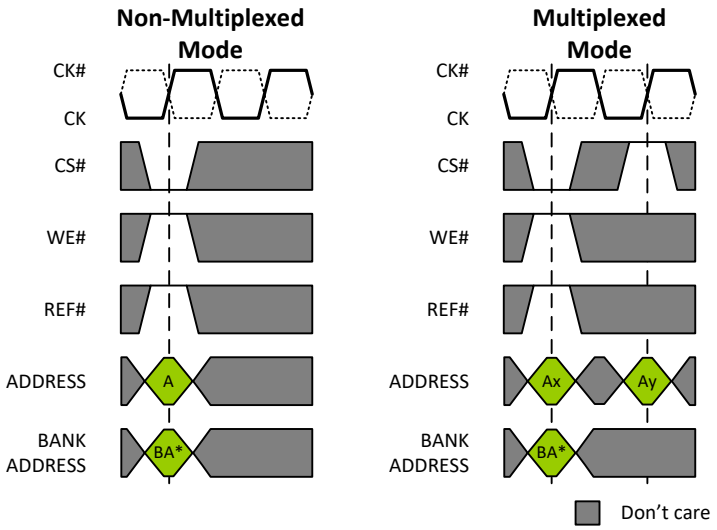
The Deselect command is used to prevent unwanted operations from being performed in the memory device during wait or idle states. Operations already registered to the memory prior to the assertion of the Deselect command will not be cancelled.

3.7 Read Operation (READ)

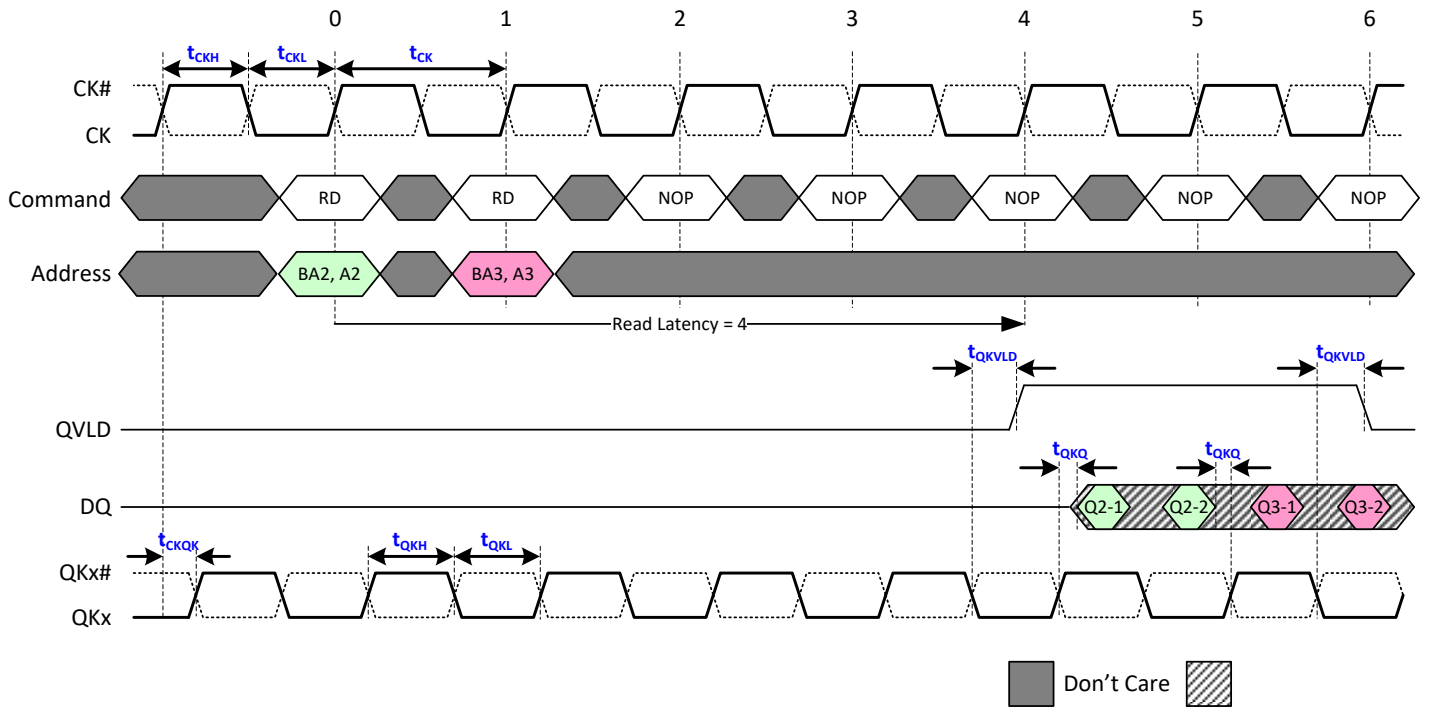
The Read command performs burst-oriented data read accesses in a bank of the memory device. The Read command is initiated by registering the WE# and REF# signals logic HIGH while the CS# is in logic LOW state. In non-multiplexed address mode, both an address and a bank address must be provided to the memory during the assertion of the Read command. In multiplexed mode, the bank address and the first part of the address, Ax, must be supplied together with the Read command. The second part of the address, Ay, must be latched to the memory on the subsequent rising edge of the CK clock. Data being accessed will be available in the data bus a certain amount of clock cycles later depending on the Read Latency Configuration setting.

Data driven in the DQ signals are edge-aligned to the free-running output data clocks QKx and QKx#. A half clock cycle before the read data is available on the data bus, the data valid signal, QVLD, will transition from logic LOW to HIGH. The QVLD signal is also edge-aligned to the data clock QKx and QKx#.

If no other commands have been registered to the device when the burst read operation is finished, the DQ signals will go to High-Z state. The QVLD signal transition from logic HIGH to logic LOW on the last bit of the READ burst. Please note that if CK/CK# violates the VID (DC) specification while a READ burst is occurring, QVLD will remain HIGH until a dummy READ command is registered. The QK clocks are free-running and will continue to cycle after the read burst is complete. Back-to-back READ commands are permitted which allows for a continuous flow of output data.



Read Command



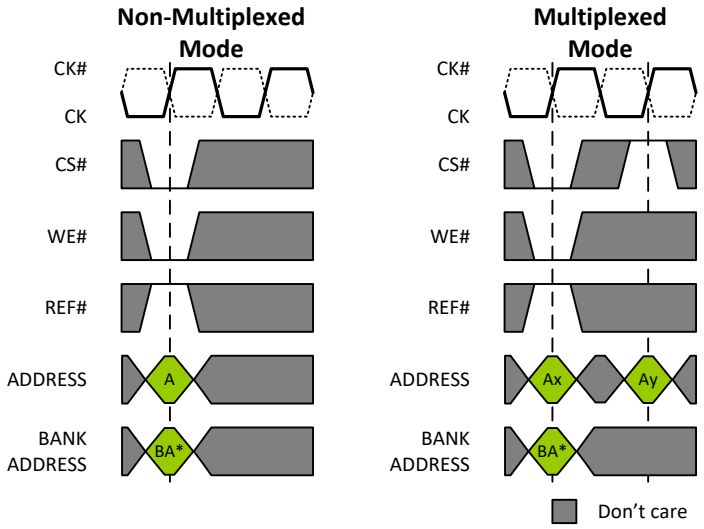
Basic READ Burst with QVLD: BL=2 & RL=4

Notes:
1. Minimum READ data valid window can be expressed as MIN(t_{QKH}, t_{QKL}) – 2 x MAX(t_{QKQx}).
2. t_{CKH} and t_{CKL} are recommended to have 50% / 50% duty.
3. t_{QKQ0} is referenced to DQ0–DQ17 in x36 and DQ0–DQ8 in x18. t_{QKQ1} is referenced to DQ18–DQ35 in x36 and DQ9–DQ17 in x18.
4. t_{QKQ} takes into account the skew between any QKx and any DQ.
5. t_{CKQK} is specified as CK rising edge to QK rising edge.

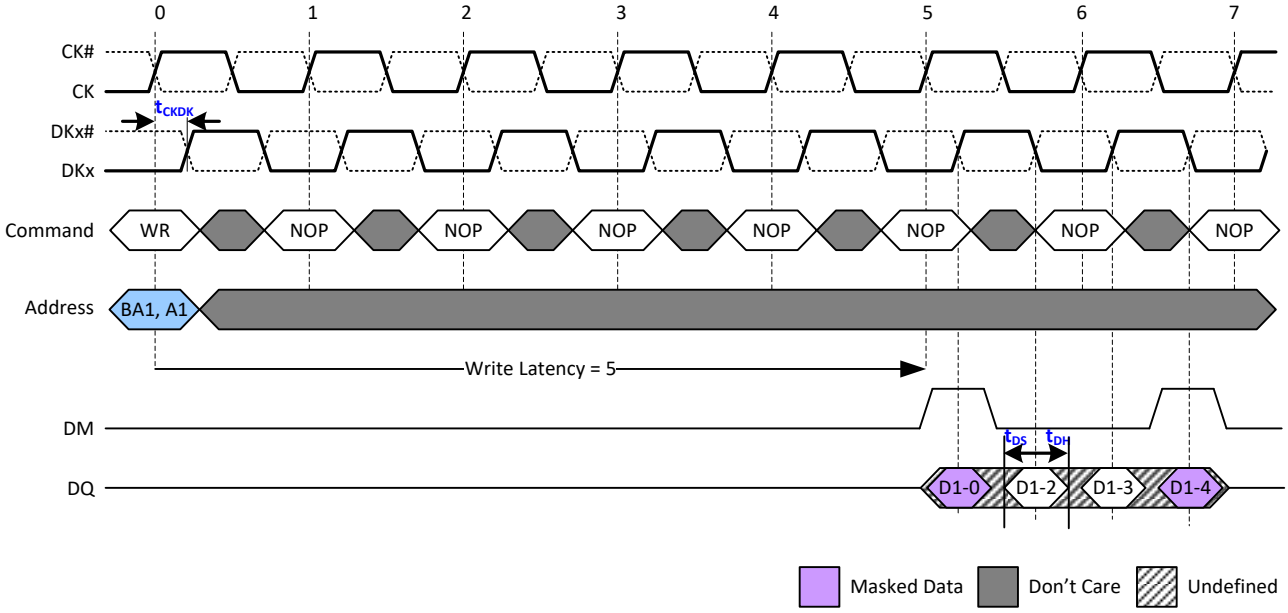
3.8 Write Operation (WRITE)

The Write command performs burst-oriented data write accesses in a bank of the memory device. The Write command is initiated by registering the REF# signal logic HIGH while the CS# and WE# signals are in logic LOW state. In non-multiplexed address mode, both an address and a bank address must be provided to the memory during the assertion of the Write command. In multiplexed mode, the bank address and the first part of the address, Ax, must be supplied together with the Write command. The second part of the address, Ay, must be latched to the memory on the subsequent rising edge of the CK clock. Input data to be written to the device can be registered several clock cycles later depending on the Write Latency Configuration setting. The write latency is always one cycle longer than the programmed read latency. The DM signal can mask the input data by setting this signal logic HIGH.

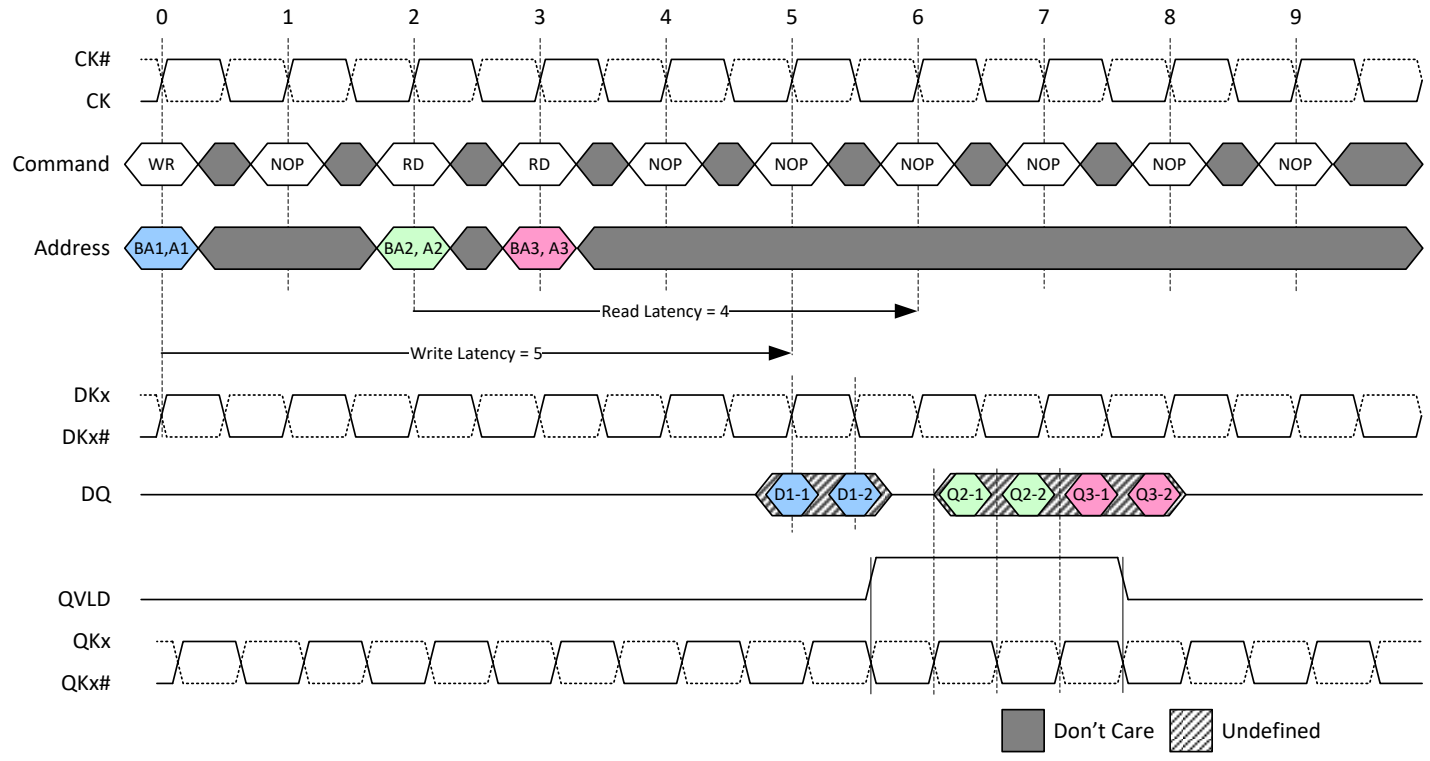
At least one NOP command in between a Read and Write commands is required in order to avoid data bus contention. The setup and hold times for DM and data signals are t_{DS} and t_{DH}, which are referenced to the DK clocks.



Write Command



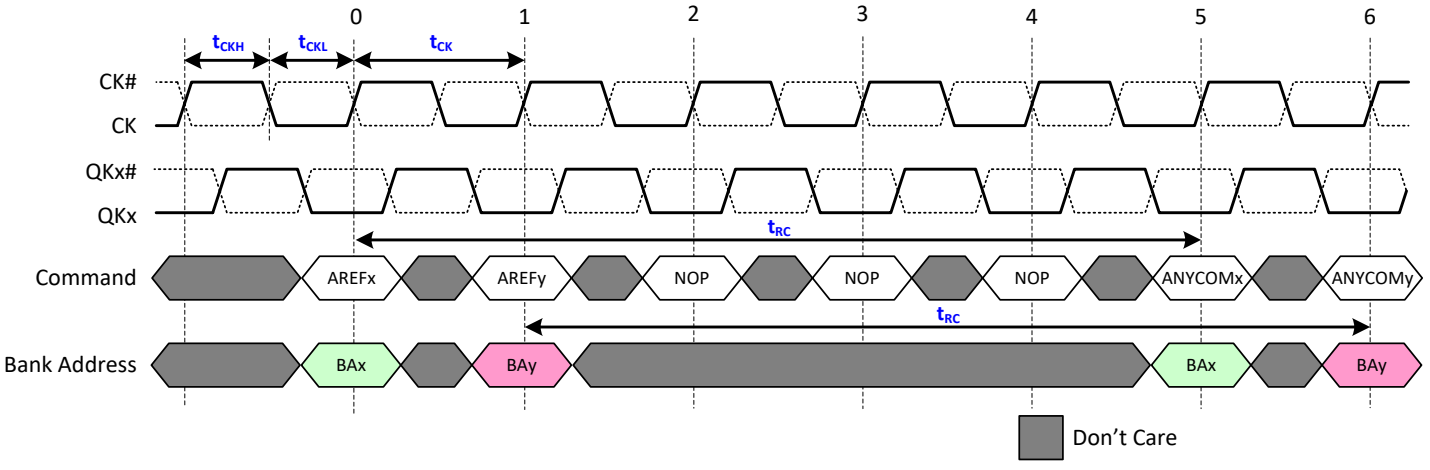
Basic WRITE Burst with DM Timing: BL=4 & WL=5



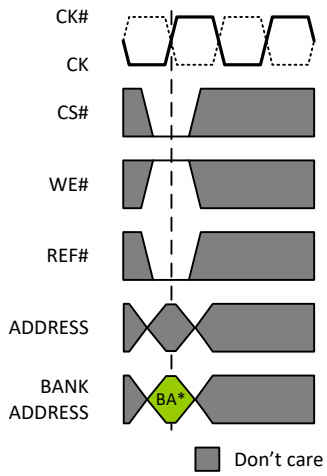
Write Followed by Read: BL=2 RL=4 & WL=5

3.9 Auto Refresh Command (AREF)

The Auto Refresh command performs a refresh cycle on one row of a specific bank of the memory. Only bank addresses are required together with the control the pins. Therefore, Auto Refresh commands can be issued on subsequent CK clock cycles on both multiplexed and non-multiplexed address mode. Any command following an Auto Refresh command must meet a tRC timing delay or later.



AREF example in $t_{RC}(t_{CK})$=5 option: Configuration=5



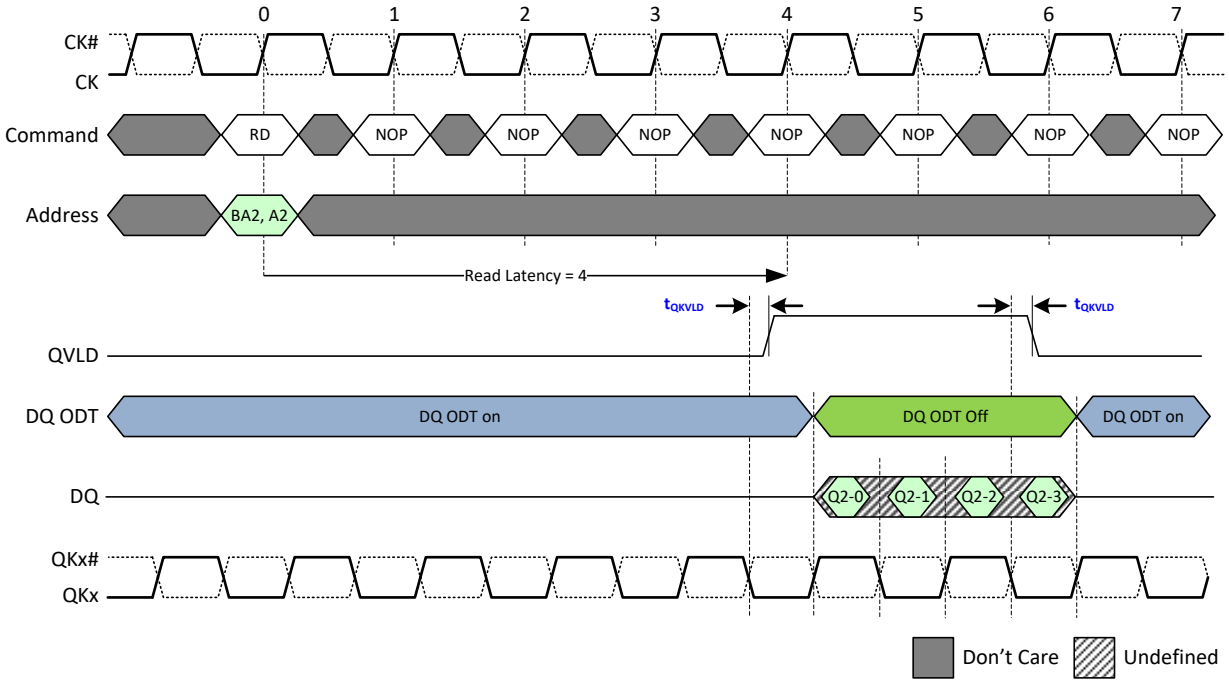
Auto Refresh Command

3.10 Command Truth Table

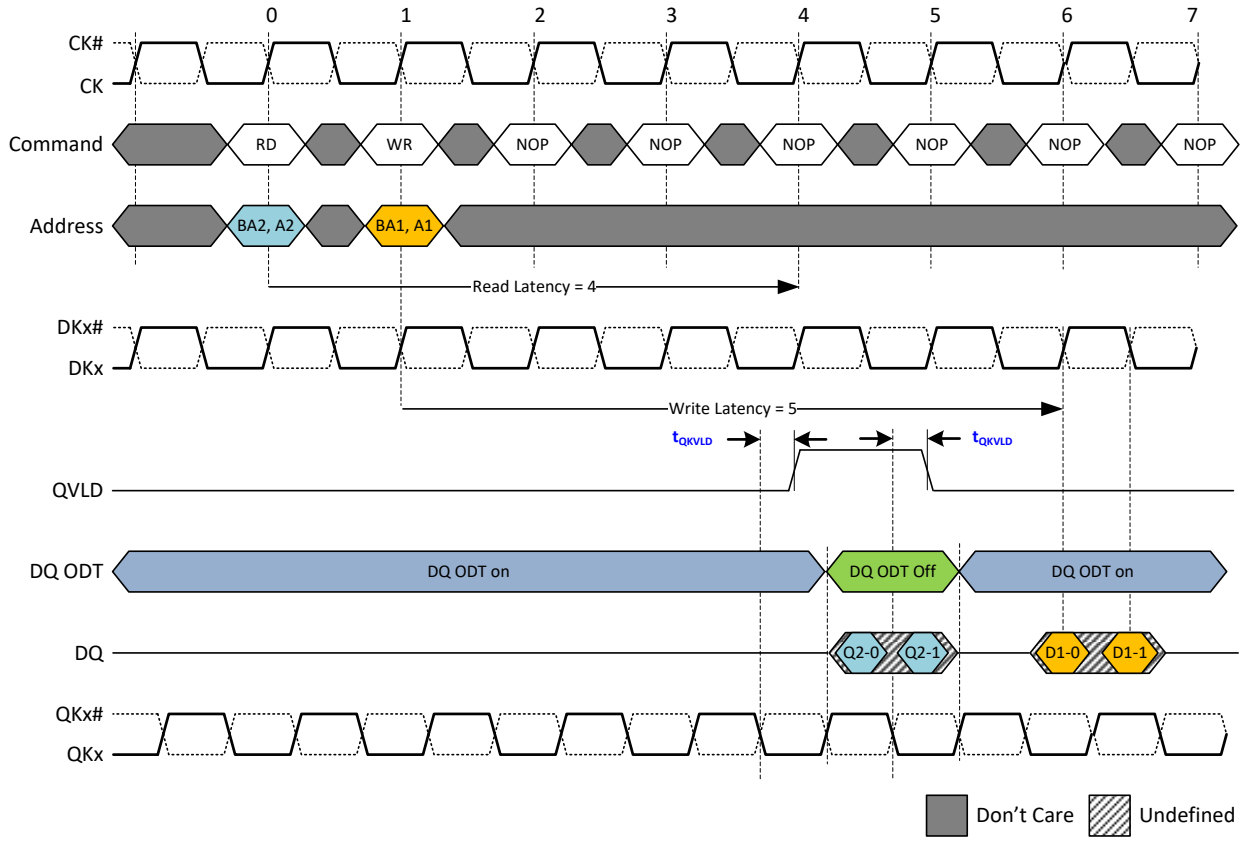
Operation	Code	CS#	WE#	REF#	Ax	BAx
Device DESELECT/No Operation	DESL/NOP	H	X	X	X	X
Mode Register Set	MRS	L	L	L	OPCODE	X
Read	READ	L	H	H	A	BA
Write	WRITE	L	L	H	A	BA
Auto Refresh	AREF	L	H	L	X	BA

Notes:
1. X = "Don't Care;" H = logic HIGH; L = logic LOW; A = Valid Address; BA = Valid Bank Address.
2. During MRS, only address inputs A0-A17 are used.
3. Address width changes with burst length.
4. All input states or sequences not shown are illegal or reserved.
5. All command and address inputs must meet setup and hold times around the rising edge of CK.

3.11 On-Die Termination (ODT) Timing Examples.



Read Operation with ODT: RL=4 & BL=4



Read to Write with ODT: RL=4 & BL=2

4 IEEE 1149.1 TAP and Boundary Scan

RLDRAM® 2 Memory devices have a serial boundary-scan test access port (TAP) that allow the use of a limited set of JTAG instructions to test the interconnection between the memory I/Os and printed circuit board traces or other components. In conformance with IEEE Standard 1149.1, the memory contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register. The TAP operates in accordance with IEEE Standard 1149.1-2001 (JTAG) with the exception of the ZQ pin. To guarantee proper boundary-scan testing of the ZQ pin, MRS bit M8 needs to be set to 0 until the JTAG testing of the pin is complete. Note that on power up, the default state of MRS bit M8 is logic LOW. The TAP is compliant with IEEE 1149.1-2013 as far as all mandatory features (BYPASS, EXTEST, PRELOAD, and SAMPLE), and several optional features (CLAMP, HIGHZ, IDCODE, ECIDCODE).

If the memory boundary scan register is to be used upon power up and prior to the initialization of the device, the CK and CK# pins meet V_{ID}(DC) or CS# be held HIGH from power up until testing. Not doing so could result in inadvertent MRS commands to be loaded, and subsequently cause unexpected results from address pins that are dependent upon the state of the mode register. If these measures cannot be taken, the part must be initialized prior to boundary scan testing. If a full initialization is not practical or feasible prior to boundary scan testing, a single MRS command with desired settings may be issued instead. After the single MRS command is issued, the t_{MRSC} parameter must be satisfied prior to boundary scan testing.

4.1 Disabling the JTAG feature

The RLDRAM® 2 Memory can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be left disconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will come up in a reset state, which will not interfere with device operation.

4.2 Test Access Port Signal List:

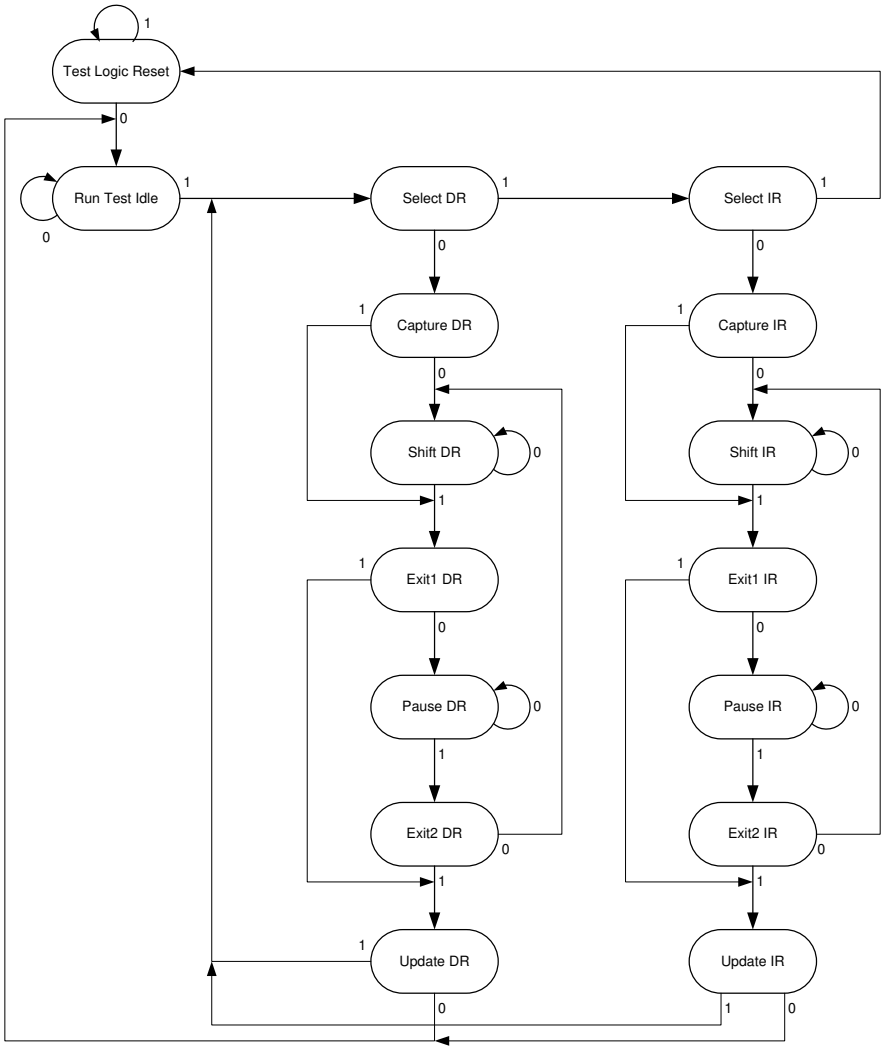
Test Clock (TCK)
This signal uses V_{DD} as a power supply. The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

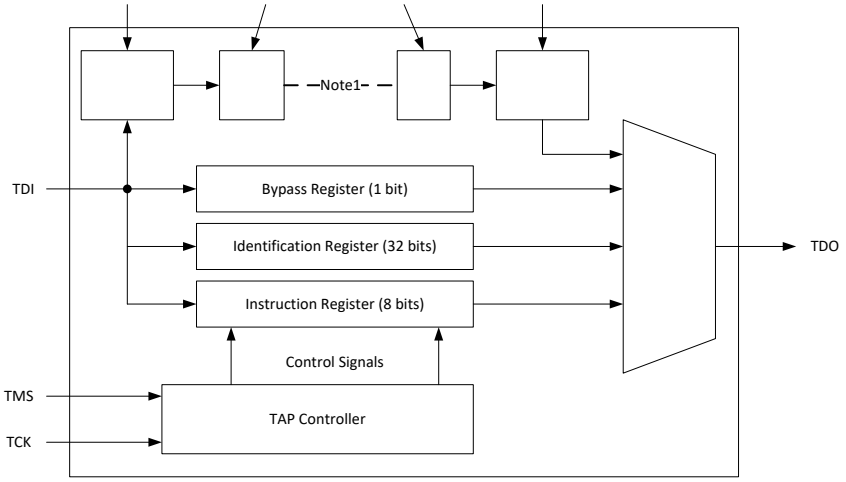
Test Mode Select (TMS)
This signal uses V_{DD} as a power supply. The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK.

Test Data-In (TDI)
This signal uses V_{DD} as a power supply. The TDI input is used to serially input test instructions and information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register. For more information regarding instruction register loading, please see the TAP Controller State Diagram.

Test Data-Out (TDO)
This signal uses V_{DDQ} as a power supply. The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. For more information, please see the TAP Controller State Diagram.

4.3 TAP Controller State and Block Diagram





Note: 113 boundary scan registers in RLDRAM® 2 Memory

4.4 Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

4.5 TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry**.** Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

This register is loaded during the update-IR state of the TAP controller. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the memory device with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the device. Several balls are also included in the scan register to reserved balls. The boundary scan register is loaded with the contents of the memory Input and Output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. Each bit corresponds to one of the balls on the device package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the device and can be shifted out when the TAP controller is in the shift-DR state.

4.6 Scan Register Sizes

Register Name	Bit Size
Instruction Register	8
Bypass Register	1
Boundary Scan Register	113
Identification (ID) Register	32

4.7 TAP Instruction Set

Many instructions are possible with an eight-bit instruction register and all valid combinations are listed in the *TAP Instruction Code* Table. All other instruction codes that are not listed on this table are reserved and should not be used. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the identification register. It also places the identification register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

High-Z

The High-Z instruction causes the bypass register to be connected between the TDI and TDO. This places all RLDRAM® 2 Memory outputs into a High-Z state.

CLAMP

When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary scan register.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register. The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the memory clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible. To ensure that the boundary scan register will capture the correct value of a signal, the memory signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}). The memory clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/ PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register. Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

4.8 TAP DC Electrical Characteristics and Operating Conditions

(+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted)

Description	Conditions	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage		V_{IH}	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1, 2
Input low (logic 0) voltage		V_{IL}	V_{SSQ} – 0.3	V_{REF} – 0.15	V	1, 2
Input leakage current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	– 5.0	5.0	µA	
Output leakage current	Output Disabled, 0V ≤ V_{IN} ≤ V_{DDQ}	I_{LO}	– 5.0	5.0	µA	
Output low voltage	I_{OLC} =100 µA	V_{OL1}	-	0.2	V	1
Output low voltage	I_{OLT} = 2mA	V_{OL2}	-	0.4	V	1
Output high voltage	|I_{OHC}| =100 µA	V_{OH1}	V_{DDQ} - 0.2	-	V	1
Output high voltage	|I_{OHT} | = 2mA	V_{OH2}	V_{DDQ} - 0.4	-	V	1

Notes:
1. All voltages referenced to VSS (GND).
2. Overshoot = V_{IH}(AC) ≤ V_{DD} + 0.7V for t ≤ t_{CK}/2; undershoot = V_{IL}(AC) ≥ –0.5V for *t* ≤ t_{CK}/2; during normal operation, V_{DDQ} must not exceed V_{DD}.

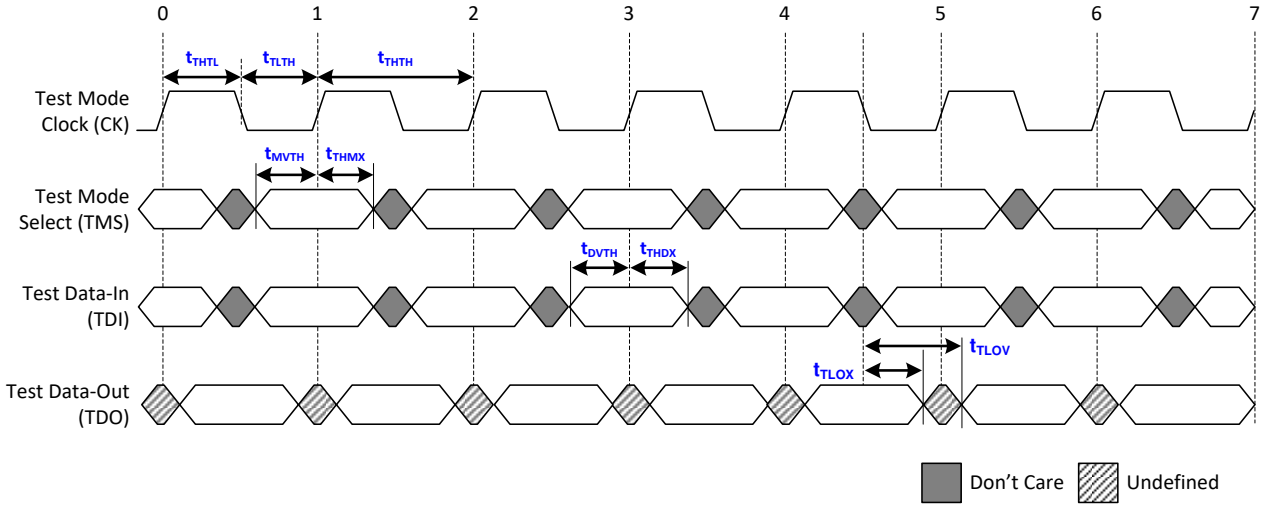
4.9 TAP AC Electrical Characteristics and Operating Conditions

(+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V)

Description	Symbol	Min	Max	Units
Clock				
Clock Cycle Time	t_{THTH}	20		ns
Clock Frequency	f_{TF}		50	MHz
Clock HIGH Time	t_{THTL}	10		ns
Clock LOW Time	t_{TLTH}	10		ns
TDI/TDO times				
TCK LOW to TDO unknown	t_{TLOX}	0		ns
TCK LOW to TDO valid	t_{TLOV}		10	ns
TDI valid to TCK High	t_{DVTH}	5		ns
TCK HIGH to TDI invalid	t_{THDX}	5		ns
Setup times				
TMS Setup	t_{MVTH}	5		ns
Capture Setup	t_{CS}	5		ns
Hold Times				
TMS hold	t_{TMHX}	5		ns
Capture hold	t_{CH}	5		ns

Note: t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.

4.10 TAP Timing



4.11 TAP Instruction Codes

Instruction	Code	Description
EXTEST	0000 0000	Captures Input and Output ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect device operations
IDCODE	0010 0001	Loads the ID register with the vendor ID code and places the register between TDI and TDO; This operation does not affect device operations
SAMPLE/PRELOAD	0000 0101	Captures I/O ring contents; Places the boundary scan register between TDI and TDO
CLAMP	0000 0111	Selects the bypass register to be connected between TDI and TDO; Data driven by output balls are determined from values held in the boundary scan register
High-Z	0000 0011	Selects the bypass register to be connected between TDI and TDO; All outputs are forced into High-Z
BYPASS	1111 1111	Places the bypass register between TDI and TDO; This operation does not affect device operations

Note: All other remaining instruction codes not mentioned in the above table are reserved and should not be used.

4.12 Identification (ID) Register Definition

Instruction Field	All Devices	Description
Revision number (31:28)	abcd	ab = die revision cd = 00 for x9, 01 for x18, 10 for x36
Device ID (27:12)	00jkidef10100111	def = 000 for 288Mb, 001 for 576Mb i = 0 for common I/O, 1 for separate I/O jk = 01 for RLDRAM® 2 Memory
Vendor ID code (11:1)	000 1101 0101	Allows unique identification of vendor
ID register presence indicator (0)	1	Indicates the presence of an ID register

4.13 TAP Input AC Logic Levels

(+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted)

Description	Symbol	Min	Max	Units
Input high (logic 1) voltage	V_{IH}	V_{REF} + 0.3	-	V
Input low (logic 0) voltage	V_{IL}	-	V_{REF} - 0.3	V

Note: All voltages referenced to V_{SS} (GND).

4.14 Boundary Scan Order

Bit#	Signal name			Bump
	x9	x18	x36	ID
1	DK	DK	DK1	K1
2	DK#	DK#	DK1#	K2
3	CS#	CS#	CS#	L2
4	REF#	REF#	REF#	L1
5	WE#	WE#	WE#	M1
6	A17	A17	A17	M3
7	A16	A16	A16	M2
8	A18	A18	A18	N1
9	A15	A15	A15	P1
10	DNU	DQ14	DQ25	N3
11	DNU	DQ14	DQ25	N3
12	DNU	DNU	DQ24	N2
13	DNU	DNU	DQ24	N2
14	DNU	DQ15	DQ23	P3
15	DNU	DQ15	DQ23	P3
16	DNU	DNU	DQ22	P2
17	DNU	DNU	DQ22	P2
18	DNU	QK1	QK1	R2
19	DNU	QK1#	QK1#	R3
20	DNU	DNU	DQ20	T2
21	DNU	DNU	DQ20	T2
22	DNU	DQ16	DQ21	T3
23	DNU	DQ16	DQ21	T3
24	DNU	DNU	DQ18	U2
25	DNU	DNU	DQ18	U2
26	DNU	DQ17	DQ19	U3
27	DNU	DQ17	DQ19	U3
28	ZQ	ZQ	ZQ	V2
29	DQ8	DQ13	DQ27	U10
30	DQ8	DQ13	DQ27	U10
31	DNU	DNU	DQ26	U11
32	DNU	DNU	DQ26	U11
33	DQ7	DQ12	DQ29	T10
34	DQ7	DQ12	DQ29	T10
35	DNU	DNU	DQ28	T11
36	DNU	DNU	DQ28	T11
37	DQ6	DQ11	DQ31	R10
38	DQ6	DQ11	DQ31	R10

Bit#	Signal name			Bump
	x9	x18	x36	ID
39	DNU	DNU	DQ30	R11
40	DNU	DNU	DQ30	R11
41	DNU	DNU	DQ32	P11
42	DNU	DNU	DQ32	P11
43	DQ5	DQ10	DQ33	P10
44	DQ5	DQ10	DQ33	P10
45	DNU	DNU	DQ34	N11
46	DNU	DNU	DQ34	N11
47	DQ4	DQ9	DQ35	N10
48	DQ4	DQ9	DQ35	N10
49	DM	DM	DM	P12
50	A19	A19	A19	N12
51	A11	A11	A11	M11
52	A12	A12	A12	M10
53	A10	A10	A10	M12
54	A13	A13	A13	L12
55	A14	A14	A14	L11
56	BA1	BA1	BA1	K11
57	CK#	CK#	CK#	K12
58	CK	CK	CK	J12
59	BA0	BA0	BA0	J11
60	A4	A4	A4	H11
61	A3	A3	A3	H12
62	A0	A0	A0	G12
63	A2	A2	A2	G10
64	A1	A1	A1	G11
65	A20	A20	(A20)	E12
66	QVLD	QVLD	QVLD	F12
67	DQ3	DQ3	DQ7	F10
68	DQ3	DQ3	DQ7	F10
69	DNU	DNU	DQ6	F11
70	DNU	DNU	DQ6	F11
71	DQ2	DQ2	DQ5	E10
72	DQ2	DQ2	DQ5	E10
73	DNU	DNU	DQ4	E11
74	DNU	DNU	DQ4	E11
75	QK0	QK0	QK0	D11
76	QK0#	QK0#	QK0#	D10

Bit#	Signal name			Bump
	x9	x18	x36	ID
77	DNU	DNU	DQ2	C11
78	DNU	DNU	DQ2	C11
79	DQ1	DQ1	DQ3	C10
80	DQ1	DQ1	DQ3	C10
81	DNU	DNU	DQ0	B11
82	DNU	DNU	DQ0	B11
83	DQ0	DQ0	DQ1	B10
84	DQ0	DQ0	DQ1	B10
85	DNU	DQ4	DQ9	B3
86	DNU	DQ4	DQ9	B3
87	DNU	DNU	DQ8	B2
88	DNU	DNU	DQ8	B2
89	DNU	DQ5	DQ11	C3
90	DNU	DQ5	DQ11	C3
91	DNU	DNU	DQ10	C2
92	DNU	DNU	DQ10	C2
93	DNU	DQ6	DQ13	D3
94	DNU	DQ6	DQ13	D3
95	DNU	DNU	DQ12	D2
96	DNU	DNU	DQ12	D2
97	DNU	DNU	DQ14	E2
98	DNU	DNU	DQ14	E2
99	DNU	DQ7	DQ15	E3
100	DNU	DQ7	DQ15	E3
101	DNU	DNU	DQ16	F2
102	DNU	DNU	DQ16	F2
103	DNU	DQ8	DQ17	F3
104	DNU	DQ8	DQ17	F3
105	A21	(A21)	(A21)	E1
106	A5	A5	A5	F1
107	A6	A6	A6	G2
108	A7	A7	A7	G3
109	A8	A8	A8	G1
110	BA2	BA2	BA2	H1
111	A9	A9	A9	H2
112	NF	NF	DK0#	J2
113	NF	NF	DK0	J1

ORDERING INFORMATION

Commercial Range: T_C = 0° to +95°C; T_A = 0°C to +70°C

Frequency	Speed	Order Part No.	Organization	Package
400 MHz	2.5ns (tRC=15ns)	IS49NLC96400-25EWBL	64M x 9	144 WBGA, Lead-free
		IS49NLC18320-25EWBL	32M x 18	144 WBGA, Lead-free
		IS49NLC36160-25EWBL	16M x 36	144 WBGA, Lead-free
400 MHz	2.5ns (tRC=20ns)	IS49NLC96400-25WBL	64M x 9	144 WBGA, Lead-free
		IS49NLC18320-25WBL	32M x 18	144 WBGA, Lead-free
		IS49NLC36160-25WBL	16M x 36	144 WBGA, Lead-free
300 MHz	3.3ns (tRC=20ns)	IS49NLC96400-33WBL	64M x 9	144 WBGA, Lead-free
		IS49NLC18320-33WBL	32M x 18	144 WBGA, Lead-free
		IS49NLC36160-33WBL	16M x 36	144 WBGA, Lead-free
200 MHz	5ns (tRC=20ns)	IS49NLC96400-5BL	64M x 9	144 WBGA, Lead-free
		IS49NLC18320-5BL	32M x 18	144 WBGA, Lead-free
		IS49NLC36160-5WBL	16M x 36	144 WBGA, Lead-free

Industrial Range: T_C = – 40°C to 95°C; T_A = – 40°C to +85°C

Frequency	Speed	Order Part No.	Organization	Package
400 MHz	2.5ns (tRC=15ns)	IS49NLC96400-25EWBLI	64M x 9	144 WBGA, Lead-free
		IS49NLC18320-25EWBLI	32M x 18	144 WBGA, Lead-free
		IS49NLC36160-25EWBLI	16M x 36	144 WBGA, Lead-free
400 MHz	2.5ns (tRC=20ns)	IS49NLC96400-25WBLI	64M x 9	144 WBGA, Lead-free
		IS49NLC18320-25WBLI	32M x 18	144 WBGA, Lead-free
		IS49NLC36160-25WBLI	16M x 36	144 WBGA, Lead-free
300 MHz	3.3ns (tRC=20ns)	IS49NLC96400-33WBLI	64M x 9	144 WBGA, Lead-free
		IS49NLC18320-33WBLI	32M x 18	144 WBGA, Lead-free
		IS49NLC36160-33WBLI	16M x 36	144 WBGA, Lead-free
200 MHz	5ns (tRC=20ns)	IS49NLC96400-5BLI	64M x 9	144 WBGA, Lead-free
		IS49NLC18320-5BLI	32M x 18	144 WBGA, Lead-free
		IS49NLC36160-5WBLI	16M x 36	144 WBGA, Lead-free

Note: Please contact ISSI for availability of -5 speed grade (200MHz) option. The -33 speed grade (300MHz) option is backward compatible with all timing specification for slower grades.

Ball Grid Array

Package Code: WB (144-ball WBGA)