CAT28LV64

64K-Bit CMOS PARALLEL EEPROM

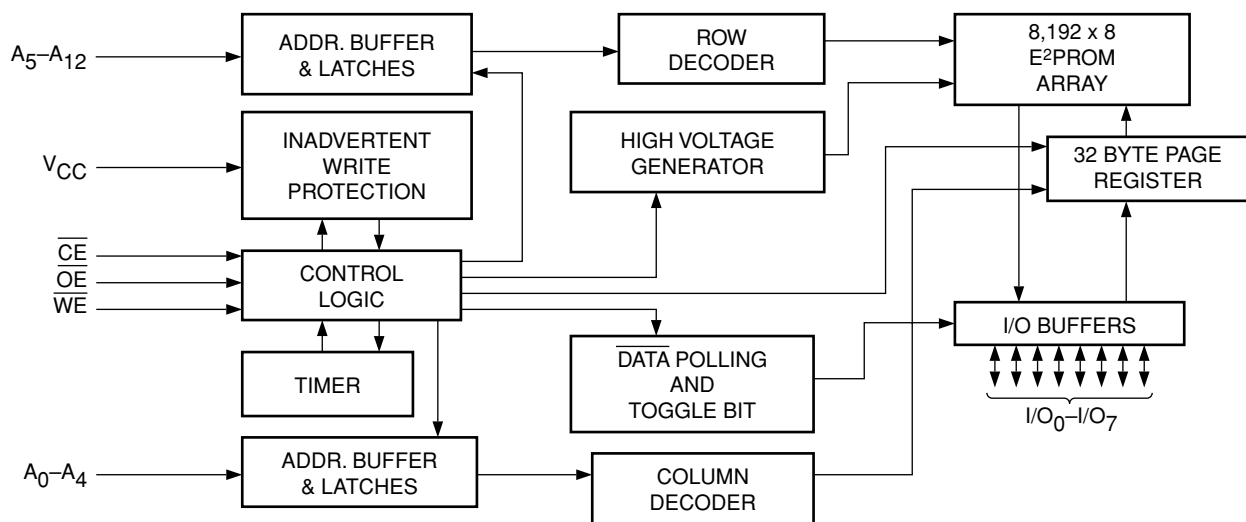## FEATURES

- **3.0V to 3.6 V Supply**

- **Read access times:**
  – **150/200/250ns**

- **Low power CMOS dissipation:**
  – **Active: 8 mA max.**
  – **Standby: 100 μA max.**

- **Simple write operation:**
  – **On-chip address and data latches**
  – **Self-timed write cycle with auto-clear**

- **Fast write cycle time:**
  – **5ms max.**

- **Commercial, industrial and automotive temperature ranges**

- **CMOS and TTL compatible I/O**

- **Automatic page write operation:**
  – **1 to 32 bytes in 5ms**
  – **Page load timer**

- **End of write detection:**
  – **Toggle bit**
  – **$\overline{DATA}$ polling**

- **Hardware and software write protection**

- **100,000 program/erase cycles**

- **100 year data retention**

DESCRIPTION

The CAT28LV64 is a low voltage, low power, CMOS parallel EEPROM organized as 8K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{DATA}$ Polling and Toggle status bit signal the start and end of the self-timed write cycle. Additionally, the CAT28LV64 features hardware and software write protection.
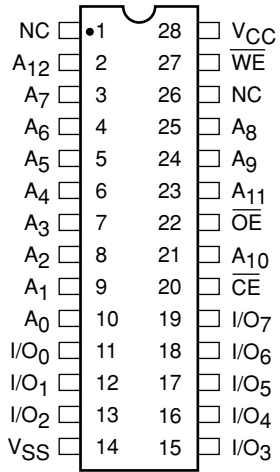
The CAT28LV64 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28-pin DIP, 28-pin TSOP, 28-pin SOIC or 32-pin PLCC packages.
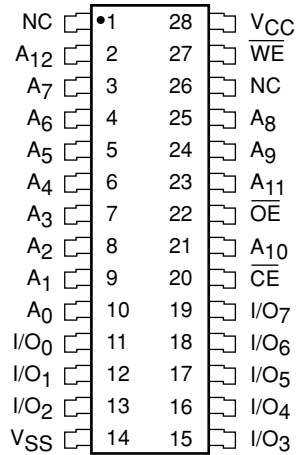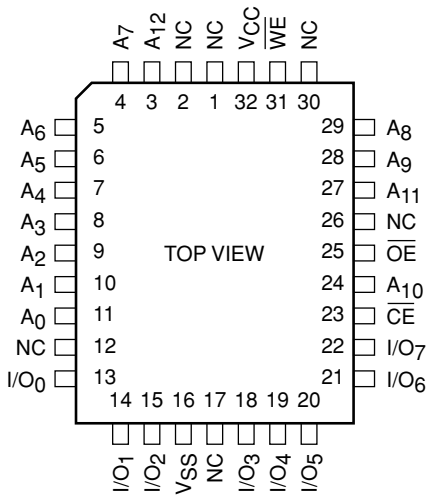
BLOCK DIAGRAM

PIN CONFIGURATION

DIP Package (P, L)

```
NC   ┌─•1    28─┐ V_CC
A12  ┌─ 2    27─┐ WE̅
A7   ┌─ 3    26─┐ NC
A6   ┌─ 4    25─┐ A8
A5   ┌─ 5    24─┐ A9
A4   ┌─ 6    23─┐ A11
A3   ┌─ 7    22─┐ OE̅
A2   ┌─ 8    21─┐ A10
A1   ┌─ 9    20─┐ CE̅
A0   ┌─ 10   19─┐ I/O7
I/O0 ┌─ 11   18─┐ I/O6
I/O1 ┌─ 12   17─┐ I/O5
I/O2 ┌─ 13   16─┐ I/O4
V_SS ┌─ 14   15─┐ I/O3
```

SOIC Package (J, W) (K, X)

```
NC   ┌─•1    28─┐ V_CC
A12  ┌─ 2    27─┐ WE̅
A7   ┌─ 3    26─┐ NC
A6   ┌─ 4    25─┐ A8
A5   ┌─ 5    24─┐ A9
A4   ┌─ 6    23─┐ A11
A3   ┌─ 7    22─┐ OE̅
A2   ┌─ 8    21─┐ A10
A1   ┌─ 9    20─┐ CE̅
A0   ┌─ 10   19─┐ I/O7
I/O0 ┌─ 11   18─┐ I/O6
I/O1 ┌─ 12   17─┐ I/O5
I/O2 ┌─ 13   16─┐ I/O4
V_SS ┌─ 14   15─┐ I/O3
```

PLCC Package (N, G)

```
           A7  A12  NC  NC  V_CC  WE̅  NC
            4   3   2   1   32  31  30

A6  ┌ 5                            29 ┐ A8
A5  ┌ 6                            28 ┐ A9
A4  ┌ 7                            27 ┐ A11
A3  ┌ 8                            26 ┐ NC
A2  ┌ 9        TOP VIEW            25 ┐ OE̅
A1  ┌ 10                           24 ┐ A10
A0  ┌ 11                           23 ┐ CE̅
NC  ┌ 12                           22 ┐ I/O7
I/O0┌ 13                           21 ┐ I/O6
            14  15  16  17  18  19  20

          I/O1 I/O2 V_SS NC I/O3 I/O4 I/O5
```

TSOP Top View (8mm x 13.4mm) (T13, H13)

```
OE̅   ┌ 1 ○                    28 ┐ A10
A11  ┌ 2                       27 ┐ CE̅
A9   ┌ 3                       26 ┐ I/O7
A8   ┌ 4                       25 ┐ I/O6
NC   ┌ 5                       24 ┐ I/O5
WE̅   ┌ 6                       23 ┐ I/O4
V_CC ┌ 7                       22 ┐ I/O3
NC   ┌ 8                       21 ┐ GND
A12  ┌ 9                       20 ┐ I/O2
A7   ┌ 10                      19 ┐ I/O1
A6   ┌ 11                      18 ┐ I/O0
A5   ┌ 12                      17 ┐ A0
A4   ┌ 13                      16 ┐ A1
A3   ┌ 14                      15 ┐ A2
```

PIN FUNCTIONS

Pin Name	Function	Pin Name	Function
A_0–A_{12}	Address Inputs	$\overline{WE}$	Write Enable
I/O$_0$–I/O$_7$	Data Inputs/Outputs	V_{CC}	3.0 to 3.6 V Supply
$\overline{CE}$	Chip Enable	V_{SS}	Ground
$\overline{OE}$	Output Enable	NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... –55°C to +125°C

Storage Temperature .... –65°C to +150°C

Voltage on Any Pin with
   Respect to Ground[2] .... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .... –2.0V to +7.0V
Package Power Dissipation
   Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .... 300°C

Output Short Circuit Current[3] .... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}[1]	Endurance	10^5		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}[1]	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}[1]	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}[1][4]	Latch-Up	100		mA	JEDEC Standard 17

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$[1]	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}[1]	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Operating, TTL)			8	mA	$\overline{CE} = \overline{OE} = V_{IL}$, f = 1/$t_{RC}$ min, All I/O's Open
I_{SBC}[3]	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE} = V_{IHC}$, All I/O's Open
I_{LI}	Input Leakage Current	−1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	−5		5	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IH}[3]	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}	Low Level Input Voltage	−0.3		0.6	V	
V_{OH}	High Level Output Voltage	2			V	I_{OH} = −100µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 1.0mA
V_{WI}	Write Inhibit Voltage	2			V	

A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

Symbol	Parameter	28LV64-15 Min.	Max.	28LV64-20 Min.	Max.	28LV64-25 Min.	Max.	Units
t_{RC}	Read Cycle Time	150		200		250		ns
t_{CE}	$\overline{CE}$ Access Time		150		200		250	ns
t_{AA}	Address Access Time		150		200		250	ns
t_{OE}	$\overline{OE}$ Access Time		70		80		100	ns
t_{LZ}[1]	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}[1]	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}[1][2]	$\overline{CE}$ High to High-Z Output		50		50		55	ns
t_{OHZ}[1][2]	$\overline{OE}$ High to High-Z Output		50		50		55	ns
t_{OH}[1]	Output Hold from Address Change	0		0		0		ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
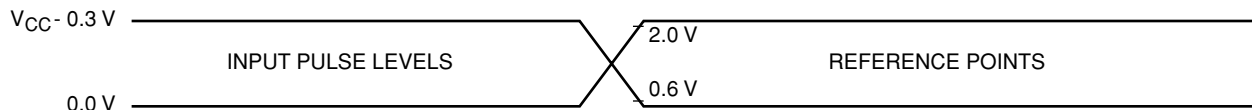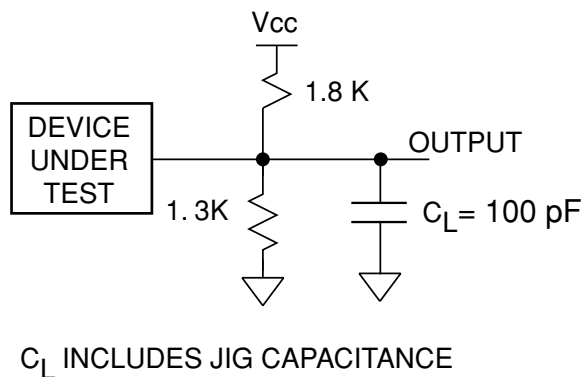(3) $V_{IHC} = V_{CC}$ −0.3V to V_{CC} +0.3V.

Figure 1. A.C. Testing Input/Output Waveform[4]

V_{CC} - 0.3 V	2.0 V
INPUT PULSE LEVELS	REFERENCE POINTS
0.0 V	0.6 V

Figure 2. A.C. Testing Load Circuit (example)

Vcc

1.8 K

DEVICE UNDER TEST

OUTPUT

1.3K

C_L = 100 pF

C_L INCLUDES JIG CAPACITANCE

A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

Symbol	Parameter	28LV64-15		28LV64-20		28LV64-25		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Setup Time0	0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{CW}[2]	$\overline{CE}$ Pulse Time	110		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	0		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	0		10		10		ns
t_{WP}[2]	$\overline{WE}$ Pulse Width	110		150		150		ns
t_{DS}	Data Setup Time	60		100		100		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}[1]	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}[1][3]	Byte Load Cycle Time	0.05	100	0.1	100	0.1	100	µs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) A write pulse of less than 20ns duration will not initiate a write cycle.
(3) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.
(4) Input rise and fall times (10% and 90%) < 10 ns.

DEVICE OPERATION

Read

Data stored in the CAT28LV64 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Figure 3. Read Cycle

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]

Page Write

The page write mode of the CAT28LV64 (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single EEPROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4

(which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]
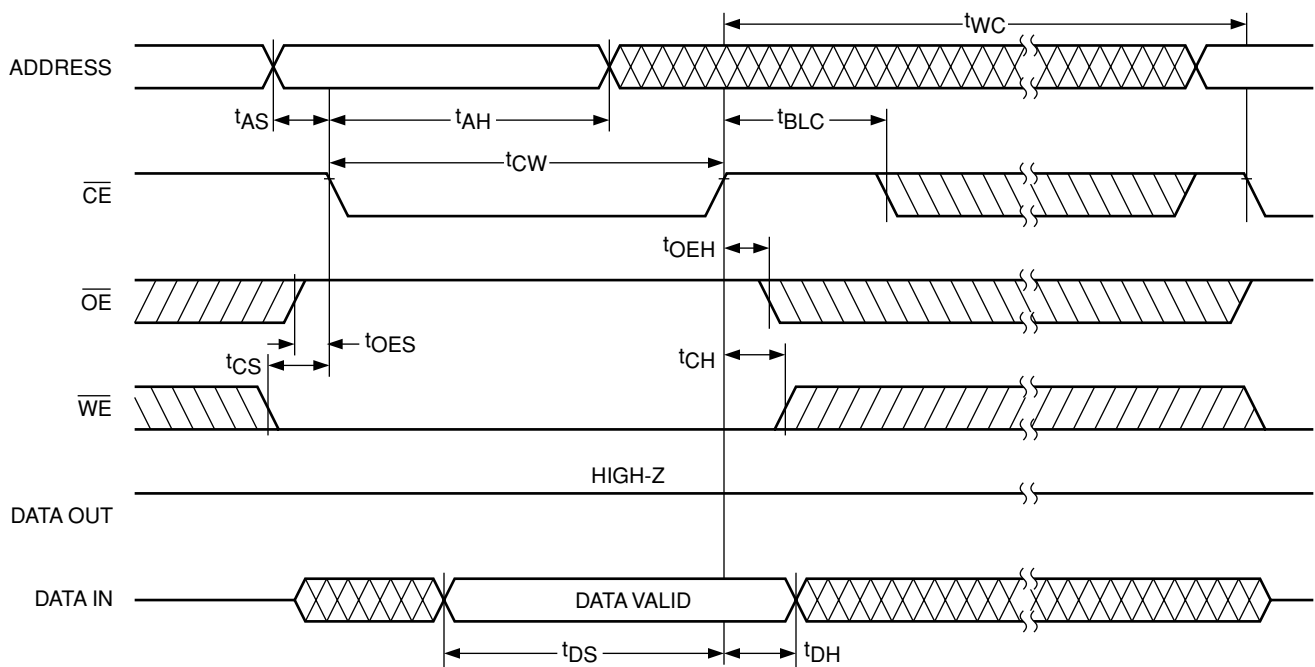
Figure 6. Page Mode Write Cycle

CAT28LV64
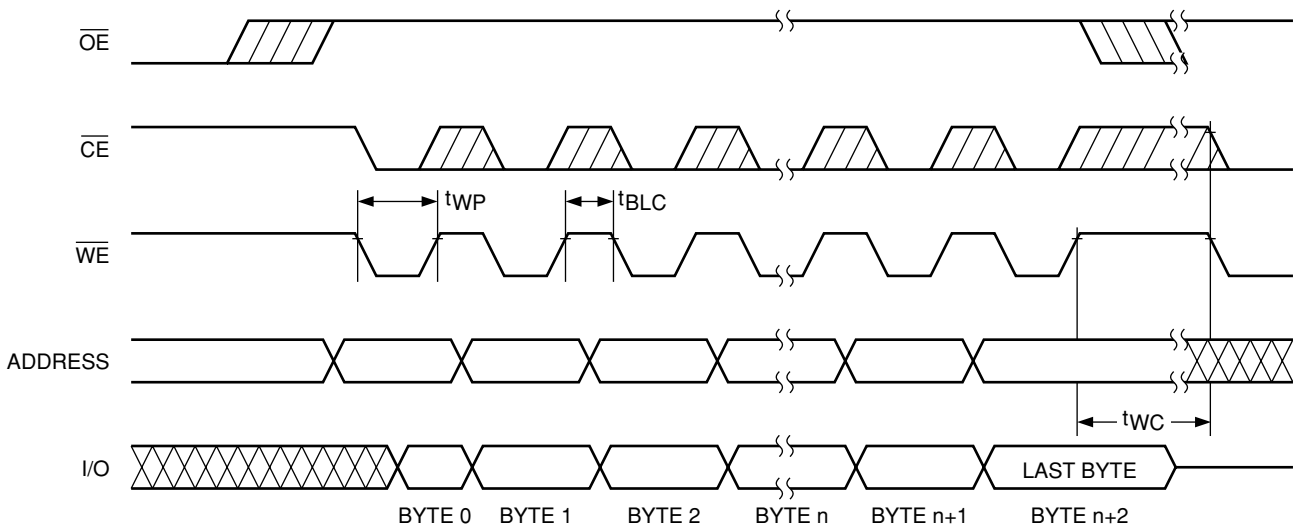
DATA Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O$_7$ (I/O$_0$–I/O$_6$ are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O$_6$ toggling between one and zero. However, once the write is complete, I/O$_6$ stops toggling and valid data can be read from the device.

Figure 7. $\overline{\text{DATA}}$ Polling
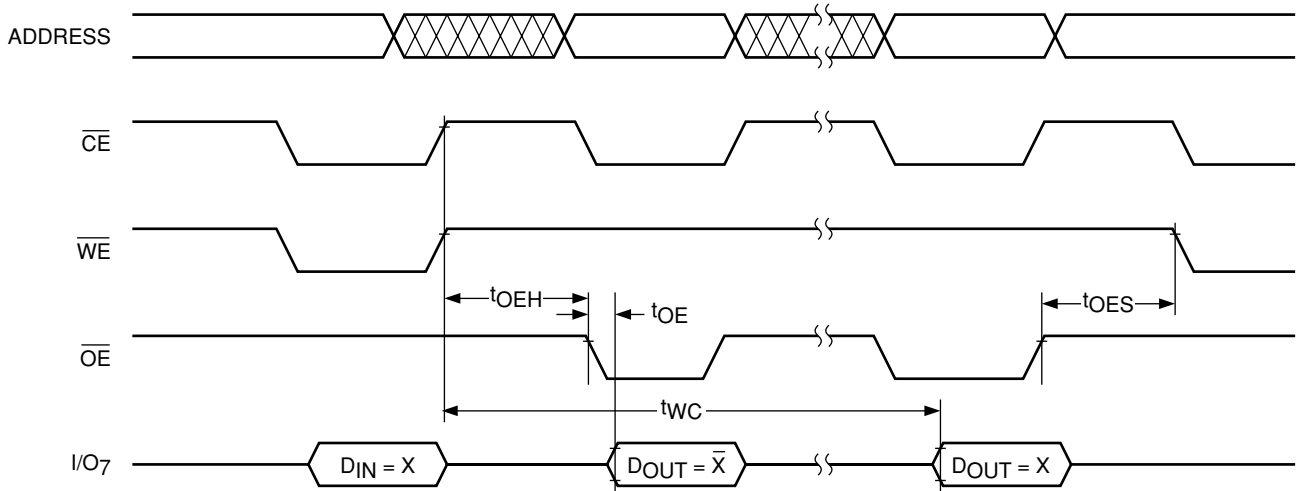
Figure 8. Toggle Bit
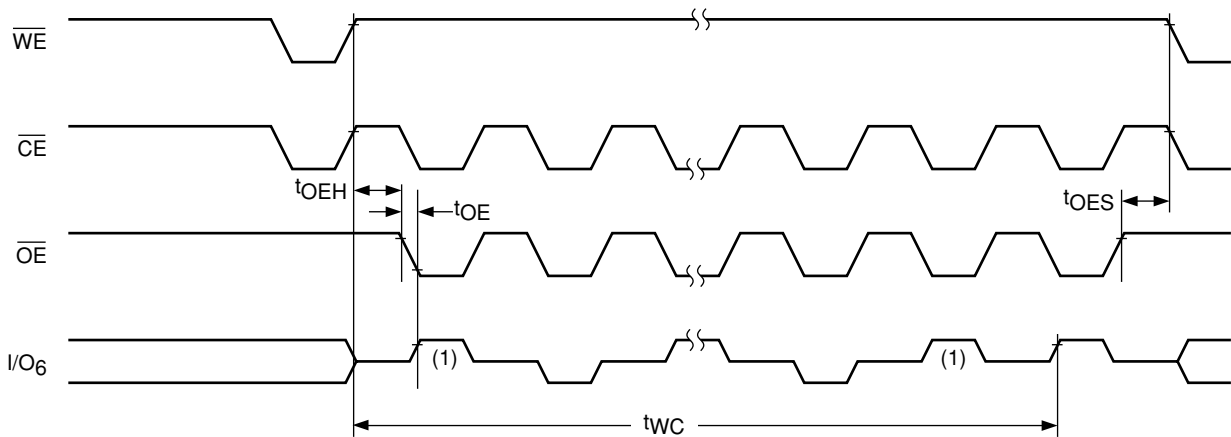
Note:
(1)   Beginning and ending state of I/O$_6$ is indeterminate.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28LV64.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 2.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 2.40V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28LV64 features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28LV64 is in the standard operating mode).

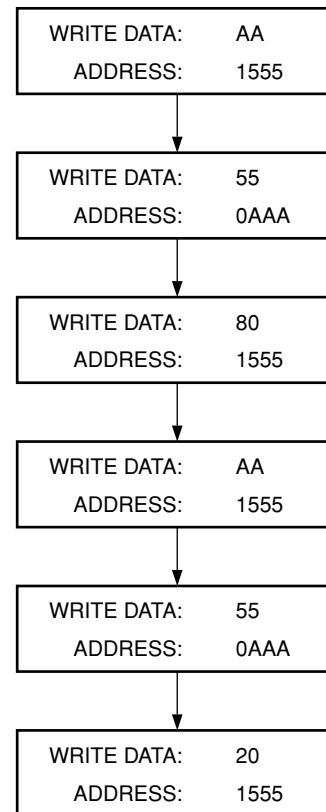**Figure 9. Write Sequence for Activating Software Data Protection**

```
┌────────────────────────┐
│ WRITE DATA:     AA      │
│ ADDRESS:        1555    │
└────────────────────────┘
            │
            ▼
┌────────────────────────┐
│ WRITE DATA:     55      │
│ ADDRESS:        0AAA    │
└────────────────────────┘
            │
            ▼
┌────────────────────────┐
│ WRITE DATA:     A0      │
│ ADDRESS:        1555    │
└────────────────────────┘
            │
            ▼
    SOFTWARE DATA
PROTECTION ACTIVATED (1)
            │
            ▼
┌────────────────────────┐
│ WRITE DATA:     XX      │
│   TO ANY ADDRESS        │
└────────────────────────┘
            ┊
┌────────────────────────┐
│   WRITE LAST BYTE       │
│        TO               │
│   LAST ADDRESS          │
└────────────────────────┘
```
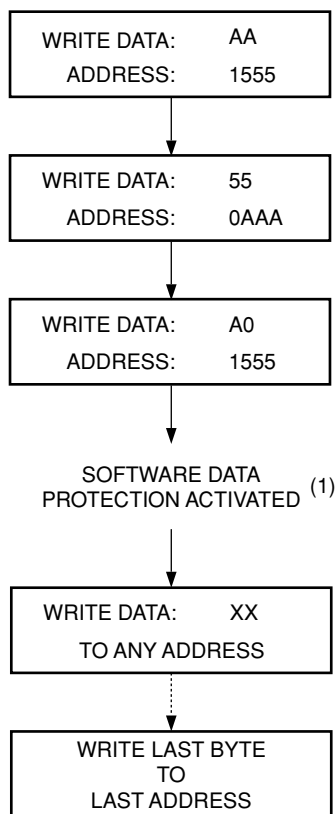
28LV64 F12

Figure 10. Write Sequence for Deactivating Software Data Protection

```
┌────────────────────────┐
│ WRITE DATA:     AA      │
│ ADDRESS:        1555    │
└────────────────────────┘
            │
            ▼
┌────────────────────────┐
│ WRITE DATA:     55      │
│ ADDRESS:        0AAA    │
└────────────────────────┘
            │
            ▼
┌────────────────────────┐
│ WRITE DATA:     80      │
│ ADDRESS:        1555    │
└────────────────────────┘
            │
            ▼
┌────────────────────────┐
│ WRITE DATA:     AA      │
│ ADDRESS:        1555    │
└────────────────────────┘
            │
            ▼
┌────────────────────────┐
│ WRITE DATA:     55      │
│ ADDRESS:        0AAA    │
└────────────────────────┘
            │
            ▼
┌────────────────────────┐
│ WRITE DATA:     20      │
│ ADDRESS:        1555    │
└────────────────────────┘
```

Note:
(1)   Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the device with an EEPROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing
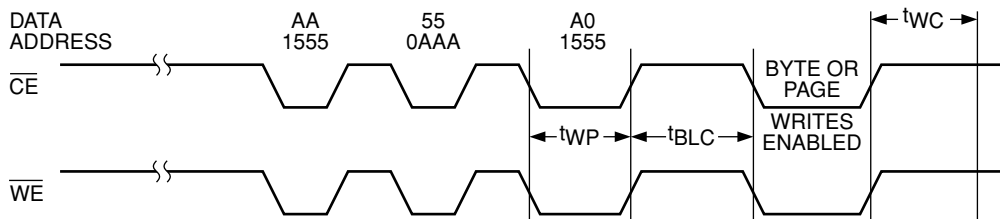
Figure 12. Resetting Software Data Protection Timing

ORDERING INFORMATION

Prefix	Device #	Suffix				
CAT	28LV64	N		I	-25	T

Optional Company ID

Product Number

Package
P: PDIP
J: SOIC (JEDEC)
K: SOIC (EIAJ)
N: PLCC
T13: TSOP (8mmx13.4mm)
L: PDIP (Lead free, Halogen free)
W: SOIC (JEDEC) (Lead free, Halogen free)
X: SOIC (EIAJ) (Lead free, Halogen free)
G: PLCC (Lead free, Halogen free)
H13: TSOP (8mmx13.4mm) (Lead free, Halogen free)

Temperature Range
Blank = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)
A = Automotive (-40°C to +105°C)*

Speed
15: 150ns
20: 200ns
25: 250ns

Tape & Reel

* -40°C to +125°C is available upon request

Notes:
(1)   The device used in the above example is a CAT28LV64NI-25T (PLCC, Industrial temperature, 250 ns Access Time, Tape & Reel).

REVISION HISTORY

Date	Revision	Comments
3/29/04	C	Added Green packages in all areas
04/20/04	D	Delete data sheet designation
		Update Ordering Information
		Update Revision History
		Update Rev Number