Features

- ESD protected for 8 high speed I/O channels
- Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±18kV (air) / ±16kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 6.5A (8/20μs)
- **For low operating voltage of 1.5V and below**
- **Ultra low capacitance: 0.5pF typical**
- Fast turn-on and low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Low leakage current
- Solid-state silicon-avalanche and active circuit triggering technology
- Simplified layout for high speed differential signaling channels
- ***Green part***

Applications

- V-by-One Interface
- LVDS Interface
- DisplayPort Interface
- Thunderbolt Interface
- USB 3.0

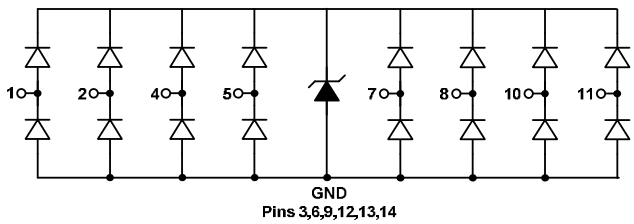
Description

AZ128S-08F is a design which includes ESD rated diode arrays to protect high speed data interfaces in an electronic system. The AZ128S-08F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD).

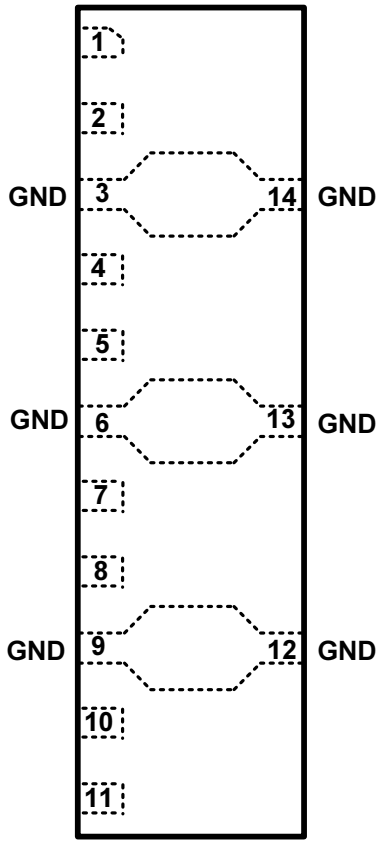
AZ128S-08F is a unique design which includes low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to the ground line, protecting any downstream components.

AZ128S-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN5515P14E (Top View)

SPECIFICATIONS

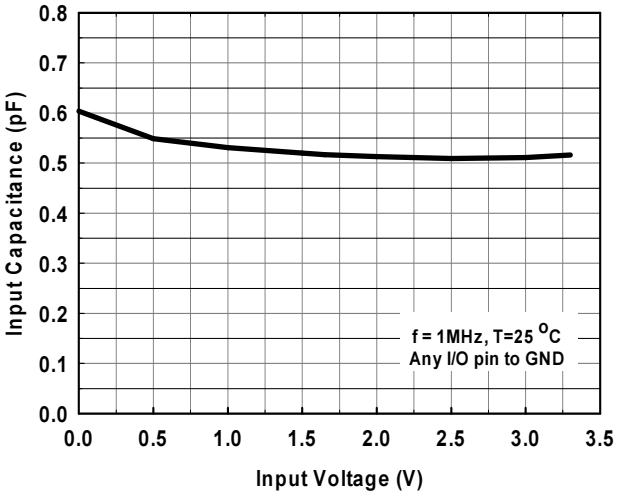
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs)	I_{PP}	6.5	A
Operating Voltage (I/O pin-GND)	V_{DC}	1.65	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±18 ±16	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Any I/O Pin to GND, T=25 °C.			1.5	V
Channel Leakage Current	I_{Leak}	V_{RWM} = 1.5V, T=25 °C, Any I/O Pin to GND			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Any I/O Pin to GND	4.5			V
Forward Voltage	V_F	I_F = 15mA, T=25 °C, GND to Any I/O Pin		0.9	1.1	V
ESD Clamping Voltage (Note 1)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, Contact mode, Any Channel pin to Ground		5.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, T=25 °C, Contact mode, Any I/O pin to Ground		0.17		Ω
Channel Input Capacitance	C_{IN}	GND = 0V, V_{IN} = 1.0V, f = 1MHz, T=25 °C. Any I/O Pin to GND		0.5	0.65	pF
Channel to Channel Input Capacitance	C_{CROSS}	GND = 0V, V_{IN} = 1.0V, f = 1MHz, T=25 °C. Between I/O Pins		0.06	0.1	pF

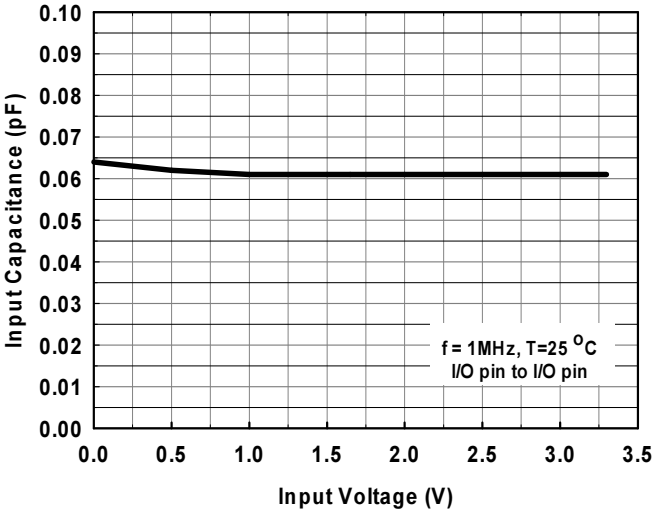
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

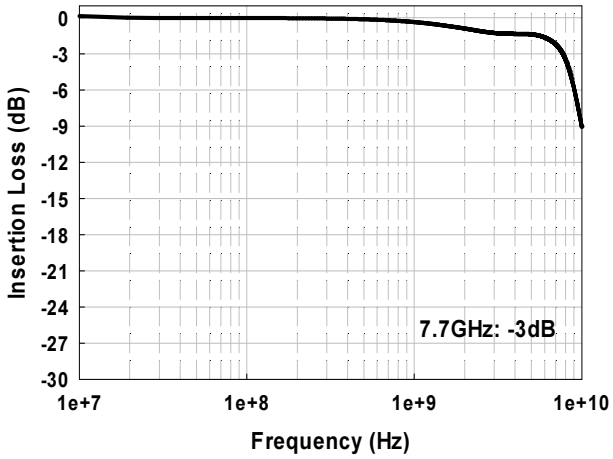
Typical variation of C_{IN} vs. V_{IN}



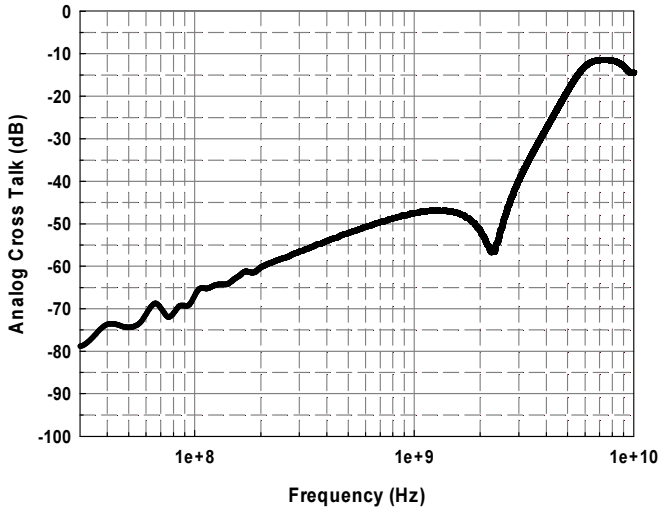
Typical variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



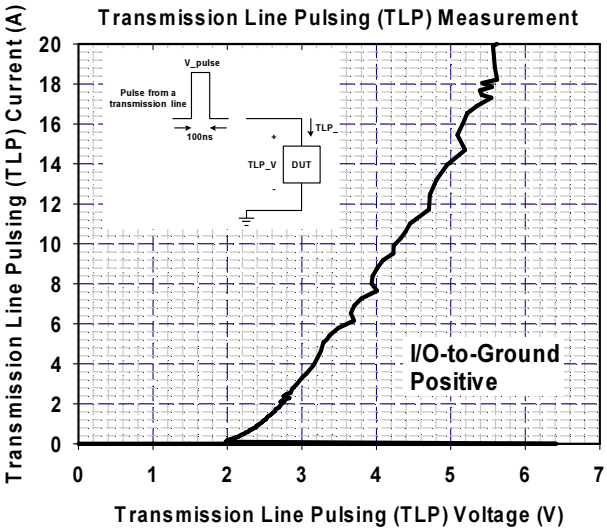
Insertion Loss S_{DD}



Analog Cross Talk



Transmission Line Pulsing (TLP) Measurement



Applications

A. Device Connection

The AZ128S-08F is designed to protect 8 high speed data lines from transient over-voltage (such as ESD stress pulse). The typical device connection of AZ128S-08F is shown in the Fig. 1. In Fig. 1, the 8 protected high speed data lines are connected to the ESD protection pins (pin1, pin2, pin4, pin5, pin7, pin8, pin10, and pin11) of AZ128S-08F. The AZ128S-08F is designed for allowing the traces to run straight through the device to simplify the PCB layout. The ground pins (pin3, pin6, pin9, pin12, pin13, and pin14) of AZ128S-08F are negative reference pins. **At least one of these pins should be directly connected to the GND rail of PCB.** To get minimum parasitic inductance, the path length should keep as short as possible.

AZ128S-08F can provide ESD protection for 8 I/O signal lines simultaneously. If the number of I/O signal lines is less than 8, the unused I/O pins can be left as NC pins.

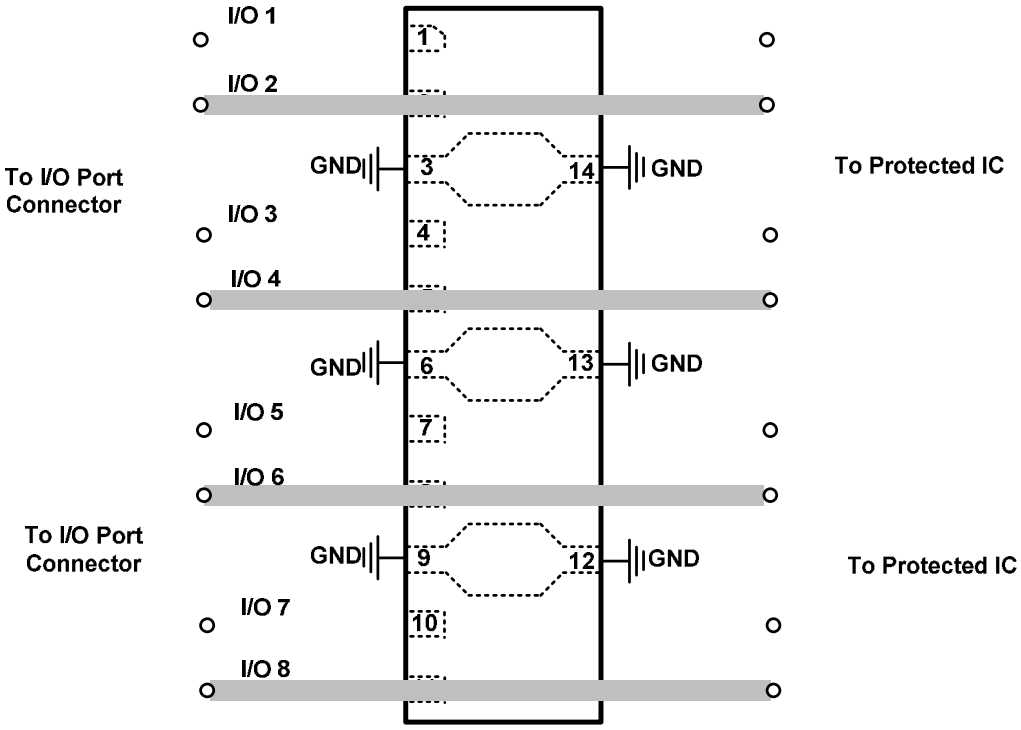


Fig. 1 Data lines connection of AZ128S-08F.

B. V-by-One Application

Fig. 2 shows how to implement the AZ128S-08F in a V-by-One application. The AZ128S-08F is designed for allowing the traces to run straight through the device to simplify the PCB layout. As shown in Fig. 2, the best way to design the PCB trace is using the flow through layout. The gray lines represent the PCB traces. The ground pins (pin3, pin6, pin9, pin12, pin13, and pin14) of AZ128S-08F are negative reference pins. **At least one of these pins should be directly connected to the GND rail of PCB.** To get minimum parasitic inductance, the path length should keep as short as possible.

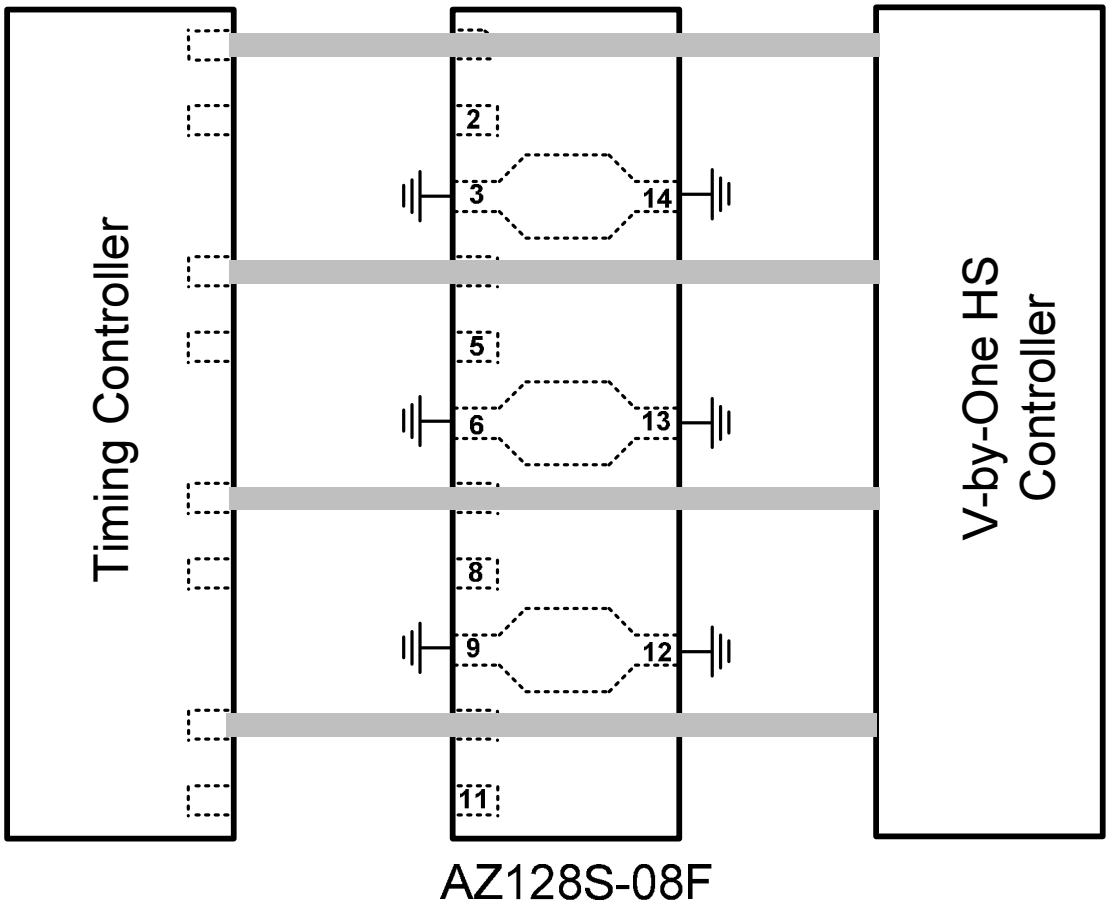


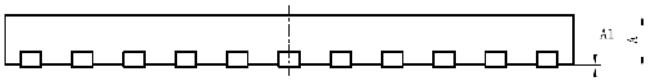
Fig. 2 V-by-One HS layout diagram (for LCD panel).

Mechanical Details

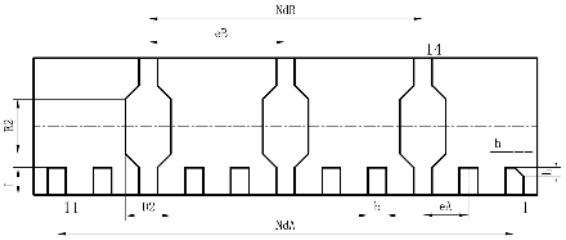
DFN5515P14E

PACKAGE DIAGRAMS

Top View



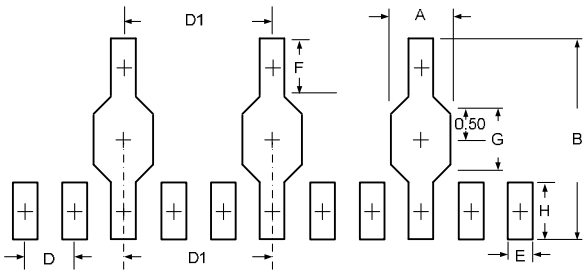
Side View



Bottom View

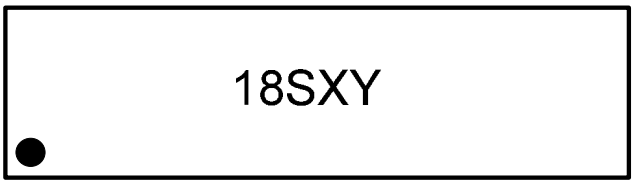
Symbol	Millimeters		
	min	nom	max
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	5.45	5.50	5.55
D2	0.45	0.50	0.55
NdA	5.00BSC		
eA	0.50BSC		
eB	1.50BSC		
NdB	3.00BSC		
E	1.45	1.50	1.55
E2	0.55	0.60	0.65
L	0.20	0.30	0.40
h	0.05	0.10	0.15

Land Layout



DIMENSIONS	
DIM	MILLIMETERS
A	0.56
B	1.80
D	0.50
D1	1.50
E	0.26
F	0.43
G	0.62
H	0.50

MARKING CODE



18S = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ128S-08F.R7G (Green Part)	18SXY

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ128S-08F.R7G	Green	T/R	7 inch	3,000/reel	3 reels= 9,000/box	6 boxes =54,000/carton

Revision History

Revision	Modification Description
Revision 2015/07/31	Preliminary Release.
Revision 2017/05/15	Formal Release.