Sup*IR*Buck™

10A HIGHLY INTEGRATED
WIDE-INPUT VOLTAGE, SYNCHRONOUS BUCK REGULATOR

Features

- Input Voltage Range: 3V to 26V
- Output Voltage Range: 0.5V to 12V
- Continuous 10A Load Capability
- Constant On-Time control
- Excellent Efficiency at very low output current levels
- Gate drive charge pump option to maximize efficiency at higher output current levels
- Compensation Loop not Required
- Programmable switching frequency, soft start, and over current protection
- Power Good Output
- Precision Voltage Reference (0.5V, +/-1%)
- Enable Input with Voltage Monitoring Capability
- Pre-bias Start Up
- Under/Over Voltage Fault Protection
- Ultra small, low profile 5 x 6mm QFN Package
- Lead-free, halogen-free and RoHS compliant

Applications

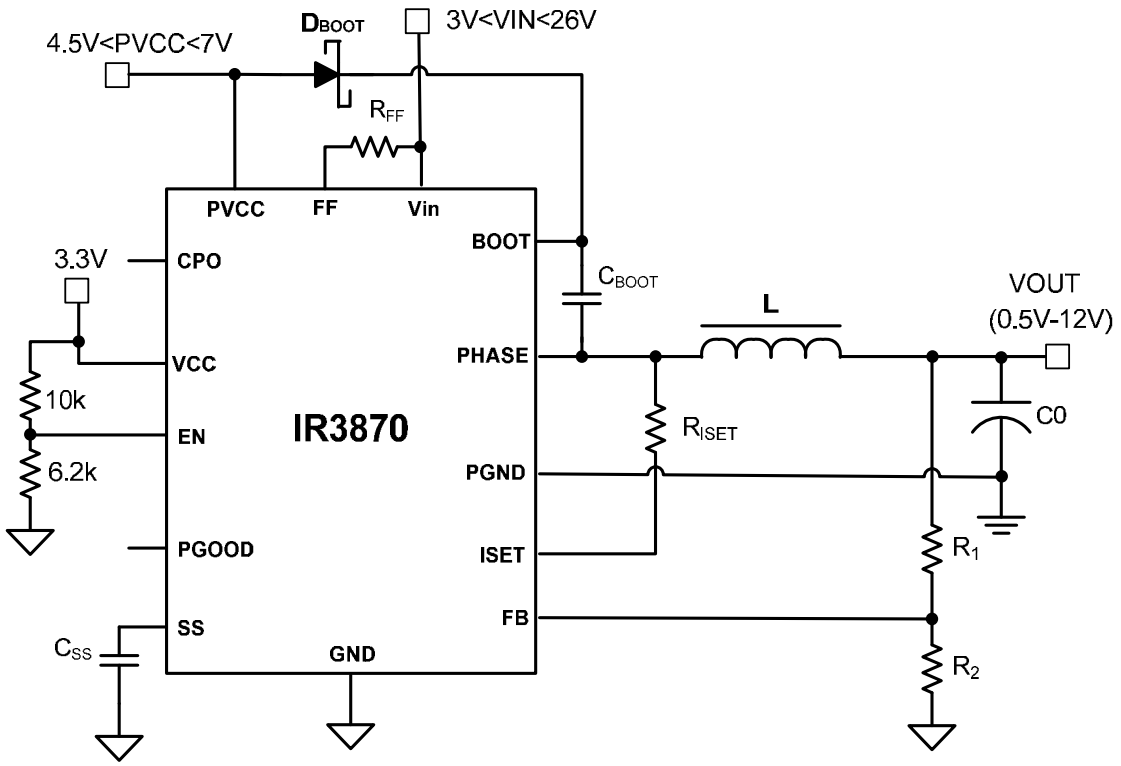
- Notebook and desktop computers
- Game consoles
- Consumer electronics - STB, LCD TV, Printers
- General purpose POL DC-DC Converters

Description

The IR3870M ***SupIRBuck™*** is an easy-to-use, fully integrated and highly efficient DC/DC voltage regulator. The onboard constant on time hysteretic controller and MOSFETs make IR3870 a space-efficient solution that delivers up to 10A of precisely controlled output voltage in 60° C ambient temperature applications without airflow.

Programmable switching frequency, soft start, and over current protection allows for a very flexible solution suitable for many different applications. The combination of the gate drive charge pump option and constant on time control allow efficiency optimization in the whole output current range, making this device an ideal choice for battery powered applications.

Additional features include pre-bias startup, very precise 0.5V reference, over/under voltage shut down, power good output, and enable input with voltage monitoring capability.



Typical Notebook Application Circuit Diagram

ABSOLUTE MAXIMUM RATINGS

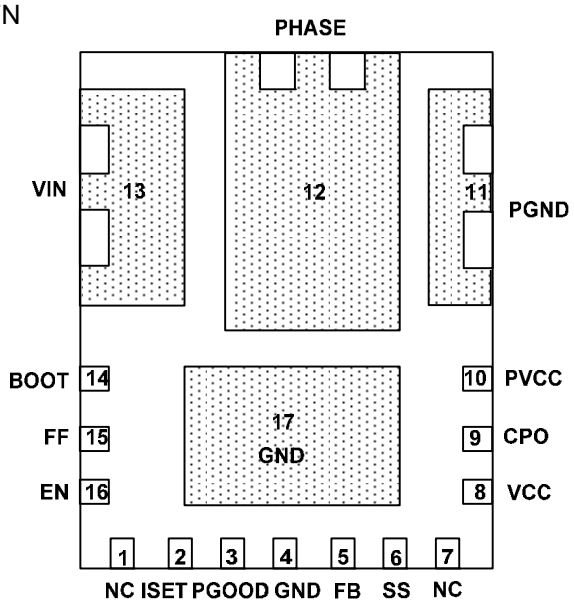
(Voltages referenced to GND unless otherwise specified)

- VIN 30V
- VCC 3.9V
- PVCC 7.5V
- Boot 40V
- PHASE ..... -0.3V to 30V(DC), -5V(100ns)
- Boot to PHASE..... 7.5V
- FF 30V
- PGND to GND ..... -0.3V to +0.3V
- All other pins 3.9V
- Storage Temperature Range ..... -65°C To 150°C
- Junction Temperature Range ..... -10°C To 150°C
- ESD Classification ..... JEDEC Class 1C
- Moisture sensitivity level..... JEDEC Level 3@260 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PACKAGE INFORMATION

5mm x 6mm POWER QFN



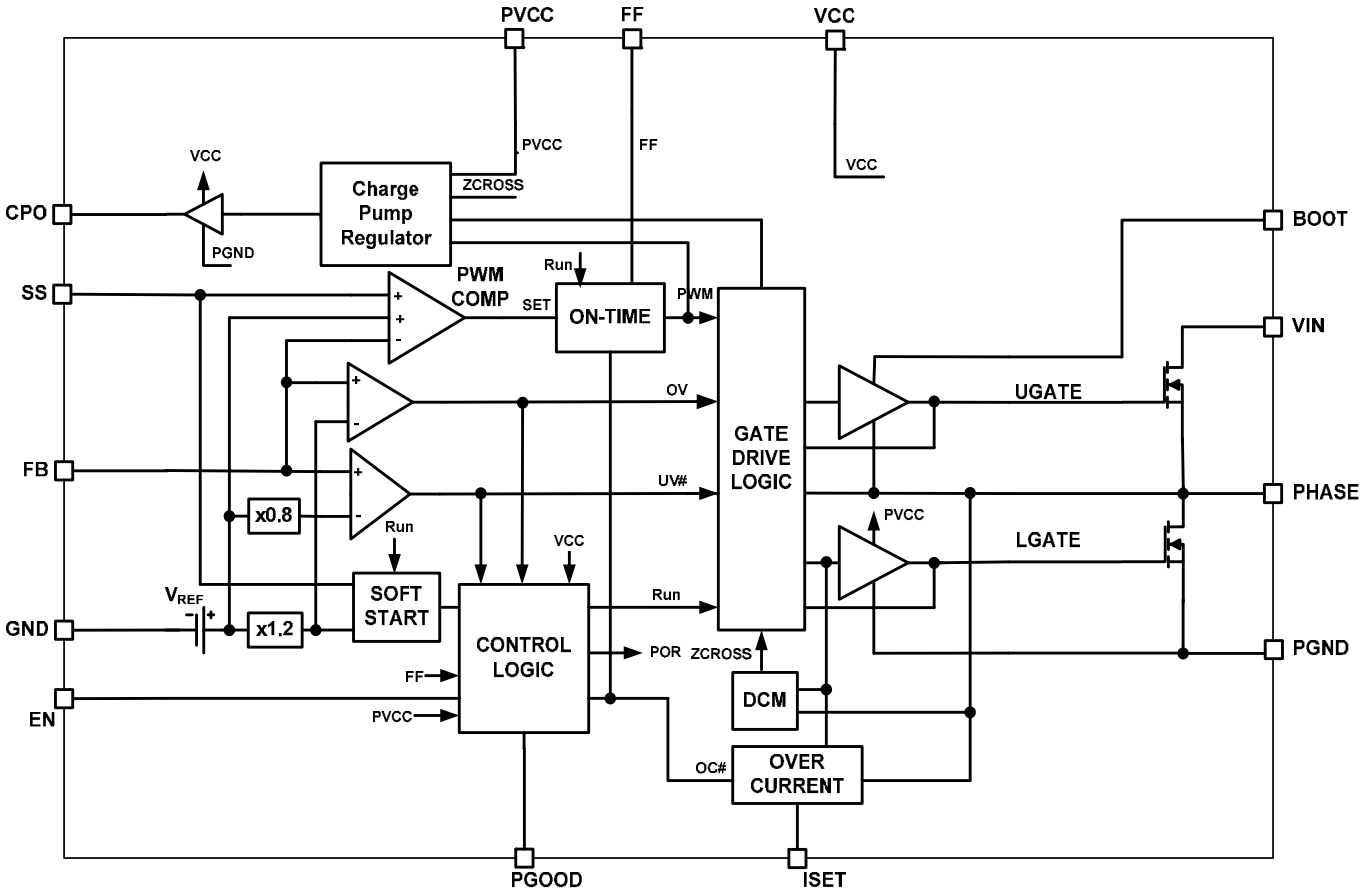
$\theta_{JA} = 35°C/W$

$\theta_{J\text{-}PCB} = 2°C/W$

ORDERING INFORMATION

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER REEL
M	IR3870MTRPbF	23	4000
M	IR3870MTR1PbF	23	750

Block Diagram



Pin Description

NAME	NUMBER	I/O LEVEL	DESCRIPTION
NC	1		No connection
ISET	2		Connecting resistor to PHASE pin sets over current trip point
PGOOD	3	5V	Power good – pull up to 5V
GND	4,17	Reference	Bias return and signal reference
FB	5	3.3V	Inverting pin of PWM comparator and OVP/PGood sense
SS	6	3.3V	Set soft start slew-rate with a capacitor to GND
NC	7		No connection
VCC	8	3.3V	Internal bias supply
CPO	9	0.75V	Charge pump output
PVCC	10	5V	Gate drive supply
PGND	11	Reference	Power return
PHASE	12	VIN	Phase node (or switching node) of MOSFET half bridge
VIN	13	VIN	Input voltage for the system.
BOOT	14	VIN +PVCC	Bootstrapped gate drive supply – connect a capacitor to PHASE
FF	15	VIN	Input voltage feed forward – sets on-time with a resistor to VIN
EN	16	5V	Enable – turns device on or off

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
VIN	Input Voltage	3	26*	V
VCC	Supply Voltage	3	3.6	
Boot to PHASE	Supply Voltage		7.0	
V_{OUT}	Output Voltage	0.5	12	
I_{OUT}	Output Current	0	10	A
Fs	Switching Frequency		1000	kHz

* Note: PHASE pin must not exceed 30V.

Electrical Specifications

Unless otherwise specified, these specification apply over VIN = 12V, PVCC = 7VDC, $0^oC \leqslant T_J \leqslant 125^oC$.

PARAMETER	NOTE	TEST CONDITION	MIN	TYP	MAX	UNIT
BIAS SUPPLIES						
VCC Turn-on Threshold					3	V
VCC Turn-off Threshold			2.65			V
VCC Threshold Hysteresis				60		mV
PVCC Turn-on Threshold					3.05	V
PVCC Turn-off Threshold			2.65			V
PVCC Threshold Hysteresis				60		mV
VCC Shutdown Current		EN=LOW		30	60	µA
VCC Operating Current		RFF = 180kΩ, EN = HIGH		1.2		mA
PVCC Operating Current		RFF = 180kΩ, EN = HIGH, Fs = 500kHz		8		mA
PVCC Shutdown Current		EN=LOW		20	60	µA
FF Shutdown Current		EN=LOW		0.1	2	µA
V_{IN} Shutdown Current		EN=LOW		0	1	µA
PHASE Shutdown Current		EN=LOW		0.25	2	µA
CONTROL LOOP						
Reference Accuracy, V_{REF}			0.495	0.5	0.505	V
On-Time Accuracy		R_{FF} = 180 kΩ, $T_J = 65^0C$	280	300	320	ns
Min Off Time				300		ns
Soft-Start Current		EN = HIGH	8	10	12	µA
FAULT PROTECTION						
ISET pin output current			18	20	22	µA
Under Voltage Threshold		Falling V_{FB} & monitor PGOOD	0.37	0.4	0.43	V
Under Voltage Hysteresis		Rising V_{FB}		7.5		mV
Over Voltage Threshold		Rising V_{FB} & monitor PGOOD	0.56	0.6	0.64	V
Over Voltage Hysteresis	1	Rising V_{FB}		7.5		mV
PGOOD Delay Threshold (V_{SS})				0.6		V

Electrical Specifications (continued)

Unless otherwise specified, these specification apply over VIN = 12V, PVCC = 7VDC, 0°C ≤ TJ ≤ 125°C.

PARAMETER	NOTE	TEST CONDITION	MIN	TYP	MAX	UNIT
GATE DRIVE						
Dead time	1	Monitor body diode conduction on PHASE pin	5		30	ns
UPPER MOSFET						
Static Drain-to-Source On-Resistance		PVCC =5V, I_D =10A, T_J =25°C		14.7		mΩ
Static Drain-to-Source On-Resistance		PVCC =5V, I_D =10A, T_J =125°C			26	mΩ
Static Drain-to-Source On-Resistance		PVCC =7V, I_D =10A, T_J =25°C		11.9		mΩ
Static Drain-to-Source On-Resistance		PVCC =7V, I_D =10A, T_J =125°C			22	mΩ
Diode Forward Voltage		V_{GS} =0V, I_S =10A, T_J =25°C			1.0	V
LOWER MOSFET						
Static Drain-to-Source On-Resistance		PVCC =5V, I_D =10A, T_J =25°C		6.2		mΩ
Static Drain-to-Source On-Resistance		PVCC =5V, I_D =10A, T_J =125°C			11	mΩ
Static Drain-to-Source On-Resistance		PVCC =7V, I_D =10A, T_J =25°C		5.1		mΩ
Static Drain-to-Source On-Resistance		PVCC =7V, I_D =10A, T_J =125°C			9	mΩ
Diode Forward Voltage		V_{GS} =0V, I_S =10A, T_J =25°C			1.0	V
CHARGE PUMP OUTPUT						
Source Resistance		I_{CPO} =15mA		3.3	5	Ω
Sink Resistance		I_{CPO} =15mA		1	2.1	Ω
Charge Pump Disable Threshold, $V_{CP\ TH}$			6.7	7.2		V
LOGIC INPUT AND OUTPUT						
EN Rising Threshold			1.13	1.21	1.29	V
EN Hysteresis			40	100	160	mV
EN Input Current					1	µA
PGOOD pull down resistance		I_{PGOOD} =2mA		50	100	Ω

Notoe1: Guaranteed by design, not tested in production

TYPICAL OPERATING DATA (25°C)

(Circuit of Figure 15, VCC = 3.3V, V5 = 5V, V_{IN} = 12.6V, F = 500kHz Unless otherwise noted)

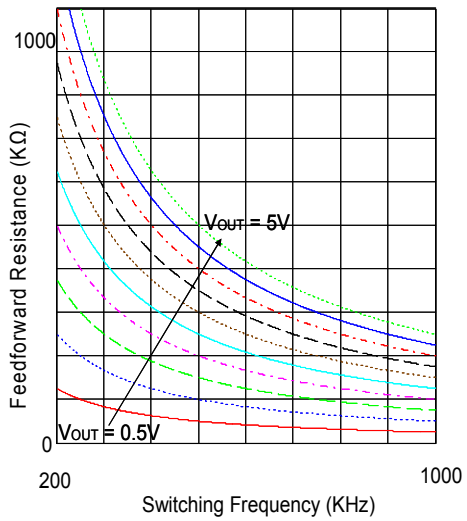


Figure 1. Feedforward Resistance Vs Switching Frequency: 0.5V V_{OUT} step

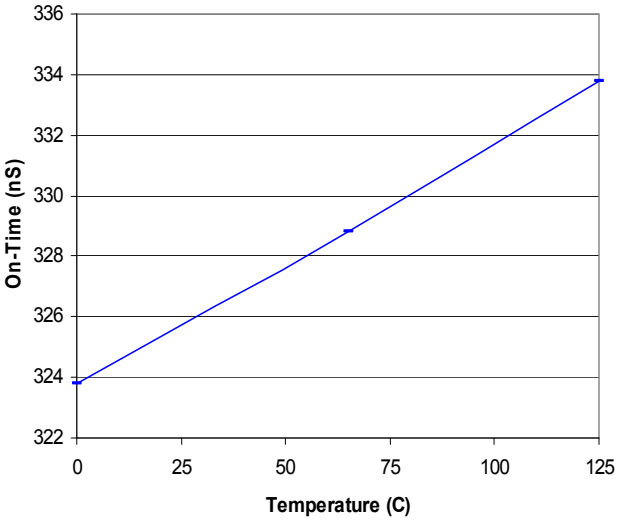


Figure 3. On-Time Variation in DCM: V_{IN} = 12V, V_{OUT} =1.1V, RFF = 180kOhm

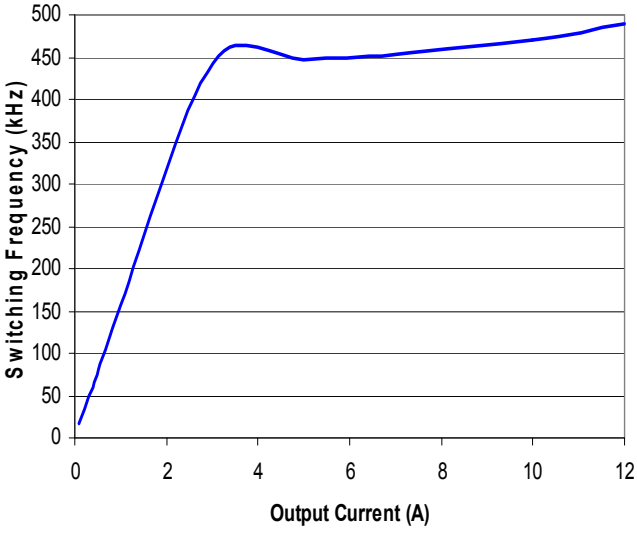


Figure 2. Switching Frequency Vs Output Current

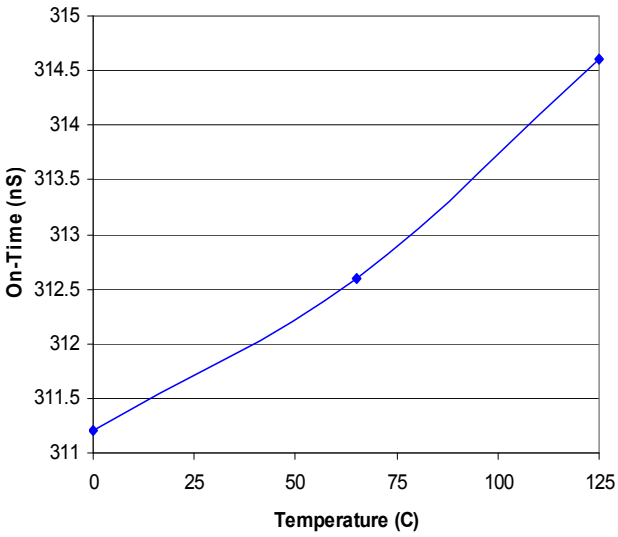


Figure 4. On-Time Variation in CCM: V_{IN} = 12V, V_{OUT} =1.1V, RFF = 180kOhm

TYPICAL OPERATING DATA (25°C)

(Circuit of Figure 15, VCC = 3.3V, V5 = 5V, V_{IN} = 12.6V, F = 500kHz Unless otherwise noted)

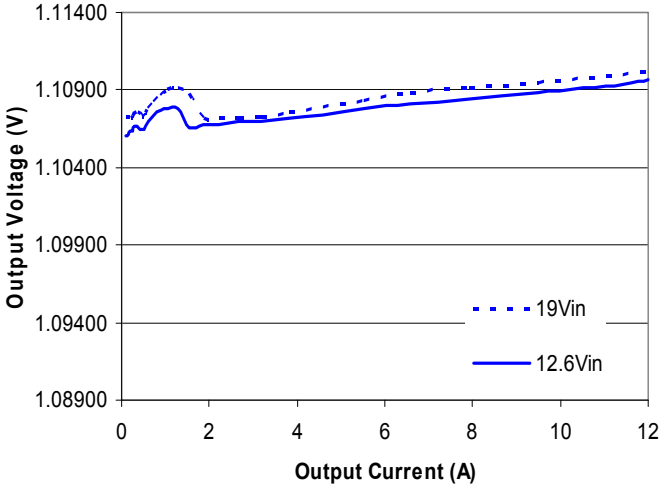


Figure 5. Output Voltage Regulation Vs Output Current

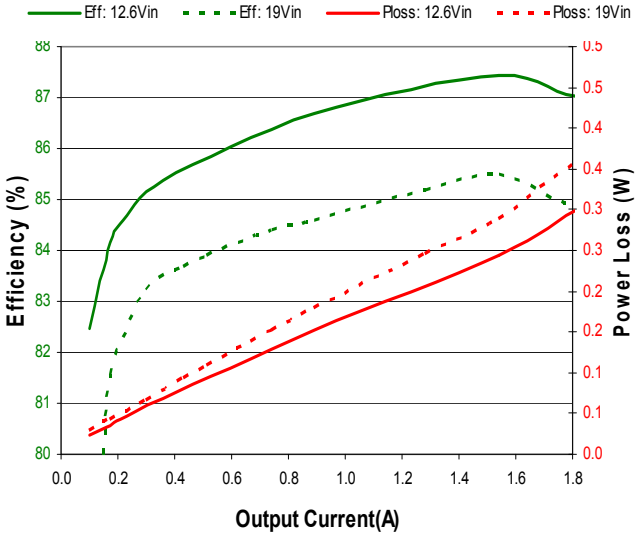


Figure 7. Light load Efficiency: V_{OUT} = 1.1V

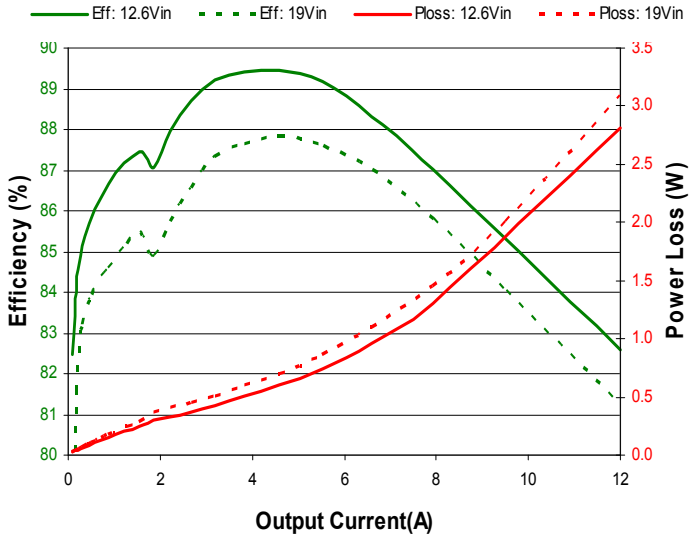


Figure 6. System Efficiency: V_{OUT} = 1.1V

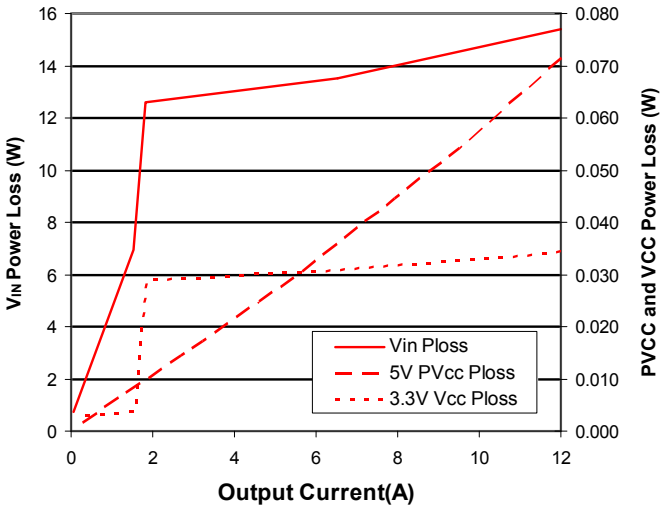
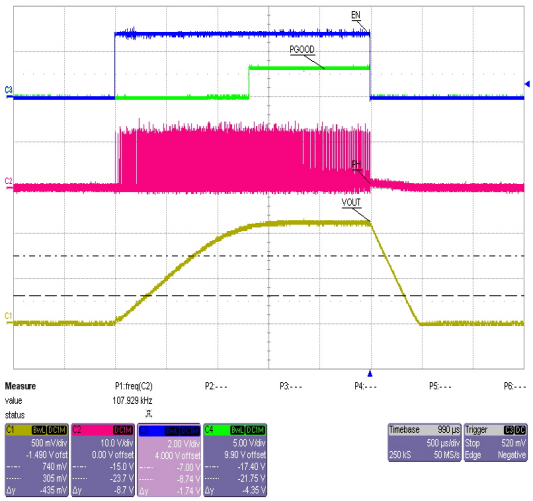


Figure 8. Input Power Vs Output Current

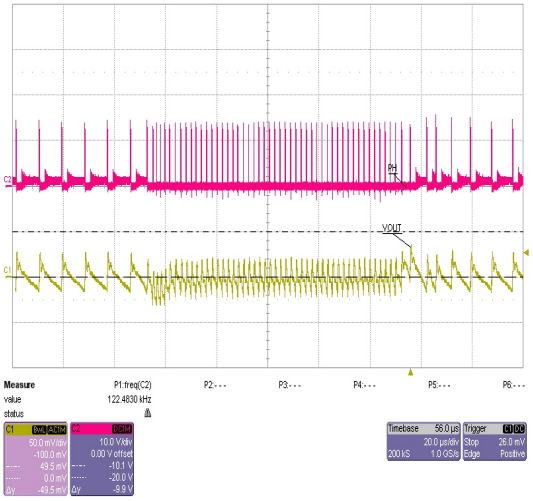
TYPICAL OPERATING WAVEFORM (25°C)

(Circuit of Figure 15, VCC = 3.3V, V5 = 5V, V_{IN} = 12.6V, F = 500kHz, Unless otherwise noted)



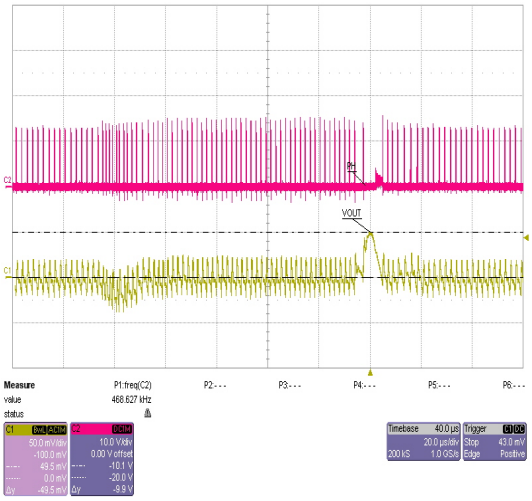
CH1: Vout (500mV/div); 500uS/div
CH2: PHASE (10V/div)
CH3: EN (2V/div) CH4: PGOOD (5V/div)

Figure 9: Shutdown/EN at I_{OUT} = 500mA



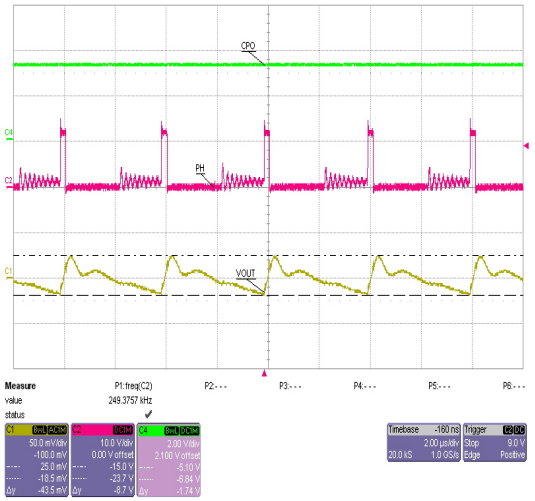
CH1: Vout (50mV/div); 20uS/div
CH2: PHASE (10V/div)

Figure 11: FCCM/CCM transition from 0.5A to 5A at 12.6V_{IN}: 30mV overshoot, 15mV undershoot



CH1: Vout (50mV/div); 20uS/div
CH2: Phase (10V/div)

Figure 10: Load Step (2A to 10A) Transient (5A/us) at 12.6V_{IN}: 50mV overshoot, 25mV undershoot

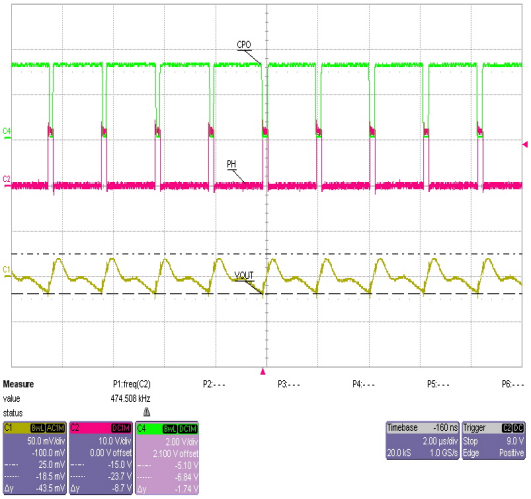


CH1: Vout (50mV/div); CH2: Phase (10V/div) CH4: CPO (2V/div); Time: 2uS/div)

Figure 12: Charge Pump Off at I_{OUT} = 1A

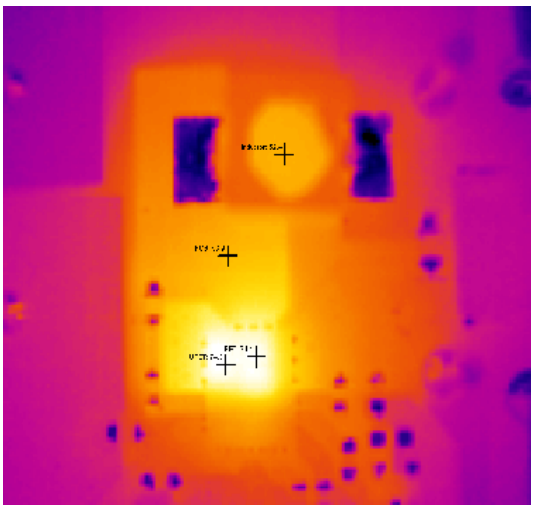
TYPICAL OPERATING WAVEFORM con't (25°C)

(Circuit of Figure 15, VCC = 3.3V, V5 = 5V, V_{IN} = 12.6V, F = 500kHz, Unless otherwise noted)



CH1: Vout (50mV/div); CH2: Phase (10V/div)
CH4: CPO (2V/div); Time: 2uS/div)

Figure 13: Charge Pump On at I_{OUT} = 3A



IC: 75°C, Inductor: 53°C, PCB: 54°C

Figure 14: Thermal Image: V_{IN} = 19V, I_{OUT} = 10A, Ta= 25°C, no air flow

TYPICAL APPLICATION CIRCUIT WITH CHARGE PUMP OPTION

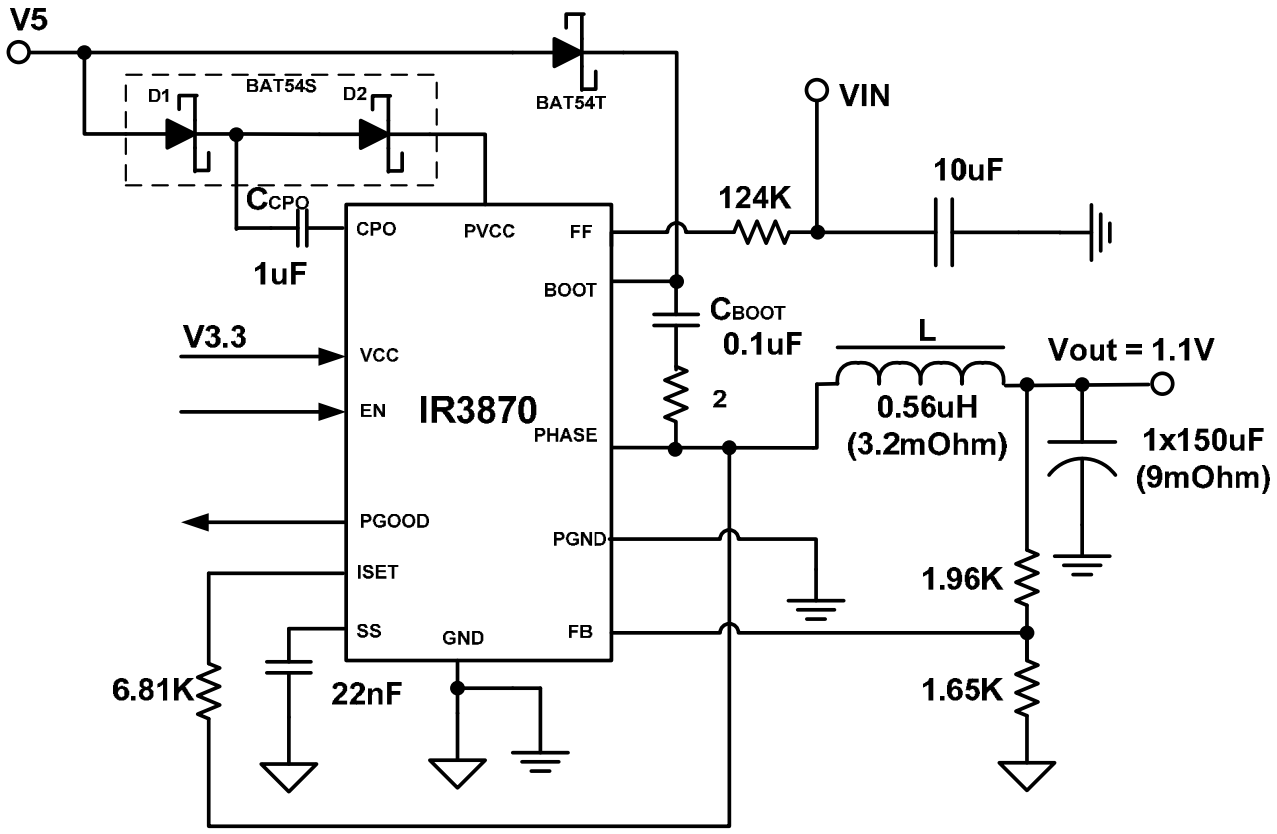


Figure 15. Application Circuit with Charge Pump used to boost Sync FET gate drive voltage from 5V to ~7V, resulting in improved efficiency at higher output current levels
F = 500kHz, V_{OUT} = 1.1V

Circuit Description

PWM COMPARATOR
The PWM comparator initiates a SET signal (PWM pulse) when the FB pin falls below the reference (VREF) or the soft start (SS) voltage.

ON-TIME GENERATOR
The PWM comparator initiates a SET signal (PWM pulse) when the FB pin falls below the reference (VREF) or the soft start (SS) voltage. The PWM on-time duration is programmed with an external resistor (RFF) from the input supply (VIN) to the FF pin. The simplified equation for RFF is shown in equation 1. The FF pin is held to an internal reference after EN goes HIGH. A copy of the current in RFF charges a timing capacitor, which sets the on-time duration, as shown in equation 2.

$$R_{FF} = \frac{V_{OUT}}{1V \cdot 20\,pF \cdot F_{SW}} \quad (1)$$

$$T_{ON} = \frac{R_{FF} \cdot 1V \cdot 20\,pF}{V_{IN}} \quad (2)$$

SOFT START
An internal 10uA current source charges the external capacitor on the SS pin to set the output voltage slew rate during the soft start interval. The output voltage reaches regulation when the FB pin is above the under voltage threshold and the UV# = HIGH. Once the voltage on the SS pin is above the PGOOD delay threshold, the combination of the SSDelay and UV# signals release the PGOOD pin. With EN = LOW, the capacitor voltage and SS pin is held to the FB pin voltage.

OVER CURRENT MONITOR
The over current circuitry monitors the output current during each switching cycle. The voltage across the synchronous MOSFET, VPHASE, is monitored for over current and zero crossing. The minimum LGATE interval allows time to sample VPHASE.
The over current trip point is programmed with a resistor from the ISET pin to PHASE pin, as shown in equation 3. When over current is detected, the output gates are tri-state and SS voltage is pulled to 0V. This initiates a new soft start cycle. If there are three consecutive OC events the IR3870 will disable switching. Toggling VCC or EN will allow the next start up.

$$R_{SET} = \frac{R_{DSON} \cdot I_{OC}}{20\ \mu A} \quad (3)$$

GATE DRIVE LOGIC
The gate drive logic features adaptive dead time, diode emulation, and a minimum lower gate interval.
An adaptive dead time prevents the simultaneous conduction of the upper and lower MOSFETs. The lower gate voltage must be below approximately 1V after PWM goes HIGH before the upper MOSFET can be gated on. Also, the upper gate voltage, the difference voltage between UGATE and PHASE, must be below approximately 1V after PWM goes LOW and before the lower MOSFET can be gated on. The control MOSFET is gated on after the adaptive delay for PWM = HIGH and the synchronous MOSFET is gated on after the adaptive delay for PWM = LOW. The lower MOSFET is driven 'off' when the signal ZCROSS indicates that the inductor current has reversed as detected by the PHASE voltage crossing the zero current threshold. The synchronous MOSFET stays 'off' until the next PWM falling edge. When the lower peak of inductor current is above zero, a forced continuous current condition is selected set. The control MOSFET is gated on after the adaptive delay for PWM = HIGH, and the synchronous MOSFET is gated on after the adaptive delay for PWM = LOW.
The synchronous MOSFET gate is driven on for a minimum duration. This minimum duration allows time to recharge the bootstrap capacitor and allows the current monitor to sample the phase voltage.

CONTROL LOGIC
The control logic monitors input power sources, sequences the converter through the soft-start and protective modes and indicates output voltage status on the PGOOD pin. PVCC and VCC pins are continuously monitored and will disable the IR3870 if the voltage of either pin drops below the falling thresholds.
The IR3870 will initiate a soft start when the PVCC is in the normal range and the EN pin = HIGH. In the event of a sustained overload a counter keeps track of 4 consecutive soft-start cycles and then disables the IR3870.
If the overload is momentary and the output

Circuit Description

voltage is within regulation before four consecutive soft-start cycles, PGOOD transitions HIGH to reset the counter.

OVER VOLTAGE PROTECTION

The IR3870 monitors the voltage at the FB node. If the FB voltage is above the over voltage threshold, the gates are turned off and the PGOOD signal is pulled low. Toggling VCC will allow the next start up.

CHARGE PUMP

The purpose of the charge pump is to improve the system efficiency. A combination of VCC, V5 and three external components are used to boost PVCC up to V_{CPTH}. PVCC drives the synchronous MOSFET and reduces the R_{DSON} when compared to a regular 5V rail driver. The lower FET RDSON reduces the conduction power loss as discussed in the *Power Loss* section. The charge pump is continuously enabled for FCCM = HIGH. The charge pump circuit is disabled when FCCM = LOW and the output loading is less than half of inductor current ripple. In this case, PVCC is two diode voltages away from the V5 rail. Therefore, the power loss for driver is reduced. The charge pump circuit stops switching the CPO pin for PVCC above V_{CPTH}.

COMPONENT SELECTION

Selection of components for the converter is an iterative process which involves meeting the specifications and trade-offs between performance and cost. The following sections will guide one through the process.

Inductor Selection

Inductor selection involves meeting the steady state output ripple requirement, minimizing the switching loss of upper MOSFETs, meeting transient response specifications and minimizing the output capacitance. The output voltage includes a DC voltage and a small AC ripple component due to the low pass filter which has incomplete attenuation of the switching harmonics. Neglecting the inductance in series with the output capacitor, the magnitude of the AC voltage ripple is determined by the total inductor ripple current flow through the total equivalent series resistance (ESR) of the output capacitor bank.

$$\Delta I = \frac{V_{OUT}}{L} \cdot (1 - D) \cdot Ts = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot L \cdot Fs} \quad (4)$$

One can use equation 4 to find the required inductance. The main advantage of small inductance is increased inductor current slew rate during a load transient, which leads to a smaller output capacitance requirement as discussed in the *Output Capacitor Selection* section. The draw back of using smaller inductances is increased switching power loss in upper MOSFET, which reduces the system efficiency and increases the thermal dissipation as discussed in the *Power Loss* section.

Input Capacitor Selection

The main function of the input capacitor bank is to provide the input ripple current and fast slew rate current during the load current step up. The input capacitor bank must have adequate ripple current carrying capability to handle the total RMS current. Figure 16 shows a typical input current. Equation 5 shows the RMS input current. The RMS input current contains the DC load current and the inductor ripple current. As shown in equation 4, the inductor ripple current is unrelated to the load current. The maximum RMS input current occurs at the maximum output current. The maximum power dissipation in the input capacitor equals the square of the maximum RMS input current times the input capacitor's total ESR.

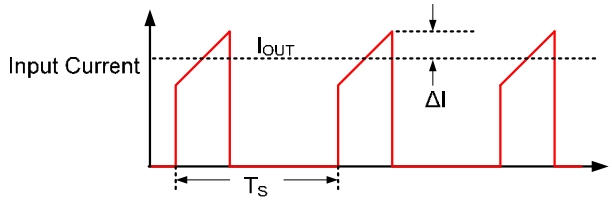


Figure 16. Typical Input Current Waveform.

$$I_{IN\_RMS} = \sqrt{\frac{1}{Ts} \cdot \int_0^{Ts} f^2(t) \cdot dt}$$

$$= I_{OUT} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta I}{I_{OUT}}\right)^2} \quad (5)$$

The voltage rating of the input capacitor needs to be greater than the maximum input voltage because of high frequency ringing at the phase node. The typical percentage is 25%.

Output Capacitor Selection

Selection of the output capacitor requires meeting voltage overshoot requirements during load removal, and meeting steady state output ripple voltage requirements. The output capacitor is the most expensive converter component and increases the overall system cost. The output capacitor decoupling in the converter typically includes the low frequency capacitor, such as Specialty Polymer Aluminum, and mid frequency ceramic capacitors.

The first purpose of output capacitors is to provide current when the load demand exceeds the inductor current, as shown in Figure 17. Equation 6 shows the charge requirement for a certain load. The advantage provided by the IR3870 at a load step is to reduce the delay compared to a fixed frequency control method (in microseconds or (1-D)*Ts). If the load increases right after the PWM signal goes low, the longest delay will be equal to the minimum lower gate on as shown in the *Electrical Specification* table. The IR3870 also reduces the inductor current slew time, the time it takes for the inductor current to reach equality with the output current, by increasing the switching frequency up to 2.5MHz. The result reduces the recovery time.

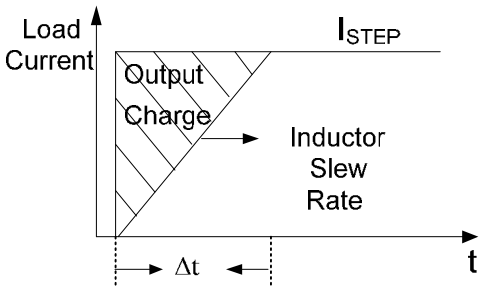


Figure 17. Charge Requirement during Load Step

$$Q = C \cdot V = 0.5 \cdot Istep \cdot \Delta t \quad (6a)$$

$$C_{OUT} = \frac{1}{V_{DROP}} \left[\frac{1}{2} \cdot \frac{L \cdot \Delta Istep^2}{(V_{IN} - V_{OUT})} \right] \quad (6b)$$

The output voltage drops, VDROP, initially depending on the characteristic of the output capacitor. VDROP is the sum of the equivalent series inductance (ESL) of the output capacitor times the rate of change of the output current and the ESR times the change of the output current.

VESR is usually much greater than VESL. The IR3870 requires a total ESR such that the ripple voltage at the FB pin is greater than 7mV.

The second purpose of the output capacitor is to minimize the overshoot of the output voltage when the load decreases as shown in Figure 18. By using the law of energy before and after the load removal, equation 7 shows the output capacitance requirement for a load step.

$$C_{OUT} = \frac{L \cdot I_{STEP}^2}{V_{OS}^2 - V_{OUT}^2} \quad (7)$$

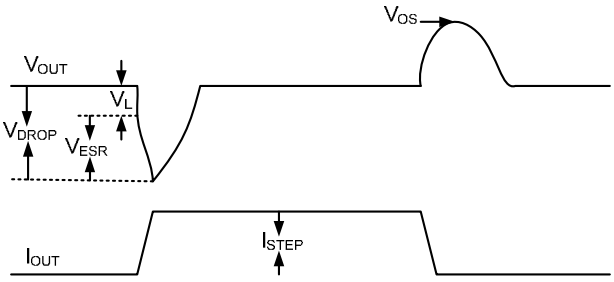


Figure 18. Typical Output Voltage Response Waveform.

Boot Capacitor Selection

The boot capacitor starts the cycle fully charged to a voltage of VB(0). Cg equals 1.16nF in IR3870. Choose a sufficiently small ΔV such that VB(0)-ΔV exceeds the maximum gate threshold voltage to turn on the high side MOSFET.

$$C_{BOOT} = C_g \cdot \left(\frac{V_B(0)}{\Delta V} - 1 \right) \quad (8)$$

Choose a boot capacitor value larger than the calculated C_{BOOT} in equation 8. A typically value of 0.1uF uses. The voltage rating of this part needs to be larger than VB(0) plus the desired derating voltage. Its ESR and ESL needs to be low in order to allow it to deliver the large current and di/dt's which drive MOSFETs most efficiently. In support of these requirements a ceramic capacitor should be chosen.

DESIGN EXAMPLE

Design Criteria:

Input Voltage, VIN, = 6V to 21V
Output Voltage, VOUT = 1.1V
Switching Frequency, FS = 500KHz
Inductor Ripple Current, ΔI = 4A
Maximum Output Current, IOUT = 10A
Over Current Trip, IOC = 14A
Overshoot Allowance, VOS = VOUT + 100mV
Undershoot Allowance, VDROP = 100mV

Find R_{FF} :

$$R_{FF} = \frac{1.1V}{1V \cdot 20\,pF \cdot 500KHz} = 110\,K\Omega$$

Pick a standard value 110 kΩ, 1% resistor.
Find R_{SET} :

$$R_{ISET} = \frac{1.4 \cdot 6.8m\Omega \cdot 14A}{20\mu A} = 6.7K\Omega$$

The R_{DSON} of the lower MOSFET could be expected to increase by a factor of 1.4 over temperature. Therefore, pick a 6.81 kΩ, 1% standard resistor.

Find a resistive voltage divider for V_{OUT} = 1.1V:

$$V_{FB} = \frac{R2}{R2 + R1} \cdot V_{OUT} = 0.5V$$

R_2 = 1.65kΩ, R_1 = 1.96 kΩ, both 1% standard resistors.

Choose the soft start capacitor:
Once the soft start time has chosen, such as 1000us to reach to the reference voltage, a 22nF for CSS is used to meet 1000us.

Choose an inductor to meet the design specification:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I \cdot F_S} = \frac{1.1V \cdot (21V - 1.1V)}{21V \cdot 4A \cdot 500KHz} = 0.52u\,H$$

$$\Delta I = \frac{1.1V \cdot (21V - 1.1V)}{21V \cdot 0.56uH \cdot 500K\,Hz} = 3.7A$$

Choose an inductor with the lowest DCR and AC power loss as possible to increase the overall system efficiency. For instance, choose an FDU0650-R56M manufactured by TOKO. The inductance of this part is 820nH and has 3.2mΩ DCR. Ripple current needs to be recalculated using the chosen inductor.

Choose an input capacitor:

$$I_{IN\_RMS} = 10A \cdot \sqrt{\frac{1.1V}{21V}} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{3.7A}{10A} \right)^2} = 2.4A$$

A Panasonic 10uF (ECJ3YB1E106M) accommodates 6 Arms of ripple current at 300KHz. Due to the chemistry of multilayer ceramic capacitors, the capacitance varies over temperature and operating voltage, both AC and DC. One 10uF capacitor is recommended. In a practical solution, one 1uF capacitor is required along with 10uF. The purpose of the 1uF capacitor is to suppress the switching noise and deliver high frequency current.

Choose an output capacitor:

To meet the undershoot specification, select a set of output capacitors which has an equivalent ESR of 10mΩ (100mV/10A). To meet the overshoot specification, equation 7 will be used to calculate the minimum output capacitance. As a result, 243uF will be needed for 10A load remover. Combine those two requirements, one can choose a set of output capacitors from manufactures such as SP-Cap (Specialty Polymer Capacitor) from Panasonic or POSCAP from Sanyo. A 270uF (EEFSX0D271) from Panasonic is recommended.

This capacitor has 9mΩ ESR which leaves margin for the voltage drop of the ESL during load step up. The typical ESL for this capacitor is around 2nH. Refer to *Output Capacitor Selection* section for all ceramic capacitor solution.

LAYOUT RECOMMENDATION

Bypass Capacitor:

One 1uF high quality ceramic capacitor should be placed as near VCC pin as possible. The other end of capacitor can be connected to a via or connected directly to GND plane. Use a GND plane instead of thin trace to the GND pin because this thin traces have too much higher impedance. A 1uF is recommended for both V5 and PVCC and repeat the layout procedure above for those signals.

Charge Pump:

We recommend that D1, D2 and C_{CPO} be placed as close to the CPO and PVCC pins as possible. If those components can not be placed on the same layer as IR3870, a minimum of two vias are needed for the connection of C_{CPO} and CPO pin and the connection of D2 and PVCC.

Boot Circuit:

C_{BOOT} should be placed near the BOOT and PHASE pins to reduce the impedance when the upper MOSFET turns on. D_{BOOT} does not need to be close to C_{BOOT} because the average current to charge C_{BOOT} is small during the on time of lower MOSFET.

Power Stage:

Figure 19 shows the flowing current path for the on and off periods. The on time path has low average DC current with high AC current. Therefore, it is recommended to place the input ceramic capacitor, upper, and lower MOSFET in a tight loop as shown in Figure 19.

The purpose of the tight loop from the input ceramic capacitor is to suppress the high frequency (10MHz range) switching noise and reduce Electromagnetic Interference (EMI). If this path has high inductance, the circuit will cause voltage spikes and ringing, and increase the switching loss. The off time path has low AC and high average DC current. Therefore, it should be laid out with a tight loop and wide trace at both ends of the inductor. Lowering the loop resistance reduces the power loss. The typical resistance value of 1-ounce copper thickness is 0.5mΩ per square inch.

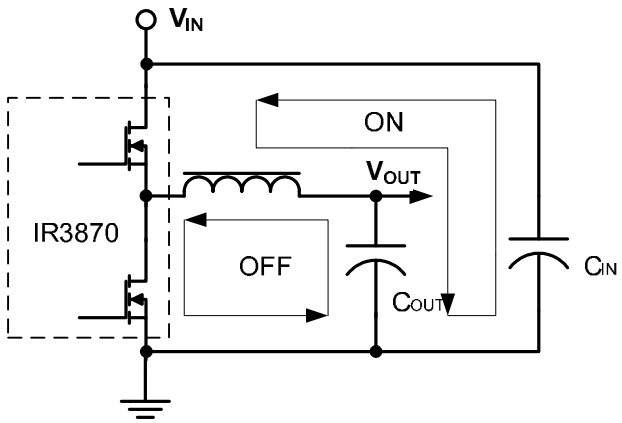


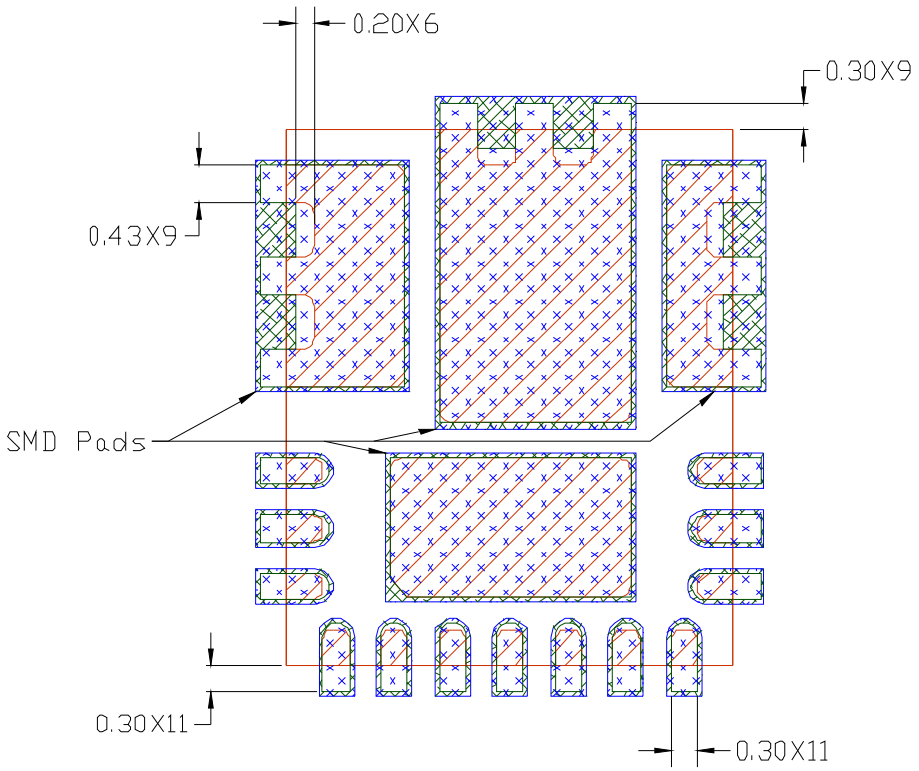
Figure 19. Current Path of Power Stage

PCB Metal and Components Placement

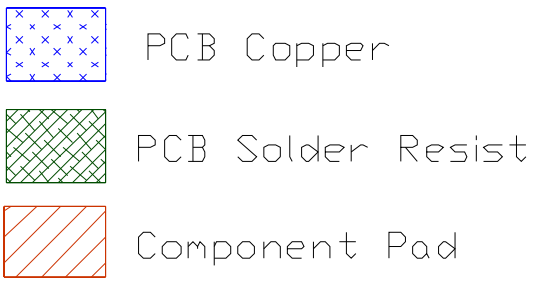
Lead lands (the 13 IC pins) width should be equal to nominal part lead width. The minimum lead to lead spacing should be ⩾ 0.2mm to minimize shorting.

Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large toe fillet that can be easily inspected.

Pad lands (the 4 big pads) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than; 0.17mm for 2 oz. Copper or no less than 0.1mm for 1 oz. Copper or no less than 0.23mm for 3 oz. Copper.



All Dimensions In mm

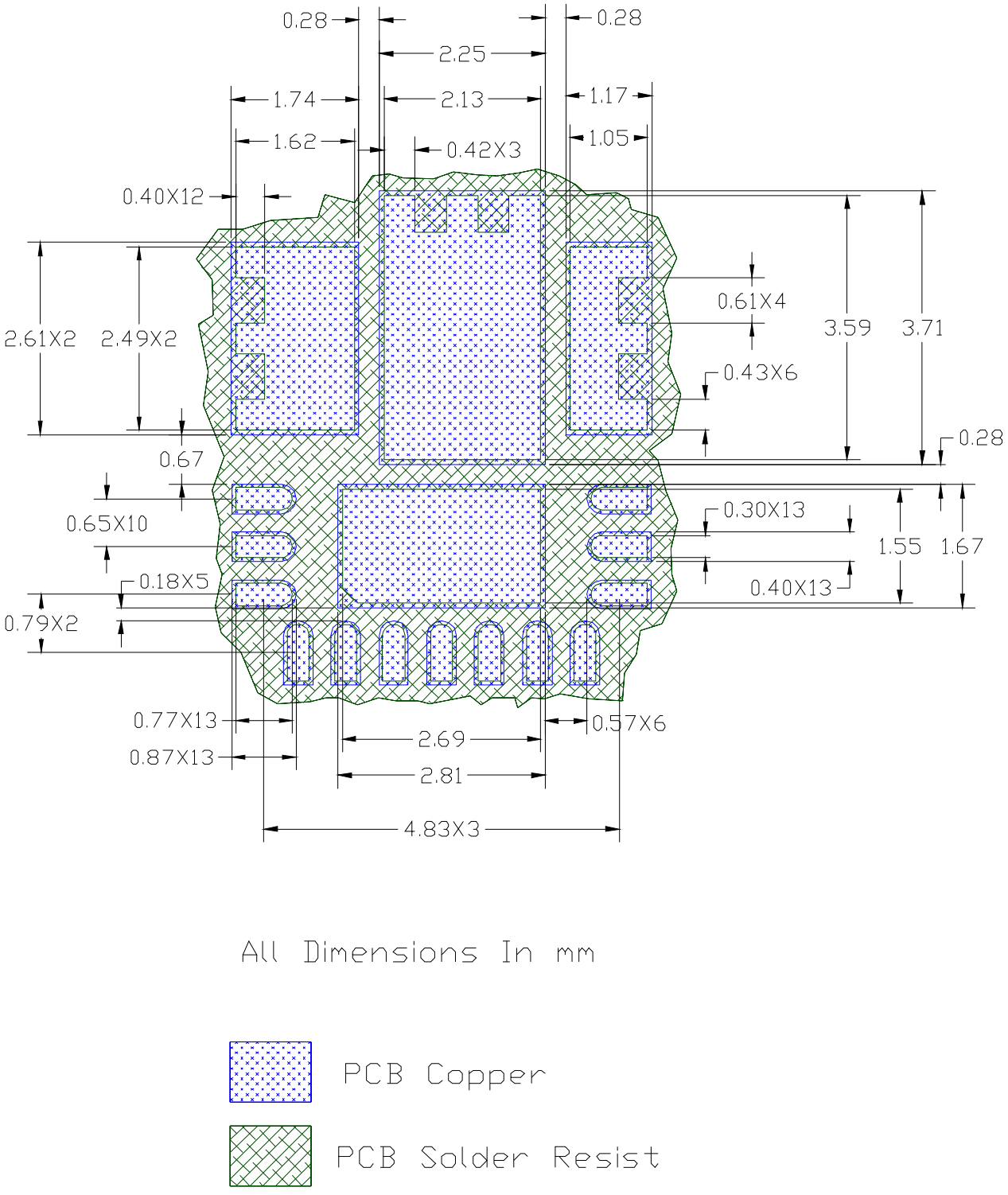


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist misalignment.

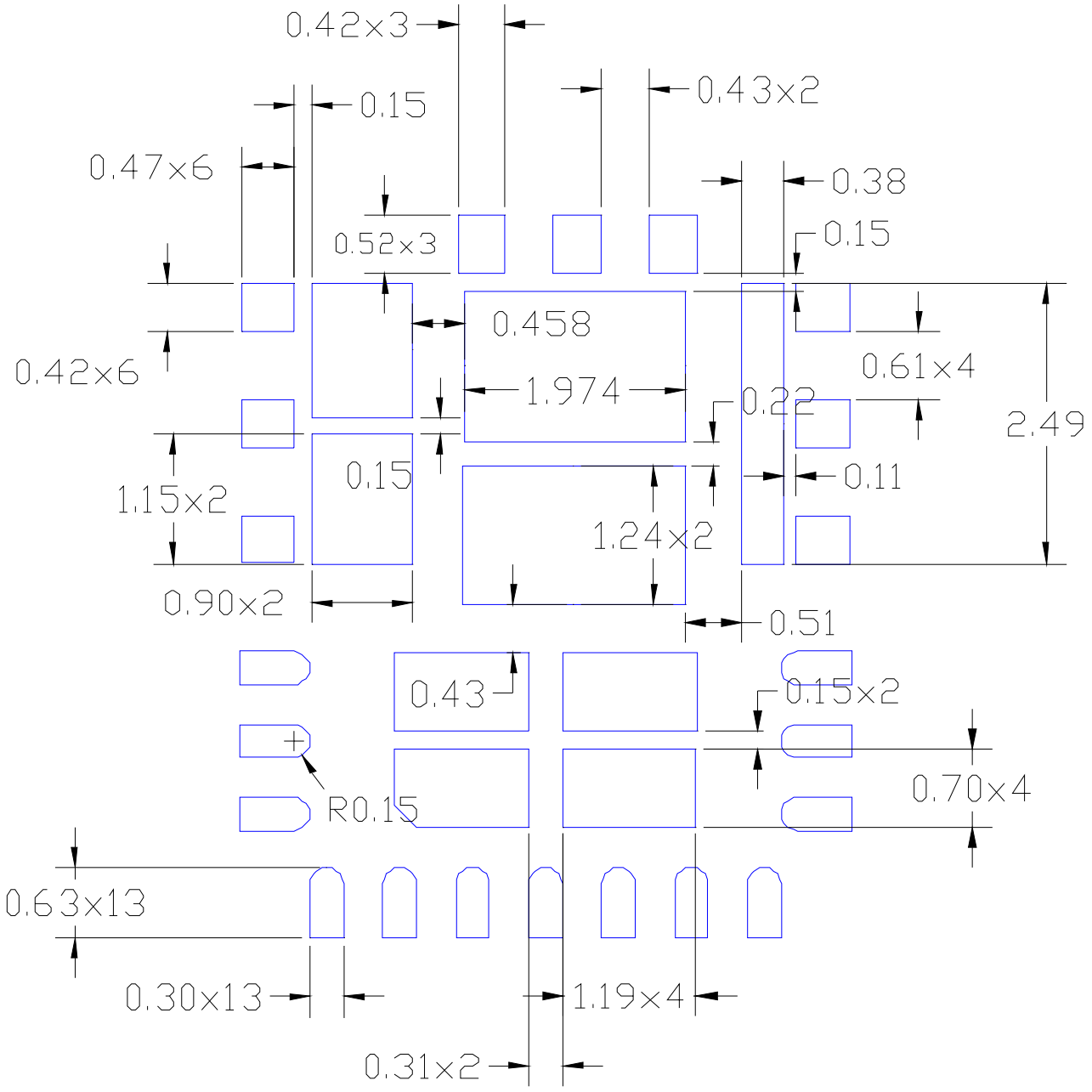
Ensure that the solder resist in between the lead lands and the pad land is ⩾ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

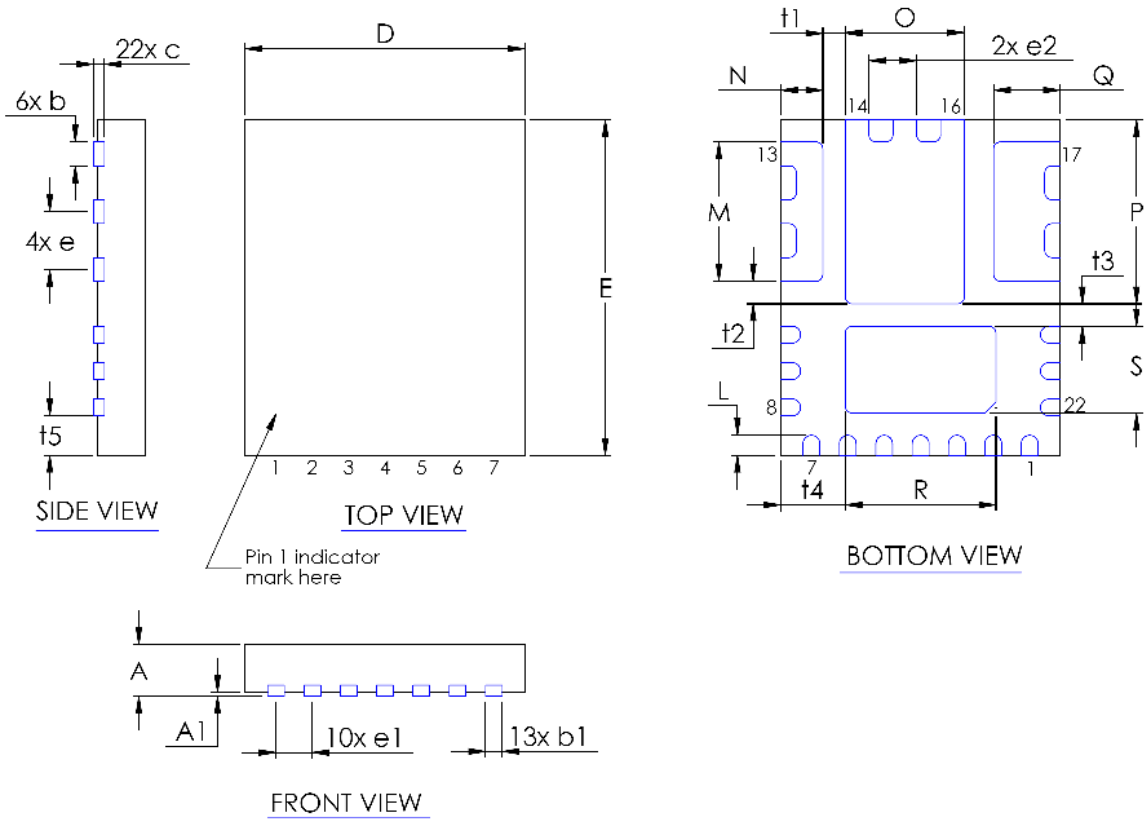


Stencil Design

The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will open.

The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back in order to decrease the risk of shorting the center land to the lead lands when the part is pushed into the solder paste.





DIM	MILIMITERS		INCHES		DIM	MILIMITERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.8	1	0.0315	0.0394	L	0.35	0.45	0.0138	0.0177
A1	0	0.05	0	0.002	M	2.441	2.541	0.0962	0.1001
b	0.375	0.475	0.1477	0.1871	N	0.703	0.803	0.0277	0.0314
b1	0.25	0.35	0.0098	0.1379	O	2.079	2.179	0.0819	0.0858
c	0.203 REF.		0.008 REF.		P	3.242	3.342	0.1276	0.1316
D	5.000 BASIC		1.970 BASIC		Q	1.265	1.365	0.0498	0.05374
E	6.000 BASIC		2.364 BASIC		R	2.644	2.744	0.1042	0.1081
e	1.033 BASIC		0.0407 BASIC		S	1.5	1.6	0.0591	0.063
e1	0.650 BASIC		0.0256 BASIC		t1, t2, t3	0.401 BASIC		0.016 BACIS	
e2	0.852 BASIC		0.0259 BASIC		t4	1.153 BASIC		0.045 BASIC	
					t5	0.727 BASIC		0.0286 BASIC	

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information