



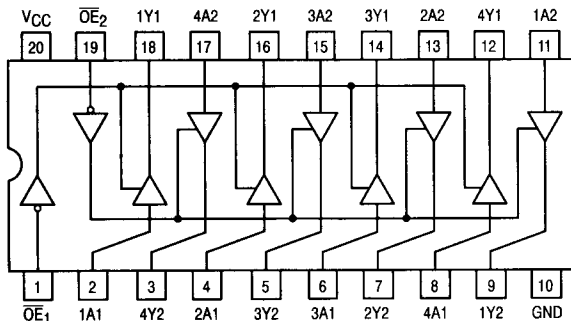
# Octal Buffer With Active Low Enable 3-State Non-Inverted Outputs

ELECTRICALLY TESTED PER:  
MIL-M-38510/33203

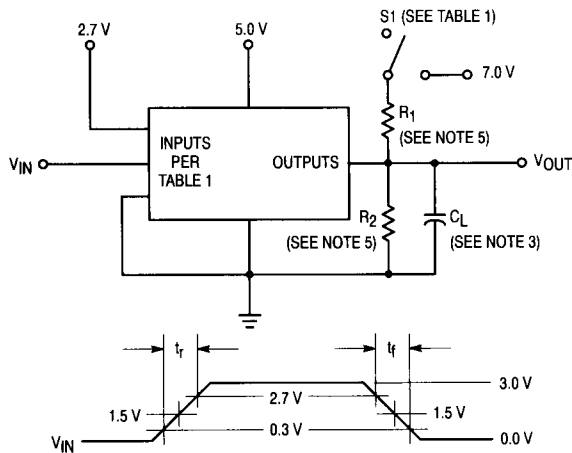
The F244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Register
- Outputs Sink 64 mA
- 15 mA Source Current
- Input Clamp Diodes Limit High Speed Termination Effects

## LOGIC DIAGRAM



## AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 4-118

## Military 54F244



### AVAILABLE AS:

- 1) JAN: JM38510/33203BXA
- 2) SMD: N/A
- 3) 883: 54F244/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: R  
CERFLAT: S  
LCC: 2 /

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

### PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
OE <sub>1</sub>	1	1	1	VCC
1A1	2	2	2	VCC
4Y2	3	3	3	OPEN
2A1	4	4	4	VCC
3Y2	5	5	5	OPEN
3A1	6	6	6	VCC
2Y2	7	7	7	OPEN
4A1	8	8	8	VCC
1Y2	9	9	9	OPEN
GND	10	10	10	GND
1A2	11	11	11	VCC
4Y1	12	12	12	OPEN
2A2	13	13	13	VCC
3Y1	14	14	14	OPEN
3A2	15	15	15	VCC
2Y1	16	16	16	OPEN
4A2	17	17	17	VCC
1Y1	18	18	18	OPEN
OE <sub>2</sub>	19	19	19	VCC
VCC	20	20	20	VCC

BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

### TRUTH TABLE

Inputs		Output
OE <sub>1</sub> , OE <sub>2</sub>	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level X = Immaterial  
L = LOW Voltage Level Z = HIGH Impedance

WAVEFORMS

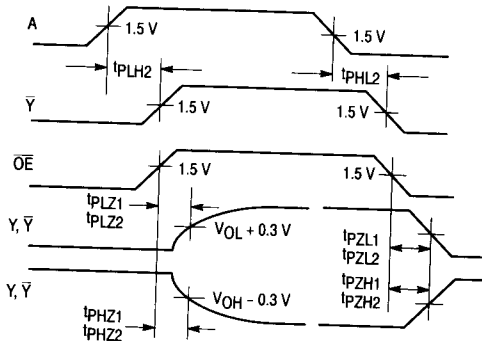


Table 1

Test Type	S1
t <sub>PLH</sub>	open
t <sub>PHL</sub>	open
t <sub>PHZ</sub>	open
t <sub>PZH</sub>	open
t <sub>PLZ</sub>	closed
t <sub>PZL</sub>	closed

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.4		2.4		2.4		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3.0 mA, V <sub>IN</sub> = 2.0 V, other input = 0.8 V.
V <sub>OL</sub>	Logical "0" Output Voltage		0.55		0.55		0.55	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA, V <sub>IN</sub> = 0.8 V (both inputs).
V <sub>IC</sub>	Input Clamping Voltage		-1.2					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs are open.
I <sub>IHH</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 7.0 V, other inputs are open.
I <sub>OD</sub>	Diode Current	65		65		65		mA	V <sub>CC</sub> = 4.5 V, V <sub>IN</sub> = GND, other input = GND, V <sub>OUT</sub> = 2.5 V.
I <sub>IL1</sub>	Logical "0" Input Current (OE)	-0.3	-1.6	-0.3	-1.6	-0.3	-1.6	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.5 V, other inputs are open.
I <sub>IL2</sub>	Logical "0" Input Current (A)	-0.3	-1.0	-0.3	-1.0	-0.3	-1.0	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.5 V, other inputs are open.
I <sub>OS</sub>	Output Short Circuit Current	-100	-325	-100	-325	-100	-325	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, other input = 0 V, V <sub>OUT</sub> = 0 V.
I <sub>IOZH</sub>	Output Off Current High		50		50		50	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.0 V, other input = 0 V, V <sub>OUT</sub> = 2.4 V.
I <sub>IOZL</sub>	Output Off Current Low		-50		-50		-50	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.0 V, other input = 4.5 V, V <sub>OUT</sub> = 0.5 V.
I <sub>CCH</sub>	Power Supply Current		60		60		60	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, other input = 0 V.
I <sub>CCL</sub>	Power Supply Current		90		90		90	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V (all inputs).
I <sub>CCZ</sub>	Power Supply Current Off		90		90		90	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, other inputs are open.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.8		0.8		0.8	V	V <sub>CC</sub> = 4.5 V.

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Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C	+ 125°C	- 55°C		
	Functional Tests	Subgroup 7		Subgroup 8A	Subgroup 8B	per Truth Table with $V_{CC} = 4.5\text{ V}$ , (Repeat at), $V_{CC} = 5.5\text{ V}$ , $V_{INL} = 0.5\text{ V}$ , $V_{INH} = 2.5\text{ V}$ .

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
	Switching Parameters:	Min	Max	Min	Max	Min	Max		
$t_{PHL2}$	Propagation Delay /Data-Output Output High-Low	1.0	6.0	1.0	7.0	1.0	7.0	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = R_2 = 500\ \Omega$ .
$t_{PLH2}$	Propagation Delay /Data-Output Output Low-High	1.0	5.2	1.0	6.5	1.0	6.5	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = R_2 = 500\ \Omega$ .
$t_{PLZ2}$	Propagation Delay /Data-Output Output Low-High	2.0	6.0	2.0	7.5	2.0	7.5	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = R_2 = 500\ \Omega$ .
$t_{PHZ2}$	Propagation Delay /Data-Output Output High-Low	2.0	6.0	2.0	7.0	2.0	7.0	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = R_2 = 500\ \Omega$ .
$t_{PZL2}$	Propagation Delay /Data-Output Output Low-High	2.0	7.0	2.0	8.5	2.0	8.5	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = R_2 = 500\ \Omega$ .
$t_{PZH2}$	Propagation Delay /Data-Output Output High-Low	2.0	5.7	2.0	7.0	2.0	7.0	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = R_2 = 500\ \Omega$ .

NOTES:

1. Pulse generator has the following characteristics:  $t_r = t_f \leq 2.5\text{ ns}$ ,  $PRR \leq 1.0\text{ MHz}$  and  $Z_{OUT} = 50\ \Omega$ .
2. Terminal conditions (pin not designated may be high  $\geq 2.0\text{ V}$ , low  $\leq 0.8\text{ V}$ , or open).
3.  $C_L = 50\text{ pF} \pm 10\%$  including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5.  $R_1 = R_2 = 500\ \Omega \pm 5.0\%$ .