Fully Integrated, 8-Channel Voltage Controlled Amplifier for Ultrasound with Passive CW Mixer, 0.75 nV/rtHz, 99 mW/CH

Check for Samples: VCA5807

FEATURES

- **8-Channel Voltage Controlled Amplifier**
  - **LNA, VCAT, PGA, LPF, and CW Mixer**
- **Programmable Low-Noise Amplifier (LNA)**
  - **24/18/12 dB Gain**
  - **0.25/0.5/1 V_{PP} Linear Input Range**
  - **0.63/0.7/0.9 nV/rtHz Input Referred Noise**
  - **Programmable Active Termination**
- **40 dB Low Noise Voltage Controlled Attenuator (VCAT)**
- **24/30 dB Programmable Gain Amplifier (PGA)**
- **3rd Order Linear Phase Low-Pass Filter (LPF)**
  - **10, 15, 20, 30 MHz**
  - **Butterworth Characteristics**
- **Noise/Power Optimizations (Full Chain)**
  - **99 mW/CH at 0.75 nV/rtHz**
  - **56 mW/CH at 1.1 nV/rtHz**
  - **80 mW/CH at CW Mode**
- **Excellent Device-to-Device Gain Matching**
  - **±0.5 dB (typical) and ±1.05 dB (max)**
- **Low Harmonic Distortion**
- **Fast and Consistent Overload Recovery**
- **Low Frequency Sonar Signal Processing**
- **Passive Mixer for Continuous Wave Doppler (CWD)**
  - **Low Close-in Phase Noise –156 dBc/Hz at 1 KHz off 2.5 MHz Carrier**
  - **Phase Resolution of 1/16λ**
  - **Support 32X,16X, 8X, 4X and 1X CW Clocks**
  - **12dB Suppression on 3rd and 5th Harmonics**
  - **Flexible Input Clocks**
- **14mm x 14mm, 100-pin TQFP**

APPLICATIONS

- **Medical Ultrasound Imaging**
- **Nondestructive Evaluation Equipments**
- **Sonar Imaging**

DESCRIPTION

The VCA5807 is an integrated Voltage Controlled Amplifier (VCA) specifically designed for ultrasound systems in which high performance and small size are required. The VCA5807 integrates a complete time-gain-control (TGC) imaging path and a continuous wave Doppler (CWD) path. It also enables users to select one of various power/noise combinations to optimize system performance. Therefore, the VCA5807 is a suitable ultrasound analog front end solution not only for high-end systems, but also for portable systems.

The VCA5807 contains eight channels of voltage controlled amplifier (VCA), and CW mixer. The VCA includes Low noise Amplifier(LNA), Voltage controlled Attenuator (VCAT), Programmable Gain Amplifier (PGA), and Low-Pass Filter (LPF). The LNA gain is programmable to support 250 mV_{PP} to 1 V_{PP} input signals. Programmable active termination is also supported by the LNA. The ultra-low noise VCAT provides an attenuation control range of 40dB and improves overall low gain SNR which benefits harmonic imaging and near field imaging. The PGA provides gain options of 24 dB and 30 dB. Before the ADC, a LPF can be configured as 10 MHz, 15 MHz, 20 MHz, or 30 MHz to support ultrasound applications with different frequencies. In addition, the signal chain of the VCA5807 can handle signal frequency lower than 100 KHz, which enables it to be used not only in ultrasound applications but also in sonar applications.

The VCA5807 integrates a low power passive mixer and a low noise summing amplifier to accomplish on-chip CWD beamformer. 16 selectable phase-delays can be applied to each analog input signal. Meanwhile a unique 3rd and 5th order harmonic suppression filter is implemented to enhance CW sensitivity.

The VCA5807 is available in a 14mm x 14mm, 100-pin TQFP package and it is specified for operation from -40°C to 85°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

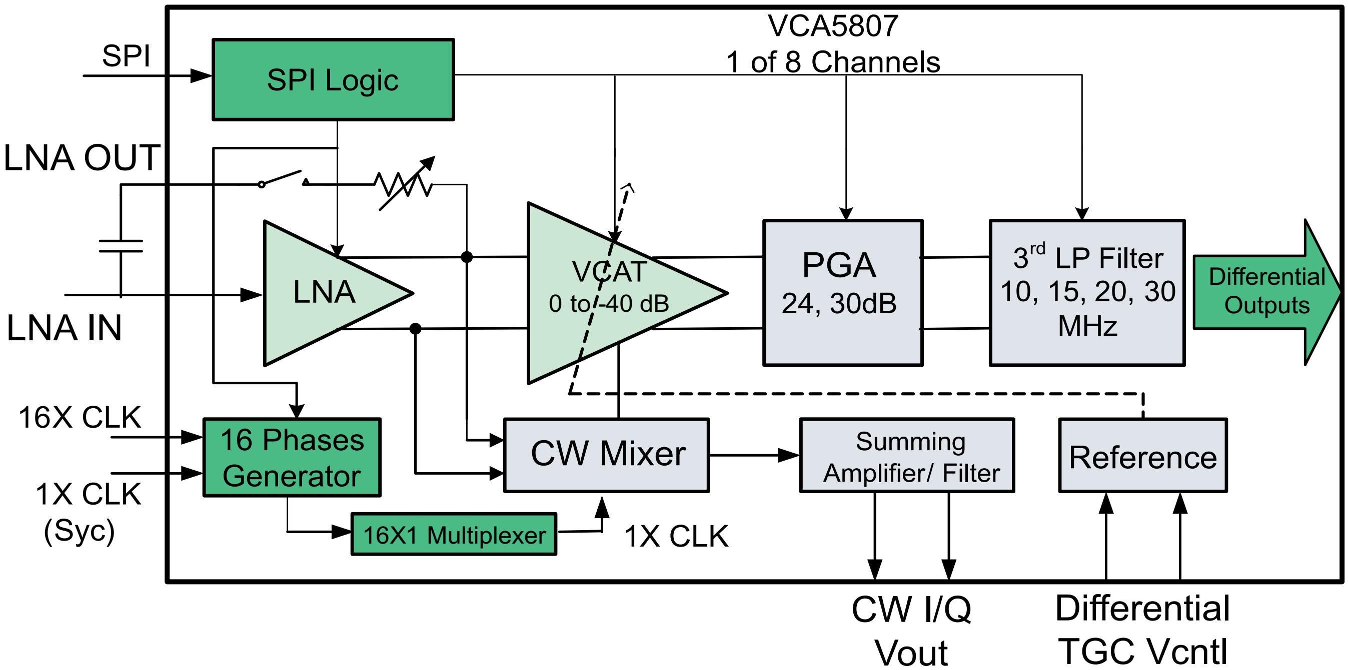


Figure 1. Block Diagram

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	PACKAGE TYPE	OPERATING	ORDERING NUMBER	PACKAGE QUANTITY
VCA5807	TQFP	-40°C to 85°C	VCA5807PZP	90

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range	AVDD	–0.3	3.9	V
	AVDD_5V	–0.3	6	V
Voltage at analog inputs and digital inputs		–0.3	min [3.6,AVDD+0.3]	V
Peak solder temperature(2)			260	°C
Maximum junction temperature (T_J), any condition			105	°C
Storage temperature range		–55	150	°C
Operating temperature range		-40	85	°C
ESD Ratings	HBM		2000	V
	CDM		500	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) Device complies with JSTD-020D.

THERMAL INFORMATION

THERMAL METRIC[1]		VCA5807 TQFP 100 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	25.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	6.1	
θ_{JB}	Junction-to-board thermal resistance	7.7	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	7.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.2	

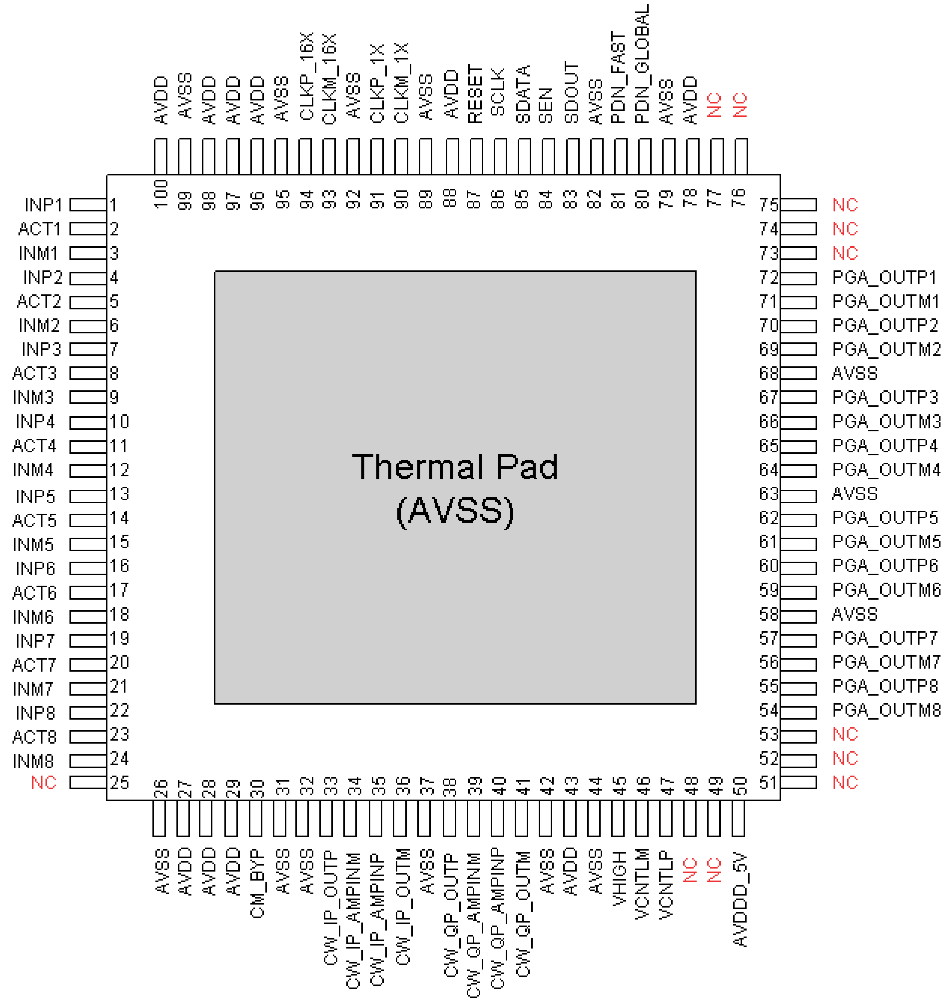
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
AVDD	3.15	3.6	V
AVDD_5V	4.75	5.5	V
Ambient Temperature, T_A	-40	85	°C

PINOUT INFORMATION

TQFP PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
2, 5, 8, 11, 14, 17, 20, 23	ACT1...ACT8	Active termination input pins for CH1~8.1 μF capacitors are recommended.
27, 28, 29, 43, 78, 88, 96, 97, 98, 100	AVDD	3.3V Analog supply for LNA, VCAT, PGA, LPF and CWD blocks.
50	AVDD_5V	5V Analog supply for LNA, VCAT, PGA, LPF and CWD blocks.
26, 31, 32, 37, 42, 44, 58, 63, 68, 79, 82. 89, 92, 95, 99	AVSS	Analog ground.
93	CLKM_16X	Negative input of differential CW 16X clock. Tie to GND when the CMOS clock mode is enabled. In the 4X, 8X, and 32X CW clock modes, this pin becomes the 4X, 8X, or 32X CLKM input. In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used. Please see CW Clock Selection.
94	CLKP_16X	Positive input of differential CW 16X clock. In 4X, 8X, and 32X clock modes, this pin becomes the 4X, 8X, or 32X CLKP input. In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used. Please see CW Clock Selection.

PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NO.	NAME	
90	CLKM_1X	Negative input of differential CW 1X clock. Tie to GND when the CMOS clock mode is enabled (Refer to Figure 94 for details). In the 1X clock mode, this pin is the In-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used. Please see CW Clock Selection.
91	CLKP_1X	Positive input of differential CW 1X clock. In the 1X clock mode, this pin is the In-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used. Please see CW Clock Selection.
30	CM_BYP	Bias voltage and bypass to ground. ≥ 1µF is recommended. To suppress ultra low frequency noise, 10µF can be used.
34	CW_IP_AMPINM	Negative differential input of the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINM and CW_IP_OUTP. This pin becomes the CH7 PGA negative output when PGA test mode is enabled. Can be floated if not used.
35	CW_IP_AMPINP	Positive differential input of the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINP and CW_IP_OUTM. This pin becomes the CH7 PGA positive output when PGA test mode is enabled. Can be floated if not used.
36	CW_IP_OUTM	Negative differential output for the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINP and CW_IP_OUTPM. Can be floated if not used.
33	CW_IP_OUTP	Positive differential output for the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINM and CW_IP_OUTP. Can be floated if not used.
39	CW_QP_AMPIN M	Negative differential input of the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINM and CW_QP_OUTP. This pin becomes CH8 PGA negative output when PGA test mode is enabled. Can be floated if not used.
40	CW_QP_AMPINP	Positive differential input of the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINP and CW_QP_OUTM. This pin becomes CH8 PGA positive output when PGA test mode is enabled. Can be floated if not used.
41	CW_QP_OUTM	Negative differential output for the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINP and CW_QP_OUTM. Can be floated if not used.
38	CW_QP_OUTP	Positive differential output for the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINM and CW_QP_OUTP. Can be floated if not used.
25, 48, 49, 51, 52, 53, 73, 74, 75, 76, 77	NC	Do not connect. Must leave floated
3, 6, 9, 12, 15, 18, 21, 24	INM1…INM8	CH1~8 complimentary analog inputs. Bypass to ground with ≥ 0.015µF capacitors. The HPF response of the LNA depends on the capacitors. Please see LOW-NOISE AMPLIFIER (LNA).
1, 4, 7, 10, 13, 16, 19, 22	INP1...INP8	CH1~8 analog inputs. AC couple to inputs with ≥ 0.1µF capacitors.
81	PDN_FAST	VCA partial (fast) power down control pin with an internal pull down resistor of 20kΩ. Active High.
80	PDN_GLOBAL	Global (complete) power-down control pin for the entire chip with an internal pull down resistor of 20kΩ. Active High.
54, 56, 59, 61, 64, 66, 69, 71	PGA_OUTMx	Negative PGA output
55, 57, 60, 62, 65, 67, 70, 72	PGA_OUTPx	Positive PGA output
87	RESET	Hardware reset pin with an internal pull-down resistor of 20kΩ. Active high.
86	SCLK	Serial interface clock input with an internal pull-down resistor of 20kΩ
85	SDATA	Serial interface data input with an internal pull-down resistor of 20kΩ
83	SDOUT	Serial interface data readout. High impedance when readout is disabled.
84	SEN	Serial interface enable with an internal pull up resistor of 20kΩ. Active low.
46	VCNTLM	Negative differential attenuation control pin.
47	VCNTLP	Positive differential attenuation control pin
45	VHIGH	Bias voltage; bypass to ground with ≥1µF. To suppress ultra low frequency noise, 10µF can be used.

ELECTRICAL CHARACTERISTICS

AVDD_5V = 5V, AVDD = 3.3V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN}= 5MHz, LNA = 18dB, PGA = 24dB, LPF Filter = 15MHz, low noise mode, V_{OUT}= –1dBFS (1.8V_{PP}), single-ended VCNTL mode, VCNTLM = GND, 2 kΩ load (ADC Rin), internal 500Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V=5V, AVDD=3.3V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
TGC FULL SIGNAL CHANNEL (LNA+VCAT+LPF)						
en (RTI)	Input voltage noise over LNA Gain(low noise mode)	R_S = 0Ω, f = 2MHz, LNA =24/18/12dB, PGA = 24dB		0.76/0.83/1.16		nV/rtHz
		R_S = 0Ω, f = 2MHz, LNA = 24/18/12dB, PGA = 30dB		0.75/0.86/1.12		
	Input voltage noise over LNA Gain(low power mode)	R_S = 0Ω, f = 2MHz, LNA = 24/18/12dB, PGA = 24dB		1.1/1.2/1.45		nV/rtHz
		R_S = 0Ω, f = 2MHz, LNA = 24/18/12dB, PGA = 30dB		1.1/1.2/1.45		
	Input Voltage Noise over LNA Gain(Medium Power Mode)	R_S = 0Ω, f = 2MHz, LNA = 24/18/12dB, PGA = 24dB		1/1.05/1.25		nV/rtHz
		R_S = 0Ω, f = 2MHz, LNA = 24/18/12dB, PGA = 30dB		0.95/1.0/1.2		
en (RTI)	Input voltage noise at low frequency	f = 100 KHz, INM Cap = 1uF, PGA integrator disabled (0x33[4]=1)		0.9		nV/rtHz
	Input referred current noise	Low Noise Mode/Medium Power Mode/Low Power Mode		2.7/2.1/2		pA/rtHz
NF	Noise figure	R_S = 200Ω, 200Ω active termination, PGA = 24dB, LNA = 12/18/24dB		3.85/2.4/1.8		dB
		R_S = 100Ω, 100Ω active termination, PGA = 24dB, LNA = 12/18/24dB		5.3/3.1/2.3		dB
NF	Noise figure	Rs = 500 Ω/1KΩ, no terminaiton, Low NF mode is enabled (Reg53[9]=1)		0.94/1.08		dB
		Rs=50Ω/200Ω, no terminaiton, Low noise mode (Reg53[9]=0)		2.35/1.05		dB
VIN_{MAX}	Maximum Linear Input Voltage	LNA gain = 24/18/12dB		250/500/1000		mV_{PP}
V_{CLAMP}	Clamp Voltage	Reg52[10:9] = 0, LNA = 24/18/12dB		350/600/1150		
	PGA Gain	Low noise mode		24/30		dB
		Medium/Low power mode		24/28.5		
	Total gain	LNA = 24dB, PGA = 30dB, Low noise mode		54		dB
		LNA = 24dB, PGA = 30dB, Med power mode		52.5		
		LNA = 24dB, PGA = 30dB, Low power mode		52.5		
$VOUT_{MAX}$	Maximum Linear Output Voltage	Defined as 0 dBFS		2		V_{PP}
	Ch-CH Noise Correlation Factor without Signal (1)	Summing of 8 channels		0		
	Ch-CH Noise Correlation Factor with Signal (1)	Full band (V_{CNTL} = 0/0.8)		0.15/0.17		
		1MHz band over carrier (V_{CNTL}= 0/0.8)		0.18/0.75		
	Output Referred Noise	V_{CNTL}= 0.6V (22 dB total channel gain)		40	67	nV/rtHz
		V_{CNTL}= 0, LNA = 18dB, PGA = 24dB		104	153	
		V_{CNTL}= 0, LNA = 24dB, PGA = 24dB		190		
	Narrow Band Integrated Output Noise	Noise over 2MHz band around carrier at V_{CNTL} = 0.6V (22dB total gain)		100	125	μV_{RMS}
	Input Common-mode Voltage	At INP and INM pins		2.4		V
	Input resistance			8		kΩ
		Preset active termination enabled		50/100/200/400		Ω
	Input capacitance			20		pF
	Input Control Voltage	V_{CNTLP} - V_{CNTLM}	0		1.5	V
	Common-mode voltage	V_{CNTLP} and V_{CNTLM}		0.75		V
	Gain Range			-40		dB
	Gain Slope	V_{CNTL}= 0.1V to 1.1V		35		dB/V
	Input Resistance	Between V_{CNTLP} and V_{CNTLM}		200		KΩ
	Input Capacitance	Between V_{CNTLP} and V_{CNTLM}		1		pF
	TGC Response Time	V_{CNTL}= 0V to 1.5V step function		1.5		µs
	3rd order-Low-pass Filter			10, 15, 20, 30		MHz
	Settling time for change in LNA gain			14		µs
	Settling time for change in active termination setting			1		µs

(1) Noise correlation factor is defined as Nc/(Nu+Nc), where Nc is the correlated noise power in single channel; and Nu is the uncorrelated noise power in single channel. Its measurement follows the below equation, in which the SNR of single channel signal and the SNR of summed eight channel signal are measured.

$$\frac{N_C}{N_u + N_C} = \frac{10^{-\frac{8CH\_SNR}{10}}}{10^{-\frac{1CH\_SNR}{10}}} \times \frac{1}{56} - \frac{1}{7}$$

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5V, AVDD = 3.3V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN}= 5MHz, LNA = 18dB, PGA = 24dB, LPF Filter = 15MHz, low noise mode, V_{OUT}= –1dBFS (1.8V_{PP}), single-ended VCNTL mode, VCNTLM = GND, 2 kΩ load (ADC Rin), internal 500Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V=5V, AVDD=3.3V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
AC ACCURACY						
	LPF Bandwidth tolerance			±5		%
	CH-CH group delay variation	2MHz to 15MHz		2		ns
	CH-CH Phase variation	15MHz signal		11		Degree
	Gain matching	0V < V_{CNTL}< 0.1V (Dev-to-Dev)		±0.5		dB
		0.1V< V_{CNTL} < 1.1V(Dev-to-Dev)	–1.05	±0.5	1.05	
		0.1V< V_{CNTL} < 1.1V(Dev-to-Dev) Temp = -40°C and 85°C	-1.25	±0.5	1.25	
		1.1V< V_{CNTL}< 1.5V(Dev-to-Dev)		±0.5		
	Gain matching	Channel-to-Channel		±0.25		dB
	Output offset	V_{CNTL}= 0, PGA = 30dB, LNA = 24dB	-6		6	mV
AC PERFORMANCE						
HD2	Second-Harmonic Distortion	F_{IN} = 2MHz; V_{OUT} = -1dBFS		–60		dBc
		F_{IN} = 5MHz; V_{OUT} = -1dBFS		–60		
		F_{IN} = 5MHz; V_{IN}= 500mV_{PP}, V_{OUT} = –1dBFS, LNA = 18dB		–55		
		F_{IN} = 5MHz; Vin = 250mV_{PP}, V_{OUT} =–1dBFS, LNA = 24dB		–55		
HD3	Third-Harmonic Distortion	F_{IN} = 2MHz; V_{OUT} = –1dBFS		–53		dBc
		F_{IN} = 5MHz; V_{OUT} = –1dBFS		–55		
		F_{IN} = 5MHz; VIN = 500mV_{PP} , V_{OUT} = –1dBFS, LNA = 18dB		–55		
		F_{IN} = 5MHz; VIN = 250mV_{PP} , V_{OUT} = –1dBFS, LNA = 24dB		–55		
THD	Total Harmonic Distortion	F_{IN} = 2MHz; V_{OUT}= –1dBFS		–52.5		dBc
		F_{IN} = 5MHz; V_{OUT}= –1dBFS		–55		
IMD3	Intermodulation distortion	f1 = 5MHz at –1dBFS, f2 = 5.01MHz at –27dBFS		–60		dBc
XTALK	Cross-talk	F_{IN} = 5MHz; V_{OUT}= –1dBFS		–65		dBc
	Phase Noise	1kHz off 5MHz (V_{CNTL}=0V)		–132		dBc/Hz
LNA						
	Input Referred Voltage Noise	R_S = 0Ω, f = 2MHz, R_{IN} = High Z, Gain = 24/18/12dB		0.63/0.70/0.9		nV/rtHz
	High-Pass Filter	-3dB Cut-off Frequency		50/100/150/200		KHz
	LNA linear output			4		Vpp
VCAT+ PGA						
	VCAT Input Noise	0dB/-40dB Attenuation		2/10.5		nV/rtHz
	PGA Input Noise	24dB/30dB		1.75		nV/rtHz
	-3dB HPF cut-off Frequency	High-Pass Filter is enabled		80		KHz
	Output Common Mode Voltage			0.9		V
$VOUT_{MAX}$	Maximum Linear Output Voltage	Defined as 0 dBFS		2		V_{PP}
	Minimum Load Impedance			1		KΩ

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5V, AVDD = 3.3V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN}= 5MHz, LNA = 18dB, PGA = 24dB, LPF Filter = 15MHz, low noise mode, V_{OUT}= –1dBFS (1.8V_{PP}), single-ended VCNTL mode, VCNTLM = GND, 2 kΩ load (ADC Rin), internal 500Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V=5V, AVDD=3.3V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
CW DOPPLER						
en (RTI)	Input voltage noise (CW)	1 channel mixer, LNA = 24dB, 500Ω feedback resistor		0.8		nV/rtHz
		8 channel mixer, LNA = 24dB, 62.5Ω feedback resistor		0.33		
en (RTO)	Output voltage noise (CW)	1 channel mixer, LNA = 24dB, 500Ω feedback resistor		12		nV/rtHz
		8 channel mixer, LNA = 24dB, 62.5Ω feedback resistor		5		
en (RTI)	Input voltage noise (CW)	1 channel mixer, LNA = 18dB, 500Ω feedback resistor		1.1		nV/rtHz
		8 channel mixer, LNA = 18dB, 62.5Ω feedback resistor		0.5		
en (RTO)	Output voltage noise (CW)	1 channel mixer, LNA = 18dB, 500Ω feedback resistor		8.1		nV/rtHz
		8 channel mixer, LNA = 18dB, 62.5Ω feedback resistor		4.0		
NF	Noise figure	R_S = 100Ω, R_{IN} = High Z, F_{IN} = 2MHz (LNA, I/Q mixer and summing amplifier/filter)		1.8		dB
f_{CW}	CW Operation Range(2)	CW signal carrier frequency, 16X mode / 32X mode		8/4		MHz
	CW Clock frequency	1X CLK (16X mode)		8		MHz
		16X CLK(16X mode)		128		
		4X CLK(4X mode)		32		
		32X CLK(32X mode)		128		
	AC coupled LVDS clock amplitude	CLKM_16X-CLKP_16X; CLKM_1X-CLKP_1X		0.7		V_{PP}
	AC coupled LVPECL clock amplitude			1.6		
	CLK duty cycle	1X and 16X CLKs	35		65	%
	Common-mode voltage	Internal provided		2.5		V
V_{CMOS}	CMOS Input clock amplitude		4		5	V
	CW Mixer conversion loss			4		dB
	CW Mixer phase noise	1kHz off 2MHz carrier		-156		dBc/Hz
DR	Input dynamic range	F_{IN} = 2MHz, LNA=24/18/12dB		160/164/165		dBFS/Hz
IMD3	Intermodulation distortion	f1 = 5 MHz, f2 = 5.01 MHz, both tones at -8.5dBm amplitude, 8 channels summed up in-phase, CW feedback resistor = 87 Ω		–50		dBc
		f1 = 5 MHz, F2= 5.01 MHz, both tones at –8.5dBm amplitude, Single channel case, CW feed back resistor = 500Ω		–60		dBc
	I/Q Channel gain matching	16X mode		±0.04		dB
	I/Q Channel phase matching	16X mode		±0.1		Degree
	I/Q Channel gain matching	4X mode		±0.04		dB
	I/Q Channel phase matching	4X mode		±0.1		Degree
	Image rejection ratio	fin = 2.01MHz, 300mV input amplitude, CW clock frequency = 2.00MHz		–50		dBc

(2) The maximum clock frequency for the 16X and 32X CLK is 128MHz. Hence, the CW operation range is limited to 8MHz in the 16X CW mode. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance, please see CW Clock Selection.

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5V, AVDD = 3.3V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN}= 5MHz, LNA = 18dB, PGA = 24dB, LPF Filter = 15MHz, low noise mode, V_{OUT}= –1dBFS (1.8V_{PP}), single-ended VCNTL mode, VCNTLM = GND, 2 kΩ load (ADC Rin), internal 500Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V=5V, AVDD=3.3V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
CW SUMMING AMPLIFIER						
V_{CMO}	Common-mode voltage	Summing amplifier inputs/outputs		1.5		V
	Summing amplifier output			4		V_{PP}
	Input referred voltage noise(3)	100Hz		2		nV/rtHz
		1kHz		1.2		nV/rtHz
		2KHz-100MHz		1		nV/rtHz
	Input referred current noise(3)	100Hz		7		pA/rtHz
		1kHz		3		pA/rtHz
		10KHz-100MHz		2.5		pA/rtHz
	Unit gain bandwidth			200		MHz
	Max output current	Linear operation range		20		mA_{PP}
POWER DISSIPATION						
	AVDD Voltage		3.15	3.3	3.6	V
	AVDD_5V Voltage		4.75	5	5.5	V
	AVDD (3.3V) Current	TGC low noise mode, no signal		203	235	mA
		TGC medium power mode, no signal		126		
		TGC low power mode, no signal		99		
		CW-mode, no signal		147	172	
		TGC low noise mode, 500mV_{PP} Input,1% duty cycle		210		
		TGC medium power mode, 500mV_{PP} Input, 1% duty cycle		133		
		TGC low power, 500mV_{PP} Input, 1% duty cycle		105		
		CW-mode, 500mV_{PP} Input		375		
	AVDD_5V Current	TGC mode no signal		25.5	35	mA
		CW Mode no signal, 16X clock = 32MHz		32		
		TGC mode, 500mV_{PP} Input,1% duty cycle		16.5		
		CW-mode, 500mV_{PP} Input		42.5		
	VCA Power dissipation	TGC low noise mode, no signal		99	121	mW/CH
		TGC medium power mode, no signal		68		
		TGC low power mode, no signal		55.5		
		TGC low noise mode, 500mV_{PP} input,1% duty cycle		102.5		
		TGC medium power mode, 500mV_{PP} Input, 1% duty cycle		71		
		TGC low power mode, 500mV_{PP} input,1% duty cycle		59.5		
	CW Power dissipation	No signal, CW Mode no signal, 16X clock = 32MHz		80		mW/CH
		500mV_{PP} input, 16X clock = 32MHz		173		
	Power dissipation in power down mode	PDN_FAST = High		12.5		mW/CH
		Complete power-down PDN_Global=High		0.6	2	
	Power-down response time	Time taken to enter power down		1		µs
	Power-up response time	VCA power down		2µs+1% of PDN time		µs
		Complete power down		2.5		ms
	Power supply modulation ratio, AVDD and AVDD_5V (TGC Mode)	fin = 5MHz, at 50mVpp noise at 1KHz on supply(4)		–65		dBc
		fin = 5MHz, at 50mV_{PP} noise at 50KHz on supply(4)		–65		dBc
	Power supply rejection ratio (TGC Mode)	f = 10kHz, V_{CNTL} = 0V (high gain), AVDD		–40		dBc
		f = 10kHz, V_{CNTL} = 0V (high gain), AVDD_5V		–55		dBc
		f = 10kHz, V_{CNTL} = 1V (low gain), AVDD		–50		dBc
	Power supply modulation ratio (CW Mode with 8 mixers active)	fin = 5MHz, 1-20 KHz 100mVpp noise on the AVDD		-57		dBc
		fin = 5MHz, 1-20 KHz 100mVpp noise on the AVDD_5V		-59		dBc
	Power supply rejection ratio (CW Mode with 8 mixers active)	fin = 5MHz, 5.001-5.02 MHz 100mVpp noise on the AVDD		-75		dBc
		fin = 5MHz, 5.001-5.02 MHz 100mVpp noise on the AVDD_5V		-40		dBc

(3) By simulation.
(4) PSMR specification is with respect to RF signal amplitude.

DIGITAL CHARACTERISTICS

(Note: This timing data was collected under 14 bit operation)
Typical values are at 25°C, AVDD = 3.3V, AVDD_5 = 5V unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = -40°C to T_{MAX} = 85°C.

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic high input voltage		2		3.3	V
V_{IL}	Logic low input voltage		0		0.3	V
	Logic high input current			200		µA
	Logic low input current			200		µA
	Input capacitance			5		pF
V_{OH}	Logic high output voltage	SDOUT pin		AVDD		V
V_{OL}	Logic low output voltage	SDOUT pin		0		V

TYPICAL CHARACTERISTICS

AVDD_5V = 5V, AVDD = 3.3V, ac-coupled with 0.1µF caps at INP and 15nF caps at INM, No active termination, VCNTL = 0V, F_{IN} = 5MHz, LNA = 18dB, PGA = 24dB, LPF Filter = 15MHz, low noise mode, single-ended VCNTL mode, VCNTLM = GND, V_{OUT} = -1dBFS ($1.8V_{PP}$), 2 kΩ load (ADC Rin), 500Ω CW feedback resistor, CMOS 16X clock, at ambient temperature T_A = 25C, unless otherwise noted.

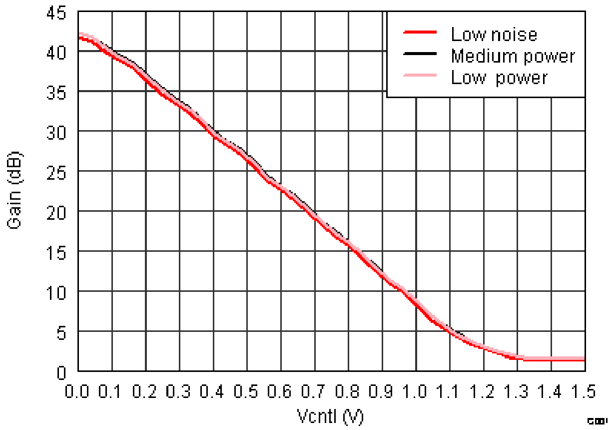


Figure 2. Gain vs. VCNTL, LNA = 18dB and PGA = 24dB

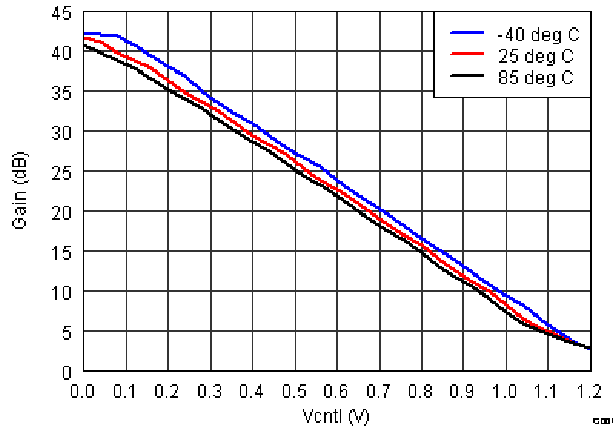


Figure 3. Gain vs. Temperature, LNA = 18dB and PGA = 24dB

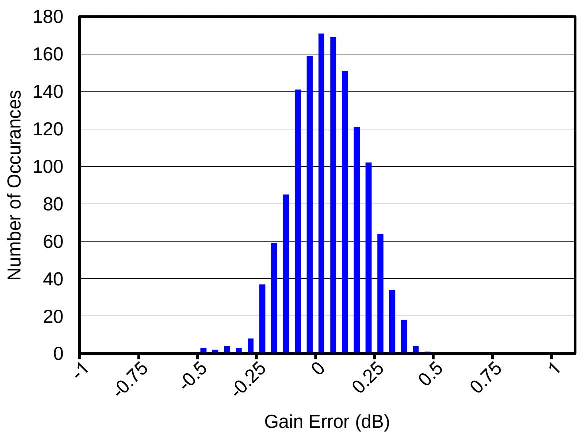


Figure 4. Gain Matching Histogram, VCNTL = 0.3V (1336channels)

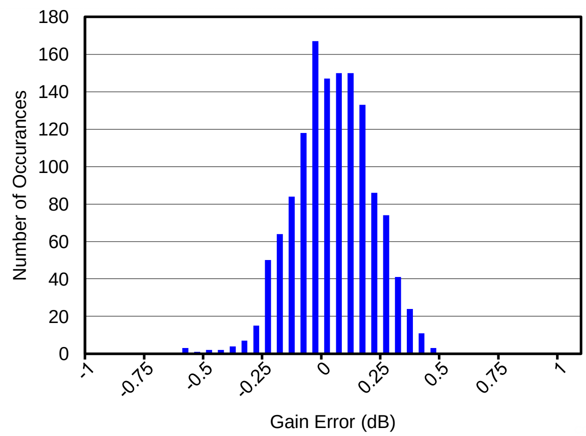


Figure 5. Gain Matching Histogram, VCNTL = 0.6V (1336 channels)

TYPICAL CHARACTERISTICS (continued)

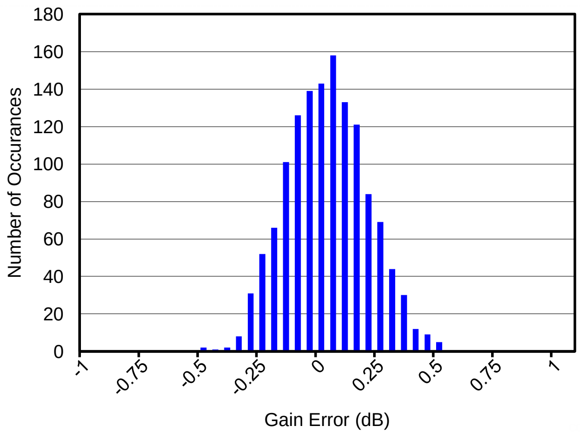


Figure 6. Gain Matching Histogram, VCNTL = 0.9V (1336 channels)

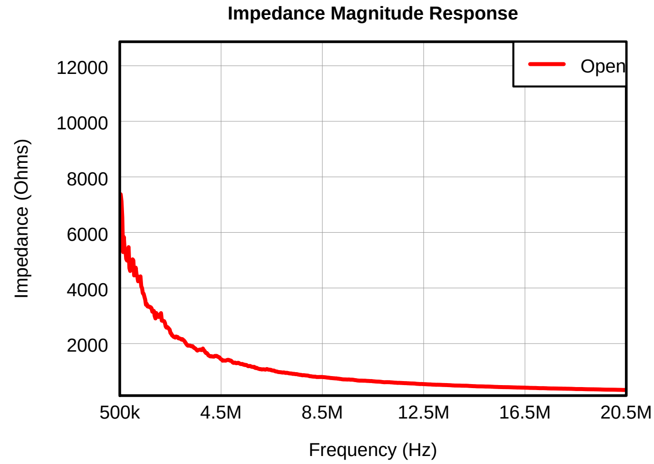


Figure 7. Input Impedance without Active Termination (Magnitude)

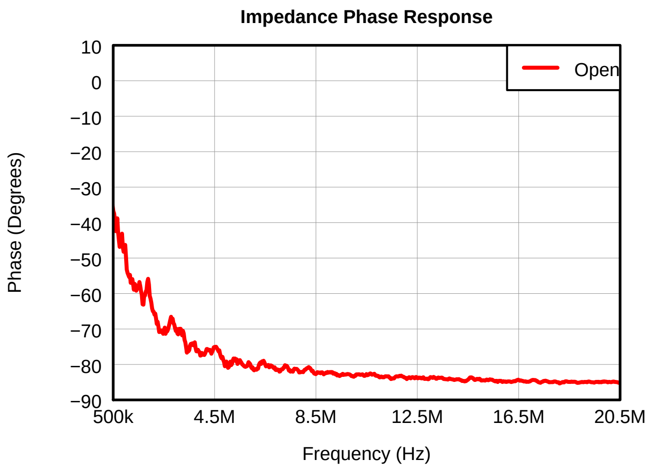


Figure 8. Input Impedance without Active Termination (Phase)

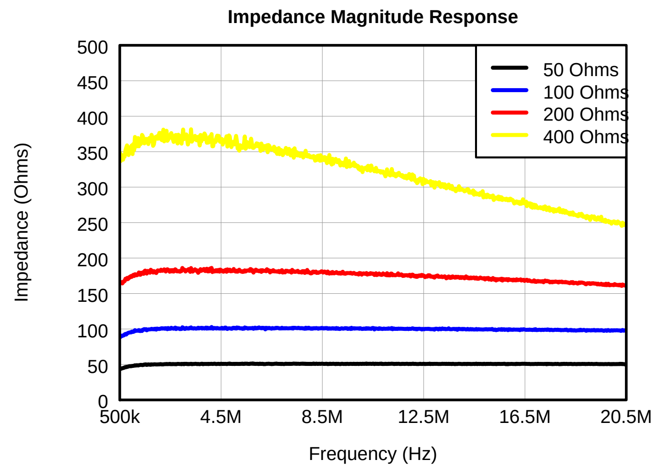


Figure 9. Input Impedance with Active Termination (Magnitude)

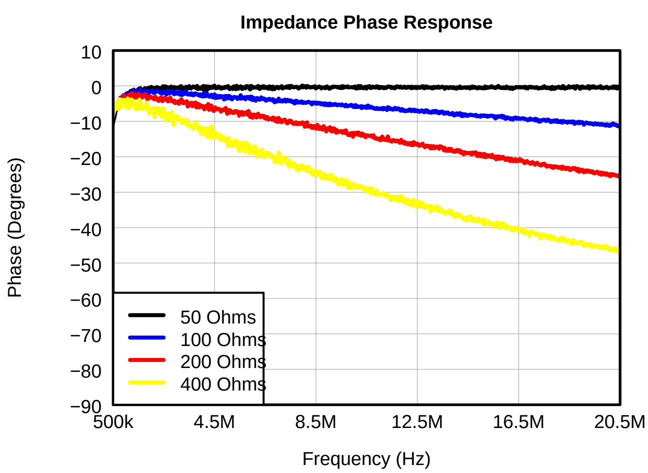


Figure 10. Input Impedance with Active Termination (Phase)

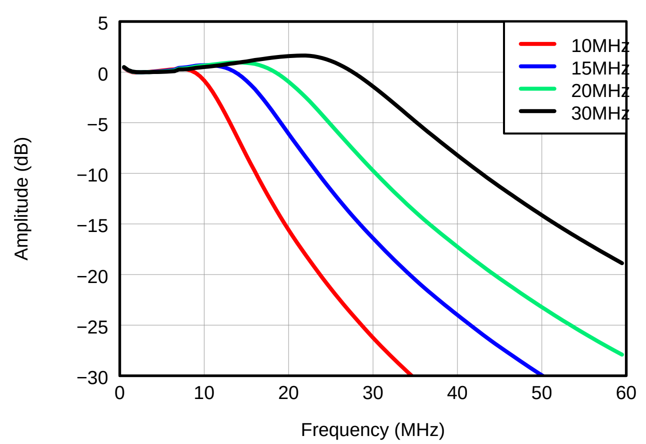


Figure 11. Low-Pass Filter Response

TYPICAL CHARACTERISTICS (continued)

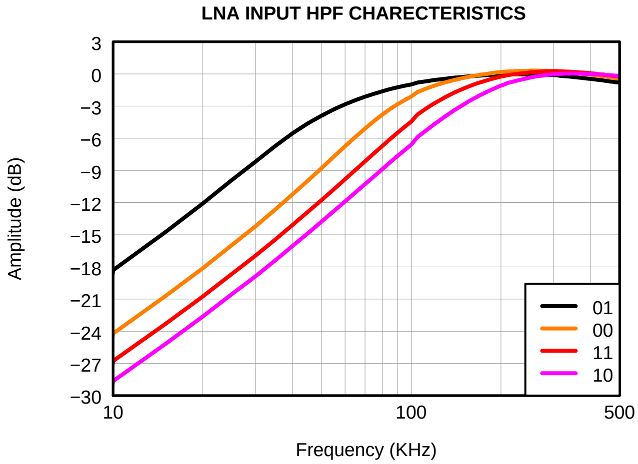


Figure 12. LNA High-Pass Filter Response vs. Reg59[3:2]

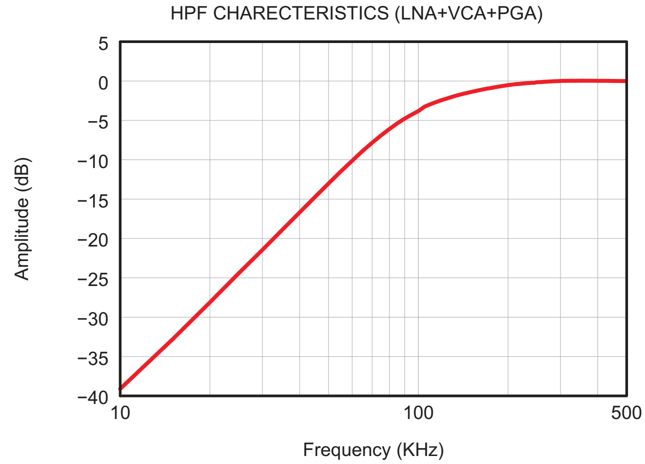


Figure 13. Full Channel High-Pass Filter Response at Default Register Setting

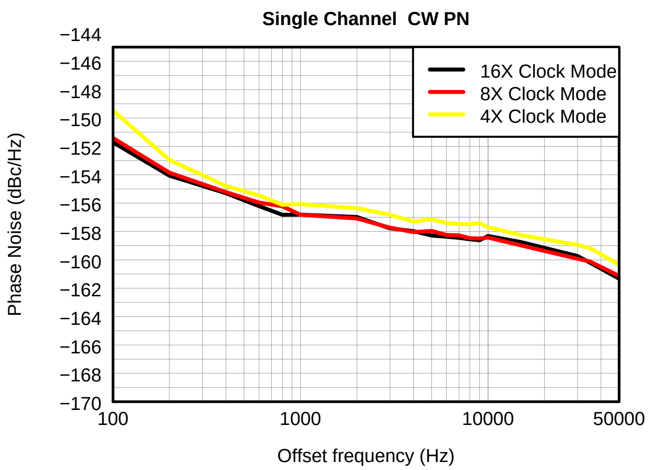


Figure 14. 1-CH CW Phase Noise, Fin = 2MHz

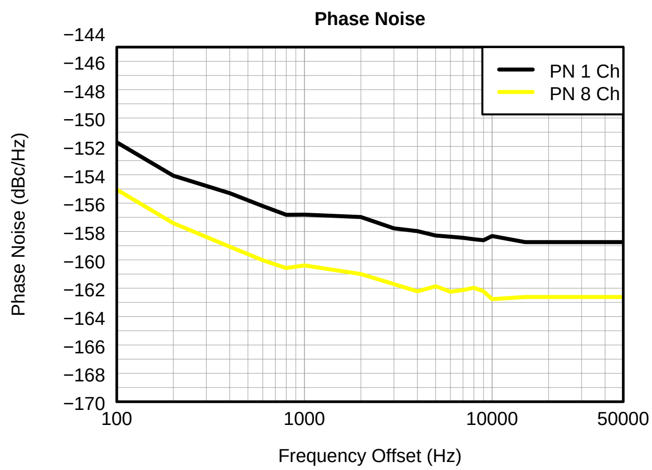


Figure 15. CW Phase Noise, Fin = 2MHz, 1-CH vs. 8-CHs

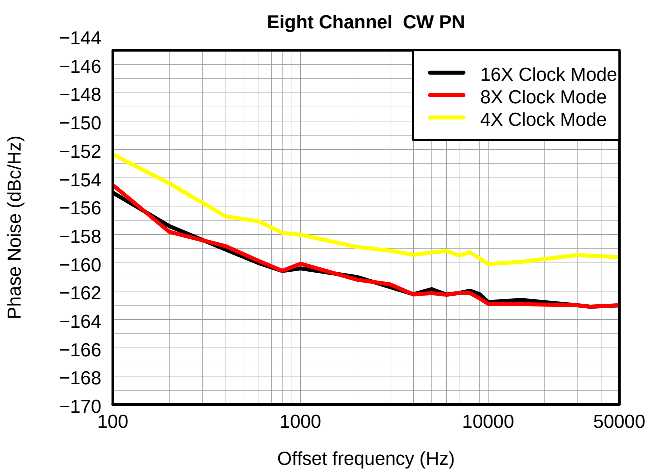


Figure 16. 8-CHs CW Phase Noise vs. Clock Modes, Fin = 2MHz

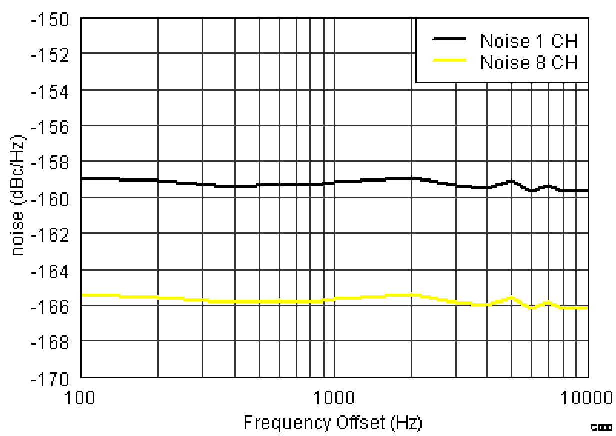


Figure 17. CW Thermal Noise 1-CH vs 8-CHs

TYPICAL CHARACTERISTICS (continued)

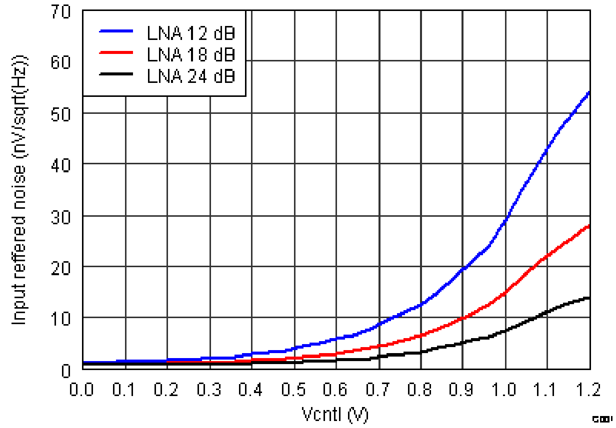


Figure 18. IRN, PGA = 24dB and Low Noise Mode

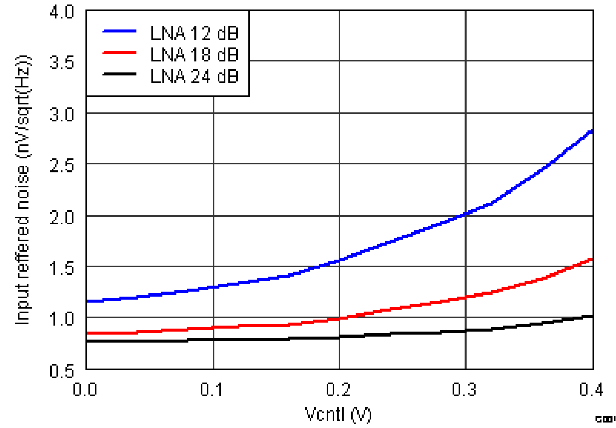


Figure 19. IRN, PGA = 24dB and Low Noise Mode Zoomed

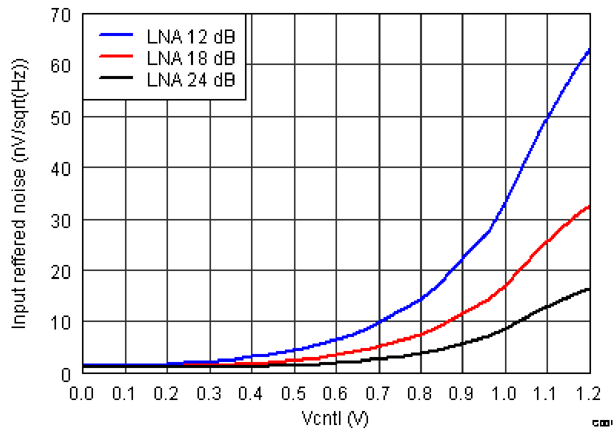


Figure 20. IRN, PGA = 24dB and Medium Power Mode

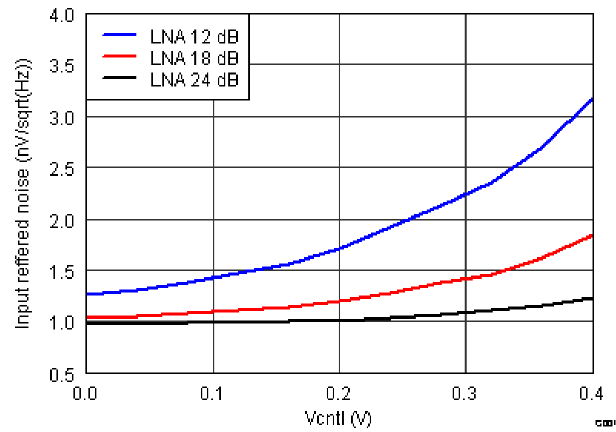


Figure 21. IRN, PGA = 24dB and Medium Power Mode Zoomed

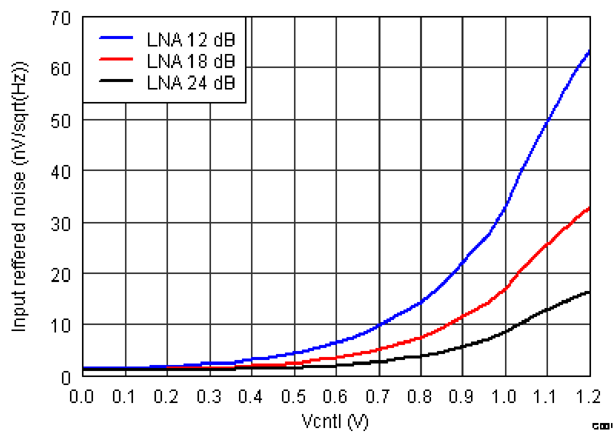


Figure 22. IRN, PGA = 24dB and Low Power Mode

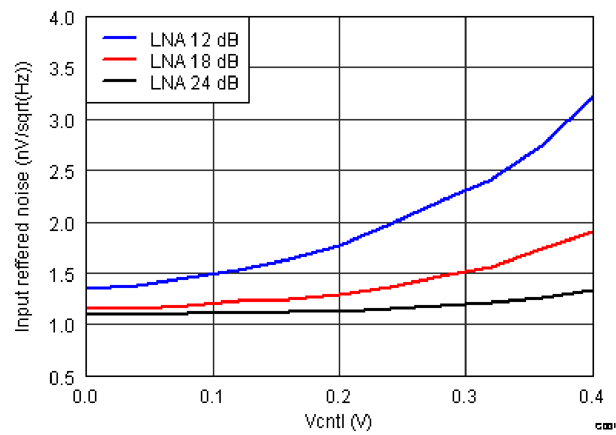


Figure 23. IRN, PGA = 24dB and Low Power Mode Zoomed

TYPICAL CHARACTERISTICS (continued)

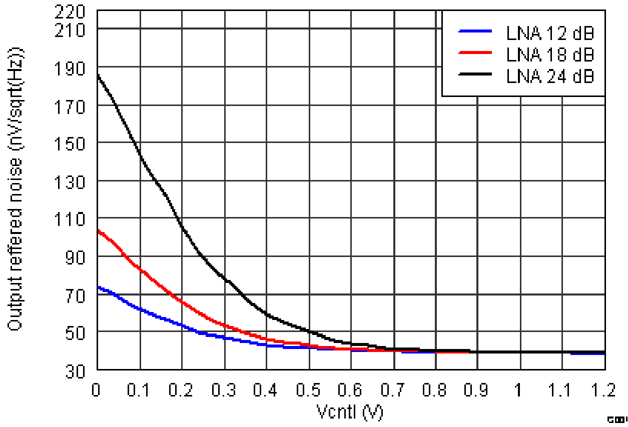


Figure 24. ORN, PGA = 24dB and Low Noise Mode

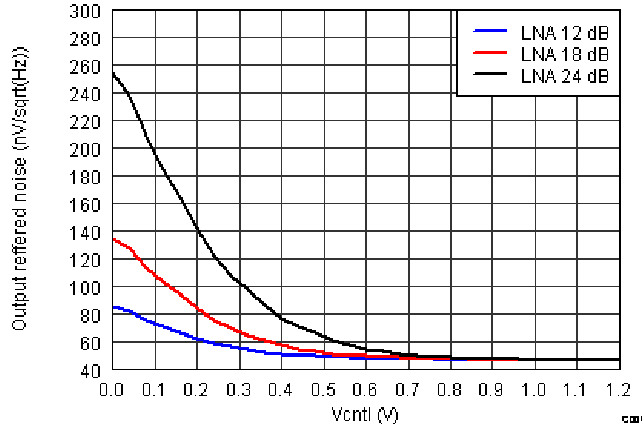


Figure 25. ORN PGA=24dB and Med Power Mode

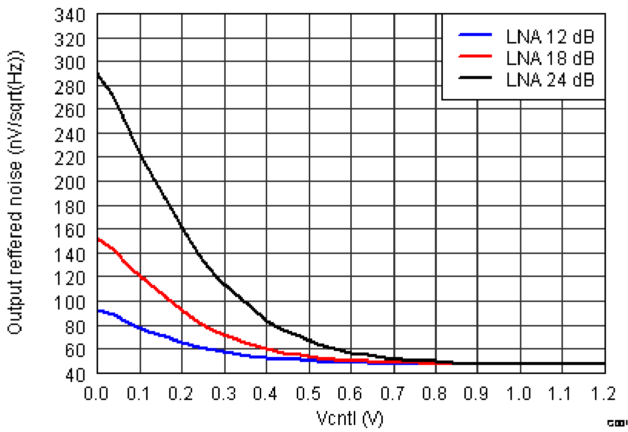


Figure 26. ORN, PGA = 24dB and Low Power Mode

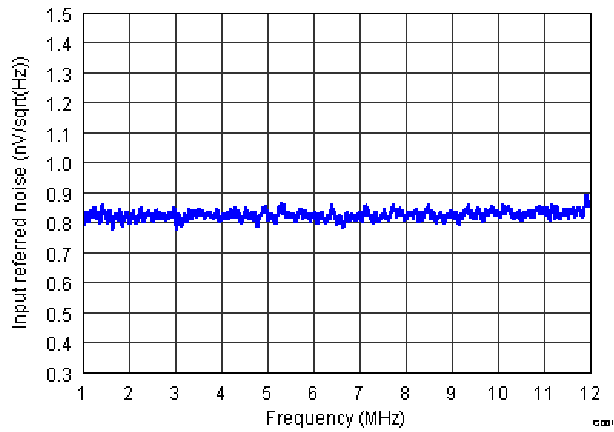


Figure 27. IRN vs Frequency, PGA = 24dB and Low Noise Mode

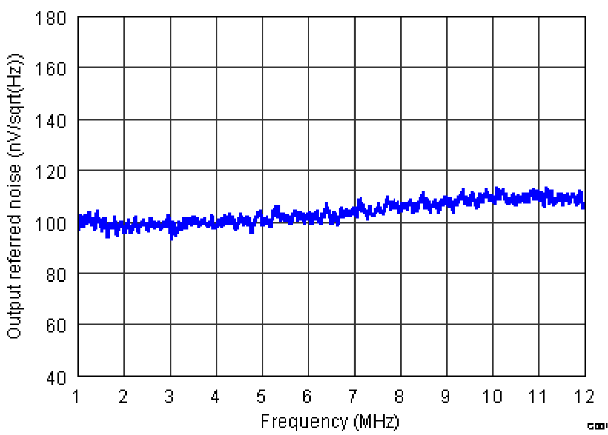


Figure 28. ORN vs Frequency, PGA = 24dB and Low Noise Mode

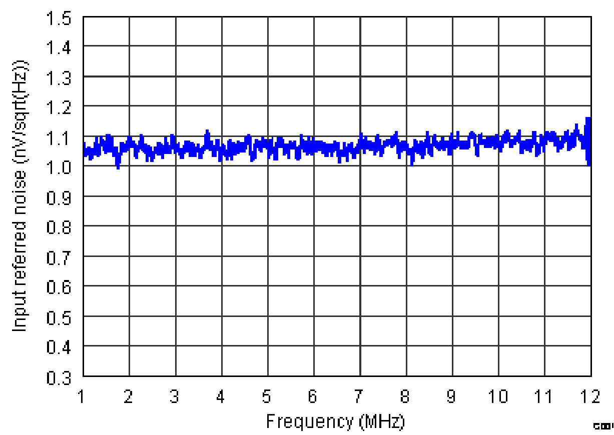


Figure 29. IRN vs Frequency, PGA = 24dB and Low NF Mode

TYPICAL CHARACTERISTICS (continued)

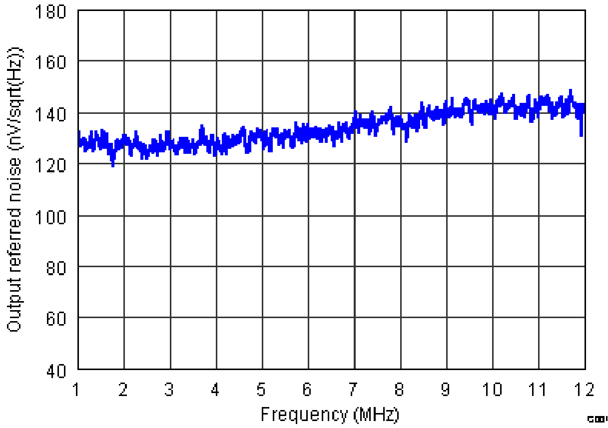


Figure 30. ORN vs Frequency, PGA = 24dB and Low NF Mode

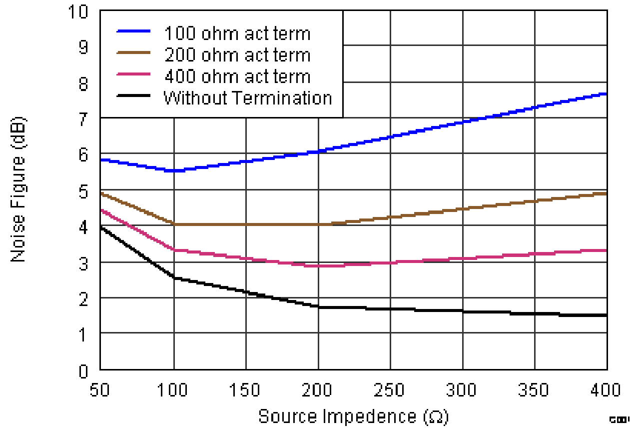


Figure 31. TGC Noise Figure, LNA = 12dB and Low Noise Mode

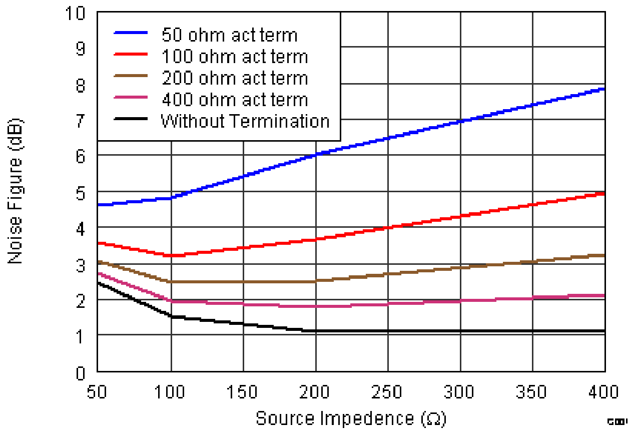


Figure 32. TGC Noise Figure, LNA = 18dB and Low Noise Mode

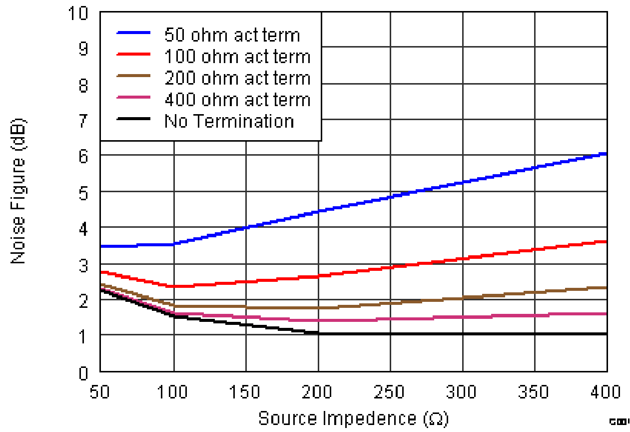


Figure 33. TGC Noise Figure, LNA = 24dB and Low Noise Mode

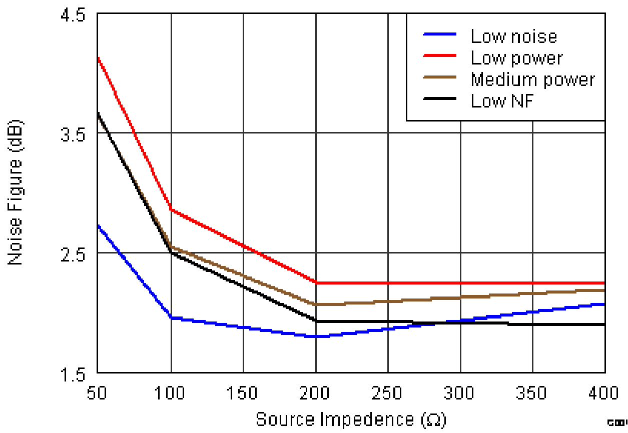


Figure 34. Noise Figure vs. Power Modes with 400Ω Active Termination

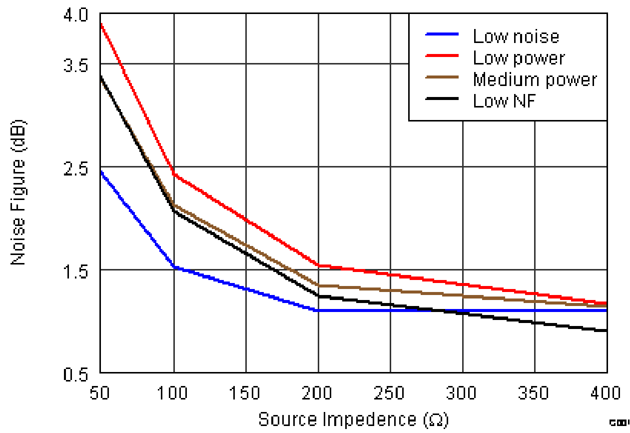


Figure 35. Noise Figure vs. Power Modes without Termination

TYPICAL CHARACTERISTICS (continued)

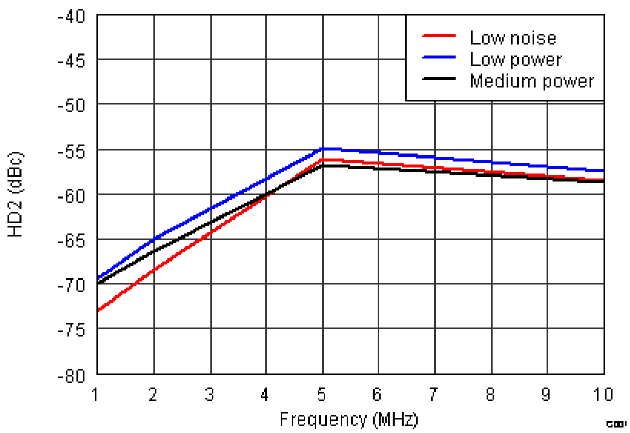


Figure 36. HD2 vs. Frequency, Vin = 500mVpp and Vout = -1dBFS

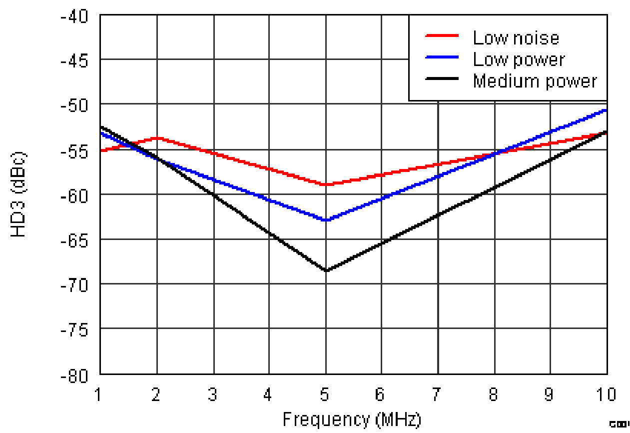


Figure 37. HD3 vs. Frequency, Vin = 500mVpp and Vout = -1dBFS

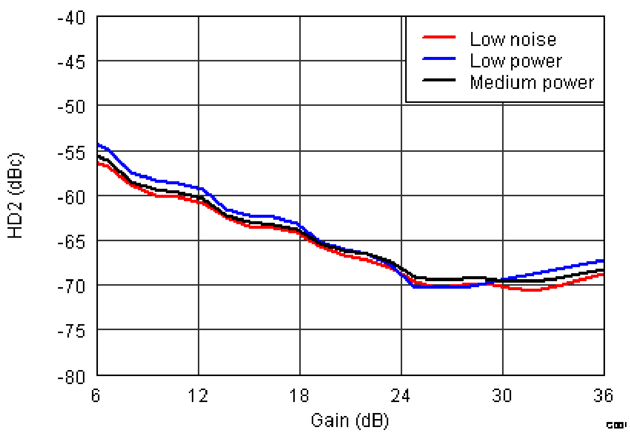


Figure 38. HD2 vs. Gain, LNA = 12dB and PGA = 24dB and Vout = -1dBFS

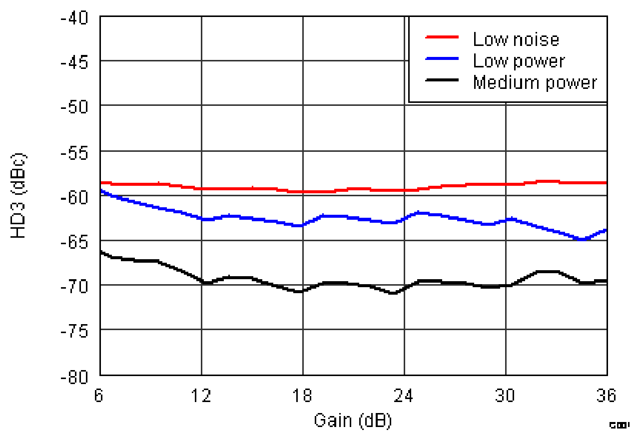


Figure 39. HD3 vs. Gain, LNA = 12dB and PGA = 24dB and Vout = -1dBFS

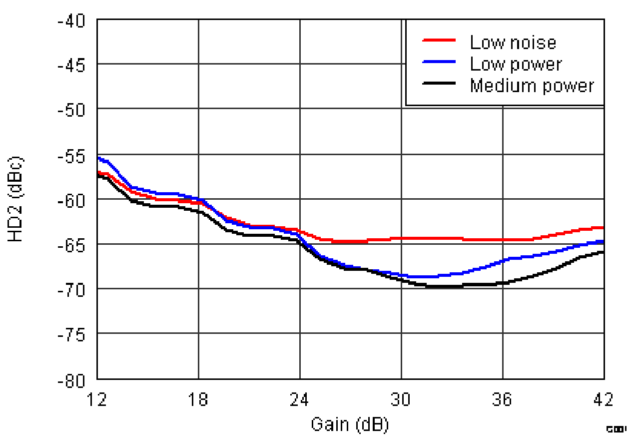


Figure 40. HD2 vs. Gain, LNA = 18dB and PGA = 24dB and Vout = -1dBFS

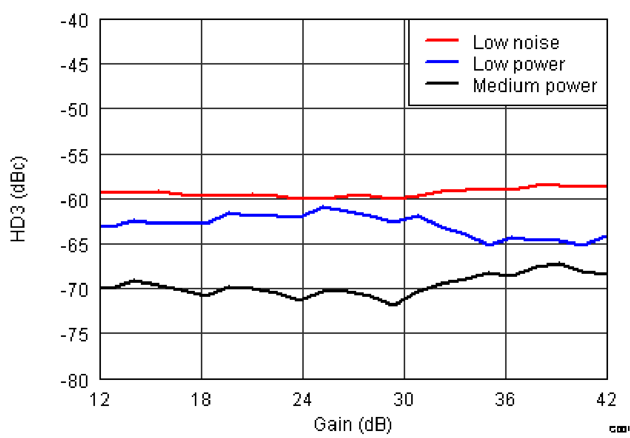


Figure 41. HD3 vs. Gain, LNA = 18dB and PGA = 24dB and Vout = -1dBFS

TYPICAL CHARACTERISTICS (continued)

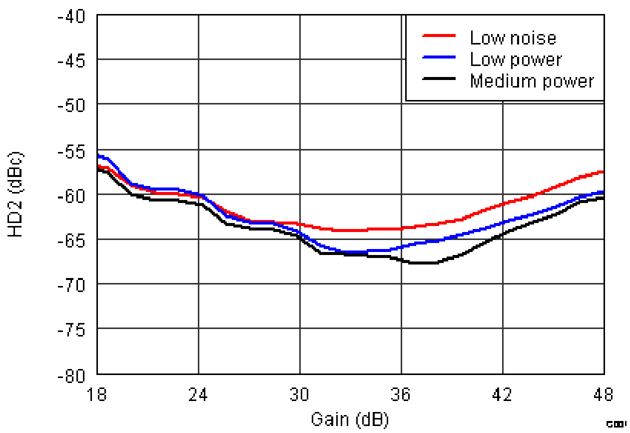


Figure 42. HD2 vs. Gain, LNA = 24dB and PGA = 24dB and Vout = -1dBFS

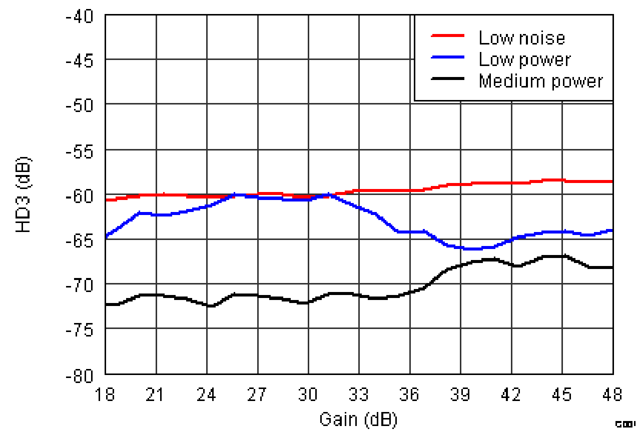


Figure 43. HD3 vs. Gain, LNA = 24dB and PGA = 24dB and Vout = -1dBFS

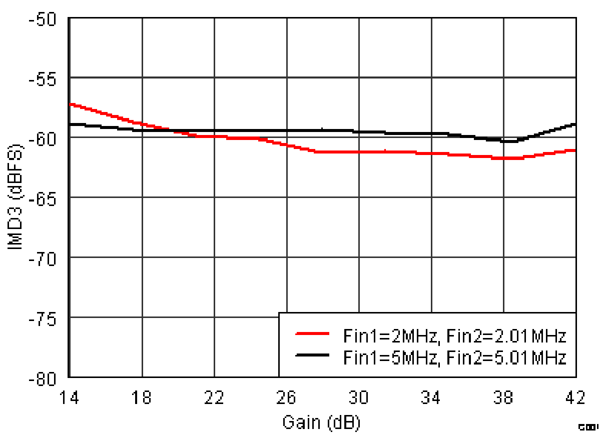


Figure 44. IMD3, Fout1 = -7dBFS and Fout2 = -7 dBFS

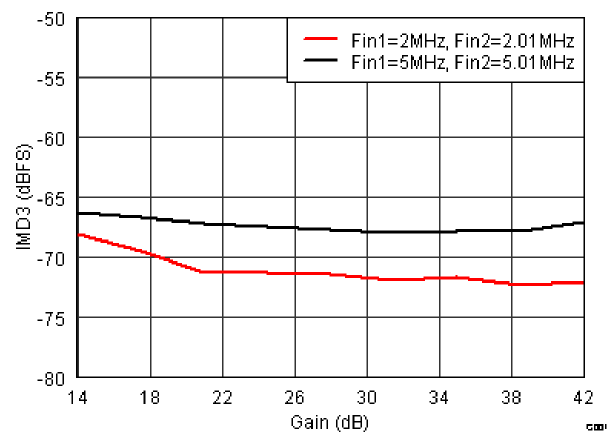


Figure 45. IMD3, Fout1 = -21dBFS and Fout2 = -21dBFS

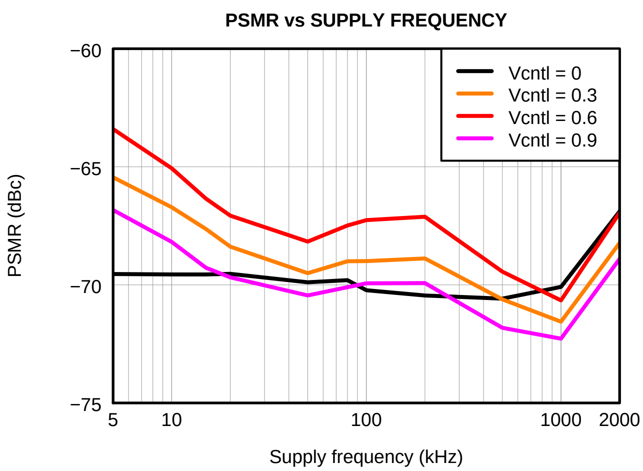


Figure 46. AVDD Power Supply Modulation Ratio, 100mVpp Supply Noise with Different Frequencies (TGC Mode)

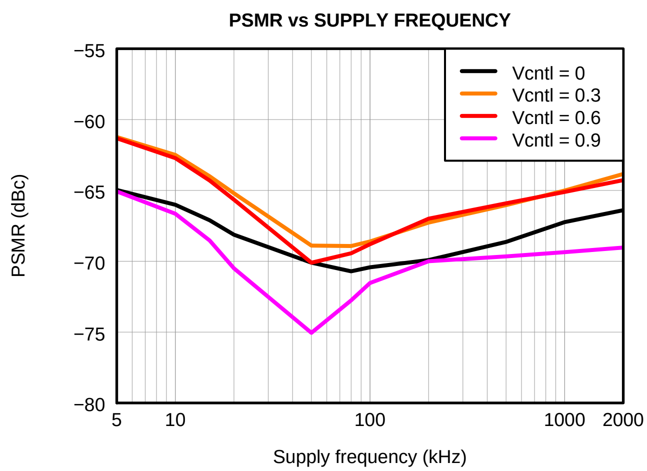


Figure 47. AVDD_5V Power Supply Modulation Ratio, 100mVpp Supply Noise with Different Frequencies (TGC Mode)

TYPICAL CHARACTERISTICS (continued)

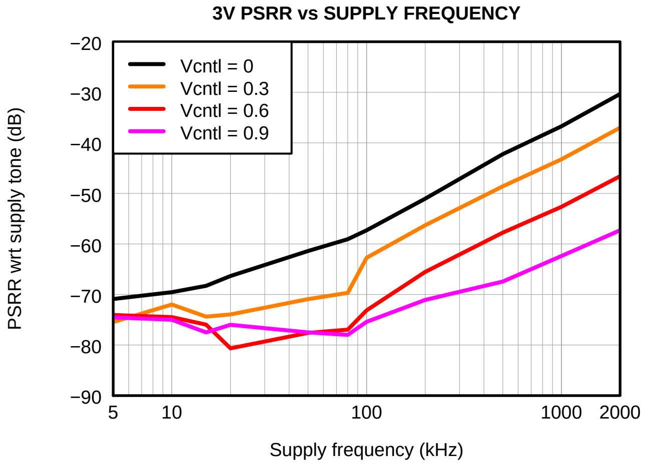


Figure 48. AVDD Power Supply Rejection Ratio, 100mVpp Supply Noise with Different Frequencies (TGC Mode)

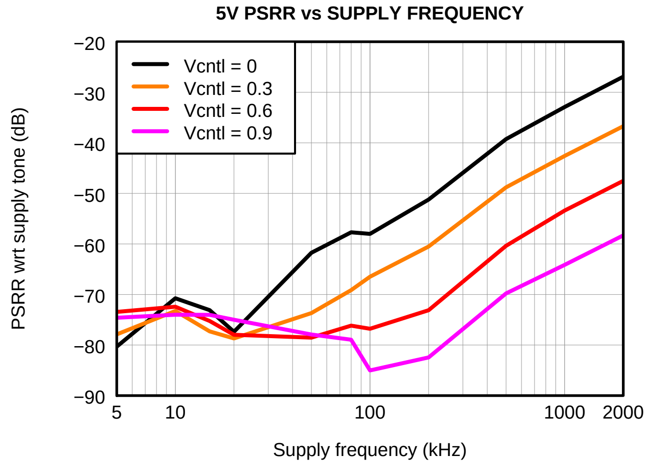


Figure 49. AVDD_5V Power Supply Rejection Ratio, 100mVpp Supply Noise with Different Frequencies (TGC Mode)

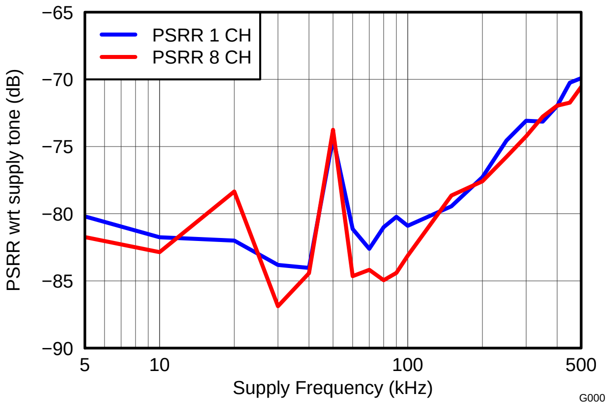


Figure 50. AVDD Power Supply Rejection Ratio, V_{noise}=100 mVpp, $Freq_{noise}$=5-500 KHz (CW Mode)

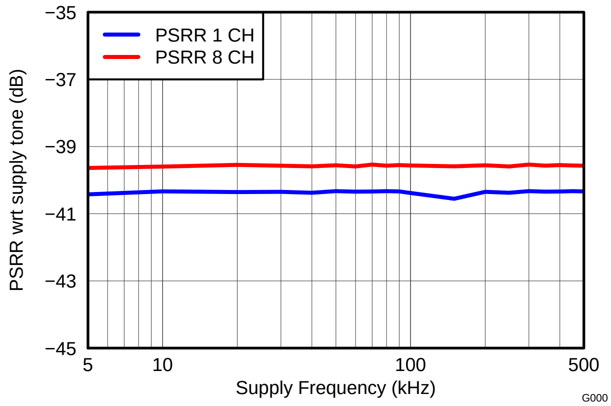


Figure 51. AVDD_5V Power Supply Rejection Ratio, V_{noise}=100 mVpp, $Freq_{noise}$=5-500 KHz (CW Mode)

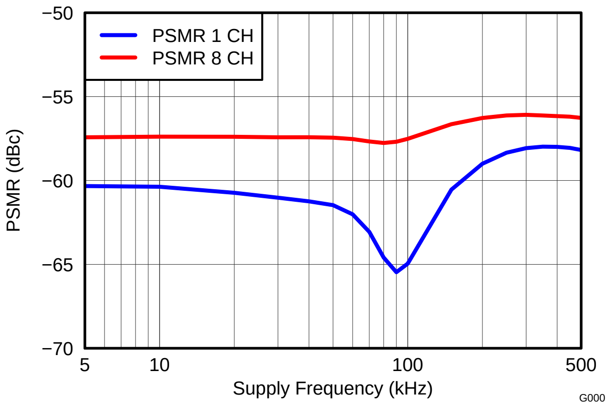


Figure 52. AVDD Power Supply Modulation Ratio, V_{noise}=100 mVpp, $Freq_{noise}$=5.005-5.5 MHz (CW Mode)

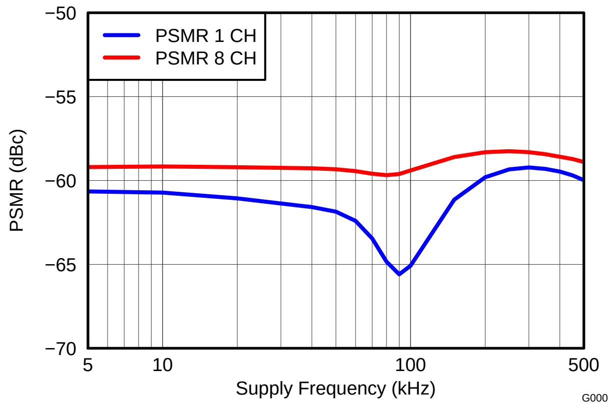


Figure 53. AVDD_5V Power Supply Modulation Ratio, V_{noise}=100 mVpp, $Freq_{noise}$=5.005-5.5 MHz (CW Mode)

TYPICAL CHARACTERISTICS (continued)

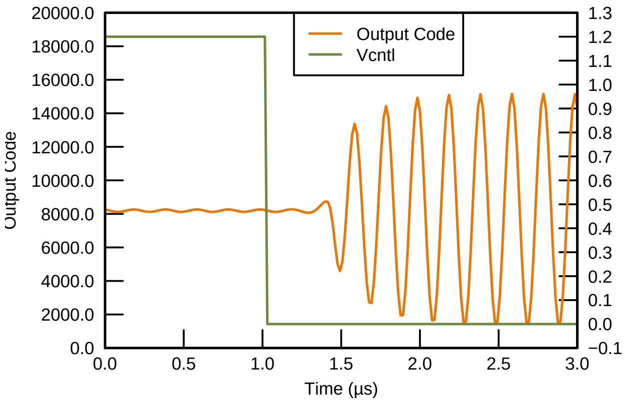


Figure 54. V_{CNTL} Response Time, LNA = 18dB and PGA = 24dB

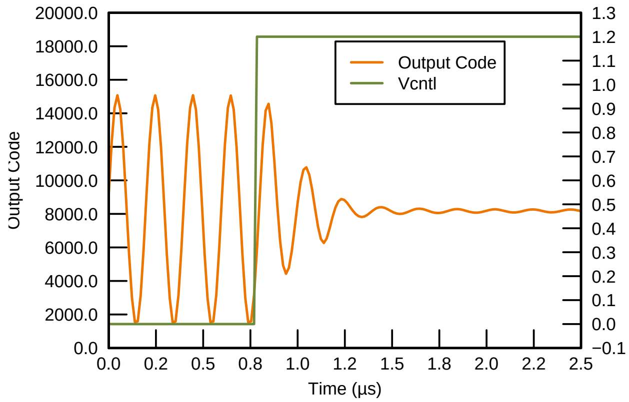


Figure 55. V_{CNTL} Response Time, LNA = 18dB and PGA = 24dB

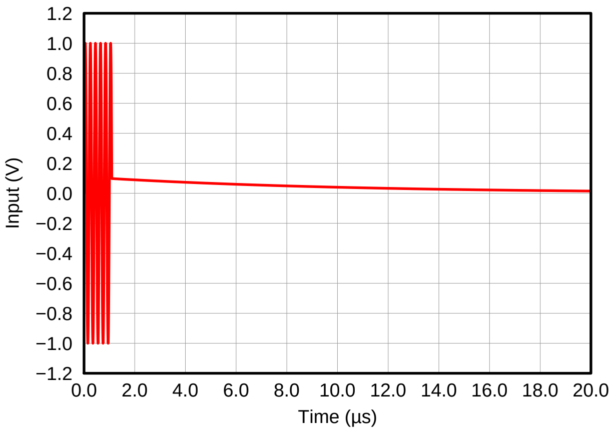


Figure 56. Pulse Inversion Asymmetrical Positive Input

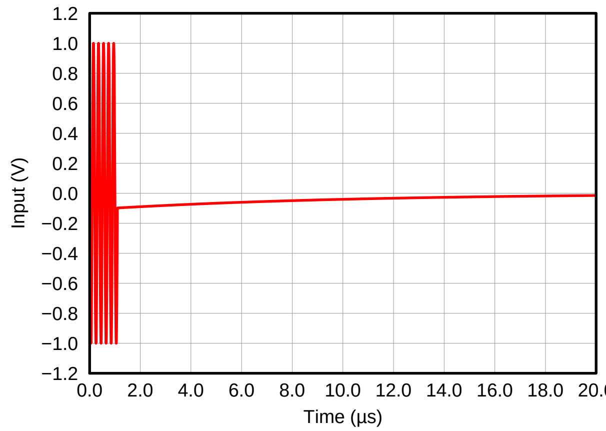


Figure 57. Pulse Inversion Asymmetrical Negative Input

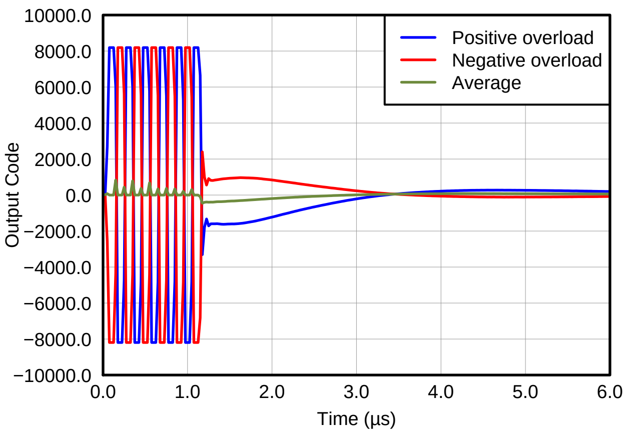


Figure 58. Pulse Inversion, Vin = 2Vpp, PRF = 1KHz, Gain = 21dB

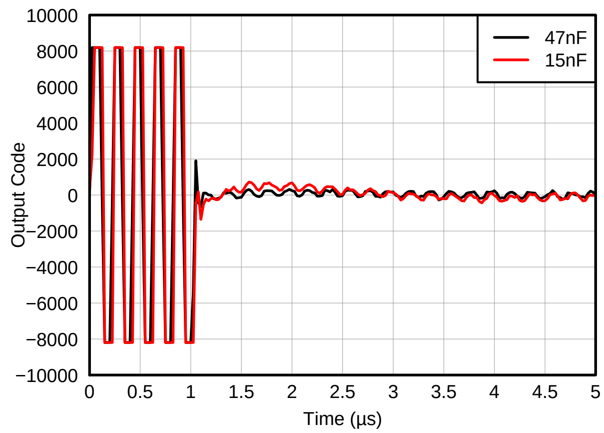


Figure 59. Overload Recovery Response vs. INM capacitor, Vin = 50 mVpp/100 µVpp, Max Gain

TYPICAL CHARACTERISTICS (continued)

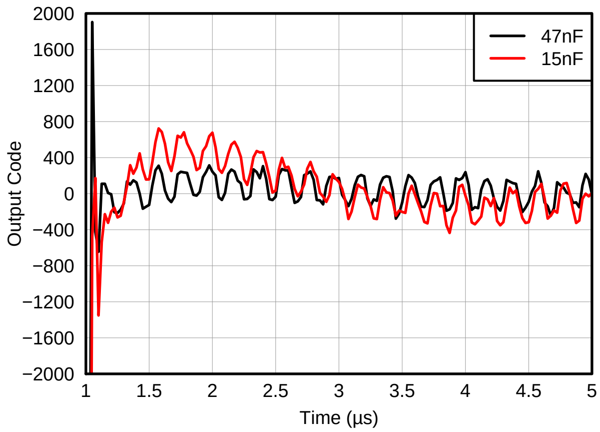


Figure 60. Overload Recovery Response vs. INM capacitor(Zoomed), Vin = 50 mVpp/100 µVpp, Max Gain

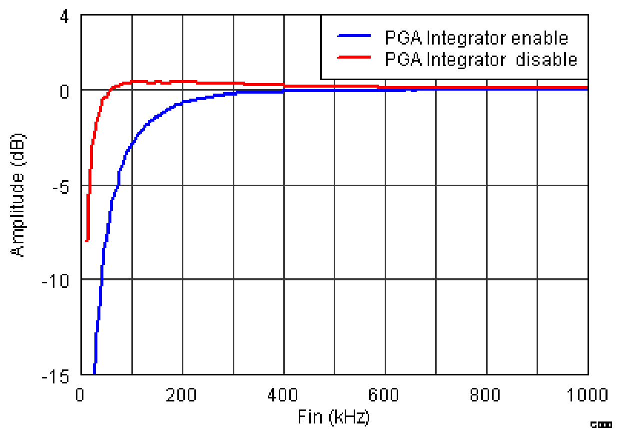


Figure 61. Signal Chain Low Frequency Response with INM Capacitor = 1 µF

Serial Peripheral Interface (SPI) Operation

Register Write Description

Programming of different modes can be done through the serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. All these pins have a pull-down resistor to GND of 20kΩ. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every rising edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiple of 24-bit words within a single active SEN pulse (there is an internal counter that counts groups of 24 clocks after the falling edge of SEN). The interface can work with the SCLK frequency from 20 MHz down to low speeds (few Hertz) and even with non-50% duty cycle SCLK. The data is divided into two main portions: a register address (8 bits) and the data itself (16 bits), to load on the addressed register. When writing to a register with unused bits, these should be set to 0. Figure 62 illustrates this process.

NOTE

RESET must be kept as '1' more than 100 ns. After resetting, >100 ns is recommended before writing SPI registers.

Typically the VCA5807 responds to new register settings immediately after 24 bits (8-bit address and 16-bit data) are written to VCA5807.

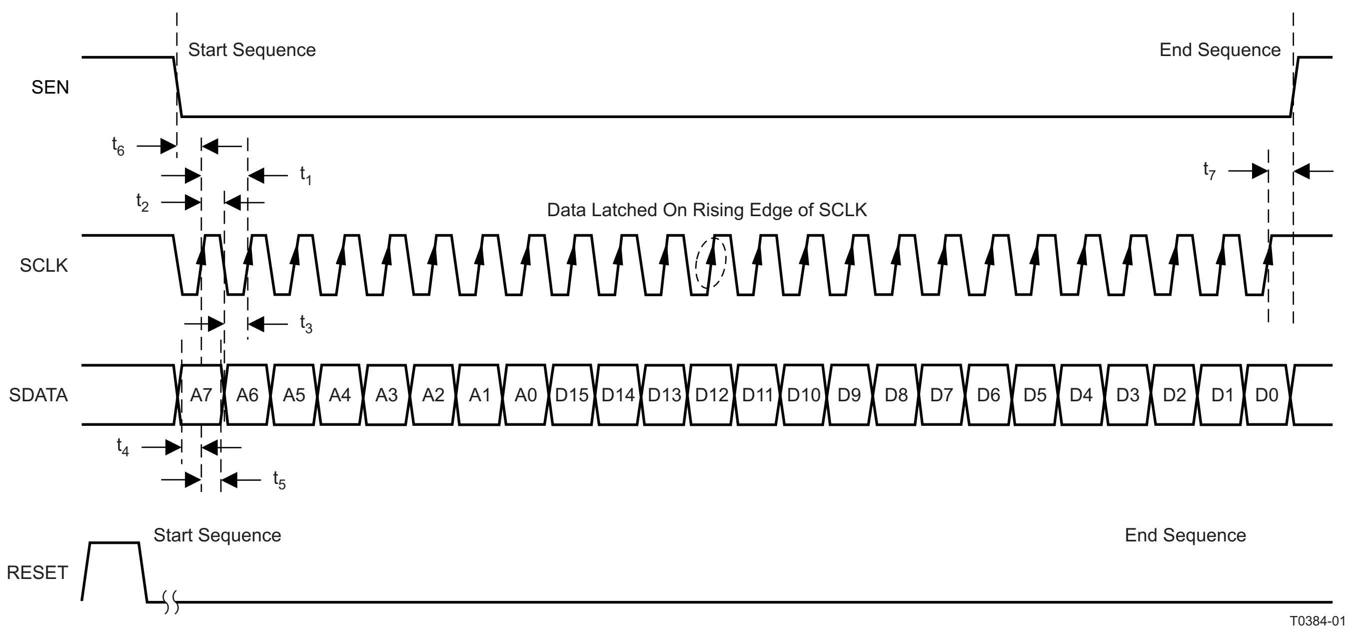


Figure 62. Serial Interface Register Write Timing

Register Readout Description

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic test to verify the serial interface communication between the external controller and the VCA. First, the <REGISTER READOUT ENABLE> bit (Reg0[1]) needs to be set to '1'. Then user should initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read. The data bits are "don’t care". The device will output the contents (D15-D0) of the selected register on the SDOUT pin. The SDOUT has a typical delay t_8 of 20 nS from the falling edge of the SCLK. For lower speed SCLK, SDOUT can be latched on the rising edge of SCLK. For higher speed SCLK, that is, the SCLK period lesser than 60nS, it would be better to latch the SDOUT at the next falling edge of SCLK. The following timing diagram shows this operation (the time specifications follow the same information provided. In the readout mode, users still can access the <REGISTER_READOUT_ENABLE> through SDATA/SCLK/SEN. To enable serial register writes, set the <REGISTER_READOUT_ENABLE> bit back to '0'.

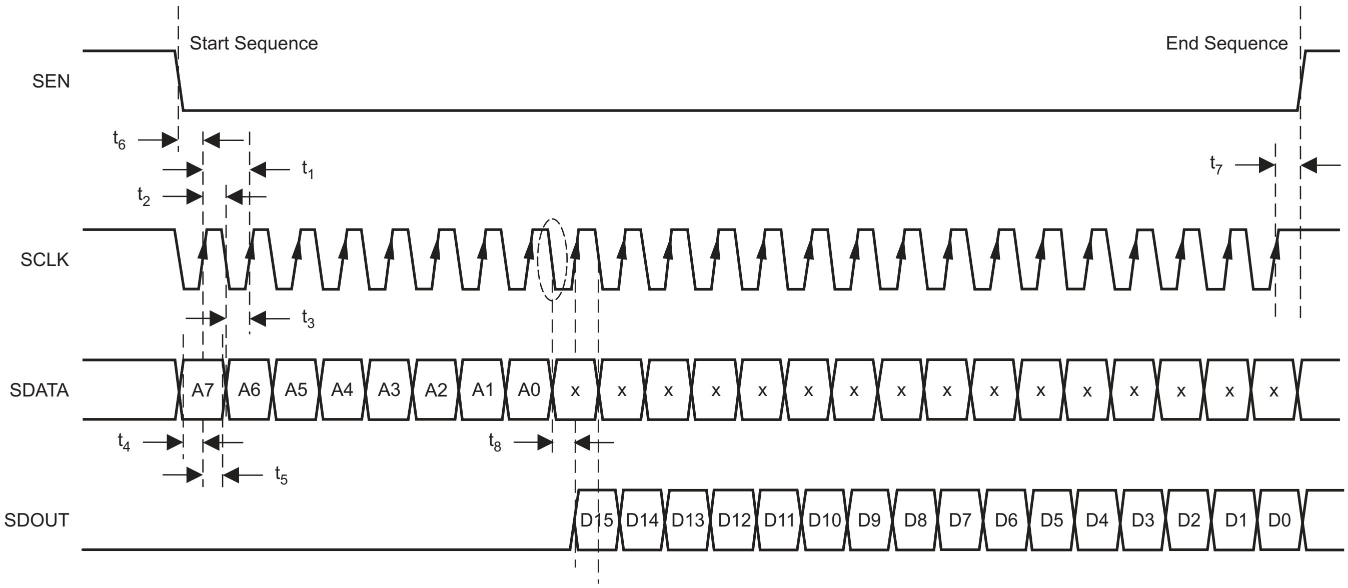


Figure 63. Serial Interface Register Readout Timing

The VCA5807 SDOUT buffer is 3-stated and will get enabled only when 0[1] (REGISTER_READOUT_ENABLE) is enabled. SDOUT pins from multiple VCA5807s can be tied together without any pull-up resistors. Level shifter SN74AUP1T34 can be used to convert 3.3V logic to 2.5V/1.8V logics if needed.

SPI Timing Characteristics

Minimum values across full temperature range t_{MIN} = –40°C to t_{MAX} = 85°C, AVDD_5V = 5V, AVDD = 3.3V

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	SEN fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to SEN rising edge	8			ns
t_8	SDOUT Delay	12	20	28	ns

VCA Register Map

A reset process is required at the VCA5807 initialization stage. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a positive pulse in the RESET pin
2. Through a software reset, using the serial interface, by setting the SOFTWARE_RESET bit to high. Setting this bit initializes the internal registers to the respective default values (all zeros) and then self-resets the SOFTWARE_RESET bit to low. In this case, the RESET pin can stay low (inactive).

After reset, all VCA registers are set to '0', that is, default setting. During register programming, all reserved/unlisted register bits need to be set as '0'.Register settings are maintained when the VCA5807 is in either partial power down mode or complete power down mode.

Table 1. VCA Register Map

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
0[0]	0x0[0]	0	SOFTWARE_RESET	0: Normal operation 1: Reset the device
0[1]	0[1]	0	REGISTER_READOUT_ENABLE	0:Disable readout 1: Enable readout of register at SDOUT Pin
51[0]	0x33[0]	0	RESERVED	0
51[3:1]	0x33[3:1]	0	LPF_PROGRAMMABILITY	000: 15MHz, 010: 20MHz, 011: 30MHz, 100: 10MHz
51[4]	0x33[4]	0	PGA_INTEGRATOR_DISABLE (PGA_HPF_DISABLE)	0: Enable 1: Disables offset integrator for PGA. Please see explanation for the PGA integrator function in PROGRAMMABLE GAIN AMPLIFIER (PGA) and PGA OUTPUT CONFIGURATION section
51[7:5]	0x33[7:5]	0	PGA_CLAMP_LEVEL	Low Noise mode: 53[11:10]=00 000: –2 dBFS 010: 0 dBFS 1XX: Clamp is disabled Low power/Medium Power mode; 53[11:10]=01/10 100: –2 dBFS 110: 0 dBFS 0XX: clamp is disabled Note: At 000 setting, PGA output HD3 will be worsen by 3 dB at –2 dBFS ADC input. In normal operation, clamp function can be set as 000 in the low noise mode. The maximum PGA output level can exceed 2Vpp with the clamp circuit enabled. Note: in the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0. Please see PGA OUTPUT CONFIGURATION.
51[13]	0x33[13]	0	PGA_GAIN_CONTROL	0:24dB; 1:30dB.
52[4:0]	0x34[4:0]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_CNTL	See Table 3 Reg 52[5] should be set as '1' to access these bits
52[5]	0x34[5]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_ENABLE	0: Disable; 1: Enable internal active termination individual resistor control
52[7:6]	0x34[7:6]	0	PRESET_ACTIVE_ TERMINATIONS	00: 50ohm, 01: 100ohm, 10: 200ohm, 11: 400ohm. (Note: the device will adjust resistor mapping (52[4:0]) automatically. 50ohm active termination is NOT supported in 12dB LNA setting. Instead, '00' represents high impedance mode when LNA gain is 12dB)
52[8]	0x34[8]	0	ACTIVE TERMINATION ENABLE	0: Disable; 1: Enable active termination

Table 1. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
52[10:9]	0x34[10:9]	0	LNA_INPUT_CLAMP_SETTING	00: Auto setting 01: 1.5Vpp 10: 1.15Vpp 11: 0.6Vpp
52[11]	0x34[11]	0	RESERVED	Set to 0
52[12]	0x34[12]	0	LNA_INTEGRATOR_DISABLE (LNA_HPF_DISABLE)	0: Enable; 1: Disable offset integrator for LNA. Please see the explanation for this function in the following section
52[14:13]	0x34[14:13]	0	LNA_GAIN	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved
52[15]	0x34[15]	0	LNA_INDIVIDUAL_CH_CNTL	0: Disable; 1: Enable LNA individual channel control. See Register 57 for details
53[7:0]	0x35[7:0]	0	PDN_CH<7:0>	0: Normal operation; 1: Powers down corresponding channels. Bit7→CH8, Bit6→CH7…Bit0→CH1. PDN_CH will shut down whichever blocks are active depending on TGC mode or CW mode
53[8]	0x35[8]	0	RESERVED	Set to 0
53[9]	0x35[9]	0	LOW_NF	0: Normal operation 1: Enable low noise figure mode for high impedance probes
53[11:10]	0x35[11:10]	0	POWER_MODES	00: Low noise mode; 01: Low power mode. At 30dB PGA, total chain gain may slightly change. See typical characteristics 10: Medium power mode. At 30dB PGA, total chain gain may slightly change. See typical characteristics 11: Reserved Note: in the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0.
53[12]	0x35[12]	0	PDN_VCAT_PGA	0: Normal operation; 1: Power down VCAT (voltage-controlled-attenuator) and PGA
53[13]	0x35[13]	0	PDN_LNA	0: Normal operation; 1: Power down LNA only
53[14]	0x35[14]	0	VCA_PARTIAL_PDN	0: Normal operation; 1: Power down LNA, VCAT, and PGA partially(fast wake response)
53[15]	0x35[15]	0	VCA_COMPLETE_PDN	0: Normal operation; 1: Power down LNA, VCAT, and PGA completely (slow wake response). This bit can overwrite 53[14].
54[4:0]	0x36[4:0]	0	CW_SUM_AMP_GAIN_CNTL	Select Feedback resistor for the CW Amplifier as per Table 3 below
54[5]	0x36[5]	0	CW_16X_CLK_SEL	0: Accept differential clock; 1: Accept CMOS clock
54[6]	0x36[6]	0	CW_1X_CLK_SEL	0: Accept CMOS clock; 1: Accept differential clock
54[7]	0x36[7]	0	RESERVED	Set to 0
54[8]	0x36[8]	0	CW_TGC_SEL	0: TGC Mode; 1 : CW Mode Note : VCAT and PGA are still working in the CW mode. They should be powered down separately through 53[12]
54[9]	0x36[9]	0	CW_SUM_AMP_ENABLE	0: Enable CW summing amplifier; 1: Disable CW summing amplifier. Note: 54[9] is only effective in the CW mode.

Table 1. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
54[11:10]	0x36[11:10]	0	CW_CLK_MODE_SEL	00: 16X mode; 01: 8X mode; 10: 4X mode; 11: 1X mode; Note: 0x3B[10]=0.
55[3:0]	0x37[3:0]	0	CH1_CW_MIXER_PHASE	0000→1111, 16 different phase delays, see Table 6
55[7:4]	0x37[7:4]	0	CH2_CW_MIXER_PHASE	
55[11:8]	0x37[11:8]	0	CH3_CW_MIXER_PHASE	
55[15:12]	0x37[15:12]	0	CH4_CW_MIXER_PHASE	
56[3:0]	0x38[3:0]	0	CH5_CW_MIXER_PHASE	
56[7:4]	0x38[7:4]	0	CH6_CW_MIXER_PHASE	
56[11:8]	0x38[11:8]	0	CH7_CW_MIXER_PHASE	
56[15:12]	0x38[15:12]	0	CH8_CW_MIXER_PHASE	
57[1:0]	0x39[1:0]	0	CH1_LNA_GAIN_CNTL	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved REG52[15] should be set as '1'
57[3:2]	0x39[3:2]	0	CH2_LNA_GAIN_CNTL	
57[5:4]	0x39[5:4]	0	CH3_LNA_GAIN_CNTL	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved REG52[15] should be set as '1'
57[7:6]	0x39[7:6]	0	CH4_LNA_GAIN_CNTL	
57[9:8]	0x39[9:8]	0	CH5_LNA_GAIN_CNTL	
57[11:10]	0x39[11:10]	0	CH6_LNA_GAIN_CNTL	
57[13:12]	0x39[13:12]	0	CH7_LNA_GAIN_CNTL	
57[15:14]	0x39[15:14]	0	CH8_LNA_GAIN_CNTL	
59[3:2]	0x3B[3:2]	0	HPF_LNA	00: 100KHz; 01: 50KHz; 10: 200KHz; 11: 150KHz Note: the above frequencies is based on 0.015uF capacitors at INMx.
59[6:4]	0x3B[6:4]	0	DIG_TGC_ATT_GAIN	000: 0dB attenuation; 001: 6dB attenuation; N: ~N×6dB attenuation when 59[7] = 1
59[7]	0x3B[7]	0	DIG_TGC_ATT	0: Disable digital TGC attenuator; 1: Enable digital TGC attenuator
59[8]	0x3B[8]	0	CW_SUM_AMP_PDN	0: Power down CW summing amplifier; 1: Normal operation. Note: 59[8] is only effective in TGC test mode.
59[9]	0x3B[9]	0	PGA_TEST_MODE	0: Normal CW operation; 1: PGA outputs appear at the CW outputs
59[10]	0x3B[10]	0	CW_32X_CLK_MODE_ENABLE	0: CW clock mode is determined by 0x36[11:10]; 1: Enable CW 32X mode

VCA Register Description

LNA Input Impedances Configuration (Active Termination Programmability)

Different LNA input impedances can be configured through the register 52[4:0]. By enabling and disabling the feedback resistors between LNA outputs and ACTx pins, LNA input impedance is adjustable accordingly. Table 2 describes the relationship between LNA gain and 52[4:0] settings. The input impedance settings are the same for both TGC and CW paths.

The VCA5807 also has 4 preset active termination impedances as described in 52[7:6]. An internal decoder is used to select appropriate resistors corresponding to different LNA gain.

Table 2. Register 52[4:0] Description

52[4:0]/0x34[4:0]	FUNCTION
00000	No feedback resistor enabled
00001	Enables 450 Ω feedback resistor
00010	Enables 900 Ω feedback resistor
00100	Enables 1800 Ω feedback resistor
01000	Enables 3600 Ω feedback resistor
10000	Enables 4500 Ω feedback resistor

Table 3. Register 52[4:0] vs LNA Input Impedances

52[4:0]/0x34[4:0]	**00000**	**00001**	**00010**	**00011**	**00100**	**00101**	**00110**	**00111**
LNA:12dB	High Z	150 Ω	300 Ω	100 Ω	600 Ω	120 Ω	200 Ω	86 Ω
LNA:18dB	High Z	90 Ω	180 Ω	60 Ω	360 Ω	72 Ω	120 Ω	51 Ω
LNA:24dB	High Z	50 Ω	100 Ω	33 Ω	200 Ω	40 Ω	66.67 Ω	29 Ω
52[4:0]/0x34[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
LNA:12dB	1200 Ω	133 Ω	240 Ω	92 Ω	400 Ω	109 Ω	171 Ω	80 Ω
LNA:18dB	720 Ω	80 Ω	144 Ω	55 Ω	240 Ω	65 Ω	103 Ω	48 Ω
LNA:24dB	400 Ω	44 Ω	80 Ω	31 Ω	133 Ω	36 Ω	57 Ω	27 Ω
52[4:0]/0x34[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
LNA:12dB	1500 Ω	136 Ω	250 Ω	94 Ω	429 Ω	111 Ω	176 Ω	81 Ω
LNA:18dB	900 Ω	82 Ω	150 Ω	56 Ω	257 Ω	67 Ω	106 Ω	49 Ω
LNA:24dB	500 Ω	45 Ω	83 Ω	31 Ω	143 Ω	37 Ω	59 Ω	27 Ω
52[4:0]/0x34[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
LNA:12dB	667 Ω	122 Ω	207 Ω	87 Ω	316 Ω	102 Ω	154 Ω	76 Ω
LNA:18dB	400 Ω	73 Ω	124 Ω	52 Ω	189 Ω	61 Ω	92 Ω	46 Ω
LNA:24dB	222 Ω	41 Ω	69 Ω	29 Ω	105 Ω	34 Ω	51 Ω	25 Ω

Programmable Gain for CW Summing Amplifier

Different gain can be configured for the CW summing amplifier through the register 54[4:0]. By enabling and disabling the feedback resistors between the summing amplifier inputs and outputs, the gain is adjustable accordingly to maximize the dynamic range of CW path. Table 4 describes the relationship between the summing amplifier gain and 54[4:0] settings.

Table 4. Register 54[4:0] Description

54[4:0]/0x36[4:0]	FUNCTION
00000	No feedback resistor
00001	Enables 250 Ω feedback resistor
00010	Enables 250 Ω feedback resistor
00100	Enables 500 Ω feedback resistor
01000	Enables 1000 Ω feedback resistor
10000	Enables 2000 Ω feedback resistor

Table 5. Register 54[4:0] vs CW Summing Amplifier Gain

54[4:0]/0x36[4:0]	00000	00001	00010	00011	00100	00101	00110	00111
CW I/V Gain	N/A	0.50	0.50	0.25	1.00	0.33	0.33	0.20
54[4:0]/0x36[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
CW I/V Gain	2.00	0.40	0.40	0.22	0.67	0.29	0.29	0.18
54[4:0]/0x36[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
CW I/V Gain	4.00	0.44	0.44	0.24	0.80	0.31	0.31	0.19
54[4:0]/0x36[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
CW I/V Gain	1.33	0.36	0.36	0.21	0.57	0.27	0.27	0.17

Programmable Phase Delay for CW Mixer

Accurate CW beamforming is achieved through adjusting the phase delay of each channel. In the VCA5807, 16 different phase delays can be applied to each LNA output; and it meets the standard requirement of typical ultrasound beamformer, that is, $\frac{1}{16}\lambda$ beamformer resolution. Table 4 describes the relationship between the phase delays and the register 55 and 56 settings.

Table 6. CW Mixer Phase Delay vs Register Settings
CH1 - 55[3:0], CH2 - 55[7:4], CH3 - 55[11:8], CH4 - 55[15:12],
CH5- 56[3:0], CH6 - 56[7:4], CH7 - 56[11:8], CH8 - 56[15:12],

CHX_CW_MIXER_PHASE	0000	0001	0010	0011	0100	0101	0110	0111
PHASE SHIFT	0	22.5°	45°	67.5°	90°	112.5°	135°	157.5°
CHX_CW_MIXER_PHASE	1000	1001	1010	1011	1100	1101	1110	1111
PHASE SHIFT	180°	202.5°	225°	247.5°	270°	292.5°	315°	337.5°

THEORY OF OPERATION

VCA5807 OVERVIEW

The VCA5807 is an integrated Voltage Controlled Amplifier (VCA) solution specifically designed for ultrasound systems in which high performance and small size are required. The VCA5807 integrates a complete time-gain-control (TGC) imaging path and a continuous wave Doppler (CWD) path. It also enables users to select one of various power/noise combinations to optimize system performance. The VCA5807 contains eight channels; each channels includes a Low-Noise Amplifier (LNA), a Voltage Controlled Attenuator (VCAT), a Programmable Gain Amplifier (PGA), a Low-pass Filter (LPF), and a CW mixer.

In addition, multiple features in the VCA5807 are suitable for ultrasound applications, such as active termination, individual channel control, fast power up/down response, programmable clamp voltage control, fast and consistent overload recovery, ands o on. Therefore, the VCA5807 brings premium image quality to ultra–portable, handheld systems all the way up to high-end ultrasound systems. In addition, the VCA5807 can support sonar applications, considering its excellent low frequency (<100 KHz) response. Its simplified function block diagram is listed in Figure 64.

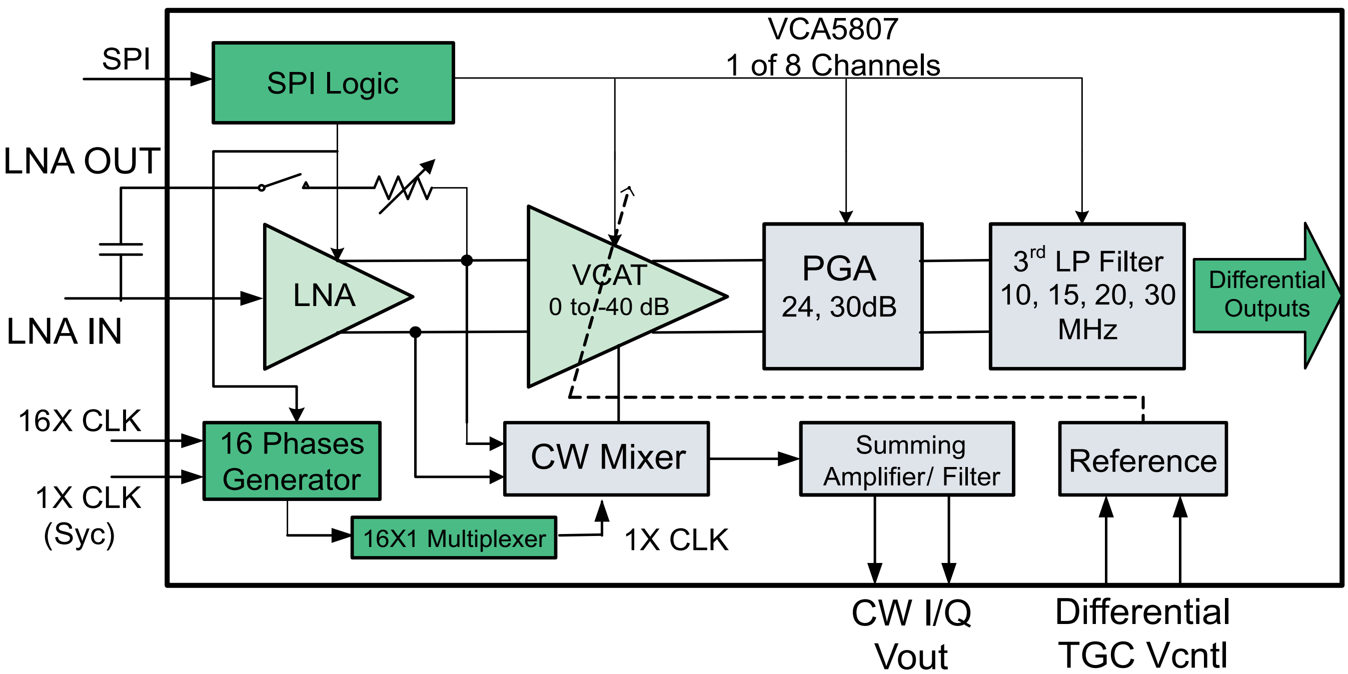


Figure 64. Functional Block Diagram

LOW-NOISE AMPLIFIER (LNA)

In many high-gain systems, a low noise amplifier is critical to achieve overall performance. Using a new proprietary architecture, the LNA in the VCA5807 delivers exceptional low-noise performance, while operating on a very low quiescent current compared to CMOS-based architectures with similar noise performance. The LNA performs single-ended input to differential output voltage conversion. It is configurable for a programmable gain of 24/18/12dB and its input-referred noise is only 0.63/0.70/0.9nV/√Hz respectively. Programmable gain settings result in a flexible linear input range up to 1Vpp, realizing high signal handling capability demanded by new transducer technologies. Larger input signal can be accepted by the LNA; however the signal can be distorted since it exceeds the LNA's linear operation region. Combining the low noise and high input range, a wide input dynamic range is achieved consequently for supporting the high demands from various ultrasound imaging modes.

The LNA input is internally biased at approximately +2.4V; the signal source should be ac-coupled to the LNA input by an adequately-sized capacitor, that is, ≥ 0.1µF. To achieve low DC offset drift, the VCA5807 incorporates a DC offset correction circuit for each amplifier stage. To improve the overload recovery, an integrator circuit is used to extract the DC component of the LNA output and then fed back to the LNA's complementary input for DC offset correction. This DC offset correction circuit has a high-pass response and can be treated as a high-pass filter. The effective corner frequency is determined by the capacitor C_{BYPASS} connected at INM. With larger capacitors, the corner frequency is lower. For stable operation at the highest HP filer cut-off frequency, a ≥15nF capacitor can be selected. This corner frequency scales almost linearly with the value of the C_{BYPASS}. For example, 15nF gives a corner frequency of approximately 100 kHz, while 47nF can give an effective corner frequency of 33 KHz. If low frequency operation is desired, the DC offset correction circuit can also be disabled/enabled through register 52[12]. A large capacitor like 1 µF can be used for setting low corner frequency (<2 KHz) of the LNA DC offset correction circuit. Figure 61 shows the frequency responses for low frequency applications.

The VCA5807 can be terminated passively or actively. Active termination is preferred in ultrasound application for reducing reflection from mismatches and achieving better axial resolution without degrading noise figure too much. Active termination values can be preset to 50, 100, 200, 400Ω; other values also can be programmed by users through register 52[4:0]. A feedback capacitor is required between ACTx and the signal source as Figure 65 shows. On the active termination path, a clamping circuit is also used to create a low impedance path when overload signal is seen by the VCA5807. The clamp circuit limits large input signals at the LNA inputs and improves the overload recovery performance of the VCA5807. The clamp level can be set to $350mV_{PP}$, $600mV_{PP}$, $1.15V_{PP}$ automatically depending on the LNA gain settings when register 52[10:9]=0. Other clamp voltages, such as $1.15V_{PP}$, $0.6V_{PP}$, and $1.5V_{PP}$, are also achievable by setting register 52[10:9]. This clamping circuit is also designed to obtain good pulse inversion performance and reduce the impact from asymmetric inputs. Please note that the clamp settings may change during LNA gain switching. Thus the clamp settling time has to be considered when adjusting LNA gain, especially when overload signals exceed the clamping voltage.

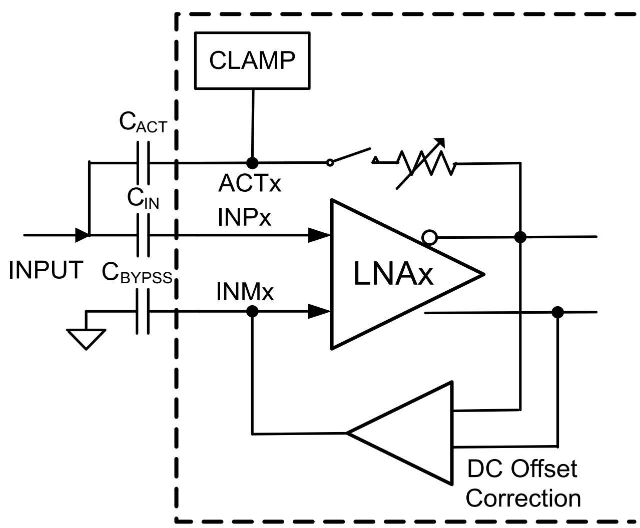


Figure 65. VCA5807 LNA with DC Offset Correction Circuit

VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator is designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB (see Figure 2) is constant for each equal increment of the control voltage (VCNTL) as shown in Figure 66. A differential control structure is used to reduce common mode noise. A simplified attenuator structure is shown in the following Figure 66 and Figure 67.

The attenuator is essentially a variable voltage divider that consists of the series input resistor (R_S) and seven shunt FETs placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A7). V_{CNTL} is the effective difference between VCNTLP and VCNTLM. Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V7 are equally spaced over the 0V to 1.5V control voltage range. As the control voltage increases through the input range of each clipping amplifier, the amplifier output rises from a voltage where the FET is nearly OFF to VHIGH where the FET is completely ON. As each FET approaches its ON state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned OFF, producing minimum signal attenuation. Similarly, high control voltages turn the FETs ON, leading to maximum signal attenuation. Therefore, each FET acts to decrease the shunt resistance of the voltage divider formed by Rs and the parallel FET network.

Additionally, a digitally controlled TGC mode is implemented to achieve better phase-noise performance in the VCA5807. The attenuator can be controlled digitally instead of the analog control voltage V_{CNTL}. This mode can be set by the register bit 59[7]. The variable voltage divider is implemented as a fixed series resistance and FET as the shunt resistance. Each FET can be turned ON by connecting the switches SW1-7. Turning on each of the switches can give approximately 6dB of attenuation. This can be controlled by the register bits 59[6:4]. This digital control feature can eliminate the noise from the VCNTL circuit and ensure the better SNR and phase noise for the TGC path.

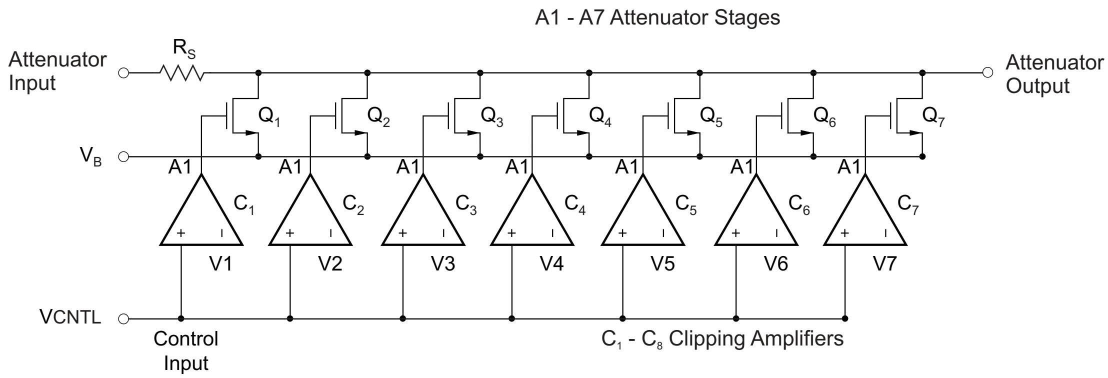


Figure 66. Simplified Voltage Controlled Attenuator (Analog Structure)

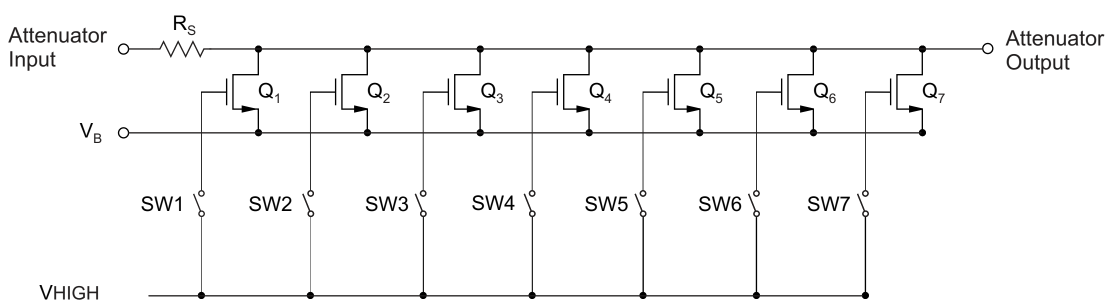


Figure 67. Simplified Voltage Controlled Attenuator (Digital Structure)

The voltage controlled attenuator's noise follows a monotonic relationship to the attenuation coefficient. At higher attenuation, the input-referred noise is higher and vice-versa. The attenuator's noise is then amplified by the PGA and becomes the noise floor at ADC input. In the attenuator's high attenuation operating range, that is, VCNTL is high, the attenuator's input noise may exceed the LNA's output noise; the attenuator then becomes the dominant noise source for the following PGA stage and ADC. Therefore, the attenuator's noise should be minimized compared to the LNA output noise. The VCA5807's attenuator is designed for achieving very low noise even at high attenuation (low channel gain) and realizing better SNR in near field. Please see PGA OUTPUT CONFIGURATION. The input referred noise for different attenuations is listed in the below table:

Table 7. Voltage-Controlled-Attenuator noise vs Attenuation

Attenuation (dB)	Attenuator Input Referred noise (nV/rtHz)
–40	10.5
–36	10
–30	9
–24	8.5

Table 7. Voltage-Controlled-Attenuator noise vs Attenuation (continued)

Attenuation (dB)	Attenuator Input Referred noise (nV/rtHz)
–18	6
–12	4
–6	3
0	2

PROGRAMMABLE GAIN AMPLIFIER (PGA)

After the voltage controlled attenuator, a programmable gain amplifier can be configured as 24dB or 30dB with a constant input referred noise of 1.75nV/rtHz. The PGA structure consists of a differential voltage-to-current converter with programmable gain, current clamping (bias control) circuits, a transimpedance amplifier with a programmable low-pass filter, and a DC offset correction circuit. Its simplified block diagram is shown below:

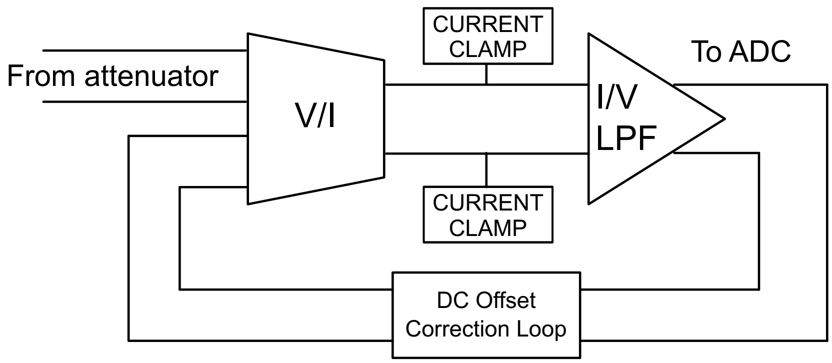


Figure 68. Simplified Block Diagram of PGA

Low input noise is always preferred in a PGA and its noise contribution should not degrade the ADC SNR too much after the attenuator. At the minimum attenuation (used for small input signals), the LNA noise dominates; at the maximum attenuation (large input signals), the PGA and ADC noise dominates. Thus 24dB gain of PGA achieves better SNR as long as the amplified signals can exceed the noise floor of the ADC.

The PGA current clamping circuit can be enabled (register 51) to improve the overload recovery performance of the VCA. If we measure the standard deviation of the output just after overload, for 0.5V V_{CNTL}, it is about 3.2 LSBs in normal case, that is the output is stable in about 1 clock cycle after overload. With the current clamp circuit disabled, the value approaches 4 LSBs meaning a longer time duration before the output stabilizes; however, with the current clamp circuit enabled, there will be degradation in HD3 for PGA output levels > -2dBFS. For example, for a –2dBFS output level, the HD3 degrades by approximately 3dB. In order to maximize the output dynamic range, the maximum PGA output level can exceed 2Vpp (0 dBFS linear output range) with the clamp circuit. Thus ADCs with excellent overload recovery performance should be selected.

NOTE

In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0

The VCA5807 integrates an anti-aliasing filter in the form of a programmable low-pass filter (LPF) in the transimpedance amplifier. The LPF is designed as a differential, active, 3rd order filter with Butterworth characteristics and a typical 18dB per octave roll-off. Programmable through the serial interface, the –1dB frequency corner can be set to one of 10MHz, 15MHz, 20MHz, and 30MHz. The filter bandwidth is set for all channels simultaneously.

A selectable DC offset correction circuit is implemented in the PGA as well. This correction circuit is similar to the one used in the LNA. It extracts the DC component of the PGA outputs and feeds back to the PGA's complimentary inputs for DC offset correction. This DC offset correction circuit also has a high-pass response with a cut-off frequency of 80KHz. If <80KHz operation is needed, the DC offset correction circuit can be disabled through the register 0x33[4].

CONTINUOUS-WAVE (CW) BEAMFORMER

Continuous-wave Doppler is a key function in mid-end to high-end ultrasound systems. Compared to the TGC mode, the CW path needs to handle high dynamic range along with strict phase noise performance. CW beamforming is often implemented in analog domain due to the mentioned strict requirements. Multiple beamforming methods are being implemented in ultrasound systems, including passive delay line, active mixer, and passive mixer. Among all of them, the passive mixer approach achieves optimized power and noise. It satisfies the CW processing requirements, such as wide dynamic range, low phase noise, accurate gain and phase matching.

A simplified CW path block diagram and an In-phase or Quadrature (I/Q) channel block diagram are illustrated below respectively. Each CW channel includes a LNA, a voltage-to-current converter, a switch-based mixer, a shared summing amplifier with a low-pass filter, and clocking circuits. All blocks include well-matched in-phase and quadrature channels to achieve good image frequency rejection as well as beamforming accuracy. As a result, the image rejection ratio from an I/Q channel is better than -46dBc which is desired in ultrasound systems.

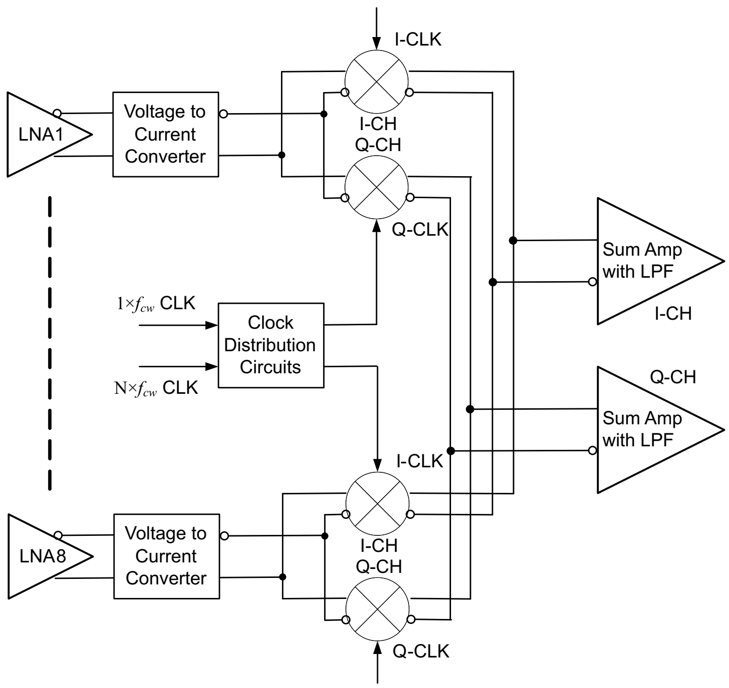
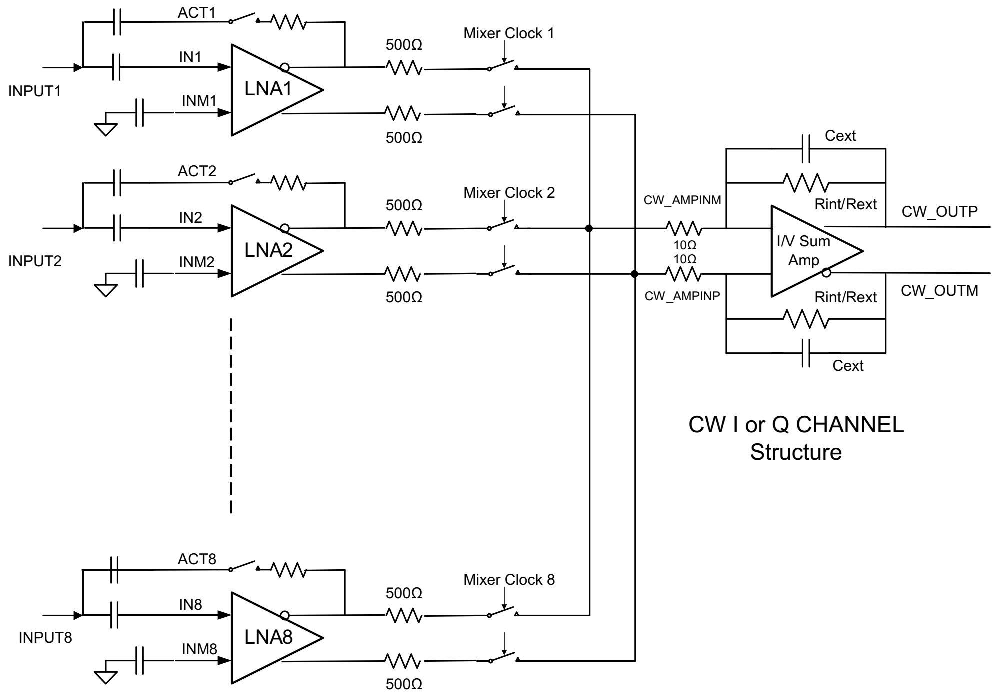


Figure 69. Simplified Block Diagram of CW Path



Note: the 10~15Ω resistors at CW_AMPINM/P are due to internal IC routing and can create slight attenuation.

Figure 70. A Complete In-phase or Quadrature Phase Channel

The CW mixer in the VCA5807 is passive and switch based; passive mixer adds less noise than active mixers. It achieves good performance at low power. The below illustration and equations describe the principles of mixer operation, where Vi(t), Vo(t) and LO(t) are input, output and local oscillator (LO) signals for a mixer respectively. The LO(t) is square-wave based and includes odd harmonic components as the below equation expresses:

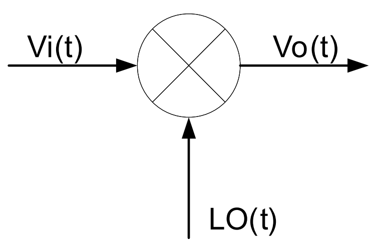


Figure 71. Block Diagram of Mixer Operation

$$Vi(t) = \sin(\omega_0 t + \omega_d t + \varphi) + f(\omega_0 t)$$

$$LO(t) = \frac{4}{\pi}\left[\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_0 t) + \frac{1}{5}\sin(5\omega_0 t)...\right]$$

$$Vo(t) = \frac{2}{\pi}\left[\cos(\omega_d t + \phi) - \cos(2\omega_0 t - \omega_d t + \phi)...\right] \tag{1}$$

From the above equations, the 3rd and 5th order harmonics from the LO can interface with the 3rd and 5th order harmonic signals in the Vi(t); or the noise around the 3rd and 5th order harmonics in the Vi(t). Therefore, the mixer's performance is degraded. In order to eliminate this side effect due to the square-wave demodulation, a proprietary harmonic suppression circuit is implemented in the VCA5807. The 3rd and 5th harmonic components from the LO can be suppressed by over 12dB. Thus the LNA output noise around the 3rd and 5th order harmonic bands will not be down-converted to base band. Hence, better noise figure is achieved. The conversion loss of the mixer is about -4dB which is derived from:

$$20\log_{10}\frac{2}{\pi} \quad (2)$$

The mixed current outputs of the 8 channels are summed together internally. An internal low noise operational amplifier is used to convert the summed current to a voltage output. The internal summing amplifier is designed to accomplish low power consumption, low noise, and ease of use. CW outputs from multiple VCA5807s can be further combined on system board to implement a CW beamformer with more than 8 channels. More detail information can be found in Figure 92.

Multiple clock options are supported in the VCA5807 CW path. Two CW clock inputs are required: N×f_{cw} clock and 1 × f_{cw} clock, where f_{cw} is the CW transmitting frequency and N could be 32, 16, 8, 4, or 1. Users have the flexibility to select the most convenient system clock solution for the VCA5807. In the 32× f_{cw}, 16 × f_{cw} and 8× f_{cw} modes, the 3rd and 5th harmonic suppression feature can be supported. Thus, the 16 × f_{cw} and 8 × f_{cw} modes achieves better performance than the 4 × f_{cw} and 1 × f_{cw} modes.

16 × f_{cw} and 32 × f_{cw} Mode

The 16 × f_{cw} mode achieves the best phase accuracy compared to other modes. It is the default mode for CW operation. In this mode, 16 × f_{cw} and 1 × f_{cw} clocks are required. 16×f_{cw} generates LO signals with 16 accurate phases. Multiple VCA5807s can be synchronized by the 1 × f_{cw} , that is, LO signals in multiple VCAs can have the same starting phase. The phase noise spec is critical only for 16X clock. 1X clock is for synchronization only and doesn’t require low phase noise. See the phase noise requirement in CW Clock Selection. In addition, the 1X clock can be either a continue wave with a frequency of f_{cw} or a single pulse with a pulse width T>(1/16 x f_{cw}).

The top level clock distribution diagram is shown in Figure 72. Each mixer's clock is distributed through a 16 × 8 cross-point switch. The inputs of the cross-point switch are 16 different phases of the 1x clock. It is recommended to align the rising edges of the 1 x f_{cw} and 16 x f_{cw} clocks.

The cross-point switch distributes the clocks with appropriate phase delay to each mixer. For example, $V_I(t)$ is a received signal with a delay of 1/16 T , a delayed $L_O(t)$ should be applied to the mixer in order to compensate for the 1/16 T delay. Thus a 22.5º delayed clock, that is, 2π/16 , is selected for this channel. The mathematic calculation is expressed in the following equations:

$$Vi(t) = \sin\left[\omega_0\left(t + \frac{1}{16f_0}\right) + \omega_d t\right] = \sin\left[\omega_0 t + 22.5^\circ + \omega_d t\right]$$

$$LO(t) = \frac{4}{\pi}\sin\left[\omega_0\left(t + \frac{1}{16f_0}\right)\right] = \frac{4}{\pi}\sin\left[\omega_0 t + 22.5^\circ\right]$$

$$Vo(t) = \frac{2}{\pi}\cos(\omega_d t) + f(\omega_n t) \quad (3)$$

Vo(t) represents the demodulated Doppler signal of each channel. When the Doppler signals from N channels are summed, the signal to noise ratio improves.

Comparing to the 16x f_{cw} configuration, an extra 2X clock divider is added in the 32x f_{cw} configuration. Same CW performance is achieved in both configurations.

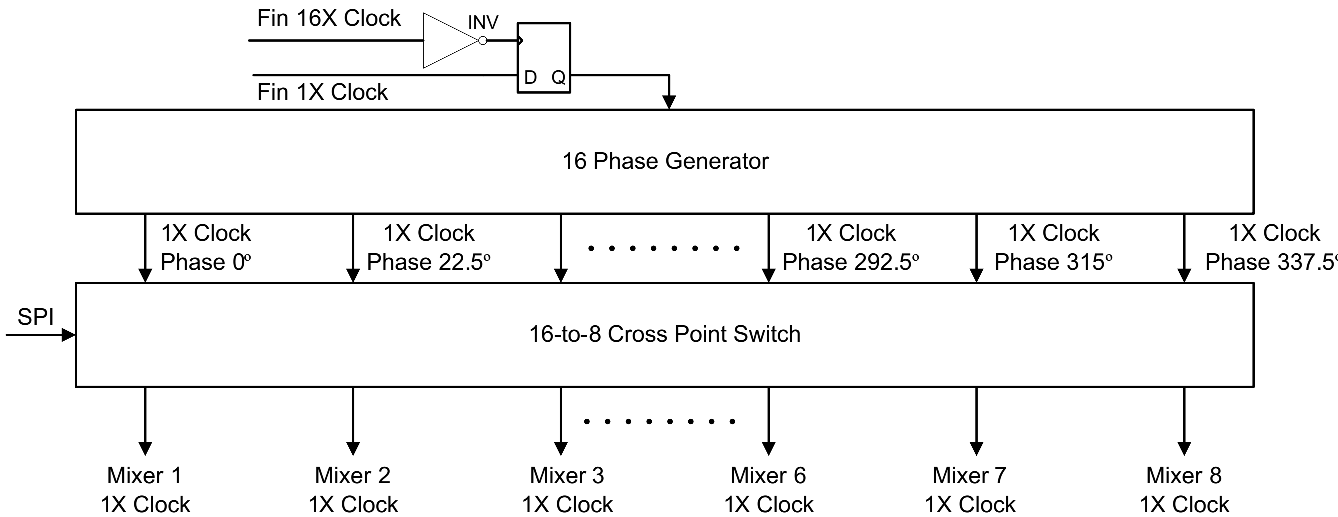


Figure 72. Block Diagram of 1x and 16x CW Clock Distribution

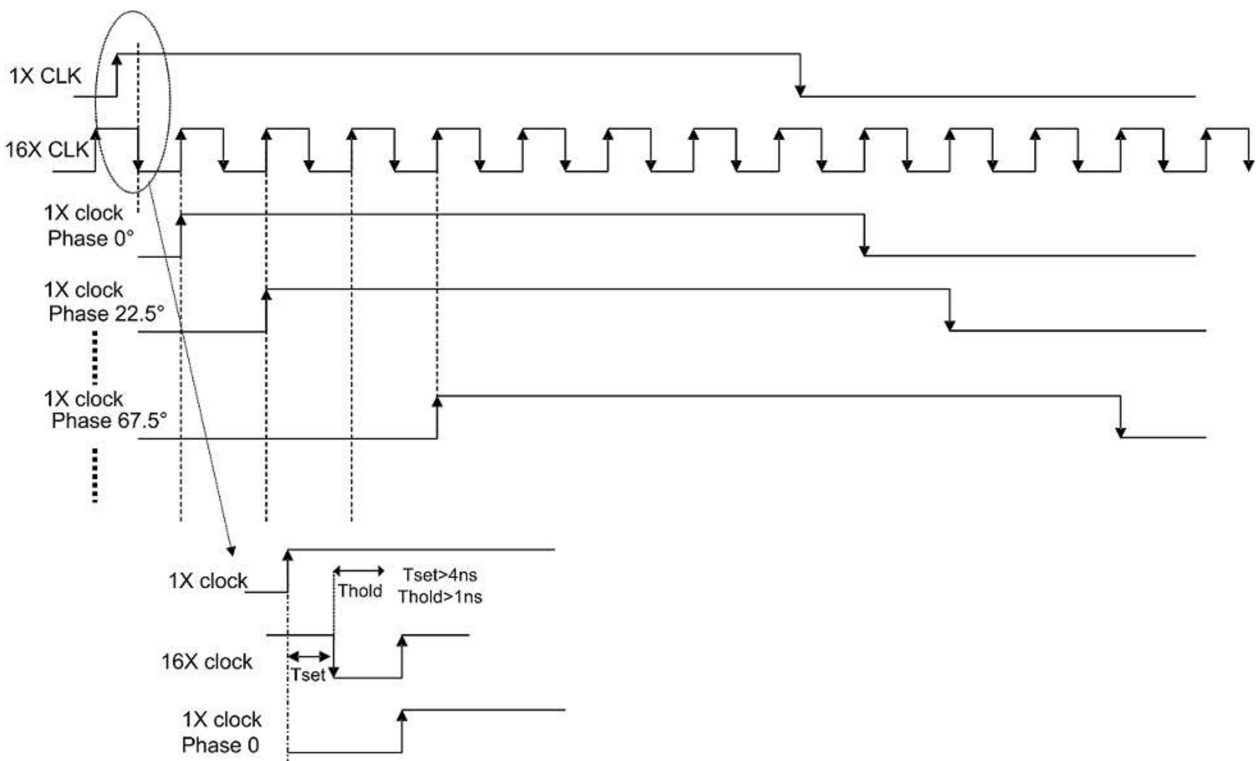


Figure 73. 1x and 16x CW Clock Timing

8 × f_{cw} and 4 × f_{cw} Modes

8 × f_{cw} and 4 × f_{cw} modes are alternative modes when higher frequency clock solution (that is, 16 × f_{cw} clock) is not available in system. The block diagram of these two modes is shown below.

Good phase accuracy and matching are also maintained. Quadature clock generator is used to create in-phase and quadrature clocks with exact 90° phase difference. The only difference between 8 × f_{cw} and 4 × f_{cw} modes is the accessibility of the 3rd and 5th harmonic suppression filter. In the 8 × f_{cw} mode, the suppression filter can be supported. In both modes, 1/16 T phase delay resolution is achieved by weighting the in-phase and quadrature paths correspondingly. For example, if a delay of 1/16 T or 22.5° is targeted, the weighting coefficients should follow the below equations, assuming I_{in} and Q_{in} are sin(ω_0t) and cos(ω_0t) respectively:

$$I_{delayed}(t) = I_{in}\cos\left(\frac{2\pi}{16}\right) + Q_{in}\sin\left(\frac{2\pi}{16}\right) = I_{in}\left(t + \frac{1}{16 f_0}\right)$$

$$Q_{delayed}(t) = Q_{in}\cos\left(\frac{2\pi}{16}\right) - I_{in}\sin\left(\frac{2\pi}{16}\right) = Q_{in}\left(t + \frac{1}{16 f_0}\right) \quad (4)$$

Therefore, after I/Q mixers, phase delay in the received signals is compensated. Mixers' outputs from all channels are aligned and added linearly to improve the signal to noise ratio. It is preferred to have the 4 × f_{cw} or 8 × f_{cw} and 1 × f_{cw} clocks aligned both at the rising edge.

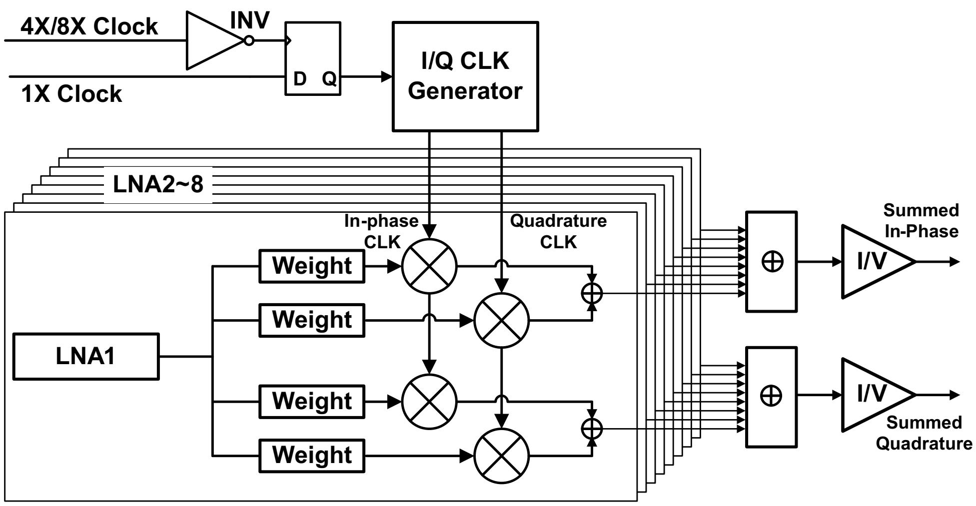


Figure 74. 8 X f_{cw} and 4 X f_{cw} Block Diagram

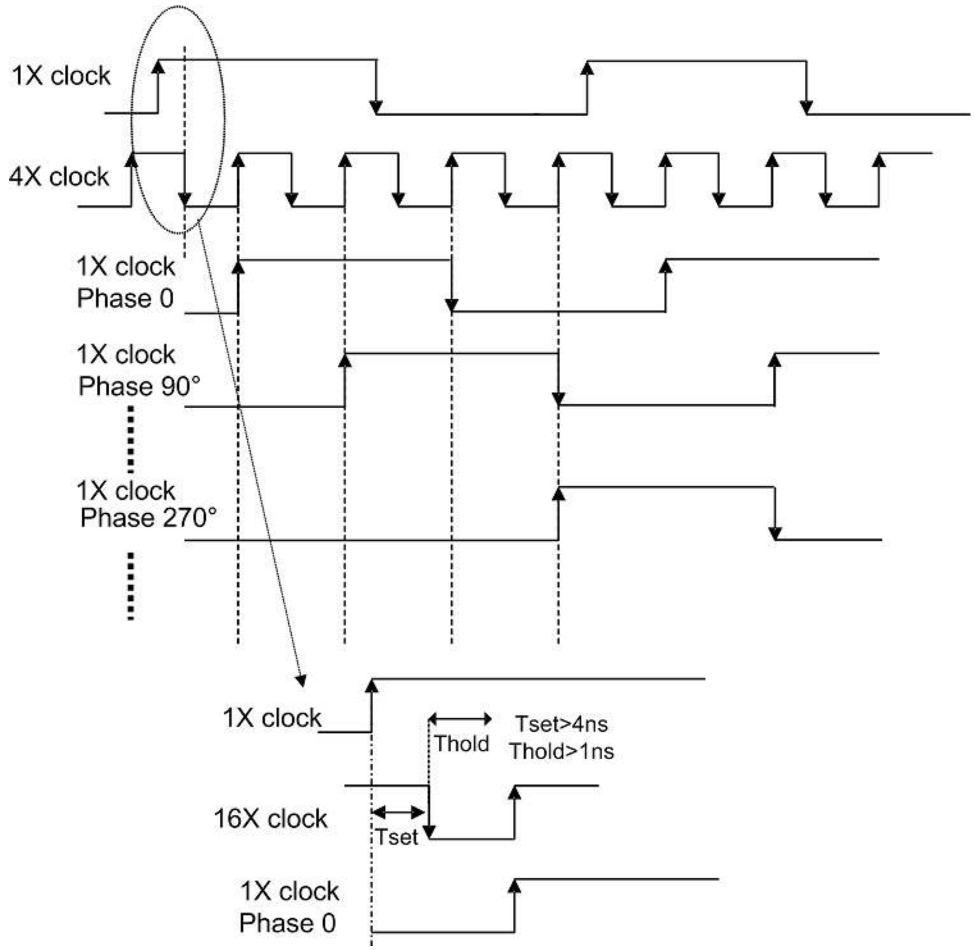


Figure 75. 8 x f_{cw} and 4 x f_{cw} Timing Diagram

1 × f_{cw} Mode

The 1x f_{cw} mode requires in-phase and quadrature clocks with low phase noise specifications. The $\frac{1}{16}T$ phase delay resolution is also achieved by weighting the in-phase and quadrature signals as described in the 8 × f_{cw} and 4 × f_{cw} modes.

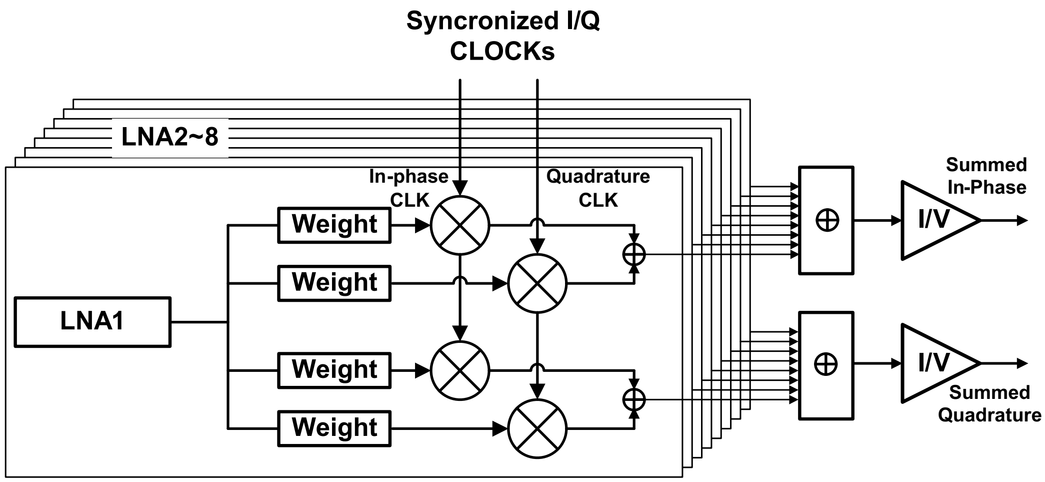


Figure 76. Block Diagram of 1 x f_{cw} mode

EQUIVALENT CIRCUITS

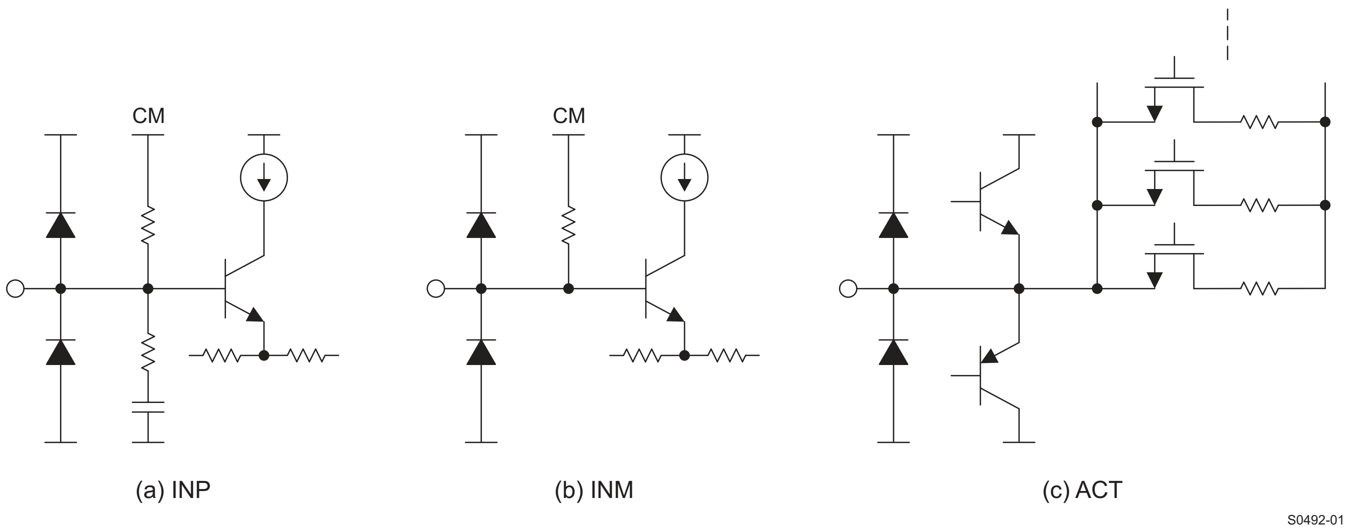


Figure 77. Equivalent Circuits of LNA inputs

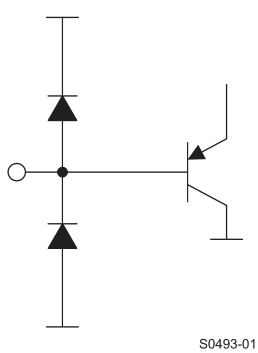


Figure 78. Equivalent Circuits of $V_{CNTLP/M}$

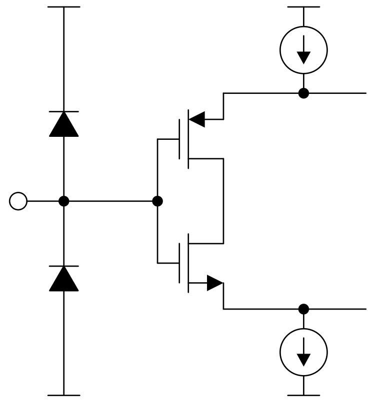
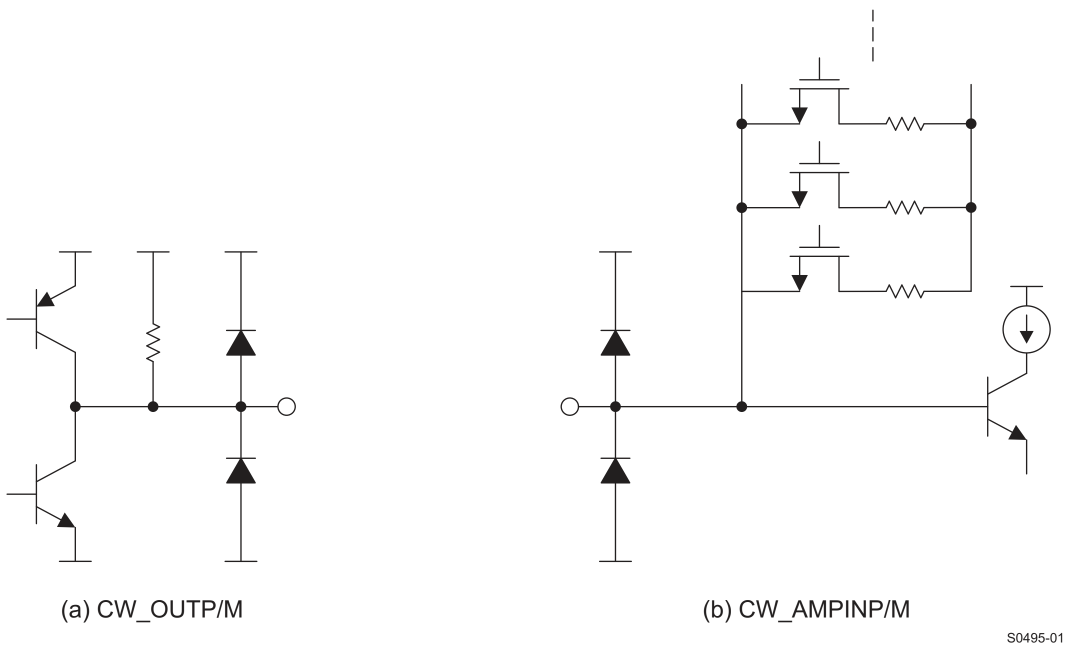


Figure 79. CW 1X and 16X Clocks



(a) CW_OUTP/M

(b) CW_AMPINP/M

Figure 80. Equivalent Circuits of CW Summing Amplifier Inputs and Outputs

APPLICATION INFORMATION

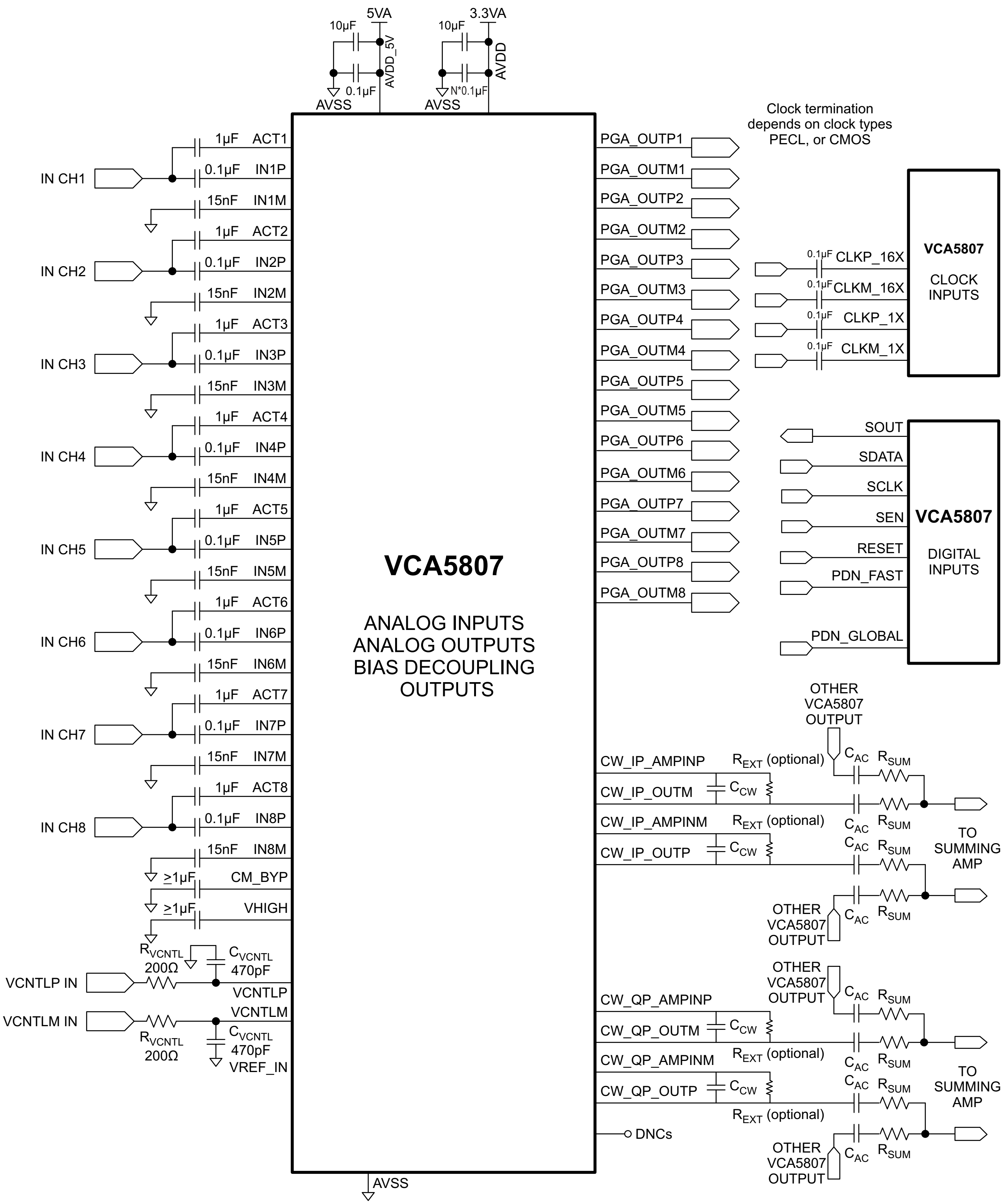
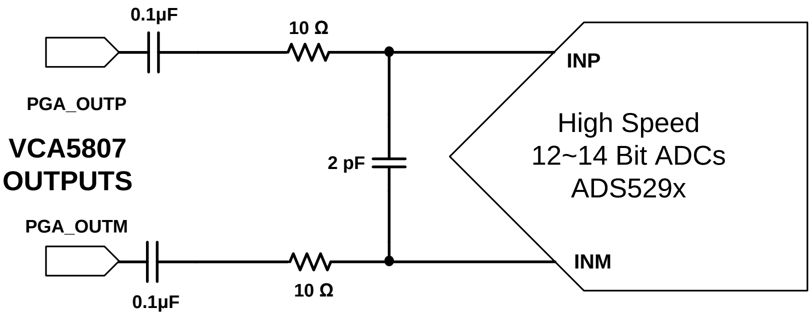
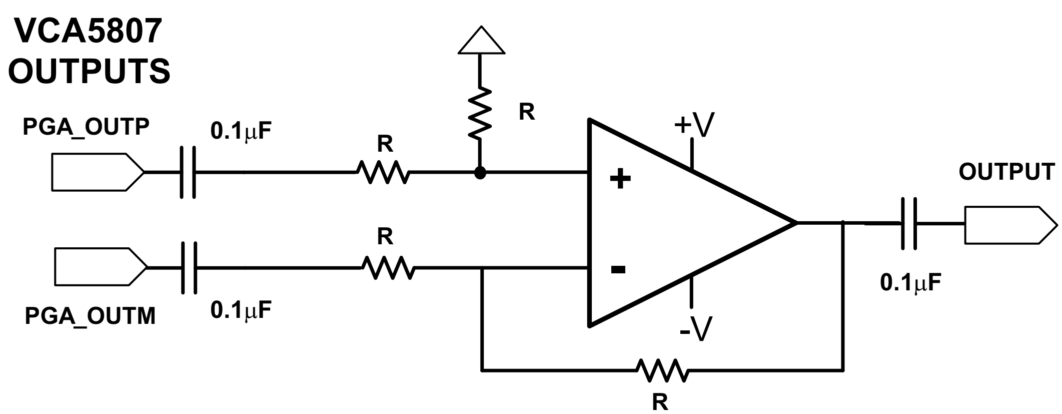


Figure 81. Application Circuit



Note: The optional R-C filter (10 Ω and 2 pF) across the ADC inputs is to absorb the glitches caused by the opening and closing of the sampling capacitors. See the corresponding ADC data sheets.

Figure 82. Typical Application Circuit between VCA5807 and ADC



Note: R ≥ 500 Ω to meet the VCA Minimum load resistance of 1 KΩ.

Figure 83. Typical Application Circuit between VCA5807 and Operational Amplifier

A typical application circuit diagram is listed above. The configuration for each block is discussed below.

LNA CONFIGURATION

LNA Input Coupling and Decoupling

The LNA closed-loop architecture is internally compensated for maximum stability without the need of external compensation components. The LNA inputs are biased at 2.4V and AC coupling is required. A typical input configuration is shown in Figure 84. C_{IN} is the input AC coupling capacitor. C_{ACT} is a part of the active termination feedback path. Even if the active termination is not used, the C_{ACT} is required for the clamp functionality. Recommended values for C_{ACT} ≥ 1µF and C_{IN} are ≥ 0.1µF. A pair of clamping diodes is commonly placed between the T/R switch and the LNA input. Schottky diodes with suitable forward drop voltage (that is, the BAT754/54 series, the BAS40 series, the MMBD7000 series, or similar) can be considered depending on the transducer echo amplitude.

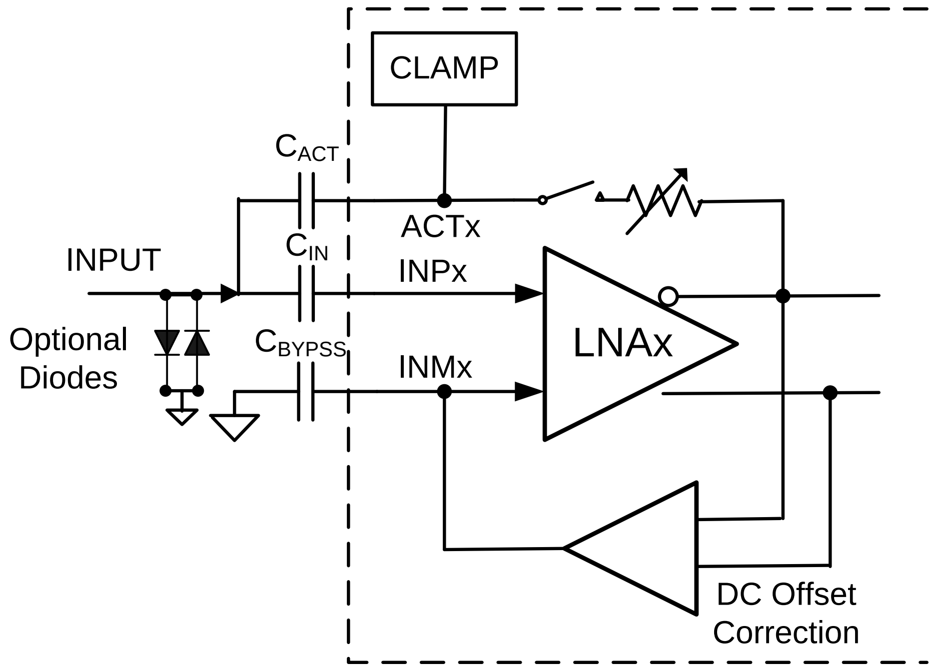


Figure 84. LNA Input Configurations

This architecture minimizes any loading of the signal source that may otherwise lead to a frequency-dependent voltage divider. The closed-loop design yields very low offsets and offset drift. C_{BYPASS} (≥0.015µF) is used to set the high-pass filter cut-off frequency and decouple the complimentary input. Its cut-off frequency is inversely proportional to the C_{BYPASS} value. The HPF cut-off frequency can be adjusted through the register 59[3:2] as Table 8 lists. Low frequency signals at T/R switch output, such as signals with slow ringing, can be filtered out. In addition, the HPF can minimize system noise from DC-DC converters, pulse repetition frequency (PRF) trigger, and frame clock. Most ultrasound systems' signal processing unit includes digital high-pass filters or band-pass filters (BPFs) in FPGAs or ASICs. Further noise suppression can be achieved in these blocks. If low frequency signal detection is desired in some applications, the LNA HPF can be disabled.

Table 8. LNA HPF Settings (C_{BYPASS} = 15 nF)

Reg59[3:2] (0x3B[3:2])	Frequency
00	100 KHz
01	50 KHz
10	200 KHz
11	150 KHz

CM_BYP and VHIGH pins, which generate internal reference voltages, need to be decoupled with ≥1uF capacitors. Bigger bypassing capacitors (>2.2uF) may be beneficial if low frequency noise exists in system.

LNA Noise Contribution

The noise spec is critical for LNA and it determines the dynamic range of entire system. The LNA of the VCA5807 achieves low power and an exceptionally low-noise voltage of 0.63nV/√Hz, and a low current noise of 2.7pA/√Hz.

Typical ultrasonic transducer's impedance Rs varies from tens of ohms to several hundreds of ohms. Voltage noise is the dominant noise in most cases; however, the LNA current noise flowing through the source impedance (Rs) generates additional voltage noise.

$$LNA\_Noise_{total} = \sqrt{V_{LNAnoise}^2 + R_s^2 \times I_{LNAnoise}^2} \tag{5}$$

The VCA5807 achieves low noise figure (NF) over a wide range of source resistances as shown in Figure 31, Figure 32, and Figure 33.

In addition, a low noise figure mode has been implemented by optimizing the current noise and voltage noise contribution. When high impedance transducers appear, the VCA5807's noise figure can be improved by enabling the low noise figure mode (register 0x35[9]). Figure 34 shows the advantages of the low noise figure mode.

Active Termination

In ultrasound applications, signal reflection exists due to long cables between transducer and system. The reflection results in extra ringing added to echo signals in pulsed-wave (PW) mode. Since the axial resolution depends on echo signal length, such ringing effect can degrade the axial resolution. Hence, either passive termination or active termination, is preferred if good axial resolution is desired. Figure 85 shows three termination configurations:

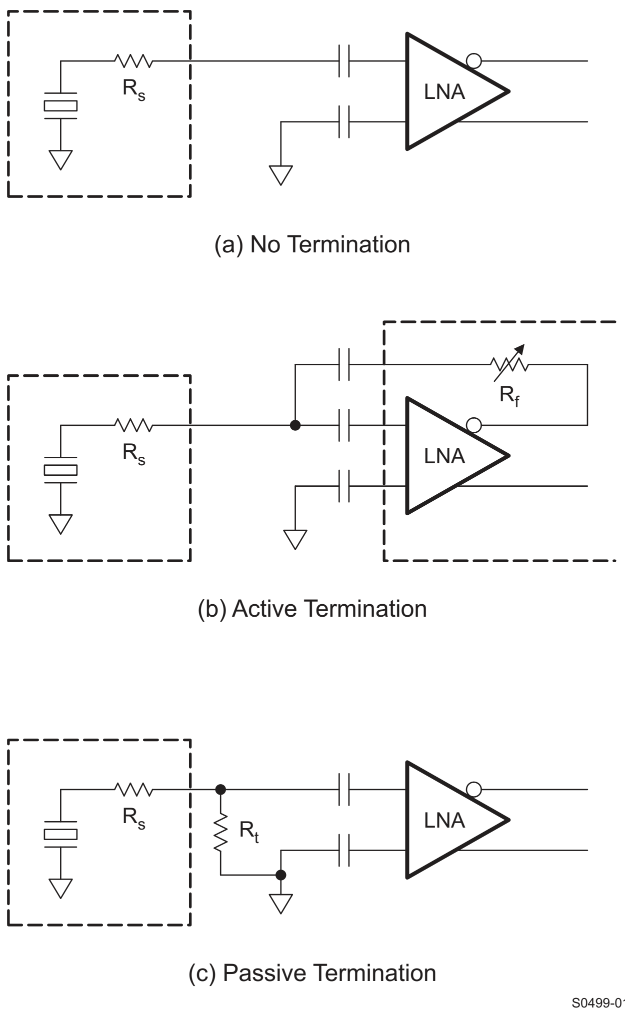


Figure 85. Termination Configurations

Under the no termination configuration, the input impedance of the VCA5807 is about 6KΩ (8K//20pF) at 1 MHz. Passive termination requires external termination resistor Rt, which contributes to additional thermal noise.

The LNA supports active termination with programmable values, as shown in Figure 86 .

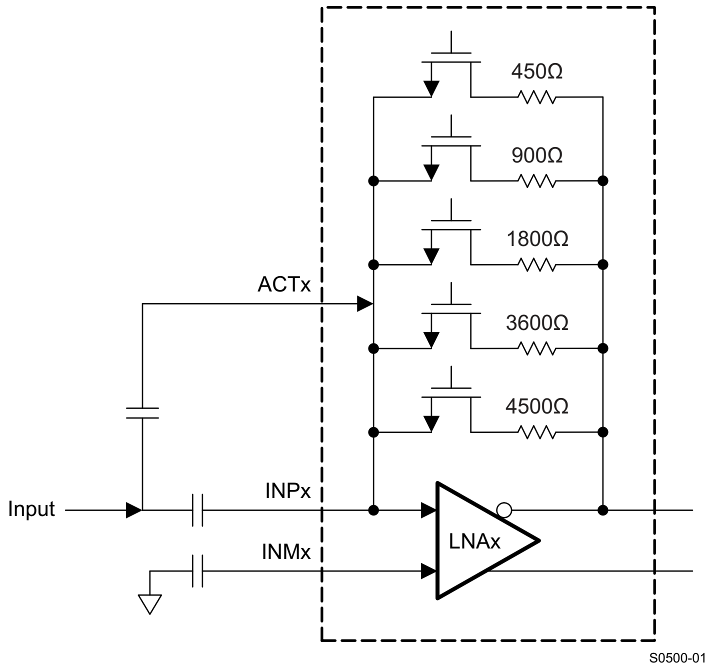


Figure 86. Active Termination Implementation

The VCA5807 has four pre-settings 50,100, 200 and 400Ω which are configurable through the registers. Other termination values can be realized by setting the termination switches shown in Figure 86. Register [52] is used to enable these switches. The input impedance of the LNA under the active termination configuration approximately follows:

$$Z_{IN} = \frac{R_f}{1 + \frac{Av_{LNA}}{2}} \tag{6}$$

Table 2 lists the LNA R_{IN} under different LNA gains. System designers can achieve fine tuning for different probes.

The equivalent input impedance is given by Equation 7 where R_{IN} (8K) and C_{IN} (20pF) are the input resistance and capacitance of the LNA.

$$Z_{IN} = \frac{R_f}{1 + \frac{Av_{LNA}}{2}} // C_{IN} // R_{IN} \tag{7}$$

Therefore, the Z_{IN} is frequency dependent and it decreases as frequency increases shown in Figure 9. Since 2MHz~10MHz is the most commonly used frequency range in medical ultrasound, this rolling-off effect doesn't impact system performance greatly. Active termination can be applied to both CW and TGC modes. Since each ultrasound system includes multiple transducers with different impedances, the flexibility of impedance configuration is a great plus.

Figure 31, Figure 32, and Figure 33 shows the NF under different termination configurations. It indicates that no termination achieves the best noise figure; active termination adds less noise than passive termination. Thus termination topology should be carefully selected based on each use scenario in ultrasound.

LNA Gain Switch Response

The LNA gain is programmable through SPI. The gain switching time depends on the SPI speed as well as the LNA gain response time. During the switching, glitches might occur and they can appear as artifacts in images. LNA gain switching in a single imaging line may not be preferred, although digital signal processing might be used here for glitch suppression.

NOTE

The clamp settings may change during LNA gain switching. The clamp settling time needs to be considered when adjusting LNA gain dynamically, especially when overload signals exceed the clamping voltage.

VOLTAGE-CONTROLLED-ATTENUATOR

The attenuator in the VCA5807 is controlled by a pair of differential control inputs, the $V_{CNTLM/P}$ pins. The differential control voltage spans from 0V to 1.5V. This control voltage varies the attenuation of the attenuator based on its linear-in-dB characteristic. Its maximum attenuation (minimum channel gain) appears at V_{CNTLP} - V_{CNTLM} = 1.5V, and minimum attenuation (maximum channel gain) occurs at V_{CNTLP} - V_{CNTLM} = 0. The typical gain range is 40dB and remains constant, independent of the PGA setting.

When only single-ended V_{CNTL} signal is available, this 1.5Vpp signal can be applied on the V_{CNTLP} pin with the V_{CNTLM} pin connected to ground. As the below figures show, TGC gain curve is inversely proportional to the V_{CNTLP} - V_{CNTLM}.

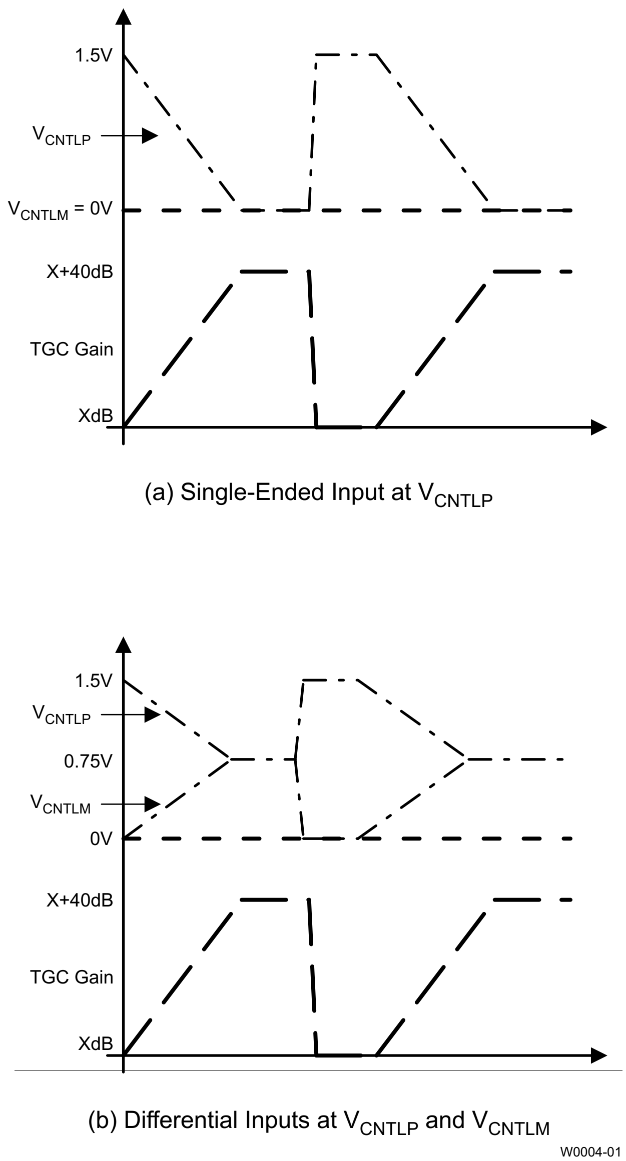


Figure 87. V_{CNTLP} and V_{CNTLM} Configurations

As discussed in the theory of operation, the attenuator architecture uses seven attenuator segments that are equally spaced in order to approximate the linear-in-dB gain-control slope. This approximation results in a monotonic slope; the gain ripple is typically less than ±0.5dB.

The control voltage input ($V_{CNTLM/P}$ pins) represents a high-impedance input. The $V_{CNTLM/P}$ pins of multiple VCA5807 devices can be connected in parallel with no significant loading effects. When the voltage level (V_{CNTLP}-V_{CNTLM}) is above 1.5V or below 0V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level respectively. It is recommended to limit the voltage from -0.3V to 2V.

When the VCA5807 operates in CW mode, the attenuator stage remains connected to the LNA outputs. Therefore, it is recommended to power down the VCAT and PGA using corresponding register bits. In this case, V_{CNTLP}-V_{CNTLM} voltage does not matter.

The VCA5807 gain-control input has a –3dB bandwidth of approximately 800KHz. This wide bandwidth, although useful in many applications (that is, fast V_{CNTL} response), can also allow high-frequency noise to modulate the gain control input and finally affect the Doppler performance. In practice, this modulation can be avoided by additional external filtering (RV_{CNTL} and CV_{CNTL}) at $V_{CNTLM/P}$ pins as Table 9 shows. However, the external filter's cutoff frequency cannot be kept too low as this results in low gain response time. Without external filtering, the gain control response time is typically less than 1 µs to settle within 10% of the final signal level of 1VPP (–6dBFS) output as indicated in Figure 54 and Figure 55.

Typical $V_{CNTLM/P}$ signals are generated by an 8bit to 12bit 10MSPS digital to analog converter (DAC) and a differential operation amplifier. TI's DACs, such as TLV5626 and DAC7821/11 (10MSPS/12bit), could be used to generate TGC control waveforms. Differential amplifiers with output common mode voltage control (that is, THS4130 and OPA1632) can connect the DAC to the $V_{CNTLM/P}$ pins. The buffer amplifier can also be configured as an active filter to suppress low frequency noise. More information can be found in the literatures SLOS318F and SBAA150. The V_{CNTL} vs Gain curves can be found in Figure 2. The below table also shows the absolute gain vs V_{CNTL}at room temperature, which may help program DAC correspondingly.

In PW Doppler and color Doppler modes, V_{CNTL} noise should be minimized to achieve the best close-in phase noise and SNR. Digital V_{CNTL} feature is implemented to address this need in the VCA5807. In the digital V_{CNTL} mode, no external V_{CNTL} is needed.

Table 9. V_{CNTLP} – V_{CNTLM} vs Gain Under Different LNA and PGA Gain Settings (Low Noise Mode and Room Temperature)

V_{CNTLP}–V_{CNTLM} (V)	Gain (dB) LNA = 12 dB PGA = 24 dB	Gain (dB) LNA = 18 dB PGA = 24 dB	Gain (dB) LNA = 24 dB PGA = 24 dB	Gain (dB) LNA = 12 dB PGA = 30 dB	Gain (dB) LNA = 18 dB PGA = 30 dB	Gain (dB) LNA = 24 dB PGA = 30 dB
0	35.8	41.8	47.8	41.6	47.6	53.6
0.1	33.3	39.3	45.3	39.1	45.1	51.1
0.2	30.4	36.4	42.4	36.2	42.2	48.2
0.3	27	33	39	32.8	38.8	44.8
0.4	23.3	29.3	35.3	29.1	35.1	41.1
0.5	20.2	26.2	32.2	26	32	38
0.6	16.6	22.6	28.6	22.4	28.4	34.4
0.7	13	19	25	18.8	24.8	30.8
0.8	9.7	15.7	21.7	15.5	21.5	27.5
0.9	5.7	11.7	17.7	11.5	17.5	23.5
1.0	2.2	8.2	14.2	8	14	20
1.1	-1.2	4.8	10.8	4.6	10.6	16.6
1.2	-3.2	2.8	8.8	2.6	8.6	14.6
1.3	-4.4	1.6	7.6	1.4	7.4	13.4
1.4	-4.7	1.3	7.3	1.1	7.1	13.1
1.5	-4.7	1.3	7.3	1.1	7.1	13.1

PGA OUTPUT CONFIGURATION

As illustrated in Figure 68, the PGA current clamping circuit can be enabled (register 51) to improve the overload recovery performance of the VCA. If we measure the standard deviation of the output just after overload, for 0.5V V_{CNTL}, it is about 3.2 LSBs in normal case, that is, the output is stable in about 1 clock cycle after overload. With the current clamp circuit disabled, the value approaches 4 LSBs meaning a longer time duration before the output stabilizes; however, with the current clamp circuit enabled, there will be degradation in HD3 for PGA output levels > -2dBFS. For example, for a –2dBFS output level, the HD3 degrades by approximately 3dB. In order to maximize the output dynamic range, the maximum PGA output level can exceed 2Vpp (0 dBFS linear output range) with the clamp circuit. Thus ADCs with excellent overload recovery performance should be selected.

NOTE

In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0

Figure 82 and Figure 83 show that the PGA outputs can be further processed by either high speed 12-14 Bit ADCs or operational amplifiers. The selection of ADCs or OPAMPs shall minimize performance impact of the VCA5807, that is, selecting devices with significant lower input noise floor compared to VCA5807's output noise. TI's multi-channel high-speed ADCs, such as ADS5294 and ADS5292 and low noise opamps OPA842 and THS4130, are suitable candidates. In portable applications, lower power ADCs and OPAMPs may be selected. The impact on performance degradation can be predicted by comparing the VCA5807 output noise to the total noise of VCA5807 and its subsequent device.

The below figures show the SNR curves when VCA5807 is sampled by ADS5294. Better than 70dBFS SNR is achieved. Further improvement is expected when a 16-bit ADC, e.g. ADS5263, is used.

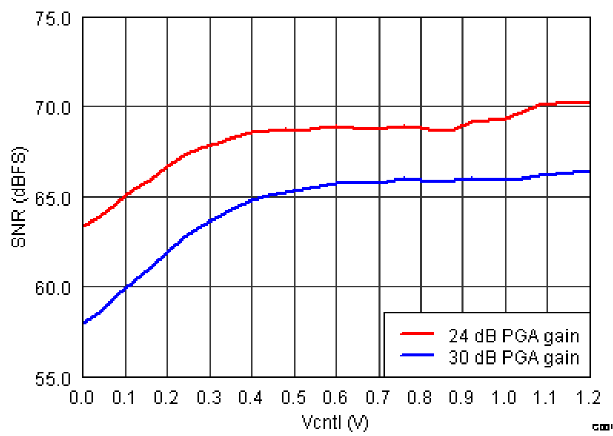


Figure 88. SNR vs Gain at PGA Low Noise Mode

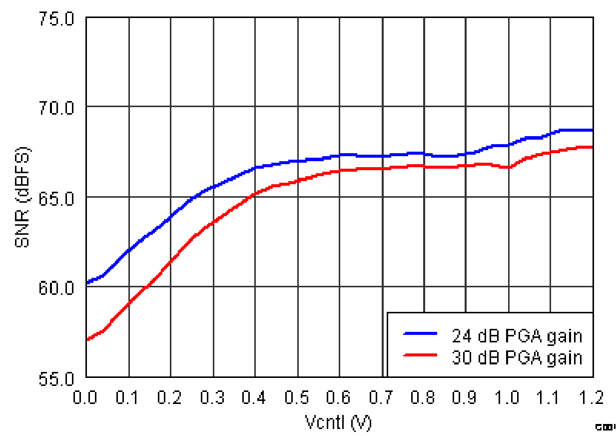


Figure 89. SNR vs Gain at PGA Low Power Mode

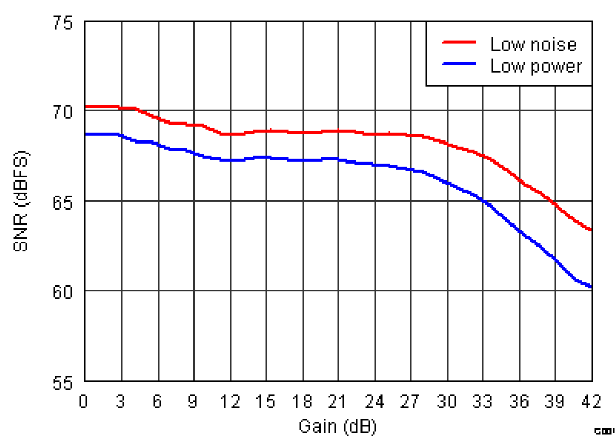


Figure 90. SNR vs Gain vs Power Modes at 24dB PGA

LOW FREQUENCY SUPPORT

The signal chain of the VCA5807 can handle signal frequency lower than 100 KHz, which enables the VCA5807 to be used not only in medical ultrasound applications but also in sonar applications. The PGA integrator has to be turned off in order to enable the low frequency support. Meanwhile, a large capacitor like 1 µF can be used for setting low corner frequency of the LNA DC offset correction circuit as shown in Figure 65. VCA5807's low frequency response can be found in Figure 61.

CW CONFIGURATION

CW Summing Amplifier

In order to simplify CW system design, a summing amplifier is implemented in the VCA5807 to sum and convert 8-channel mixer current outputs to a differential voltage output. Low noise and low power are achieved in the summing amplifier while maintaining the full dynamic range required in CW operation.

This summing amplifier has 5 internal gain adjustment resistors which can provide 32 different gain settings (register 54[4:0], Figure 86 and Table 4). System designers can easily adjust the CW path gain depending on signal strength and transducer sensitivity. For any other gain values, an external resistor option is supported. The gain of the summation amplifier is determined by the ratio between the 500Ω resistors after LNA and the internal or external resistor network $R_{EXT/INT}$. Thus the matching between these resistors plays a more important role than absolute resistor values. Better than 1% matching is achieved on chip. Due to process variation, the absolute resistor tolerance could be higher. If external resistors are used, the gain error between I/Q channels or among multiple VCAs may increase. It is recommended to use internal resistors to set the gain in order to achieve better gain matching (across channels and multiple VCAs). With the external capacitor C_{EXT} , this summing amplifier has 1st order LPF response to remove high frequency components from the mixers, such as 2f0±fd. Its cut-off frequency is determined by:

$$f_{HP} = \frac{1}{2\pi R_{INT/EXT} C_{EXT}} \tag{8}$$

Note that when different gain is configured through register 54[4:0], the LPF response varies as well.

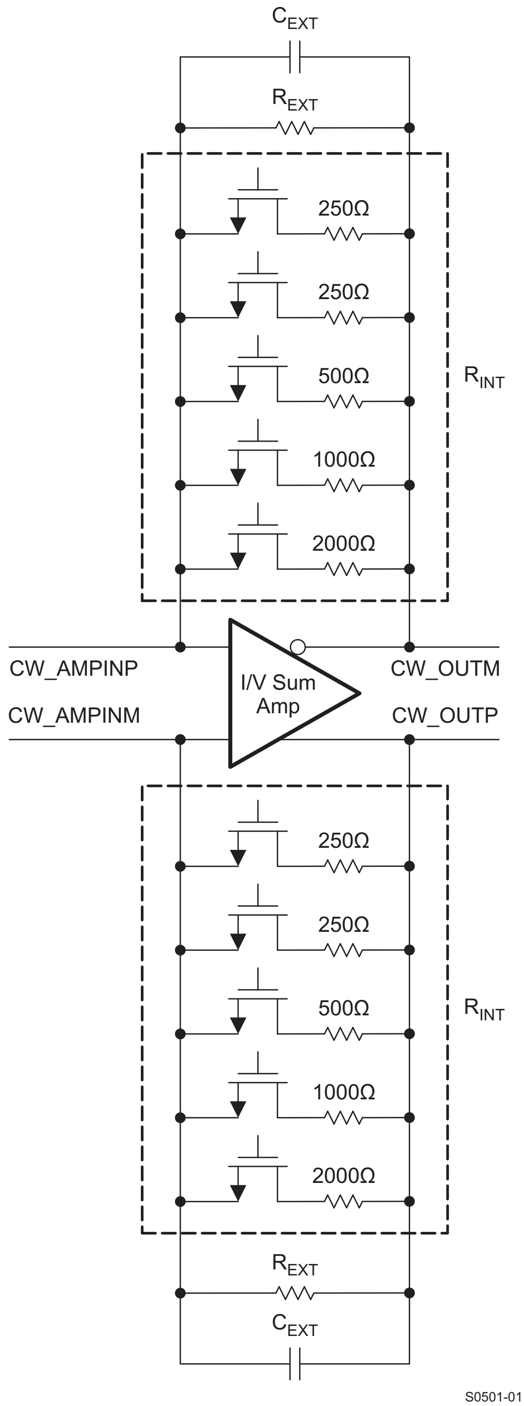


Figure 91. CW Summing Amplifier Block Diagram

Multiple VCA5807s are usually utilized in parallel to expand CW beamformer channel count. These VCA5807s' CW outputs can be summed and filtered externally further to achieve desired gain and filter response. AC coupling capacitors C_{AC} are required to block DC component of the CW carrier signal. C_{AC} can vary from 1uF to 10s μF depending on the desired low frequency Doppler signal from slow blood flow. Multiple VCA5807s' I/Q outputs can be summed together with a low noise external differential amplifiers before 16/18-bit differential audio ADCs. Ultralow noise differential precision amplifier OPA1632 and THS4130 can be considered.

An alternative current summing circuit is shown in Figure 93. However this circuit only achieves good performance when a lower noise operational amplifier is available compared to the VCA5807's internal summing differential amplifier.

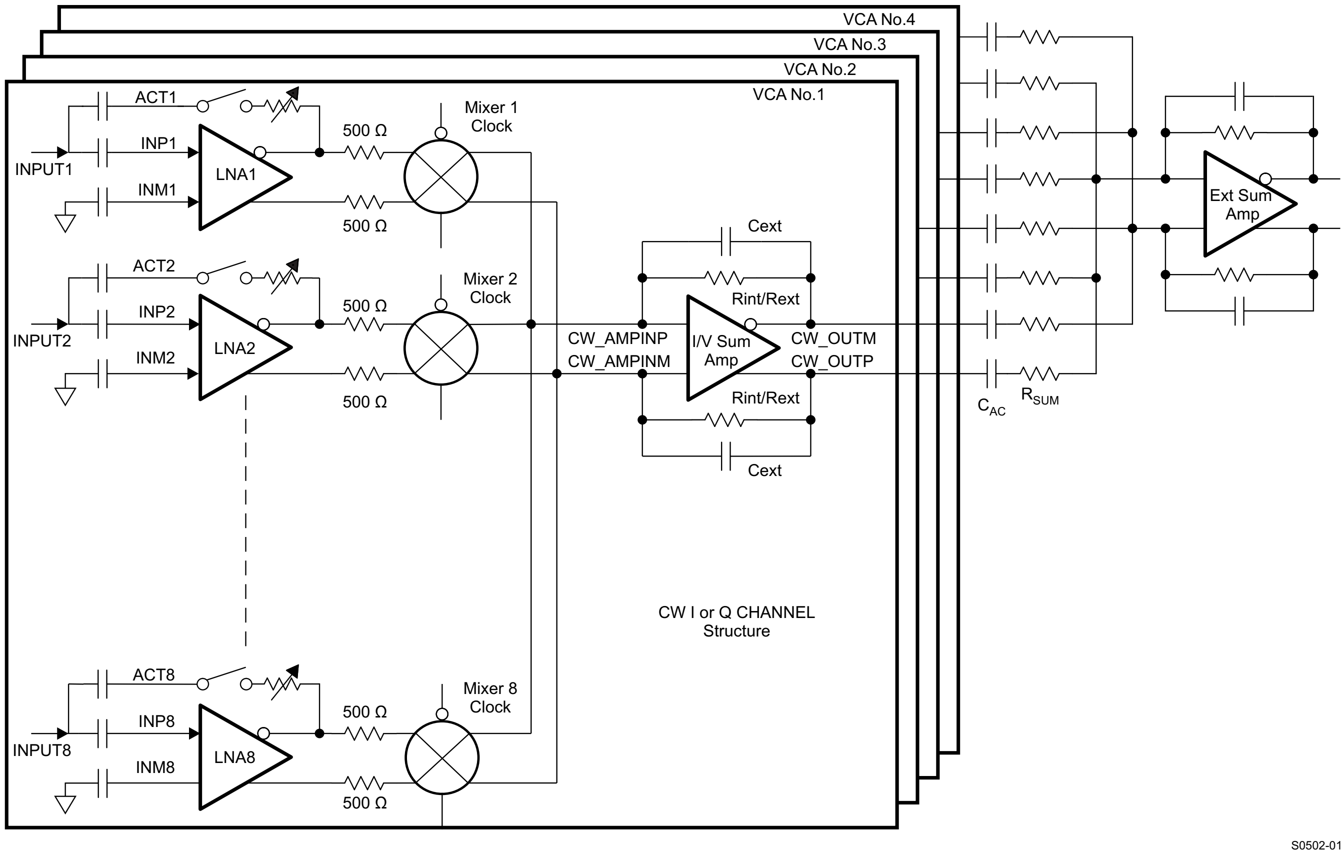


Figure 92. CW circuit with Multiple VCA5807s (Voltage output mode)

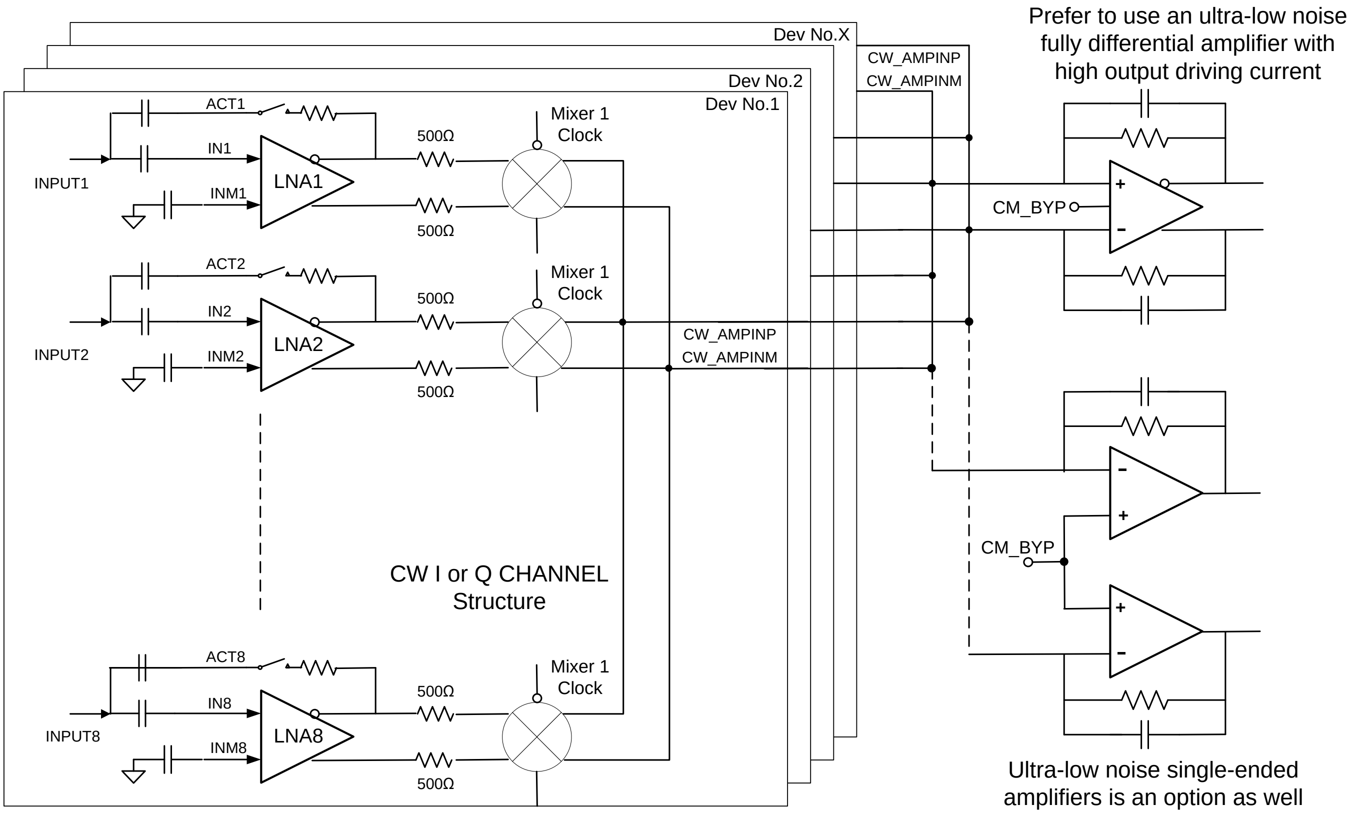


Figure 93. CW Circuit with Multiple VCA5807s (Current output mode)

The CW I/Q channels are well matched internally to suppress image frequency components in Doppler spectrum. Low tolerance components and precise operational amplifiers should be used for achieving good matching in the external circuits as well.

CW Clock Selection

The VCA5807 can accept differential LVDS, LVPECL, and other differential clock inputs as well as single-ended CMOS clock. An internally generated VCM of 2.5V is applied to CW clock inputs, that is, CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X. Since this 2.5V VCM is different from the one used in standard LVDS or LVPECL clocks, AC coupling is required between clock drivers and the VCA5807 CW clock inputs. When CMOS clock is used, CLKM_1X and CLKM_16X should be tied to ground. Common clock configurations are illustrated in Figure 94. Appropriate termination is recommended to achieve good signal integrity.

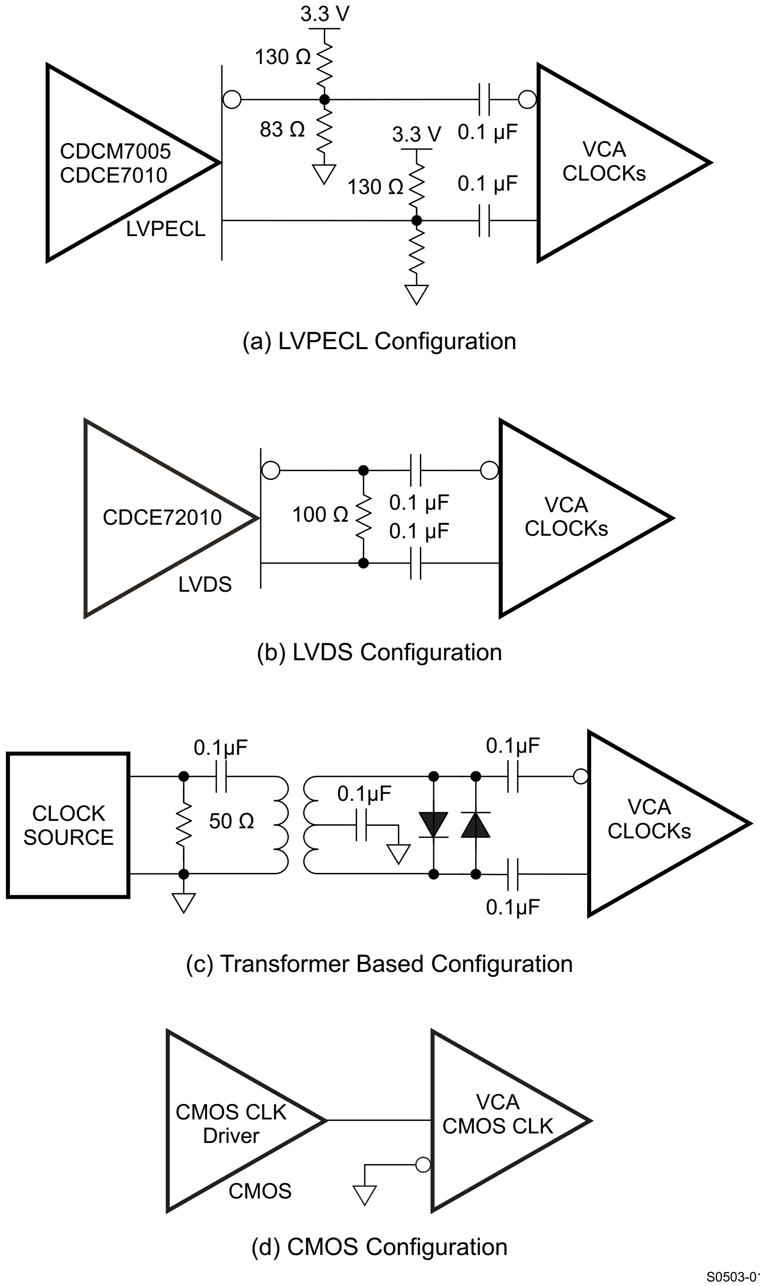


Figure 94. Clock Configurations

The combination of the clock noise and the CW path noise can degrade the CW performance. The internal clocking circuit is designed for achieving excellent phase noise required by CW operation. The phase noise of the VCA5807 CW path is better than 155dBc/Hz at 1KHz offset. Consequently the phase noise of the mixer clock inputs needs to be better than 155dBc/Hz.

In the 16, 8, 4 × f_{cw} operations modes, low phase noise clock is required for 16, 8, 4 × f_{cw} clocks (that is, CLKP_16X/ CLKM_16X pins) in order to maintain good CW phase noise performance. The 1 × f_{cw} clock (that is, CLKP_1X/ CLKM_1X pins) is only used to synchronize the multiple VCA5807 chips and is not used for demodulation. Thus 1 f_{cw} clock's phase noise is not a concern. Either a continue clock with a frequency of f_{cw} or a single pulse with a width >1/(Nf_{cw}) can be used.

On the other hand, in the 1 × f_{cw} operation mode, low phase noise clocks are required for both CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X pins since both of them are used for mixer demodulation. In general, higher slew rate clock has lower phase noise; thus clocks with high amplitude and fast slew rate are preferred in CW operation. In the CMOS clock mode, 5V CMOS clock can achieve the highest slew rate.

Clock phase noise can be improved by a divider as long as the divider's phase noise is lower than the target phase noise. The phase noise of a divided clock can be improved approximately by a factor of $20\log_{10}N$ dB where N is the dividing factor of 16, 8, or 4. If the target phase noise of mixer LO clock 1 × f_{cw} is 160dBc/Hz at 1KHz off carrier, the 16 × f_{cw} clock phase noise should be better than $160-20\log_{10}16$ = 136dBc/Hz. TI's jitter cleaners **LMK048X**/CDCM7005/CDCE72010 exceed this requirement and can be selected for the VCA5807. In the 4X/1X modes, higher quality input clocks are expected to achieve the same performance since N is smaller. Thus the 16X mode is a preferred mode since it reduces the phase noise requirement for system clock design. In addition, the phase delay accuracy is specified by the internal clock divider and distribution circuit. In the 16X operation mode, the CW operation range is limited to 8 MHz due to the 16X CLK. The maximum clock frequency for the 16X CLK is 128 MHz. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance, e.g. the phase noise is degraded by 9 dB at 15 MHz, compared to 2 MHz.

As the channel number in a system increases, clock distribution becomes more complex. It is not preferred to use one clock driver output to drive multiple VCAs since the clock buffer's load capacitance increases by a factor of N. As a result, the falling and rising time of a clock signal is degraded. A typical clock arrangement for multiple VCA5807s is illustrated in Figure 95. Each clock buffer output drives one VCA5807 in order to achieve the best signal integrity and fastest slew rate, that is, better phase noise performance. When clock phase noise is not a concern, thai is. the 1 × f_{cw} clock in the 32, 16, 8, 4 × f_{cw} operation modes, one clock driver output may excite more than one VCA5807s. Nevertheless, special considerations should be applied in such a clock distribution network design. In typical ultrasound systems, it is preferred that all clocks are generated from a same clock source, such as 16 × f_{cw} , 1 × f_{cw} clocks, audio ADC clocks, RF ADC clock, pulse repetition frequency signal, frame clock and so on. By doing this, interference due to clock asynchronization can be minimized

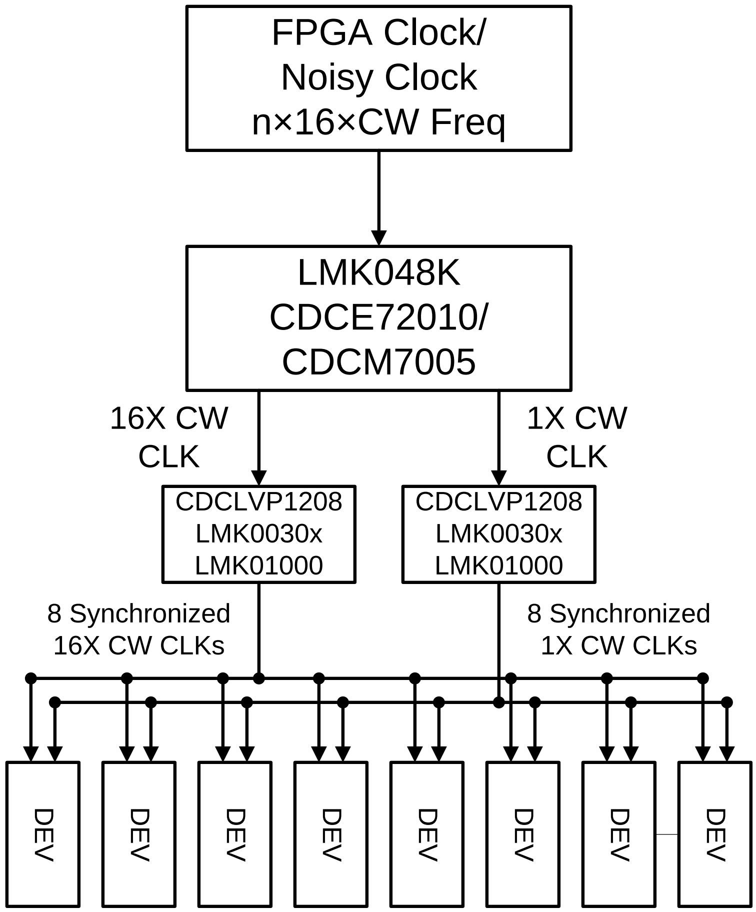


Figure 95. CW Clock Distribution

CW Supporting Circuits

As a general practice in CW circuit design, in-phase and quadrature channels should be strictly symmetrical by using well matched layout and high accuracy components.

In systems, additional high-pass wall filters (20Hz to 500Hz) and low-pass audio filters (10KHz to 100KHz) with multiple poles are usually needed. Since CW Doppler signal ranges from 20Hz to 20KHz, noise under this range is critical. Consequently low noise audio operational amplifiers are suitable to build these active filters for CW post-processing, that is, OPA1632, OPA2211, LME49990, LMH6629, or THS4130 . More filter design techniques can be found from www.ti.com. TI's active filter design tool http://focus.ti.com/docs/toolsw/folders/print/filter-designer.html

The filtered audio CW I/Q signals are sampled by audio ADCs and processed by DSP or PC. Although CW signal frequency is from 20 Hz to 20 KHz, higher sampling rate ADCs are still preferred for further decimation and SNR enhancement. Due to the large dynamic range of CW signals, high resolution ADCs (≥16bit) are required, such as ADS8413 (2MSPS/16it/92dBFS SNR) and ADS8472 (1MSPS/16bit/95dBFS SNR). ADCs for in-phase and quadature-phase channels must be strictly matched, not only amplitude matching but also phase matching, in order to achieve the best I/Q matching,. In addition, the in-phase and quadrature ADC channels must be sampled simultaneously.

POWER MANAGEMENT

Power/Performance Optimization

The VCA5807 has options to adjust power consumption and meet different noise performances. This feature would be useful for portable systems operated by batteries when low power is more desired. Please refer to characteristics information listed in the table of electrical characteristics as well as the typical characteristic plots.

Power Management Priority

Power management plays a critical role to extend battery life and ensure long operation time. The VCA5807 has fast and flexible power down/up control which can maximize battery life. The VCA5807 can be powered down/up through external pins or internal registers. The following table indicates the affected circuit blocks and priorities when the power management is invoked. In the device, all the power down controls are logically ORed to generate final power down for different blocks. Thus, the higher priority controls can cover the lower priority ones. The VCA5807 register settings are maintained when the VCA5807 is in either partial power down mode or complete power down mode.

Table 10. Power Management Priority

	Name	Blocks	Priority
Pin	PDN_GLOBAL	All	High
Pin	PDN_FAST	LNA + VCAT+ PGA	Medium
Register	VCA_PARTIAL_PDN	LNA + VCAT+ PGA	Low
Register	VCA_COMPLETE_PDN	LNA + VCAT+ PGA	Medium
Register	PDN_VCAT_PGA	VCAT + PGA	Lowest
Register	PDN_LNA	LNA	Lowest

Partial Power-Up/Down Mode

The partial power up/down mode is also called as fast power up/down mode. In this mode, most amplifiers in the signal path are powered down, while the internal reference circuits remain active.

The partial power down function allows the VCA5807 to be wake up from a low-power state quickly. This configuration ensures that the external capacitors are discharged slowly; thus a minimum wake-up time is needed as long as the charges on those capacitors are restored. The VCA wake-up response is typically about 2 µs or 1% of the power down duration whichever is larger. The longest wake-up time depends on the capacitors connected at INP and INM, as the wake-up time is the time required to recharge the caps to the desired operating voltages. For 0.1µF at INP and 15nF at INM can give a wake-up time of 2.5ms. For larger capacitors this time will be longer. Thus, the VCA5807 wake-up time is more dependent on the VCA wake-up time. The power-down time is instantaneous, less than 1µs.

This fast wake-up response is desired for portable ultrasound applications in which the power saving is critical. The pulse repetition frequency of a ultrasound system could vary from 50KHz to 500Hz, while the imaging depth (that is, the active period for a receive path) varies from 10 µs to hundreds of us. The power saving can be significant when a system's PRF is low. In some cases, only the VCA would be powered down while the ADC keeps running normally to ensure minimum impact to FPGAs.

In the partial power-down mode, the VCA5807 typically dissipates only 12.5 mW/ch, representing a >80% power reduction compared to the normal operating mode. This mode can be set using either pin PDN_FAST or register bit VCA_PARTIAL_PDN.

Complete Power-Down Mode

To achieve the lowest power dissipation of 0.7 mW/CH, the VCA5807 can be placed into a complete power-down mode. This mode is controlled through the registers VCA_COMPLETE_PDN or PDN_GLOBAL pin. In the complete power-down mode, all circuits including reference circuits within the VCA5807 are powered down; and the capacitors connected to the VCA5807 are discharged. The wake-up time depends on the time needed to recharge these capacitors. The wake-up time depends on the time that the VCA5807 spends in shutdown mode. 0.1µF at INP and 15nF at INM can give a wake-up time close to 2.5ms.

Power Saving in CW Mode

Usually only half the number of channels in a system are active in the CW mode. Thus the individual channel control through VCA_PDN_CH <7:0> can power down unused channels and save power consumption greatly. Under the default register setting in the CW mode, the voltage controlled attenuator, PGA, is still active. During the debug phase, both the PW and CW paths can be running simultaneously. In real operation, these blocks need to be powered down manually.

TEST MODES

When direct probing VCA outputs is not feasible, the VCA5807 has a test mode in which the CH7 and CH8 PGA outputs can be brought to the CW pins. By monitoring these CW pins, the functionality of VCA operation can be verified. The PGA outputs are connected to the virtual ground pins of the summing amplifier (CW_IP_AMPINM/P, CW_QP_AMPINM/P) through 5KΩ resistors. The PGA outputs can be monitored at the summing amplifier outputs when the LPF capacitors C_{EXT} are removed. Note that the signals at the summing amplifier outputs are attenuated due to the 5KΩ resistors. The attenuation coefficient is $R_{INT/EXT}$/5KΩ

If users would like to check the PGA outputs without removing CEXT, an alternative way is to measure the PGA outputs directly at the CW_IP_AMPINM/P and CW_QP_AMPINM/P when the CW summing amplifier is powered down

Some registers are related to this test mode. PGA Test Mode Enable: Reg59[9]; Buffer Amplifier Power Down Reg59[8]; and Buffer Amplifier Gain Control Reg54[4:0]. Based on the buffer amplifier configuration, the registers can be set in different ways:

Configuration 1:

In this configuration, the test outputs can be monitored at CW_AMPINP/M

Reg59[9]=1 ;Test mode enabled

Reg59[8]=0 ;Buffer amplifier powered down

Configuration 2:

In this configuration, the test outputs can be monitored at CW_OUTP/M

Reg59[9]=1 ;Test mode enabled

Reg59[8]=1 ;Buffer amplifier powered on

Reg54[4:0]=10H; Internal feedback 2K resistor enabled. Different values can be used as well

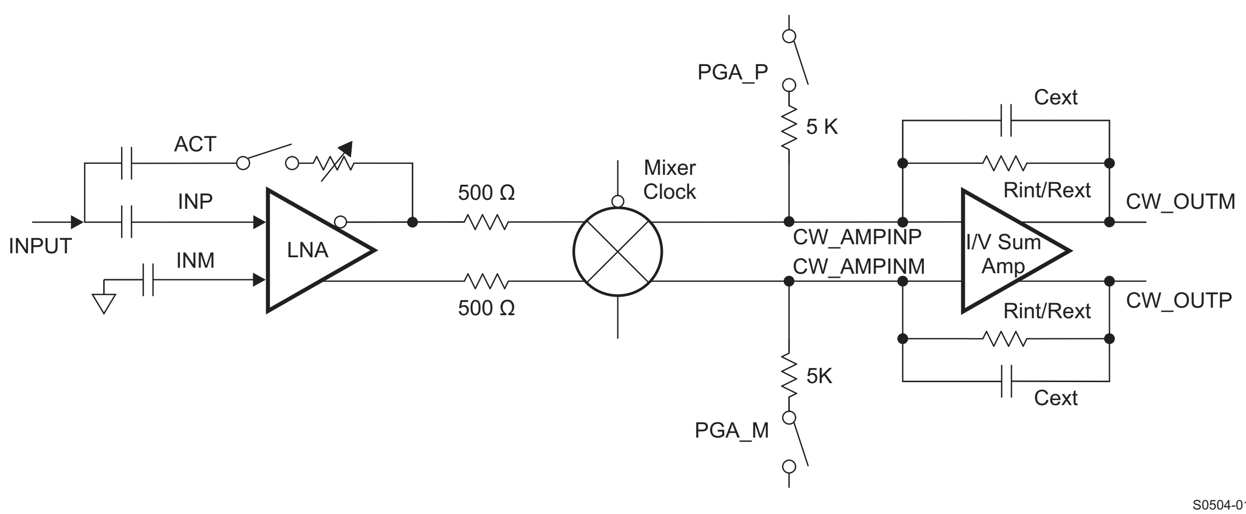


Figure 96. VCA5807 PGA Test Mode

POWER SUPPLY, GROUNDING AND BYPASSING

In a mixed-signal system design, power supply and grounding design plays a significant role. In most cases, it should be adequate to lay out the printed circuit board (PCB) to use a single ground plane for the VCA5807. Care should be taken that this ground plane is properly partitioned between various sections within the system to minimize interactions between analog and digital circuitry. In addition, optical isolator or digital isolators, such as ISO7240, can separate the analog portion from the digital portion completely. Consequently they prevent digital noise to contaminate the analog portion. Table 10 lists the related circuit blocks for each power supply.

Table 11. Supply vs Circuit Blocks

Power Supply	Ground	Circuit Blocks
AVDD (3.3VA)	AVSS	LNA, attenuator, PGA with clamp and BPF, reference circuits, CW summing amplifier, CW mixer, VCA SPI
AVDD_5V (5VA)	AVSS	LNA, CW clock circuits, reference circuits

All bypassing and power supplies for the VCA5807 should be referenced to their corresponding ground planes. All supply pins should be bypassed with 0.1µF ceramic chip capacitors (size 0603 or smaller). In order to minimize the lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors 2.2µF to 10µF, effective at lower frequencies) may also be used on the main supply pins. These components can be placed on the PCB in proximity (< 0.5 in or 12.7 mm) to the VCA5807 itself.

The VCA5807 has a number of reference supplies needed to be bypassed, such CM_BYP, VHIGH, and VREF_IN. These pins should be bypassed with at least 1µF; higher value capacitors can be used for better low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors (size 0402, > 1µF) and place them as close as possible to the device pins.

High-speed mixed signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer/drivers. For the VCA5807, care has been taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimum amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductance of the supply and ground pins leads to improved noise suppression. For this reason, multiple pins are used to connect each supply and ground sets. It is important to maintain low inductance properties throughout the design of the PCB layout by use of proper planes and layer thickness.

BOARD LAYOUT

Proper grounding and bypassing, short lead length, and the use of ground and power-supply planes are particularly important for high-frequency designs. Achieving optimum performance with a high-performance device such as the VCA5807 requires careful attention to the PCB layout to minimize the effects of board parasitics and optimize component placement. A multilayer PCB usually ensures best results and allows convenient component placement.

In addition, appropriate delay matching should be considered for the CW clock path, especially in systems with high channel count. For example, if clock delay is half of the 16x clock period, a phase error of 22.5°C could exist. Thus the timing delay difference among channels contributes to the beamformer accuracy.

To avoid noise coupling through supply pins, it is recommended to keep sensitive input pins, such as INM, INP, ACT pins always from the AVDD 3.3 V and AVDD 5V planes. For example, either the traces or vias connected to these pins should NOT be routed across the AVDD 3.3 V and AVDD 5V planes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VCA5807PZP	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	VCA5807	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

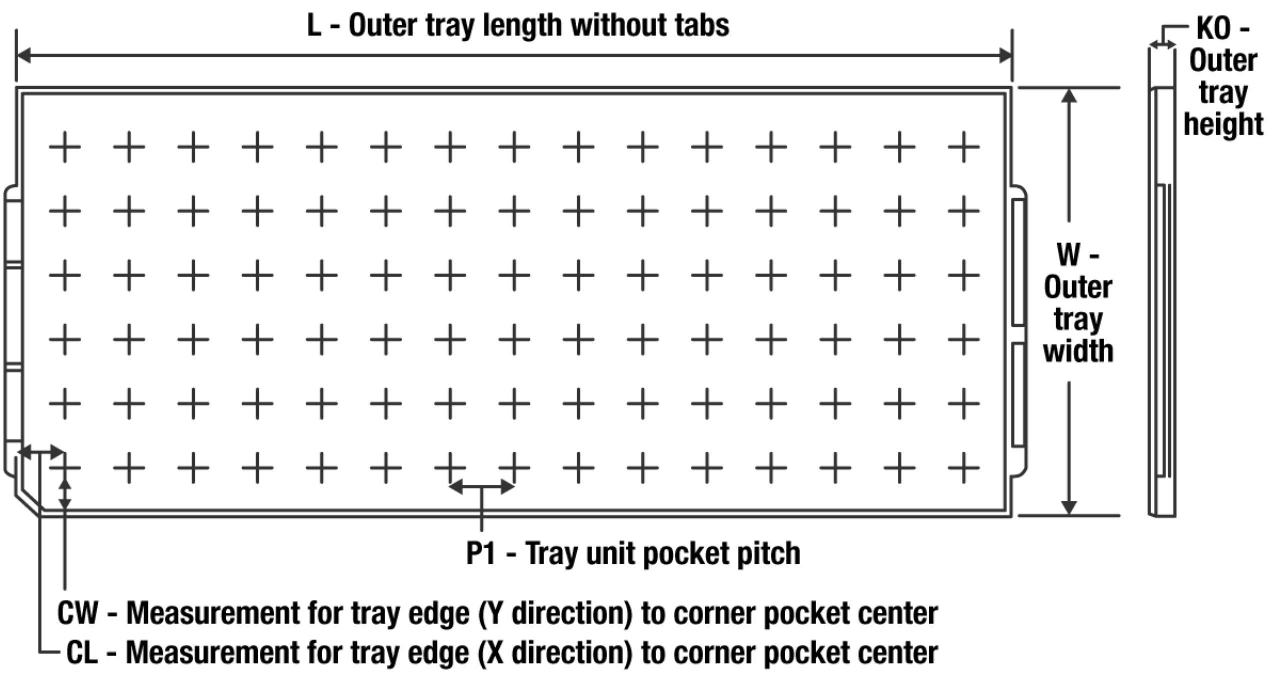
[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
VCA5807PZP	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45

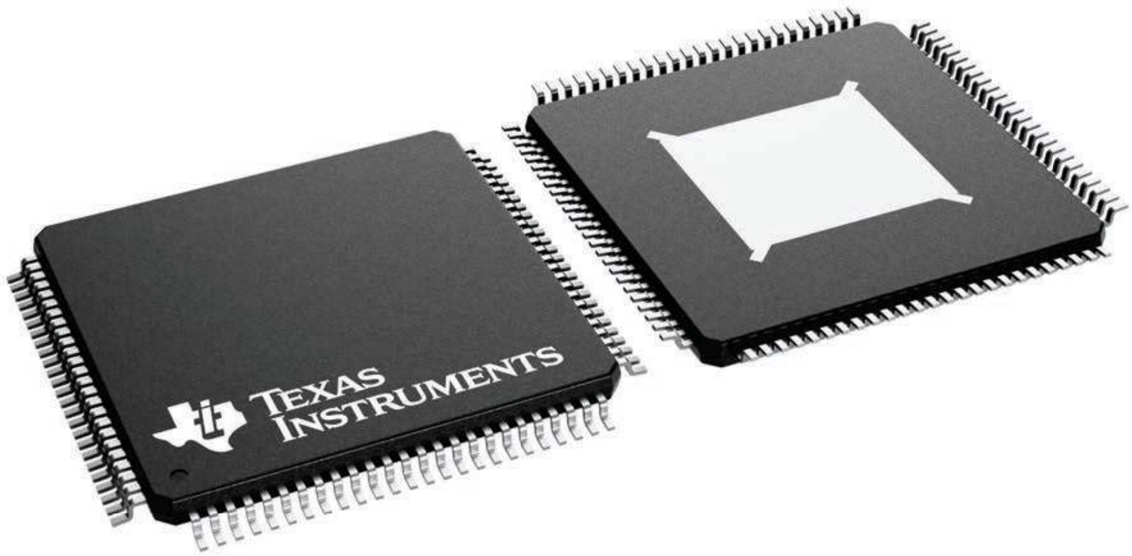
PZP 100

PowerPAD ™ TQFP - 1.2 mm max height

14 x 14 mm Pkg Body, 0.5 mm pitch
16 x 16 mm Pkg Area

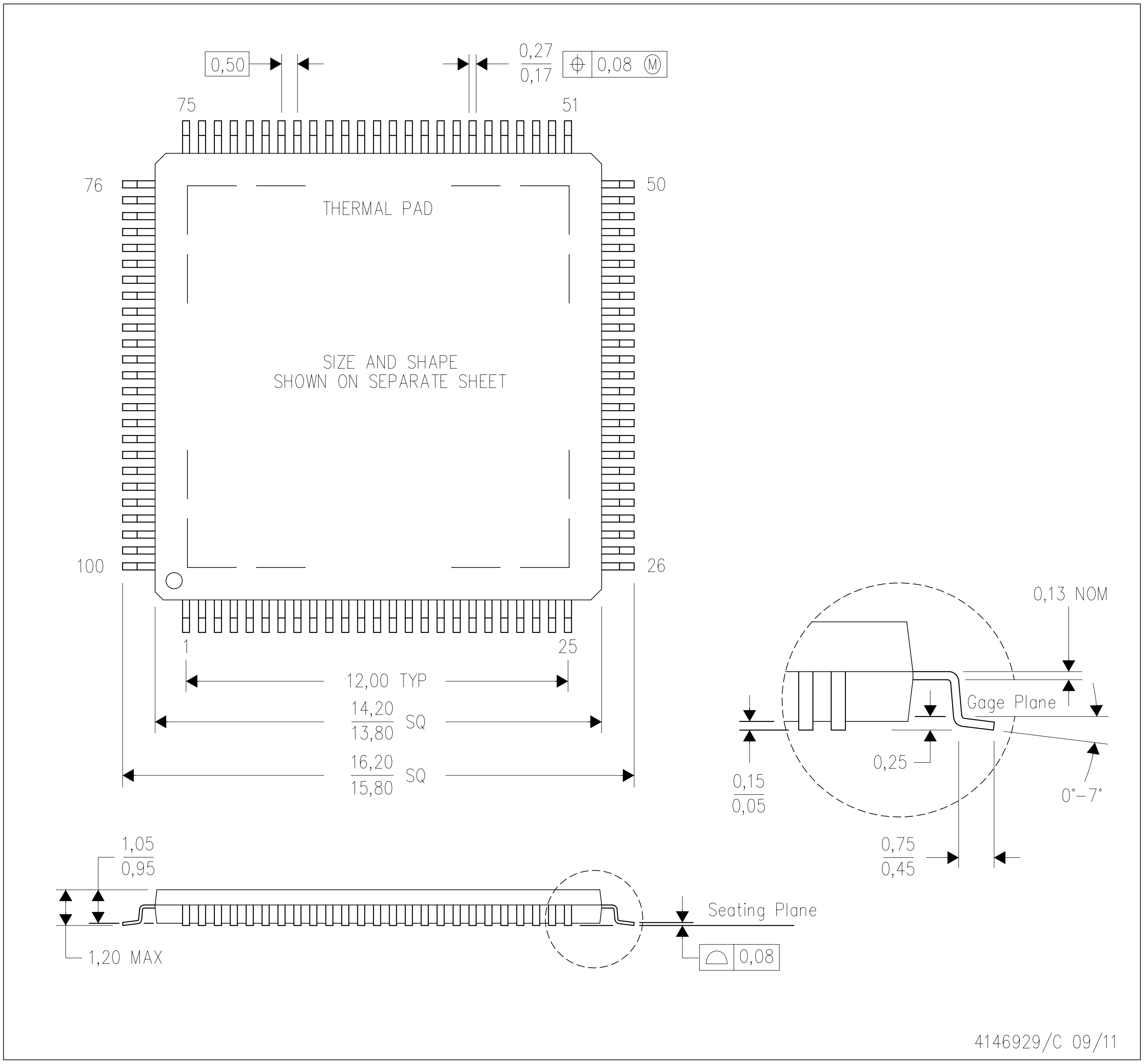
PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224739/B

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

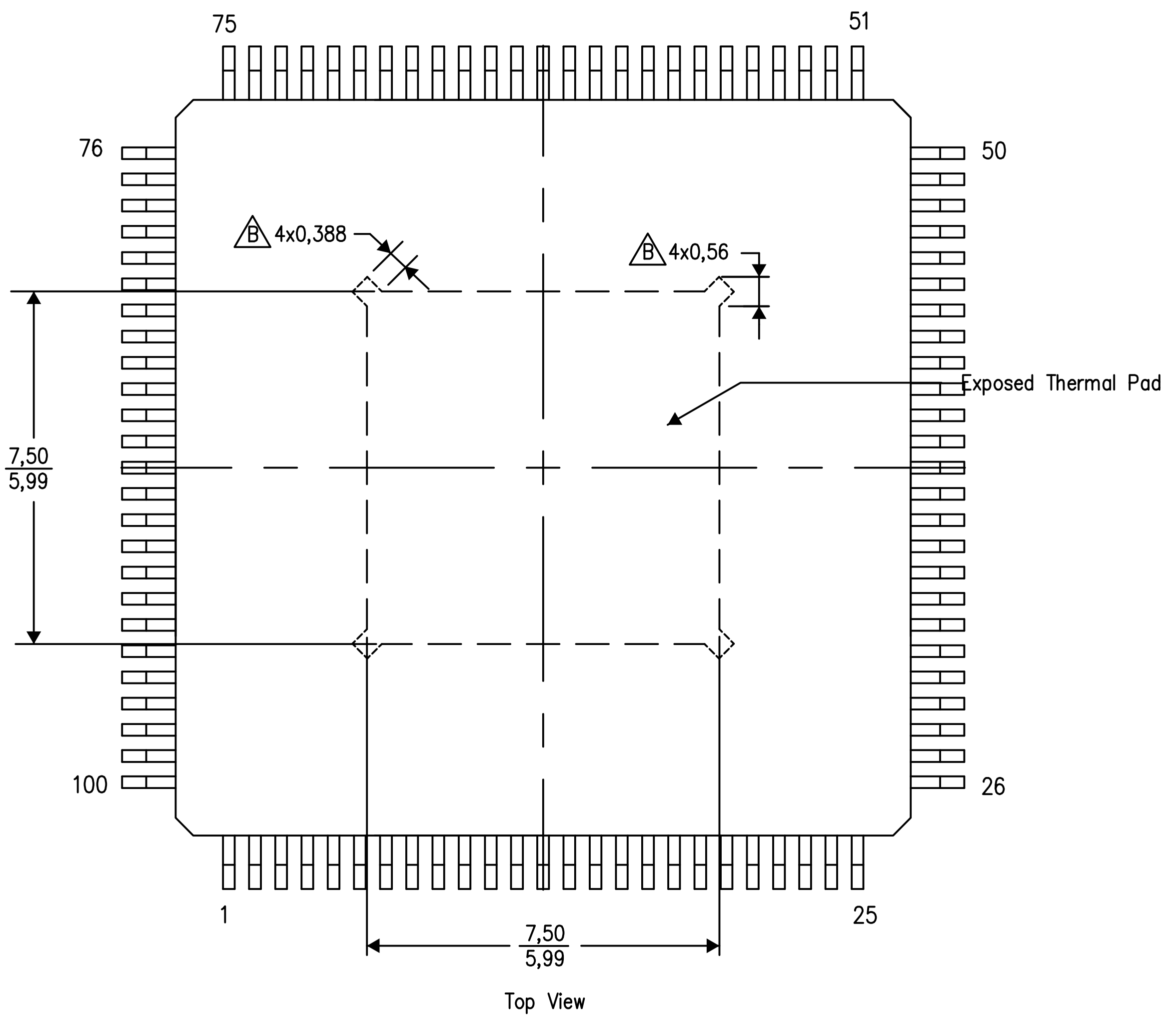
PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

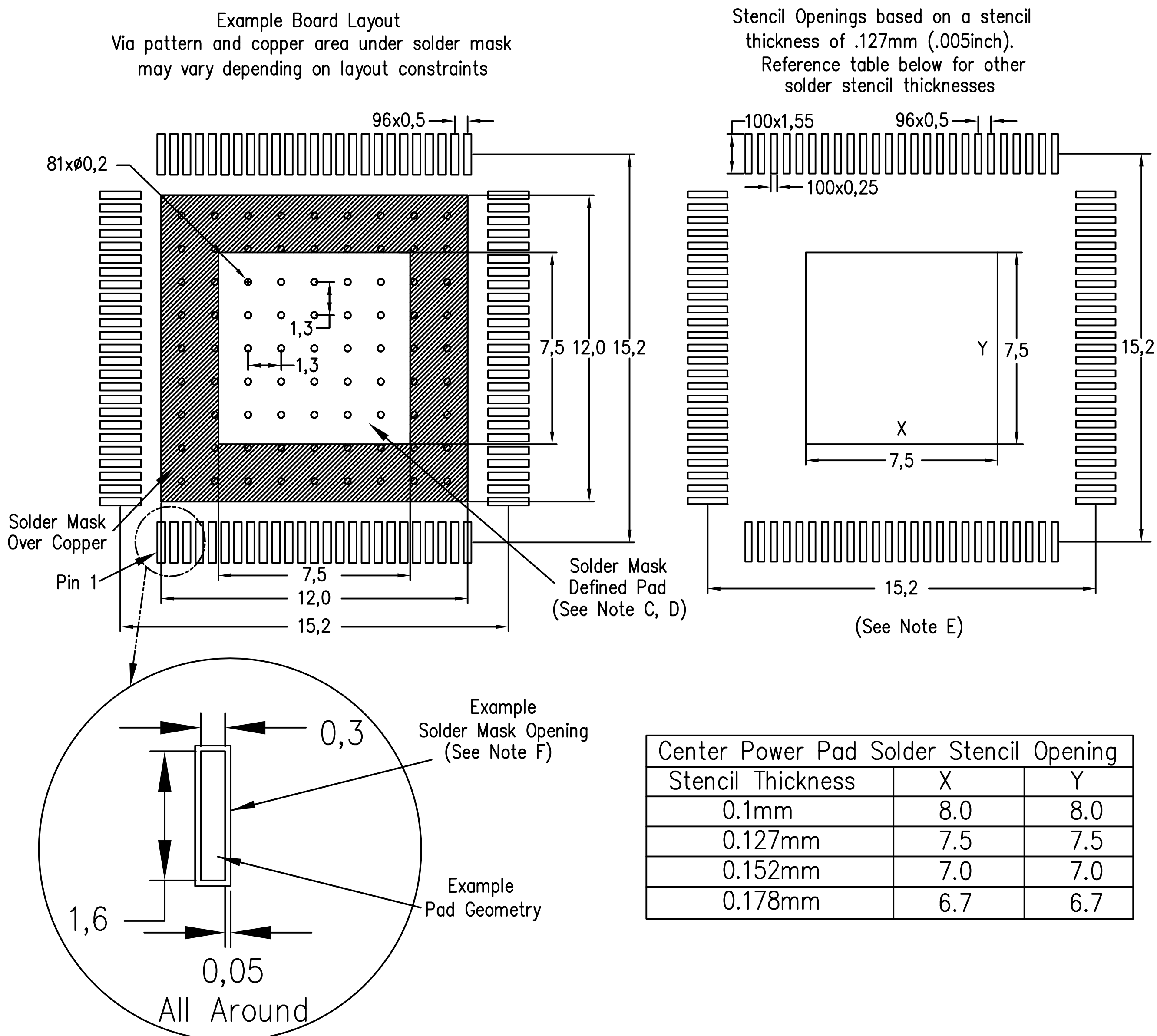
4206333–4/L 05/14

NOTE: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PZP (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	8.0	8.0
0.127mm	7.5	7.5
0.152mm	7.0	7.0
0.178mm	6.7	6.7

4209826-7/C 01/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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