Three Phase Sensorless Sinusoidal Fan Driver

FEATURES AND BENEFITS

- Standby mode
- Sensorless operation
- Low-noise sinusoidal modulation
- Quiet startup
- Low R_{DSON} power MOSFETs
- Minimal external components
- PWM speed input
- FG speed output
- Lock detection
- Soft start
- Short-circuit protection (OCP)
- Overcurrent limit (OCL)

PACKAGES:

10-lead SSOP (suffix LN)

10-lead eSOIC with exposed thermal pad (suffix LK)

Not to scale

DESCRIPTION

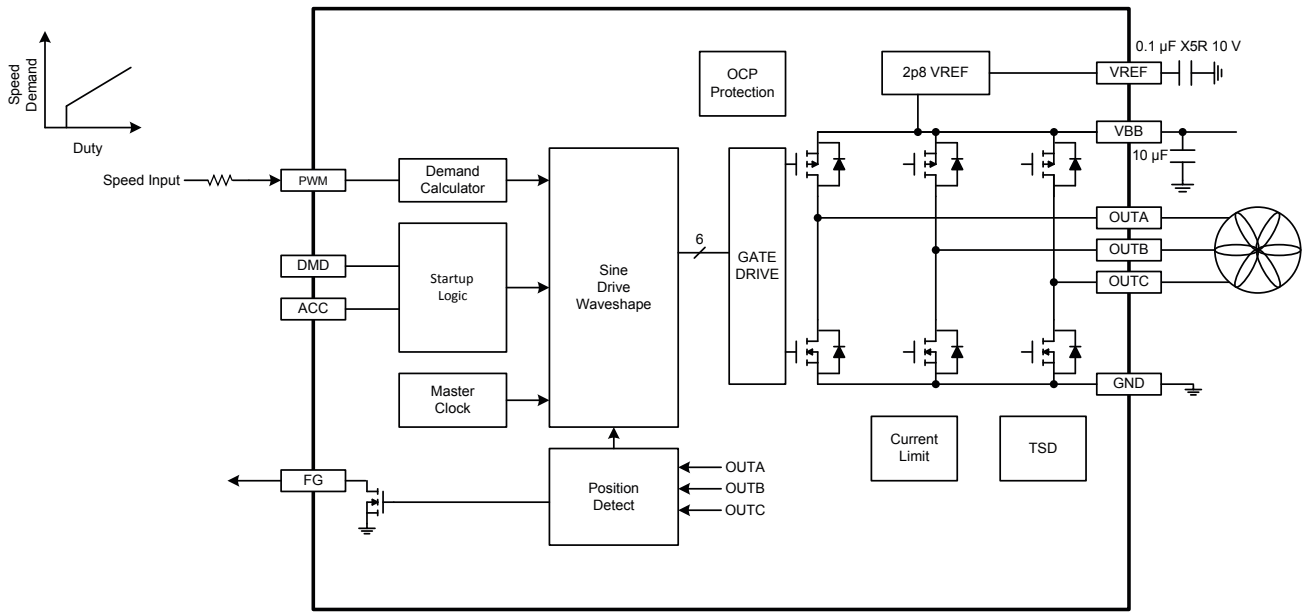
The A5936 three phase motor driver incorporates sinusoidal drive to minimize vibration for fan applications.

A sinusoidal voltage profile is applied to the windings of the motor at startup to quickly and quietly start up and gradually ramp up the motor to desired speed.

The motor speed is controlled by applying a duty cycle command to the PWM input. The PWM input is allowed to operate over a wide frequency range.

The A5936 is available in a 10-lead SSOP (suffix LN), and a 10-lead eSOIC with exposed power pad (suffix LK). The packages are lead (Pb) free, with 100% matte-tin leadframe plating.

TYPICAL APPLICATION



SELECTION GUIDE

Part Number	Ambient Temperature Range	Packing	Package
A5936GLKTR-T	–40°C to 105°C	3000 pieces per 13-inch reel	10-lead eSOIC with exposed thermal pad
A5936GLNTR-T	–40°C to 105°C	3000 pieces per 13-inch reel	10-lead SSOP

ABSOLUTE MAXIMUM RATINGS

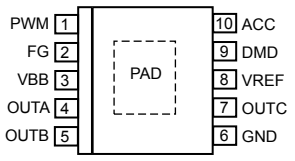
Characteristic	Symbol	Notes	Value	Unit
Supply Voltage	V_{BB}	t_w < 10 ms	20	V
			18	V
Logic Input Voltage Range	V_{IN}	PWM, DMD	–0.3 to 6	V
Logic Output	V_O	FG	V_{BB}	V
Analog Input Range	V_{IN}	ACC	–0.3 to V_{REF}	V
Output Current	I_{OUT}		I_{OCL}	A
Output Voltage	V_{OUT}	OUTA, OUTB, OUTC	V_{BB} + 1	V
Operating Temperature Range	T_A	G temperature range	–40 to 105	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS

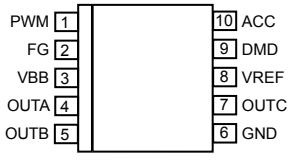
Characteristic	Symbol	Package	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LK	2-sided PCB with 1 in.^{2} copper	35	°C/W
		LN	2-sided PCB with 1 in.^{2} copper	100	°C/W

Terminal List Table

Name	Pin Number		Function
	LN	LK	
PWM	1	1	Logic input – speed demand
FG	2	2	Output signal
VBB	3	3	Input supply
OUTA	4	4	Motor terminal
OUTB	5	5	Motor terminal
GND	6	6	Ground
OUTC	7	7	Motor terminal
VREF	8	8	Reference voltage output
DMD	9	9	Logic input
ACC	10	10	Analog input
PAD	–	PAD	Thermal pad



Package LK Pinouts



Package LN Pinouts

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ELECTRICAL CHARACTERISTICS: Valid at T_A = 25°C, V_{BB} = 5 to 16 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Supply Current	I_{BB}	Active Mode (PWM duty < DC_ON)	–	7.5	10	mA
	I_{BBS}	Standby Mode	–	<1	10	µA
VREF Output Voltage	V_{REF}	I = 0 to 5 mA	2.85	2.9	2.95	V
Logic Input Low Level	V_{IL}		0.8	–	–	V
Logic Input High Level	V_{IH}		–	–	2	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Input Current (DMD, PWM, ACC)	I_{IN}		–10	<1	10	µA
Output Saturation Voltage (FG)	V_{SAT}	I = 5 mA	–	–	0.3	V
Output Leakage (FG)	I_{FG}	V = 16 V, PWM = Low	–	–	5	µA
POWER DRIVER						
Total Driver On-Resistance (Sink + Source)	$R_{DS(on)}$	I = 1 A, T_J = 25°C, V_{BB} = 8 V	–	1	1.25	Ω
		Source driver	–	650	–	mΩ
		Sink driver	–	350	–	mΩ
		I = 1 A, T_J = 25°C, V_{BB} = 4 V	–	–	2	Ω
Motor PWM Frequency	f_{PWMOUT}		23.4	24.4	25.4	kHz
PWM Duty Cycle Range	f_{PWMIN}		0.1	–	100	kHz
Duty Cycle On Threshold	DC_{ON}		–	10	–	%
Duty Cycle Off Threshold	DC_{OFF}		–	7.4	–	%
ACC Accuracy	V_{ACC}	Relative to Parameter Table Target	–40	–	40	mV
PROTECTION						
Lock Protection	t_{OFF}		4.8	5	5.2	s
VBB Undervoltage Lockout (UVLO)	V_{BBUVLO}	V_{BB} rising	–	4.7	4.9	V
		V_{BB} falling	–	3.85	3.95	V
VBB UVLO Hysteresis	$V_{BBUVLOHYS}$		–	850	–	mV
Overcurrent Limit	I_{OCL}		1.5	2	3	A
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	35	–	°C

Note 1: Specified limits are tested at a single temperature and assured across the operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The A5936 targets fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds.

The speed of the fan can be controlled by voltage mode (control of power supply amplitude) or variable duty cycle PWM input. Use of the PWM input allows overall system cost savings by eliminating the requirement of an external variable power supply. Operation down to 4 V can be achieved to allow the IC to fit into legacy systems with voltage mode operation.

The PWM input is measured and converted to a 9-bit number. This 9-bit "demand" is applied to a PWM generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120-degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

A BEMF detection "window" is opened on phase A modulation profile to measure the rotor position so as to define the modulation timing. The control system maintains the window to a small level to minimize the disturbance and approximate the ideal sinusoidal current waveform as much as possible.

Protection features include lock detection with restart, overcurrent limit, motor output short circuit, supply undervoltage monitor, and thermal shutdown.

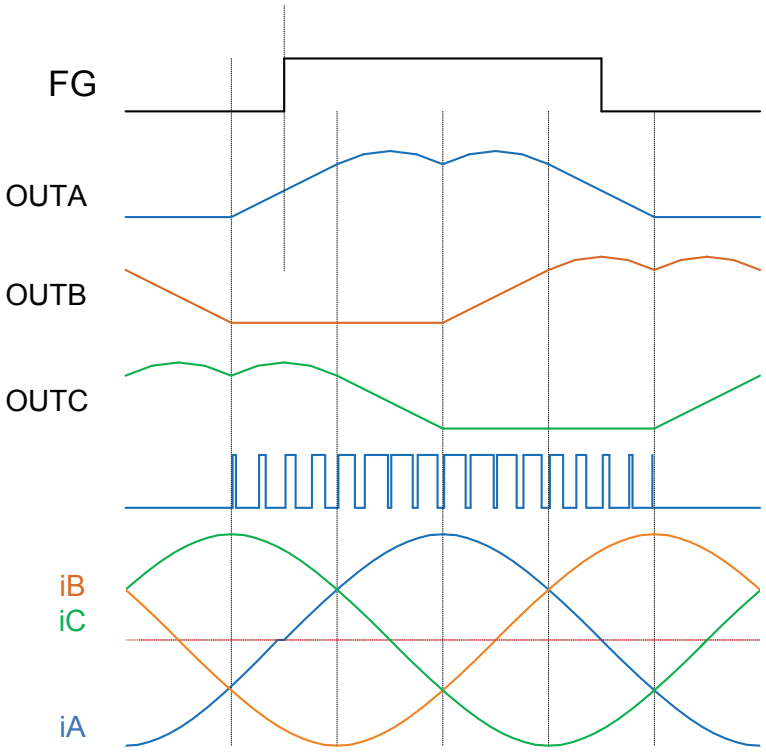

Figure 1: Sinusoidal PWM

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Lock Detect. Speed is monitored to determine if rotor is locked. If a lock condition is detected, the IC will be disabled for t_{OFF} before an auto-restart is attempted.

Standby Mode. Standby mode can be achieved by holding PWM pin low for longer than the Lock off-time. The IC powers up in standby mode. Standby mode is released after a short pulse (>1 µs) is applied to PWM pin. During standby mode, V_{REF} is powered down to allow minimum current draw.

FG. Open-drain output provides speed information to the system. For the default setting, FG changes state one period per electrical revolution of the motor (as shown in Figure 1).

Current Limit. Load current is monitored on the low-side MOSFET. If the current has reached I_{OCL}, the source drivers will turn off for the remaining time of the PWM cycle.

ACC. Startup setting selection (see Startup section).

DMD. Startup setting selection (see Startup section).

PWM. A duty cycle measurement circuit converts the applied duty to a demand value (9-bit resolution) to control speed of the fan. The motor drive will be enabled if duty is larger than DC_ON. The PWM input is filtered to prevent spurious noise from turning on or off unexpectedly.

Power Supply Modulation. Speed can be controlled simply by varying the power supply voltage. Motor drive will be enabled and disabled at undervoltage rising and falling thresholds. To use this method of speed control, pullup PWM pin to VBB with 50 kΩ resistor.

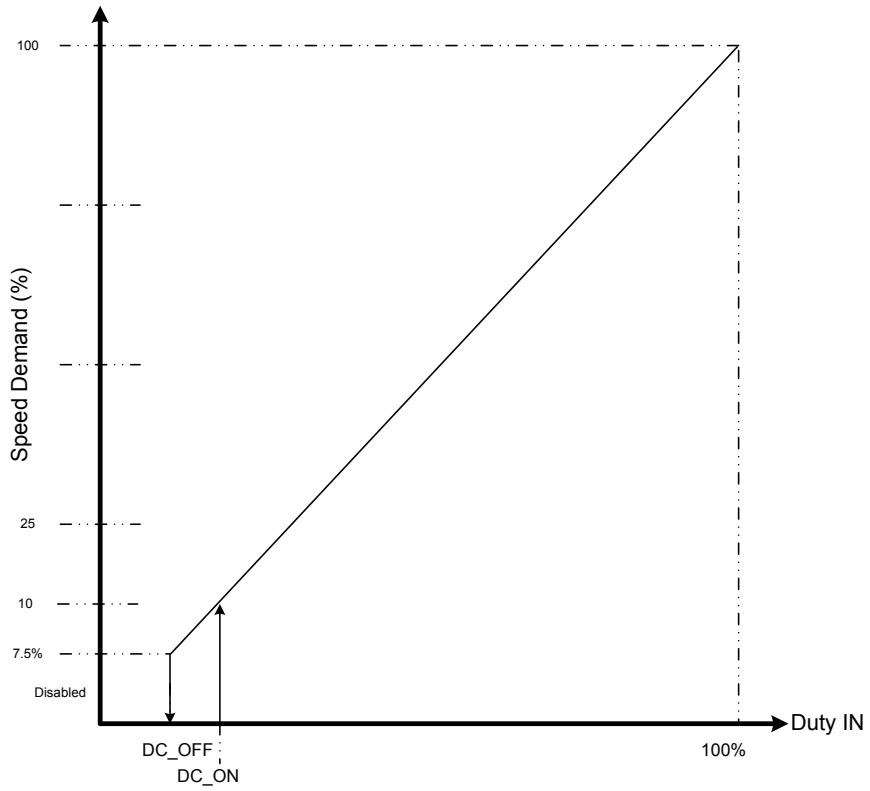

Figure 2: PWM Speed Input Characteristic

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Quiet Startup Operation

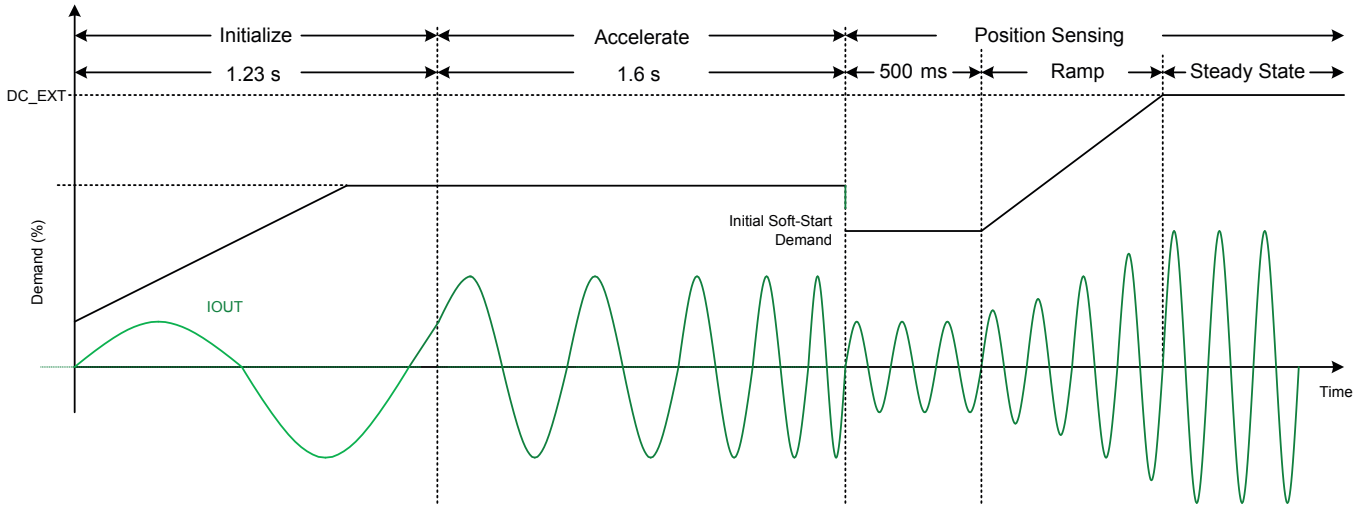

Figure 3: Applied Demand (Modulated Voltage) and Resultant (I_{OUT}) Typical Wave During Startup

A5936 achieves quiet startup with the following sequence:

1. The Demand value is selected by combination of logic level on DMD voltage applied to pin ACC.
2. Slowly ramp PWM duty from low value to a chosen Open-Loop Demand level by applying one cycle of sine drive at frequency of 812 mHz.
3. Ramp up frequency of open-loop sinusoidal modulation for 1.6 s. The acceleration value is selected by voltage applied to pin ACC.
4. Switch to position measurement mode, and apply an initial soft-start demand level of 51% of the level applied during acceleration stage.
5. Hold the PWM duty at same level for 500 ms. This short delay helps the motor synchronize.
6. Ramp up duty to final value:

   A. Time to ramp to final value depends on initial demand (V_{INIT}), V_{BB}, and applied input duty (DC_EXT).

   B. The ramp rate is 15 ms/count for duty < 25% and 7.5 ms/count for duty cycles > 25%

   Example:

   V_{BB} = 12 V, V_{INIT} = 6 V, DC_EXT = 80%

   Initial Soft-Start Demand = [(V_{INIT}/V_{BB}) × 51%] = 25.5% → Counts = 511 × 25.5% = 130

   DC_EXT = 80% → Counts = 511 × 80% = 409

   T_RAMP = (409 – 130) × 7.5 ms/count → 2 s

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Startup Adjustment

Various permutations of startup parameters are chosen via lookup table with A/D conversion.

Sixteen choices of startup parameters are selected by applying voltage at pin ACC.

Choose resistor divider ratio from the table below. The circuit compensates for minor variation of V_{REF}. It is recommended to select R1+R2 in range 10 to 200 kΩ. ACC must be connected to a voltage between VREF and GND and should not be left open circuit.

The parameters are loaded at power-on. When testing, V_{BB} must be powercycled to check new values.

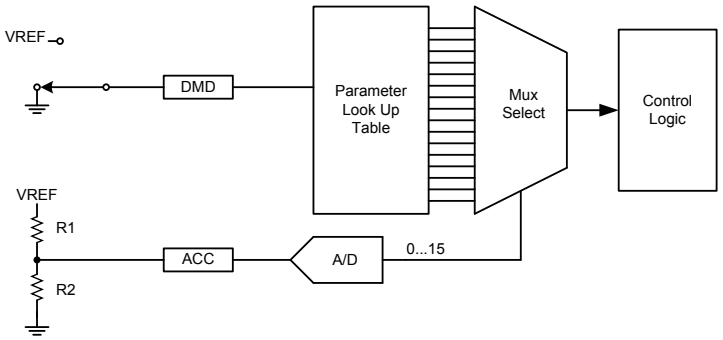

Figure 4

ACC	Resistor Ratio (R2/R1+R2)	Code	Standard Values (kΩ) R1	Standard Values (kΩ) R2	Acceleration (Hz/s)	V_{INIT} (V) During Open Loop (DMD = HI)	V_{INIT} (V) During Open Loop (DMD = LO)	Max. Electrical Frequency (Hz)
GND	n/a	0	n/a	n/a	3.1	6	3	500
0.322	0.112	1	90.9	11.5	5.1	6	3	500
0.644	0.223	2	34.8	10	7	6	3	500
0.966	0.335	3	102	51.1	9	6	3	500
1.288	0.446	4	9.09	11.5	10.9	6	3	500
1.610	0.558	5	9.09	11.5	14.8	6	3	500
1.932	0.669	6	11.5	23.2	18.8	6	3	500
2.254	0.781	7	2.8	10	26.6	6	3	500
V_{REF}	n/a	8	n/a	n/a	26.6	2	1	1000

Note: ACC Target voltages based on V_{REF} of 2.885 V

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APPLICATION INFORMATION

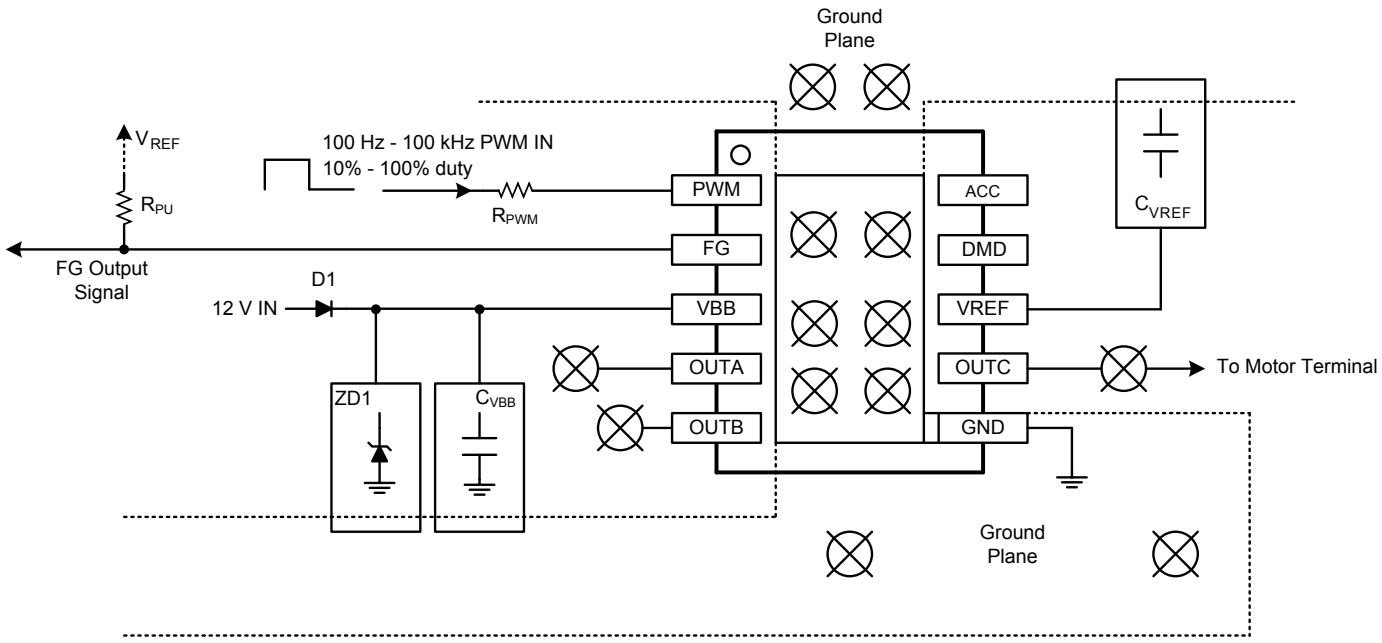

Figure 5: Typical Application Circuit

Name	Suggested Value	Comment
C_{VREF}	0.1 µF, X5R, 10 V	Ceramic capacitor required
C_{VBB}	4.7 to 47 µF	Power Supply Stabilization – Electrolytic or ceramic OK.
R_{FG}	10 kΩ	Optional – pullup resistor for speed feedback
D1	Not Installed	May be required to isolate motor from system or for reverse polarity protection
ZD1	SMBJ14A	Optional TVS to limit maximum V_{BB} due to transients due to motor generation or power line. Suggested to clamp below 18 V (EX: Fairchild SMBJ14A). Typically required if blocking diode D1 is used.
R_{PWM}	1 kΩ	Optional – If PWM wired to connector – R_{PWM} will isolate IC pin from noise or overvoltage transients.

Layout Notes

1. Add thermal vias to exposed pad area.
2. Add ground plane on top and bottom of PCB.
3. Place C_{VREF} and C_{VBB} as close as possible to IC , connected to GND plane.

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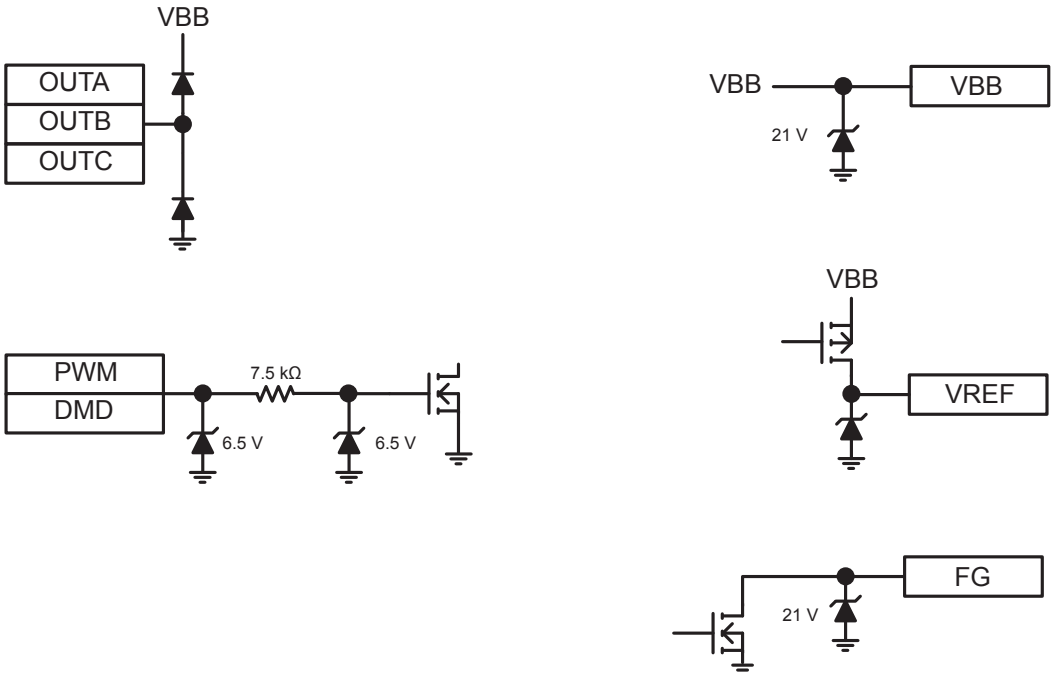
PIN DIAGRAMS



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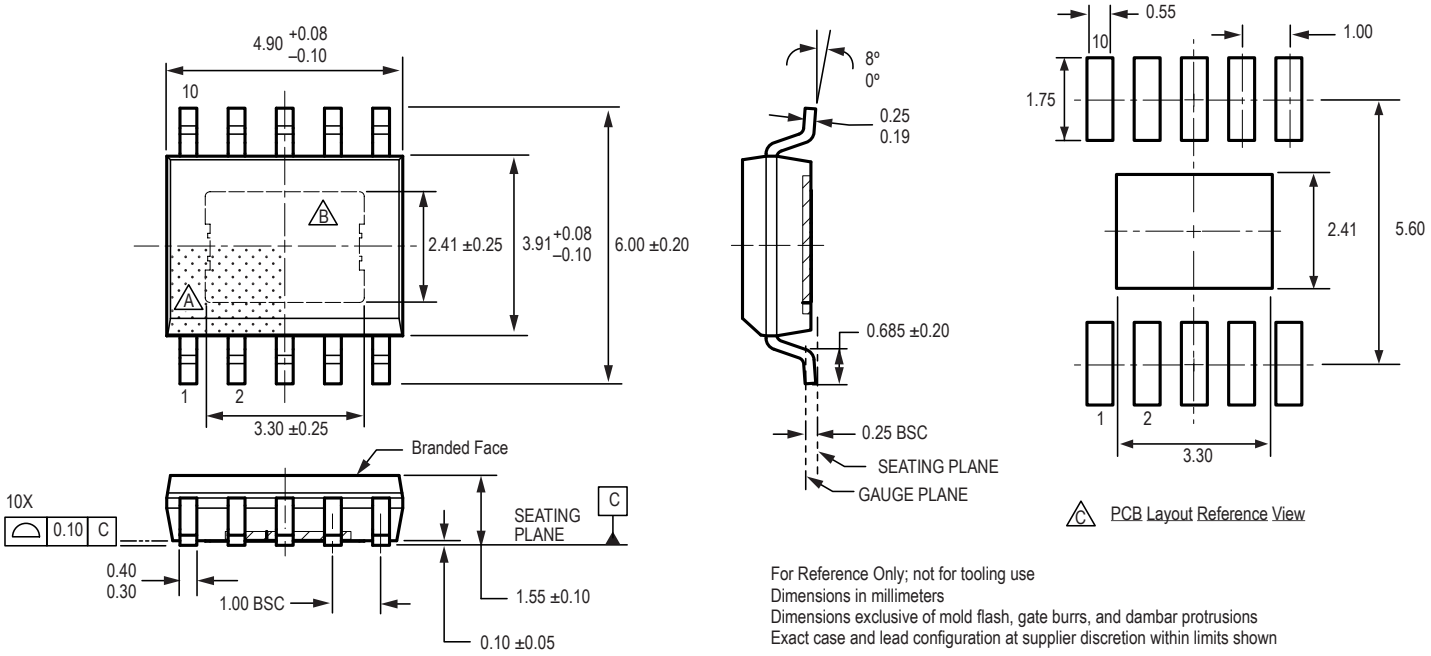
Package LK, 10-Lead eSOIC with Exposed Pad



For Reference Only; not for tooling use
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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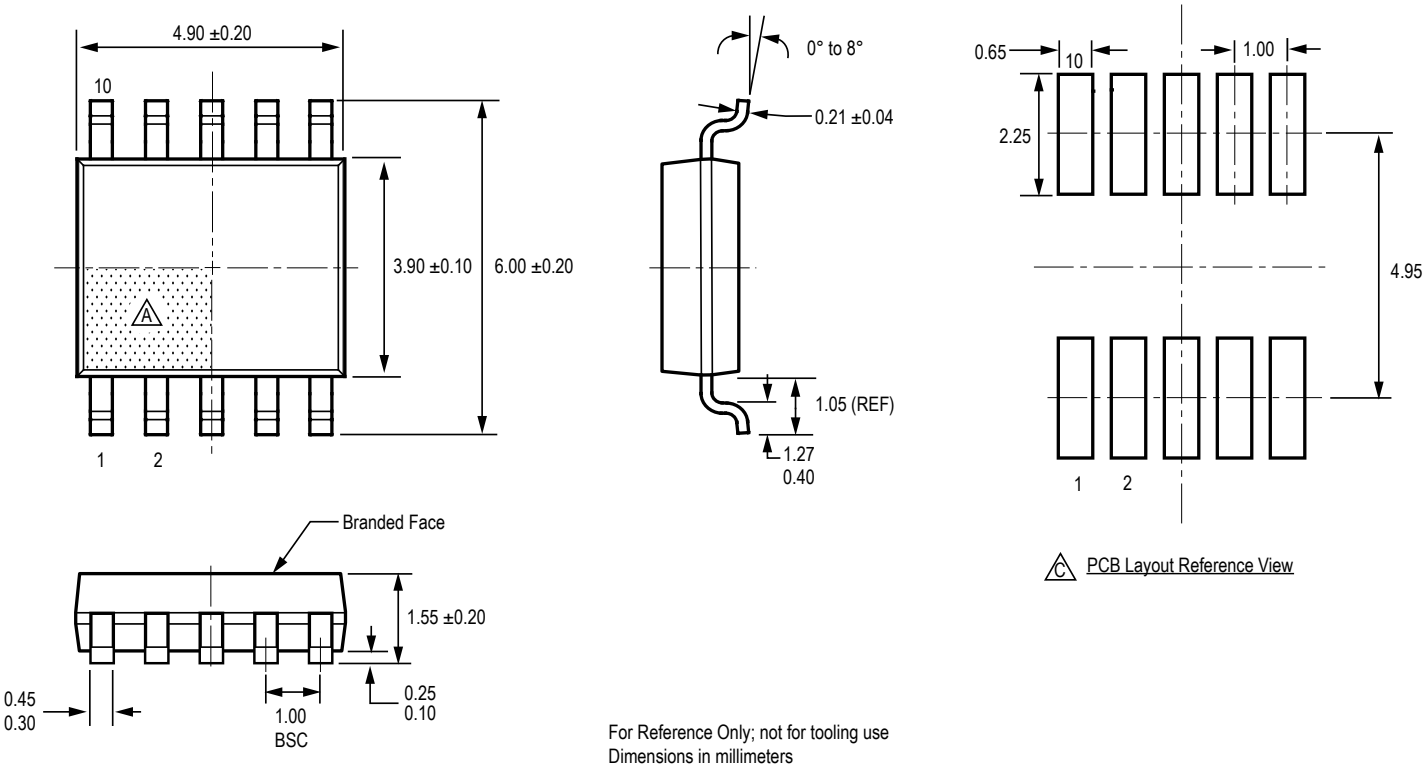
Package LN, 10-Lead SSOP



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Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout. All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias near the pin lands can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-7)

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Revision History

Number	Date	Description
–	February 13, 2017	Initial release
1	June 26, 2017	Corrected typo in Figure 1
2	July 5, 2018	Minor editorial updates
3	July 15, 2019	Minor editorial updates

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