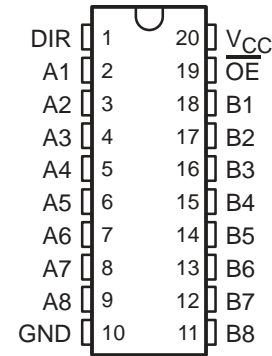


# SN74LVC245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS218C – JANUARY 1993 – REVISED JULY 1994

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE  
(TOP VIEW)



## description

This octal bus transceiver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

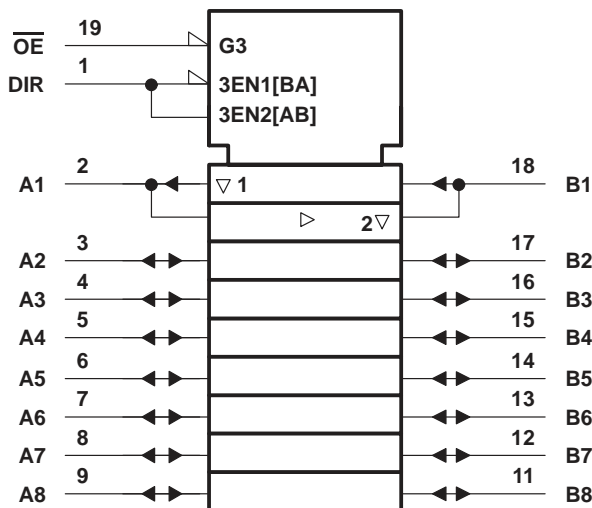
The SN74LVC245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC245 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

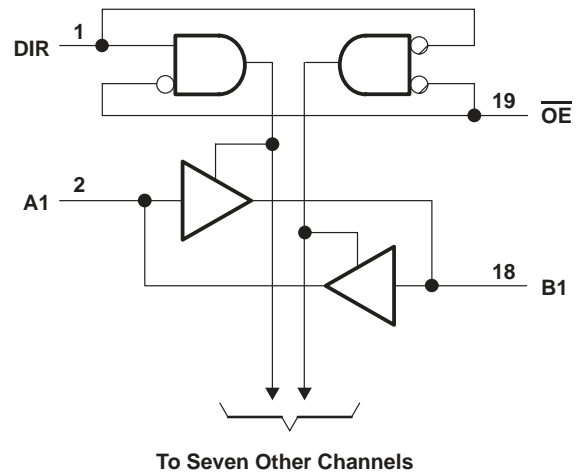
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
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# SN74LVC245

## OCTAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ : except I/O ports	–0.5 V to 4.6 V
I/O ports (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 4.6 V maximum.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature# SCBD002B.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V	–12	mA
		$V_{CC} = 3$ V	–24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

# SN74LVC245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> †	T <sub>A</sub> = -40°C to 85°C			UNIT
			MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I <sub>OH</sub> = -24 mA	3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	MIN to MAX	0.2			V
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			
		3 V	0.55			
	I <sub>OL</sub> = 24 mA	3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5			μA
I <sub>OZ</sub> ‡	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	20			μA
ΔI <sub>CC</sub>	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND		500			μA
C <sub>i</sub>	Control inputs V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5.5			pF
C <sub>io</sub>	A or B ports V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	6.7			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		UNIT
			MIN	TYP§	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	1.5	4	7	8		ns
t <sub>en</sub>	$\overline{OE}$	A or B	1.5	4.5	9	10		ns
t <sub>dis</sub>	$\overline{OE}$	A or B	1.5	5.5	8	9		ns

§ All typical values are V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

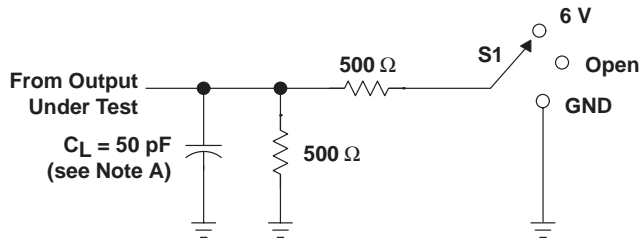
**operating characteristics, V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	C <sub>L</sub> = 50 pF, f = 10 MHz	25	pF
			2	

# SN74LVC245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

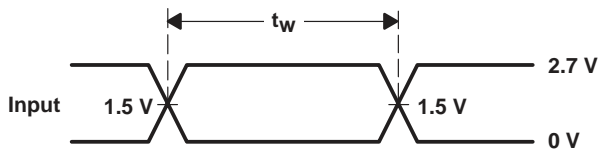
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## PARAMETER MEASUREMENT INFORMATION

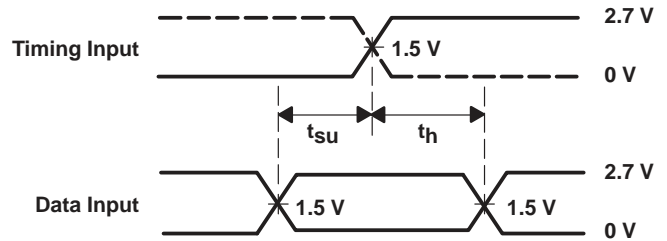


LOAD CIRCUIT FOR OUTPUTS

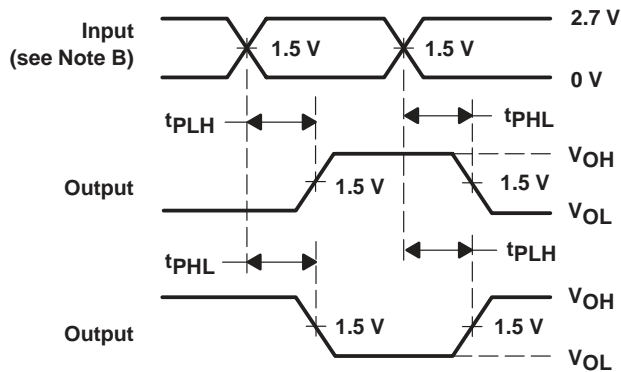
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



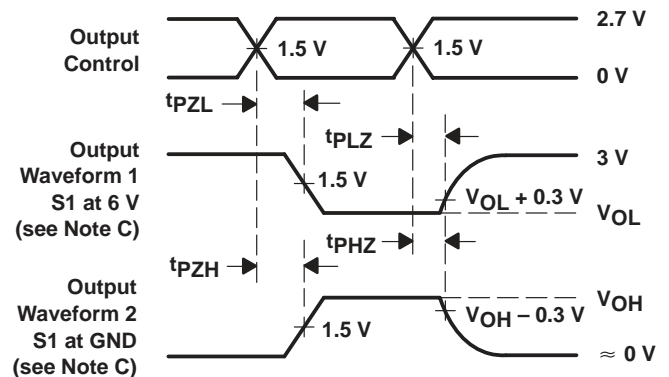
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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