

PE42424

Document Category: Product Specification

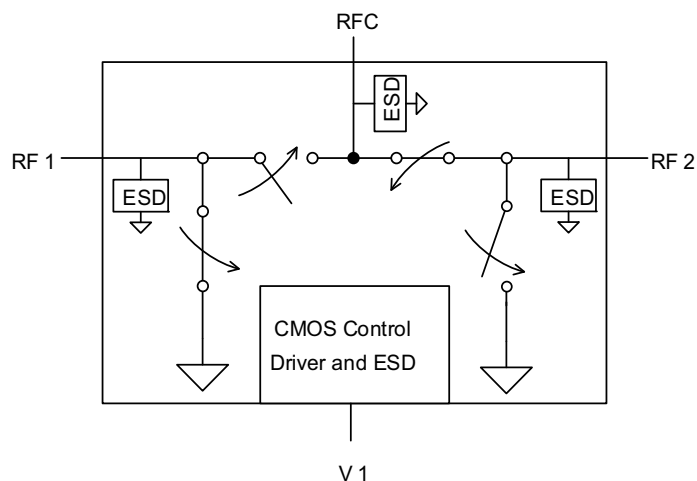
UltraCMOS® SPDT RF Switch, 100 MHz–8.5 GHz



Features

- 802.11 a/b/g/n/ac/ax, Wi-Fi 6E and ultra-wideband (UWB) support
- Exceptional isolation
 - 48 dB @ 2.4 GHz
 - 35 dB @ 5.8 GHz
- Fast switching
 - 145 ns switching time
 - 125 kHz switching rate
- High power handling
 - 39 dBm pulsed
 - 30 dBm CW
- High linearity across supply range
 - IIP3 of 61 dBm
 - IIP2 of 125 dBm
- 1.8V control logic compatible
- 105 °C operating temperature
- ESD performance
 - 2500V HBM on RF pins to GND
- Packaging – 6-lead 1.5 × 1.5 mm DFN

Figure 1 ■ PE42424 Functional Diagram



DOC-02108

Product Description

The PE42424 is a HaRP™ technology-enhanced reflective 50Ω SPDT RF switch designed for use in high power and high performance WLAN 802.11 a/b/g/n/ac/ax and Wi-Fi 6E applications such as carrier and enterprise Wi-Fi products and UWB applications supporting bandwidths up to 8.5 GHz.

This switch features exceptional port-to-port isolation, fast switching speed, and high power handling, all in a compact 1.5 × 1.5 mm package. PE42424 also features high linearity that remains invariant over the full power supply range. In addition, this device has robust ESD and temperature performance and does not require blocking capacitors or any external matching components.

The PE42424 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 ■ Absolute Maximum Ratings for PE42424

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input (V1)	V_{CTRL}	-0.3	3.6	V
RF input power, 100–6000 MHz	$P_{MAX,ABS}$		41	dBm
RF input power, 6000–8500 MHz	$P_{MAX,ABS}$		40	dBm
Storage temperature range	T_{ST}	-65	150	°C
ESD voltage HBM ⁽¹⁾	$V_{ESD,HBM}$		1000	V
All pins			2500	V
RF pins to GND				
ESD voltage CDM, all pins ⁽²⁾	$V_{ESD,MM}$		1000	V
Notes:				
1) Human body model (MIL-STD 883 Method 3015)				
2) Charged device model (JEDEC JESD22-C101)				

Recommended Operating Conditions

Table 2 lists the recommending operating conditions for the PE42424. Devices should not be operated outside the operating conditions listed below.

Table 2 ■ Recommended Operating Conditions for PE42424

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3	3.3	5.5	V
Supply current	I_{DD}		130 ⁽¹⁾ 200 ⁽²⁾	200 300	μ A μ A
Digital input high (V1)	V_{IH}	1.4		3.6	V
Digital input low(V1)	V_{IL}	-0.3		0.6	V
RF input power, CW, 100-6000 MHz	$P_{MAX,CW}$			30	dBm
RF input power, CW, 6000-8500 MHz	$P_{MAX,CW}$			29	dBm
RF input power, pulsed, 100-6000 MHz ⁽³⁾	$P_{MAX,PULSED}$			39	dBm
RF input power, pulsed, 6000-8500 MHz ⁽³⁾	$P_{MAX,PULSED}$			38	dBm
Operating temperature range	T_{OP}	-40	25	105	°C
Notes: 1) $V_{IH} > 1.7V$ 2) $1.4V < V_{IH} < 1.7V$ 3) Pulsed, 5% duty cycle of 4620 μ s period, 50 Ω					

Electrical Specifications

Table 3 provides the PE42424 key electrical specifications @ 25°C, $V_{DD} = 3.3V$, ($Z_L = Z_S = 50\Omega$) unless otherwise specified, unless otherwise specified.

Table 3 ■ PE42424 Electrical Specifications

Parameter	Symbol	Path	Condition	Min	Typ	Max	Unit
Operating frequency				0.1		8.5	GHz
Insertion loss	IL	RFC-RFX	0.1–2.5 GHz		0.8	0.95	dB
			2.5–5.825 GHz		0.9	1.15	dB
			5.825–6.0 GHz		0.95	1.2	dB
			6.0–8.5 GHz		1.08	1.6	dB
Isolation	ISO	RFC-RFX	0.1–2.5 GHz	45	47		dB
			2.5–5.825 GHz	33	35		dB
			5.825–6.0 GHz	33	34		dB
			6.0–8.5 GHz	27	29		dB
		RFX-RFX	0.1–2.5 GHz	37	39		dB
			2.5–5.825 GHz	29	30		dB
			5.825–6.0 GHz	29	30		dB
			6.0–8.5 GHz	24	26		dB
Return loss (common and active port)	RL	RFX	0.1–6.0 GHz		21		dB
			6.0–8.5 GHz		21		dB
Input 1dB compression point ⁽¹⁾	P1dB	RFC-RFX	6.0 GHz		41		dBm
			6.0–8.5 GHz		40		dBm
3rd Order Input Intercept Point ⁽²⁾	IIP3	RFC-RFX	1900 MHz		60		dBm
3rd harmonic	3fo	RFC-RFX	$P_{IN} = +30$ dBm @ 1900 MHz		74		dBc
2nd Order Input Intercept Point ⁽²⁾	IIP2	RFC-RFX	1900 MHz		125		dBm
2nd harmonic	2fo	RFC-RFX	$P_{IN} = +30$ dBm @ 1900 MHz		85		dBc
Switching time	T_{SW}		50% CTRL to 90% or 10% of final value		145	230	ns
Notes:							
1) The input P0.1dB compression point is a linearity figure of merit. Refer to Table 2 for the operating RF input power (50Ω).							
2) The input intercept point remains invariant over the full supply range as defined in Table 3.							

Switching Capability

The PE42424 has a maximum 125 kHz switching rate with the control pin input capacitance of 2 pF. Switching rate describes the time duration between switching events.

Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spurious Performance

Typical spurious performance of the PE42424 is -126 dBm.

Control Logic Truth Table

Table 4 provides the control logic truth table for the PE42424.

Table 4 • Truth Table for PE42424

V1	RFC–RF1	RFC–RF2
0	OFF	ON
1	ON	OFF

Typical Performance Data

Figure 2–Figure 10 show the typical performance data @ 25 °C and $V_{DD} = 3.3V$, unless otherwise specified.

Figure 2 ■ Insertion Loss (RFC–RFX)

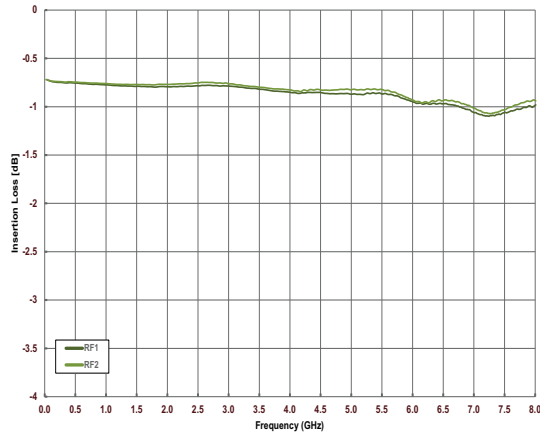


Figure 3 ■ Insertion Loss vs. Temp (RFC–RFX)

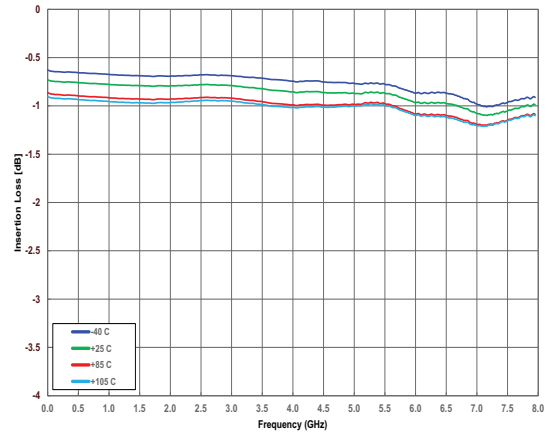


Figure 4 ■ Insertion Loss vs. V_{DD} (RFC–RFX)

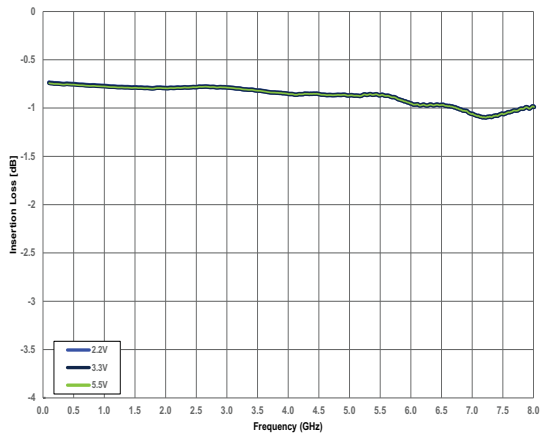


Figure 5 ■ Return Loss vs. Temp (RFC-RFX)

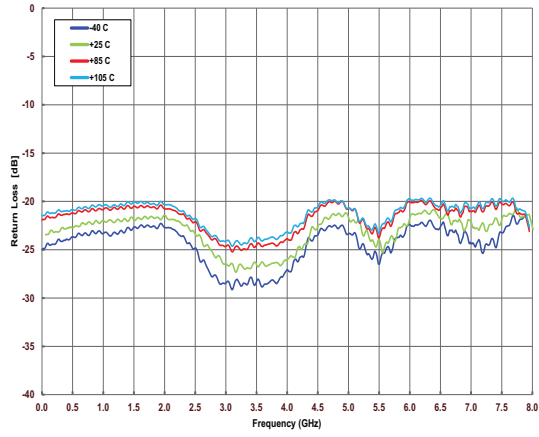


Figure 6 ■ Return Loss vs. V_{DD} (RFC-RFX)

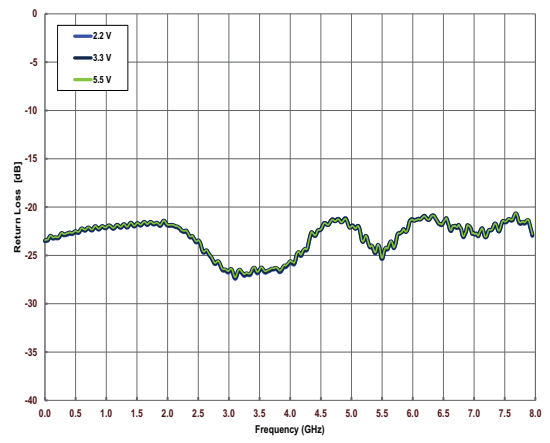


Figure 7 ■ Isolation vs. Temp (RFC-RFX)

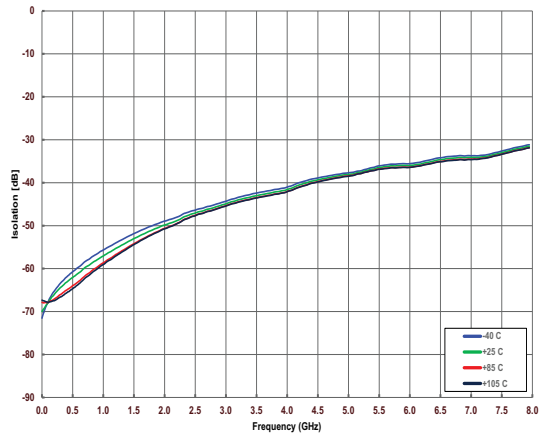


Figure 8 ■ Isolation vs. V_{DD} (RFC-RFX)

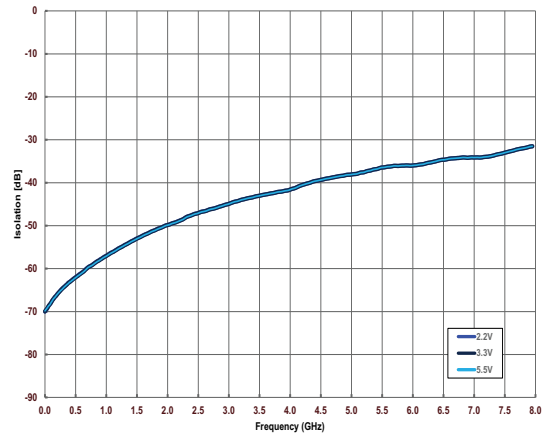


Figure 9 ■ Isolation vs. Temp (RFX–RFX)

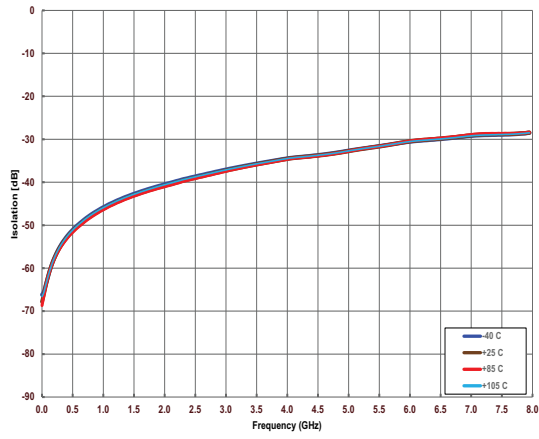
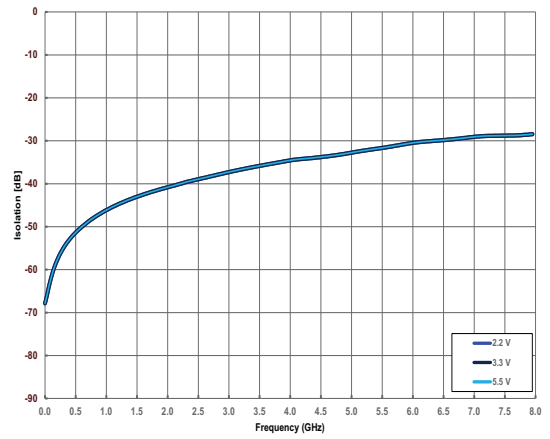


Figure 10 ■ Figure 12. Isolation vs. V_{DD} (RFX–RFX)



Pin Information

This section provides pinout information for the PE42424. **Figure 11** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

Figure 11 ▪ Pin Configuration (Top View)

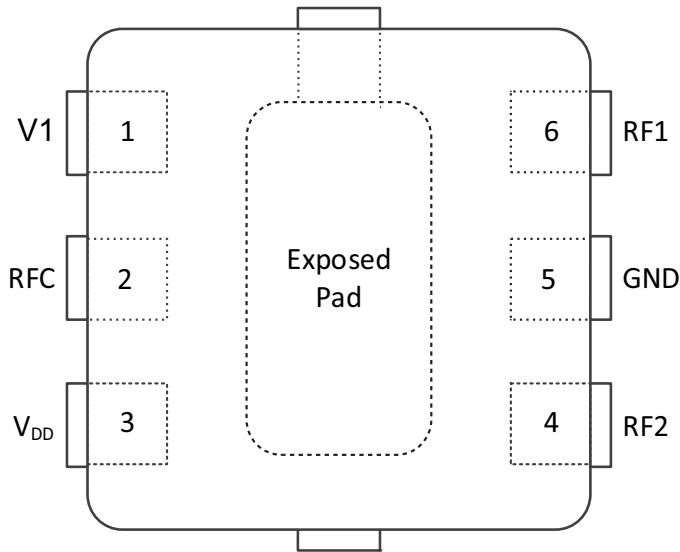


Table 5 ▪ Pin Descriptions for PE42424

Pin No.	Pin Name	Description
1	V1	Digital control logic input 1
2	RFC ^(*)	RF common
3	VDD	Supply voltage (nominal 3.3V)
4	RF2 ^(*)	RF port 2
5	GND	Ground
6	RF1 ^(*)	RF port 1
Pad	GND	Ground

Note: * RF pins 2, 4 and 6 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met.

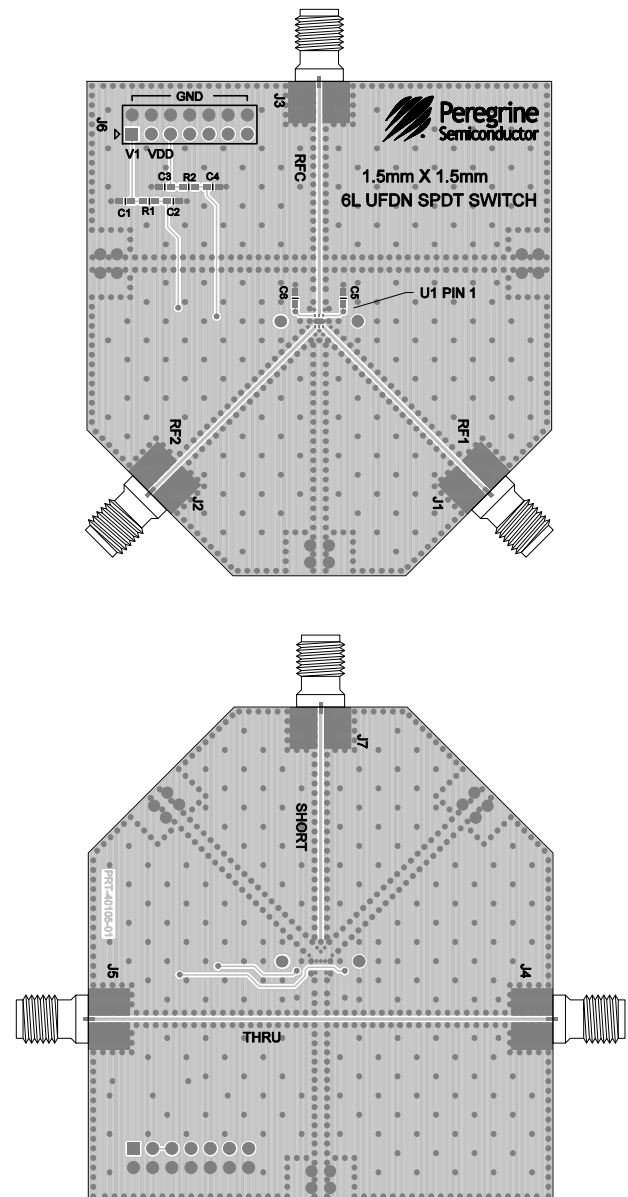
Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of pSemi's PE42424 RF switch. The RF common port is connected to the device through a 50Ω transmission line via SMA connector J3. RF1 and RF2 ports are connected to the device through 50Ω transmission lines via SMA connectors J1 and J2, respectively. A transmission line has been included on the reverse side of the PCB, accessible via SMA connectors J4 and J5. This transmission line provides an equivalent length to de-embed PCB trace losses. DC and digital inputs are provided to the device via J6.

This PCB is constructed of a four metal layer material with total thickness of 62 mils. The top and bottom RF layers are Rogers RO4003 material with an 8 mil RF core. The middle layers provide ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 16 mils and 10 mil trace gap, with 2.1 mils of metal thickness.

For the true performance of the PE42424 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

Figure 12 ■ Evaluation Kit Layout for PE42424



PRT-40105

Packaging Information

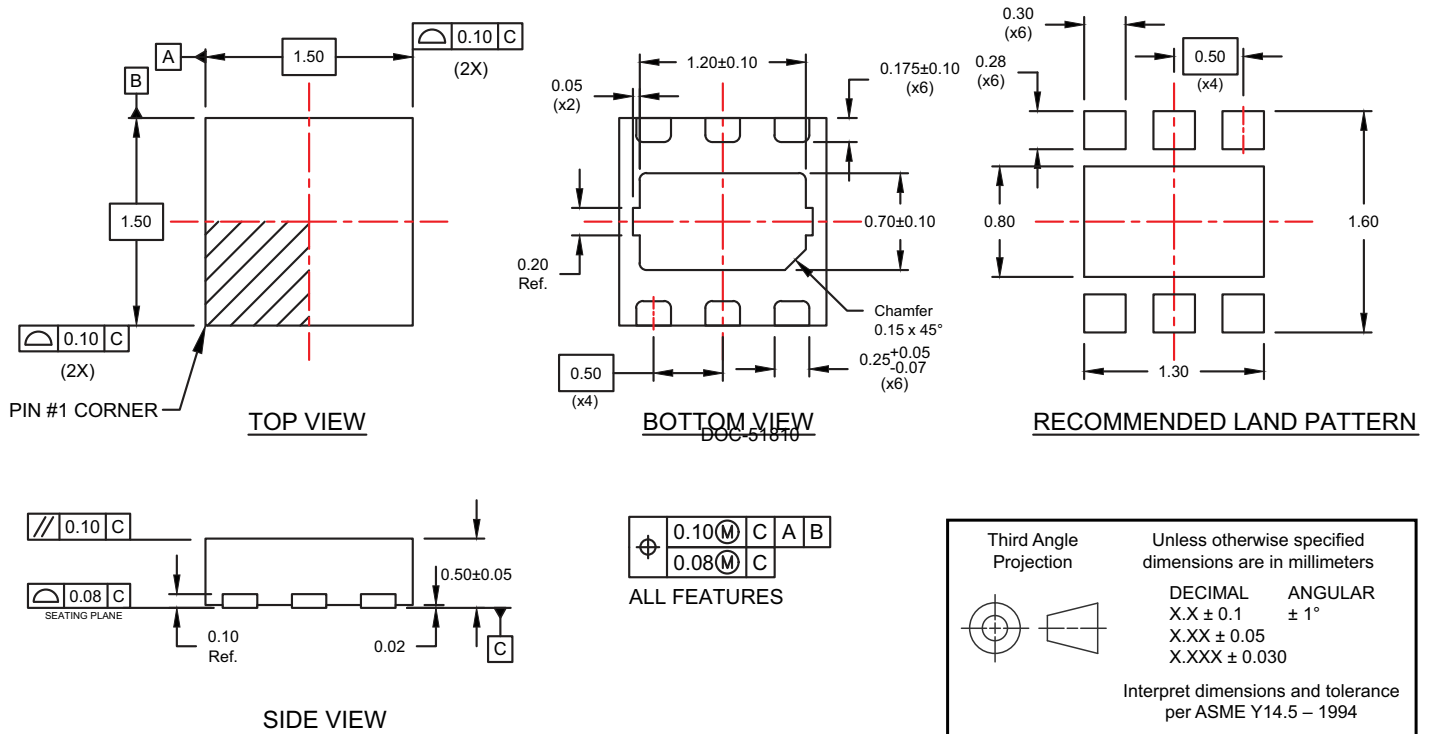
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42424 in the 6-lead 1.5 x 1.5 mm DFN package is MSL 1.

Package Drawing

Figure 14 ■ Package Mechanical Drawing for 6-lead 1.5 x 1.5 mm DFN



DOC-51810

Top-Marking Specification

Figure 15 ■ Package Marking Specifications for PE42424



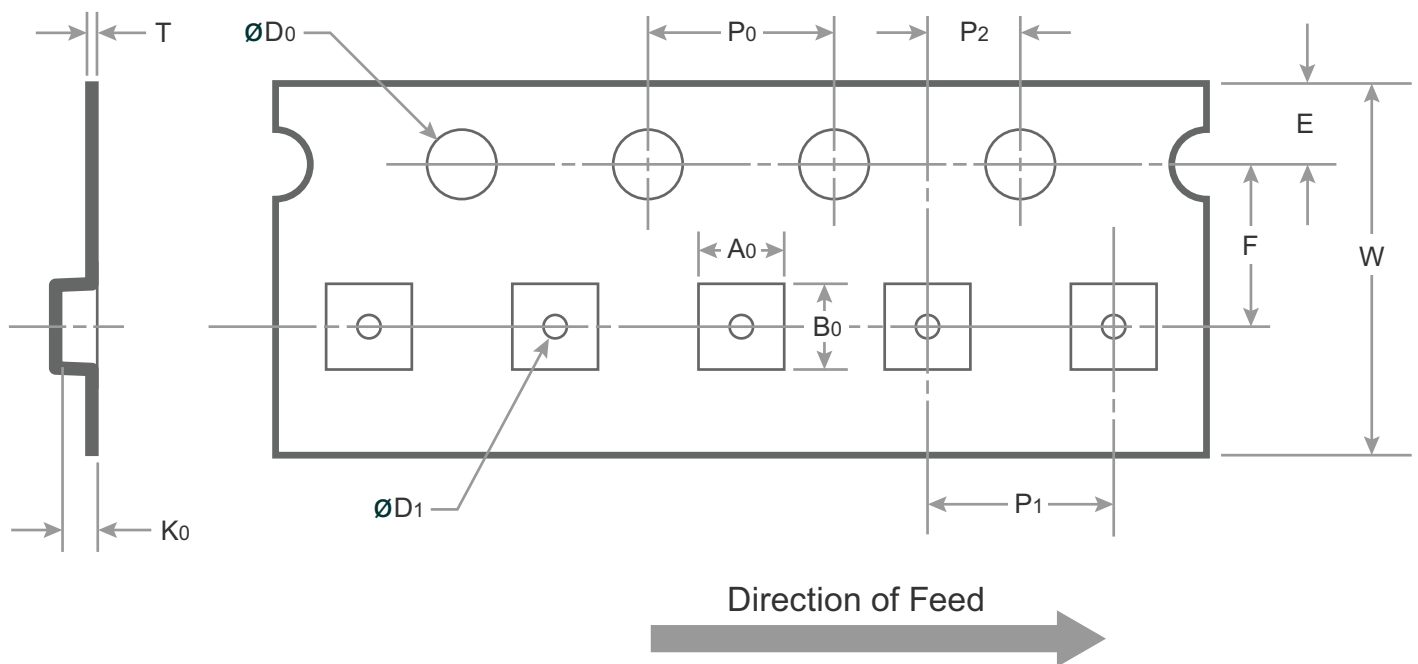
- = Pin 1 indicator
- P = Part number code*
- ZZ = Last two characters of the assembly lot code
- Y = Last digit of year, starting from 2010
- WW = Work week

Note: * The part number marking for PE42424 is E.

DOC-51207

Tape and Reel Specification

Figure 16 ■ Tape and Reel Specifications for 6-lead 1.5 x 1.5 mm DFN



Notes:
Not drawn to scale.
Dimensions are in millimeters.
Maximum cavity angle 5 degrees.
Bumped die are oriented active side down.

Carrier Tape Dimension Table					
Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
A0	1.70	+/- 0.05	D1	0.5	+ 0.5 - 0.1
B0	1.70	+/- 0.05	D0	1.5	+ 0.1
K0	0.76	+/- 0.05	E	1.75	+/- 0.1
P1	4.00	+/- 0.1	P0	4.0	+/- 0.1
W	8.00	+ 0.3 - 0.1	P2	2.0	+/- 0.05
F	3.50	+/- 0.5	T	0.25	+/- 0.02

DOC-85004

Ordering Information

Table 6 lists the available ordering codes for the PE42424 as well as available shipping methods.

Table 6 ■ Order Codes for PE42424

Order Codes	Description	Packaging	Shipping Method
PE42424A-Z	PE42424 SPDT RF switch	Green 6-lead 1.5 x 1.5 mm DFN	3000 units/T&R
EK42424-01	PE42424 Evaluation kit	Evaluation kit	1/Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark

©2015–2020, pSemi Corporation. All rights reserved. The Peregrine Semiconductor name, Peregrine Semiconductor logo and UltraCMOS are registered trademarks and the pSemi name, pSemi logo, HaRP and DuNE are trademarks of pSemi Corporation in the U.S. and other countries.