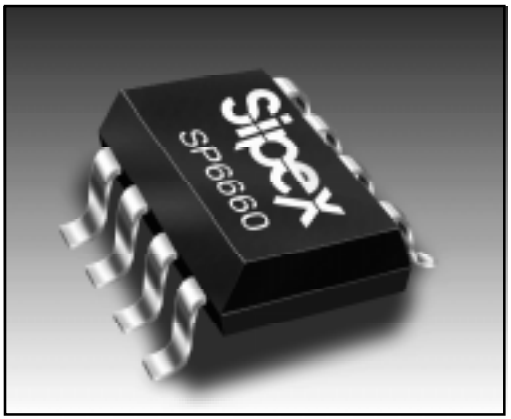
200mA Charge Pump Inverter or Doubler

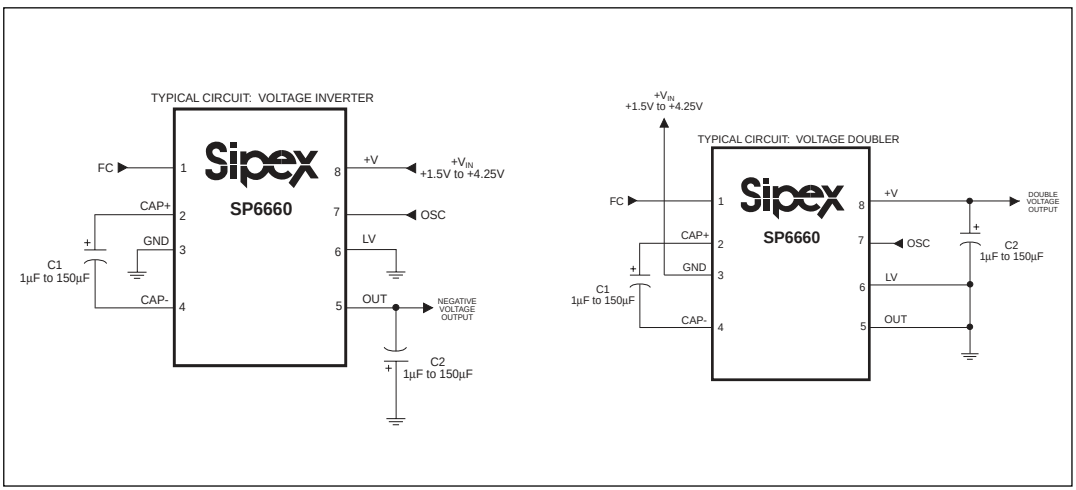
- Inverts or Doubles Input Supply Voltage
- 93% Power Efficiency at 3.6V
- 10kHz/80kHz Selectable Oscillator
- **External Oscillator up to 700KHz**
- 5Ω Output Resistance at 3.6V
- Low Voltage Battery Operation
- **Ideal for 3.6V Lithium Ion Battery**
- **High Output Current – 200mA**
- Pin-Compatible High-Current Upgrade of the ICL7660 and 660 Industry Standard
- **Smallest Package Available for the 660 Industry Standard – 8pin μSOIC**



Now Available in Lead Free Packaging

DESCRIPTION

The **SP6660** is a CMOS DC-DC Monolithic Voltage Converter that can be implemented as a Voltage Inverter or a Positive Voltage Doubler. As a Voltage Inverter, a -1.5V to -4.25V output can be converted from a +1.5V to +4.25V input. As a Voltage Doubler, the **SP6660** can provide a +8.0V output at 100mA from a +4.25V input. The **SP6660** is ideal for both battery-powered and board level voltage conversion applications with a typical operating current of 400μA and a high efficiency (>90%) over most of its load-current range. Typical end products for this device are operational amplifier and interface power supplies, medical instruments, and hand-held and laptop computers. The **SP6660** is available in 8-pin DIP, SOIC, and μSOIC packages.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Power Supply Voltage
(V+ to GND or GND to OUT).....+4.5V
LV Input Voltages.....(OUT - 0.3V) to (V+ + 0.3V)
FC and OSC Input Voltages.....The least negative of
(OUT - 0.3V) or (V+ - 4.5V) to (V+ + 0.3V)

OUT and V+ Continuous Output Current.....250mA
Output Short-Circuit Duration to GND.....1s
Operating Temperature Ranges
SP6660C_.....0˚C to +70˚C
SP6660E_.....-40˚C to +85˚C
Continuous Power Dissipation (T_{AMB} = 70˚C)
PDIP (derate 9.09mW/˚C above +70˚C).....727mW
NSOIC (derate 5.88mW/˚C above +70˚C).....471mW
µSOIC (derate 4.10mW/˚C above +70˚C).....330mW
Operating Temperature.....-40˚C to +85˚C
Storage Temperature.....-65˚C to +150˚C
Lead Temperature (soldering 10s).....+300˚C

SPECIFICATIONS

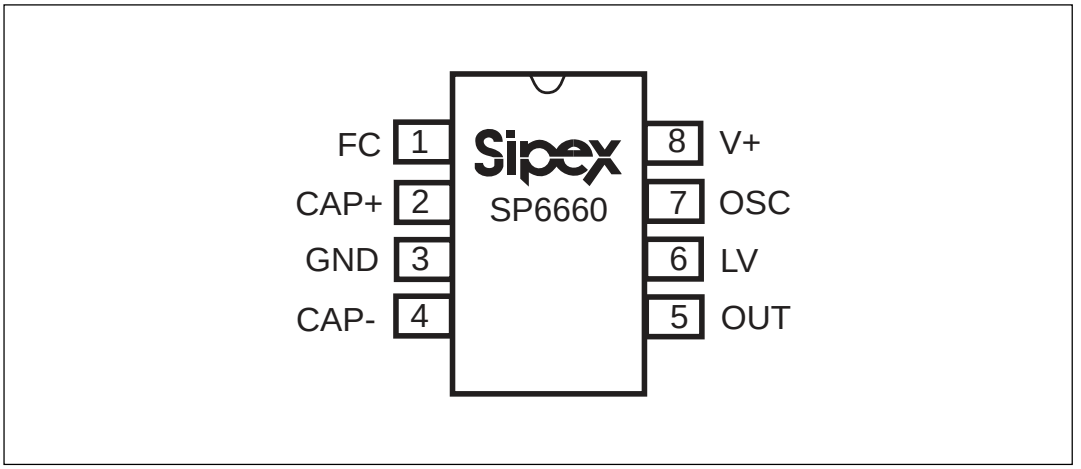
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Inverter Circuit at Low Frequency with 150µF Capacitors					
V+ = 3.6V, C1 = C2 = 150µF, FC = open, $T_{AMB} = T_{MIN}$ to T_{MAX}; refer to ***Figure 1*** test circuit. Note 2					
Supply Voltage	1.5	0.93	4.25	V	R_L = 500Ω, Note 4
Supply Current		0.4	0.8	mA	No Load
Output Current	200			mA	
Oscillator Input Current		±1		µA	
Oscillator Frequency	5	10	20	kHz	
Output Resistance		5.2	10	Ω	I_L = 100mA, Note 3
Voltage Conversion Efficiency	99.00	99.96		%	No Load
Power Efficiency	88 80 63	94 85 70		%	R_L = 500Ω I_L = 100mA I_L = 200mA
Doubler Circuit at Low Frequency with 150µF Capacitors					
V+ = 3.6V, C1 = C2 = 150µF, FC = open, $T_{AMB} = T_{MIN}$ to T_{MAX}; refer to ***Figure 2*** test circuit. Note 2					
Supply Voltage	2.5	1.5	4.25	V	R_L = 1kΩ, Note 4
Supply Current		0.4	0.8	mA	No Load
Output Current	200			mA	
Oscillator Input Current		±1		µA	
Oscillator Frequency	5	10	20	kHz	
Output Resistance		5.2	10	Ω	I_L = 100mA, Note 3
Voltage Conversion Efficiency	99.00	99.96		%	No Load
Power Efficiency	91 89 79	96 93 85		%	R_L = 1KΩ I_L = 100mA I_L = 200mA

SPECIFICATIONS (continued)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Inverter Circuit at High Frequency with 22µF Capacitors					
V+ = 3.6V, C1 = C2 = 22µF, FC = V+, T_{AMB} = T_{MIN} to T_{MAX}; refer to ***Figure 1*** test circuit. Note 2					
Supply Voltage	1.5	0.97	4.25	V	R_L = 500Ω, Note 4
Supply Current		0.6	1.5	mA	No Load
Output Current	200			mA	
Oscillator Input Current		±8		µA	
Oscillator Frequency	40	80	160	kHz	
Output Resistance		5.0	10	Ω	I_L = 100mA, Note 3
Voltage Conversion Efficiency	99.00	99.96		%	No Load
Power Efficiency	86 80 63	92 86 71		%	R_L = 500Ω I_L = 100mA I_L = 200mA
Doubler Circuit at HIgh Frequency with 22µF Capacitors					
V+ = 3.6V, C1 = C2 = 22µF, FC = V+, T_{AMB} = T_{MIN} to T_{MAX}; refer to ***Figure 2*** test circuit. Note 2					
Supply Voltage	2.5	1.6	4.25	V	R_L = 1kΩ, Note 4
Supply Current		0.6	1.5	mA	No Load
Output Current	200			mA	
Oscillator Input Current		±8		µA	
Oscillator Frequency	40	80	160	kHz	
Output Resistance		5.0	10	Ω	I_L = 100mA, Note 3
Voltage Conversion Efficiency	99.00	99.96		%	No Load
Power Efficiency	90 89 79	94 93 85		%	R_L = 1KΩ I_L = 100mA I_L = 200mA

NOTE 1: Specified output resistance is a combination of internal switch resistance and capacitor ESR.
NOTE 2: In the test circuit capacitors C1 and C2 are 150µF, 0.2 maximum ESR, tantalum or 22µF, 0.2 maximum ESR, tantalum. Capacitors with higher ESR may reduce output voltage and efficiency. Refer to Capacitor Selection section.
NOTE 3: Specified output resistance is a combination of internal switch resistance and capacitor ESR. Refer to Capacitor Selection section.
NOTE 4: Typical value indicates start-up voltage.

PINOUT



PIN ASSIGNMENTS

Pin 1— FC — Frequency Control for the internal oscillator. FC = open, f_{OSC} = 10KHz typical; FC = V+, f_{OSC} = 80KHz typical

Pin 2 — CAP+ — Connect to the positive terminal of the charge pump capacitor.

Pin 3 — GND — (Voltage Inverter Circuit) Ground.

Pin 3 — GND — (Positive Voltage Doubler Circuit) Positive supply voltage input.

Pin 4 — CAP- — Connect to the negative terminal of the charge pump capacitor.

Pin 5 — OUT — (Voltage Inverter Circuit) Negative voltage output pin.

Pin 5 — OUT — (Positive Voltage Doubler Circuit) Ground pin for power supply.

Pin 6 — LV

Low-voltage operation input pin in 660 circuits. In SP6660 circuits can be connected to GND, OUT or left open as desired with no effect.

Pin 7 — OSC — Control pin for the oscillator. Internally connected to 15pf capacitor. An external capacitor can be added to slow the oscillator. Be careful to minimize stray capitance. An external oscillator can be connected to overdrive the OSC pin.

Pin 8 — V+ — (Voltage Inverter Circuit) Positive voltage input pin for the power supply.

Pin 8 — V+ — (Positive Voltage Doubler Circuit) Positive voltage output.

DESCRIPTION

The **SP6660** Charge Pump DC-DC Voltage Converter either inverts or doubles the input voltage. As a negative voltage inverter, as shown in ***Figure 1***, a +1.5V to +4.25V input can be converted to a -1.5V to -4.25V output. ***Figure 2***, as a positive voltage doubler, a +2.5V to +4.25V input can be converted to a +5.0V to +8.5V output.

Typical performance curves in ***Figures 3*** to ***20*** are generated using the test circuits found in ***Figure 1*** and ***Figure 2***. Four operating modes are shown in the curves: Voltage inverter in low and high frequency modes and voltage doubler in low and high frequency modes.

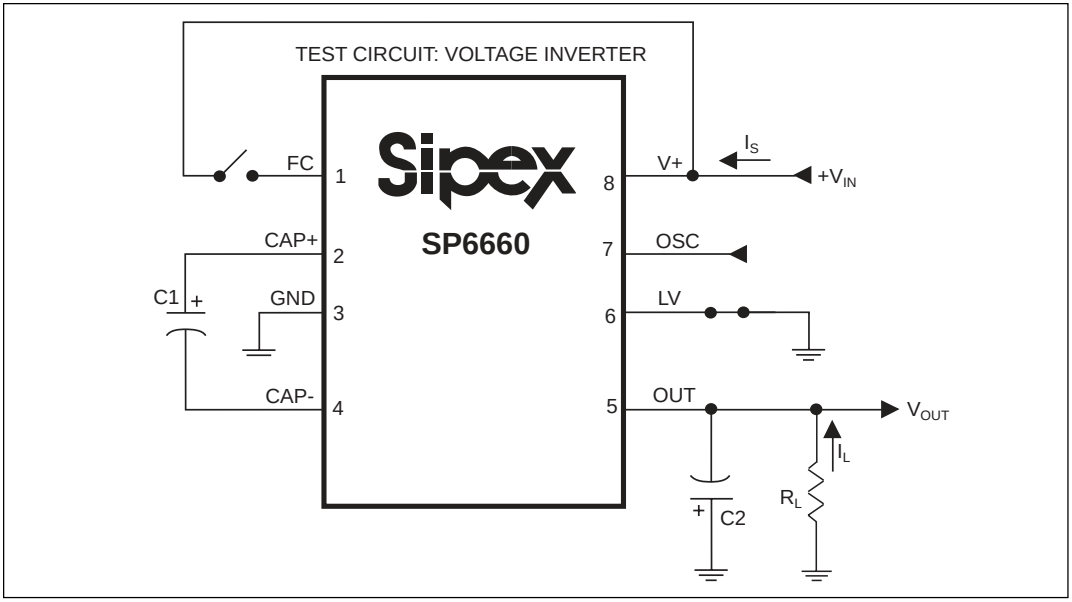


Figure 1. SP6660 Test Circuit for the Voltage Inverter

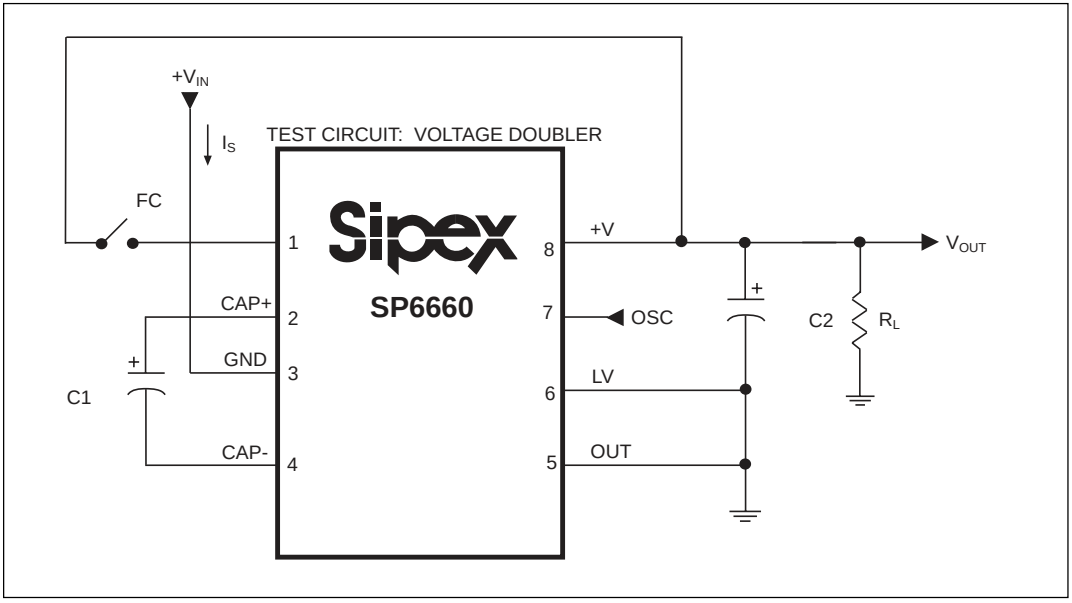


Figure 2. Test Circuit for the Positive Voltage Doubler

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +3.6V, T_{AMB} = 25°C unless otherwise noted. LF = Low Frequency, FC = Open, C1 = C2 = 150µF.
HF = High Frequency, FC = V+, C1 = C2 = 22µF. Inverter Circuit use ***Figure 1***. Doubler Circuit use ***Figure 2***.

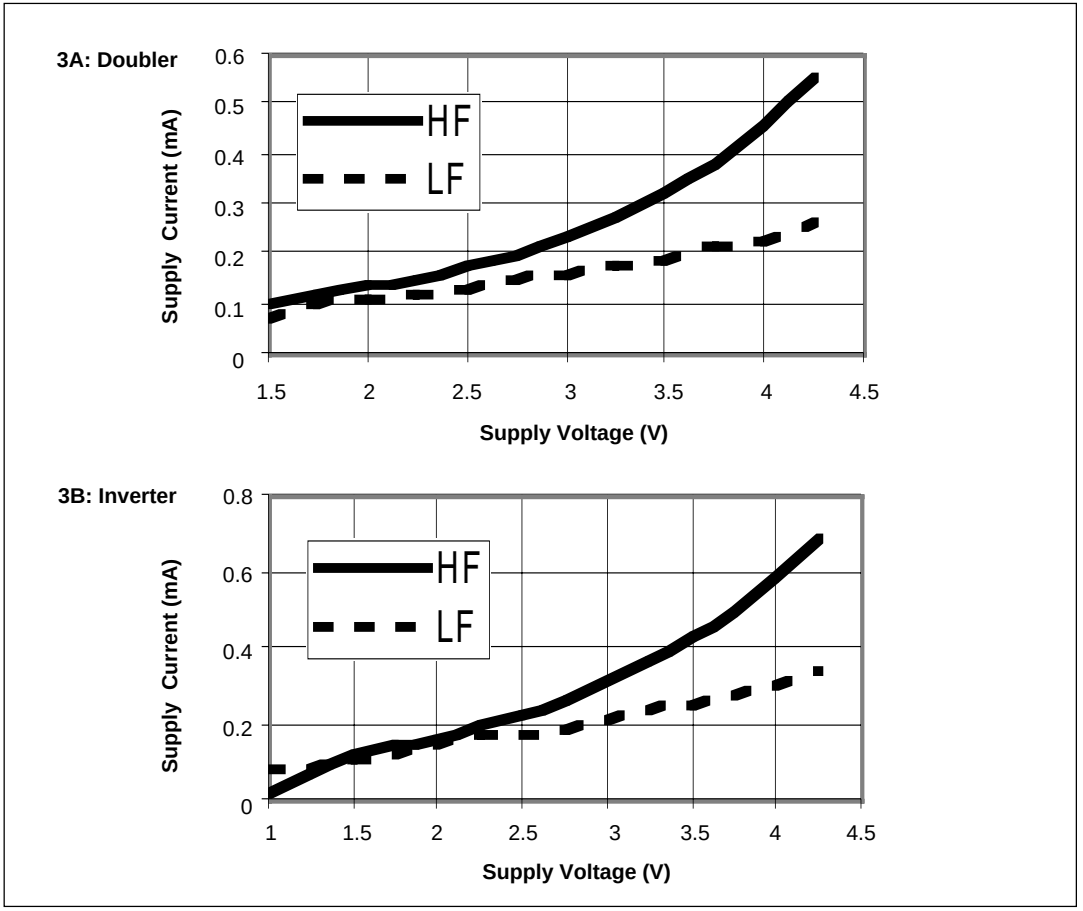


Figure 3A and 3B Supply Current vs. Supply Voltage

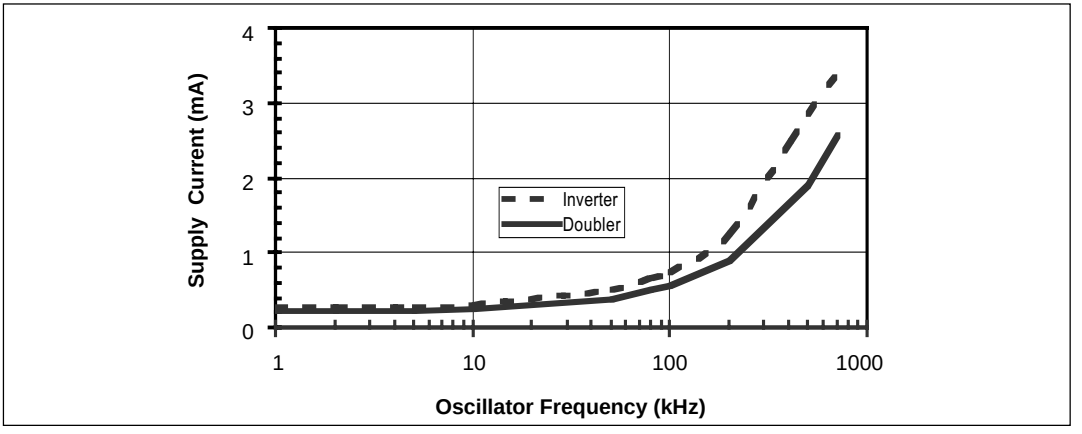


Figure 4. Supply Current vs. Oscillator Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +3.6V, T_{AMB} = 25°C unless otherwise noted. LF = Low Frequency, FC = Open, C1 = C2 = 150µF.
HF = High Frequency, FC = V+, C1 = C2 = 22µF. Inverter Circuit use ***Figure 1***. Doubler Circuit use ***Figure 2***.

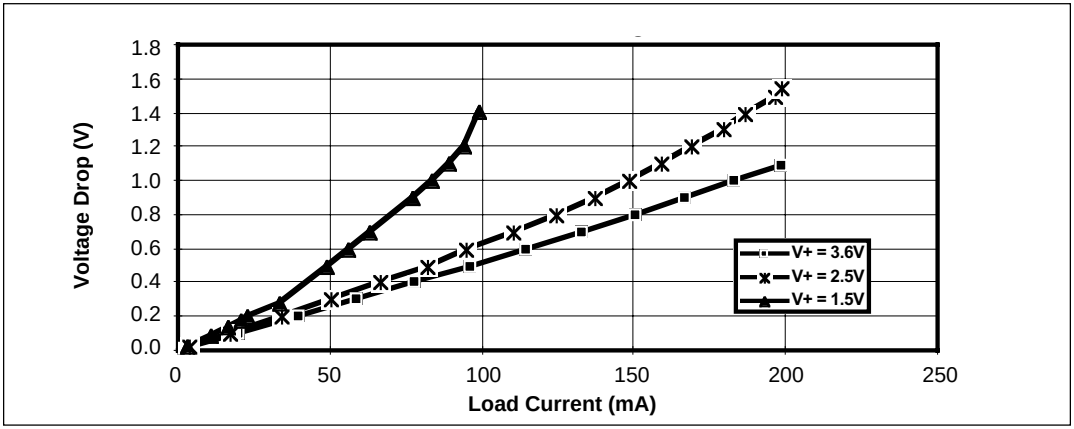


Figure 5. Output Voltage Drop vs. Load Current – Inverter LF

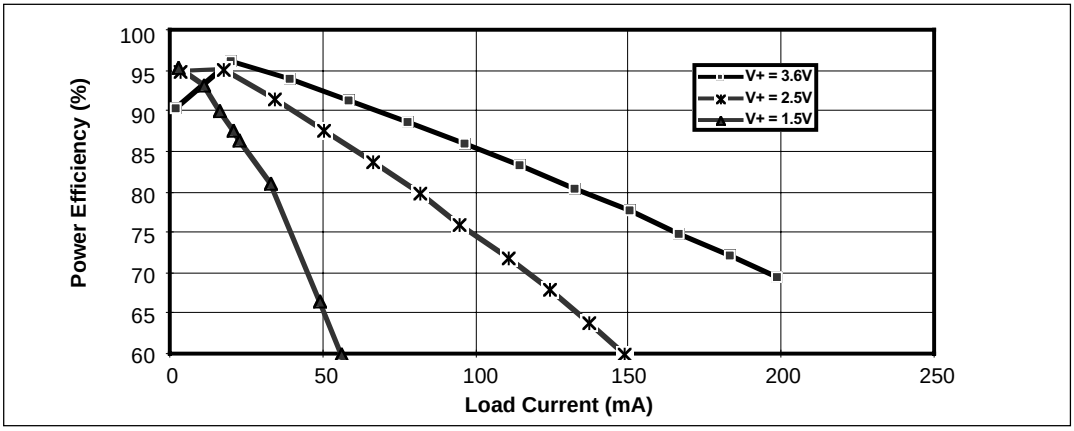


Figure 6. Power Efficiency vs. Load Current – Inverter LF

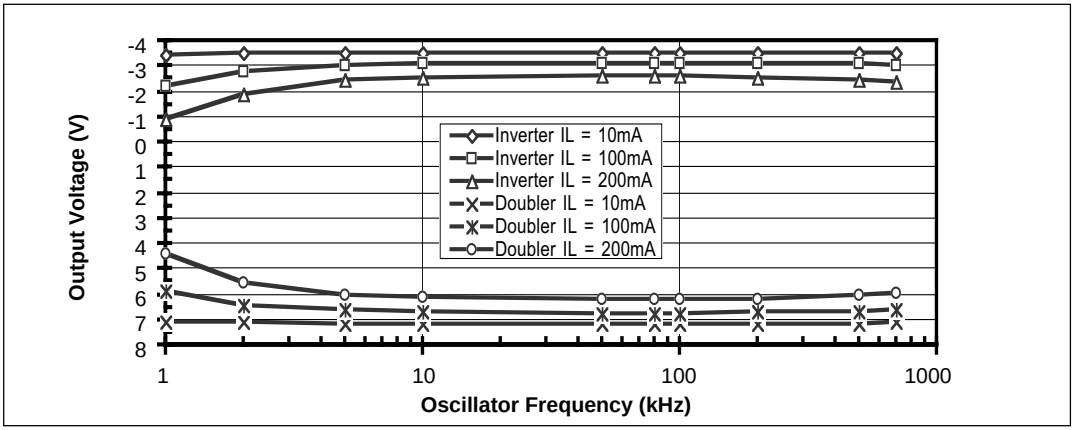


Figure 7. Output Voltage vs. Oscillator Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +3.6V, T_{AMB} = 25°C unless otherwise noted. LF = Low Frequency, FC = Open, C1 = C2 = 150µF.
HF = High Frequency, FC = V+, C1 = C2 = 22µF. Inverter Circuit use ***Figure 1***. Doubler Circuit use ***Figure 2***.

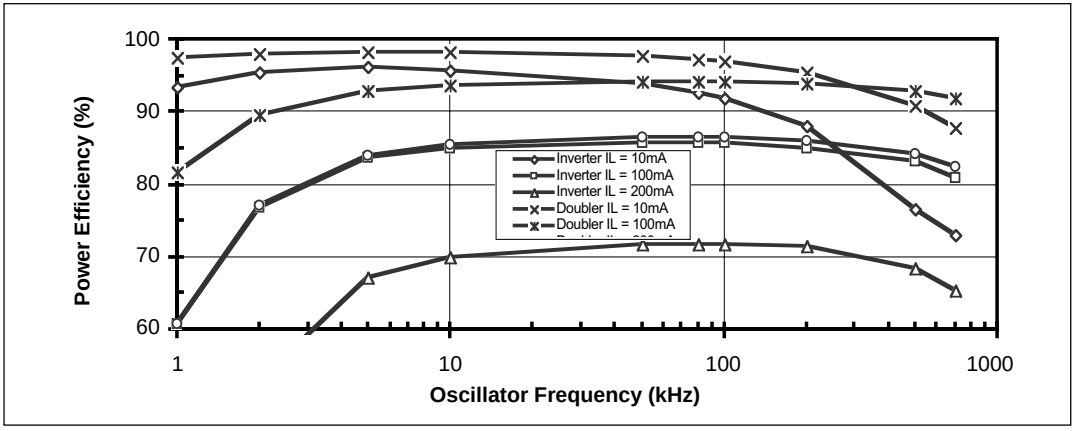


Figure 8. Power Efficiency vs. Oscillator Frequency

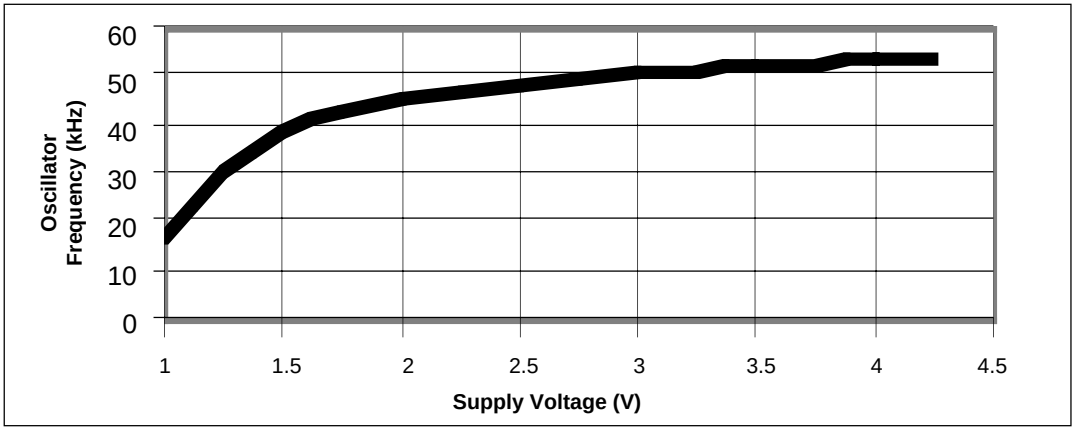


Figure 9. Oscillator Frequency vs. Supply Voltage – HF

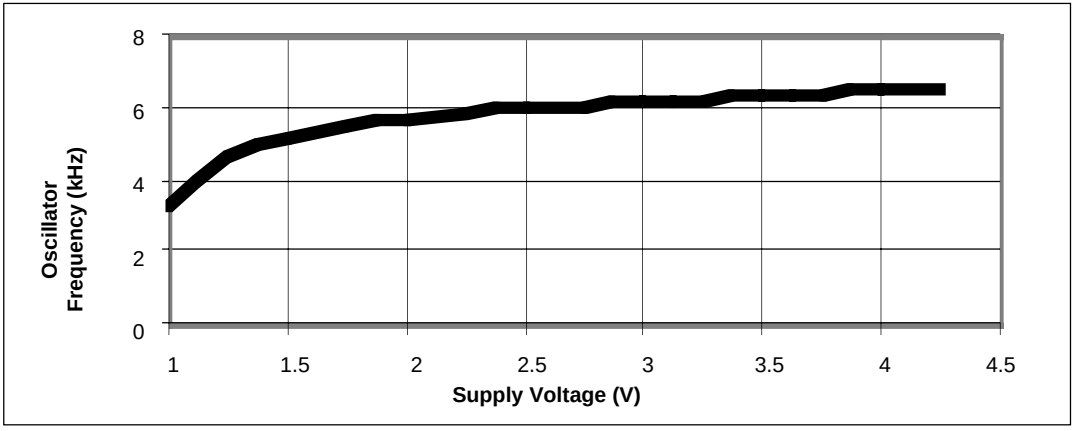


Figure 10. Oscillator Frequency vs. Supply Voltage – LF

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +3.6V, T_{AMB} = 25°C unless otherwise noted. LF = Low Frequency, FC = Open, C1 = C2 = 150µF.
HF = High Frequency, FC = V+, C1 = C2 = 22µF. Inverter Circuit use ***Figure 1***. Doubler Circuit use ***Figure 2***.

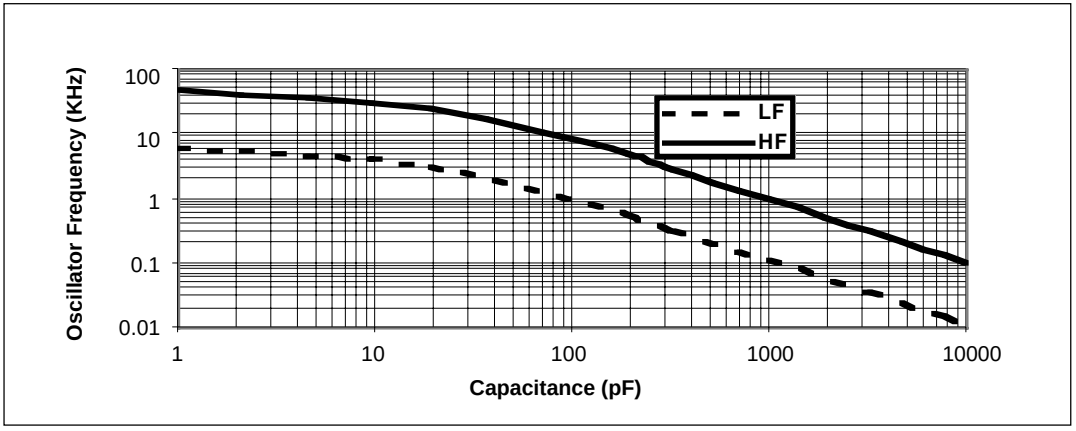


Figure 11. Oscillator Frequency vs. External Capacitance

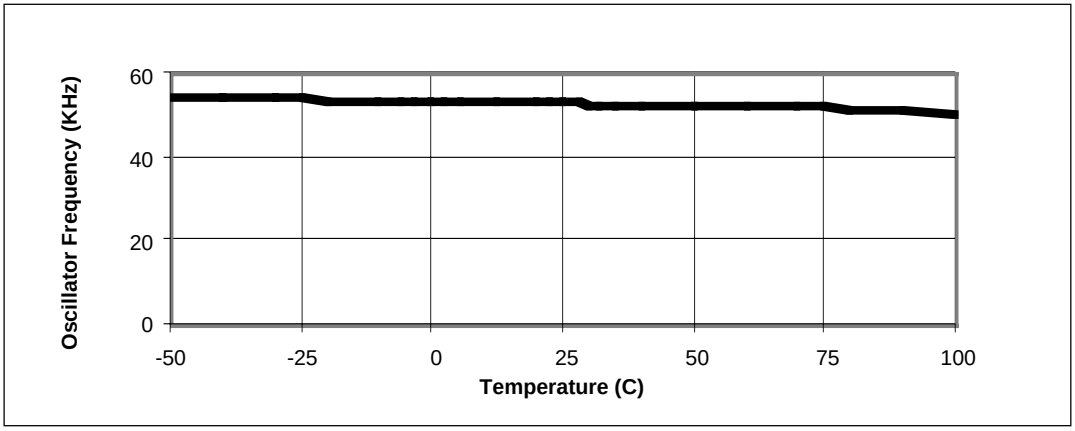


Figure 12. Oscillator Frequency vs. Temperature where FC=V+

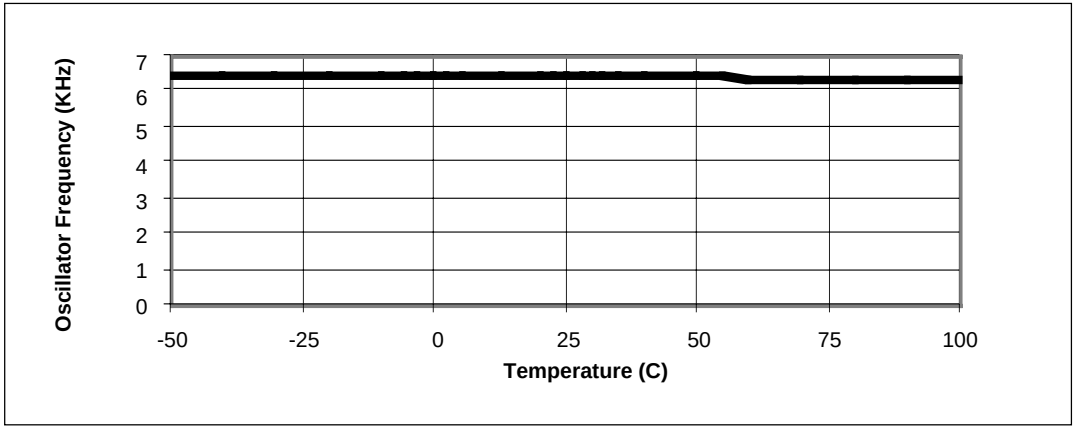


Figure 13. Oscillator Frequency vs. Temperature where FC=open

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +3.6V, T_{AMB} = 25ºC unless otherwise noted. LF = Low Frequency, FC = Open, C1 = C2 = 150µF.
HF = High Frequency, FC = V+, C1 = C2 = 22µF. Inverter Circuit use ***Figure 1***. Doubler Circuit use ***Figure 2***.

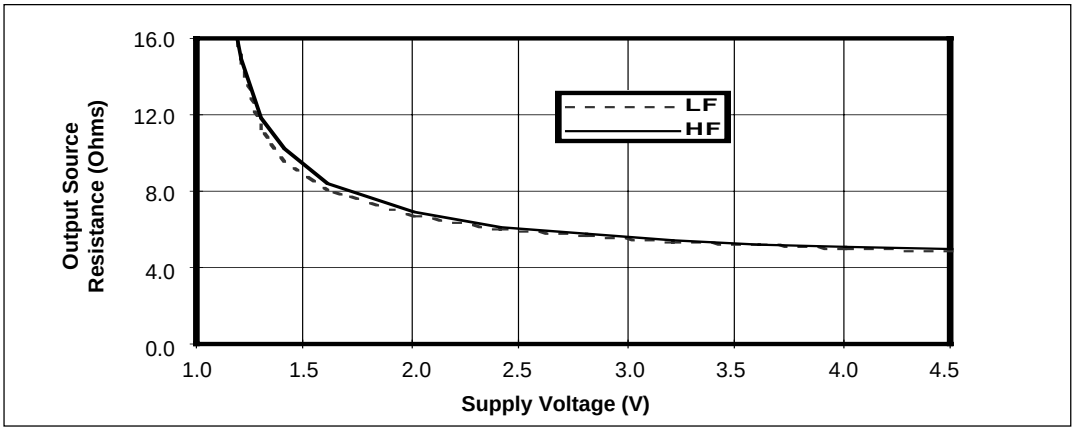


Figure 14. Output Source Resistance vs. Supply Voltage

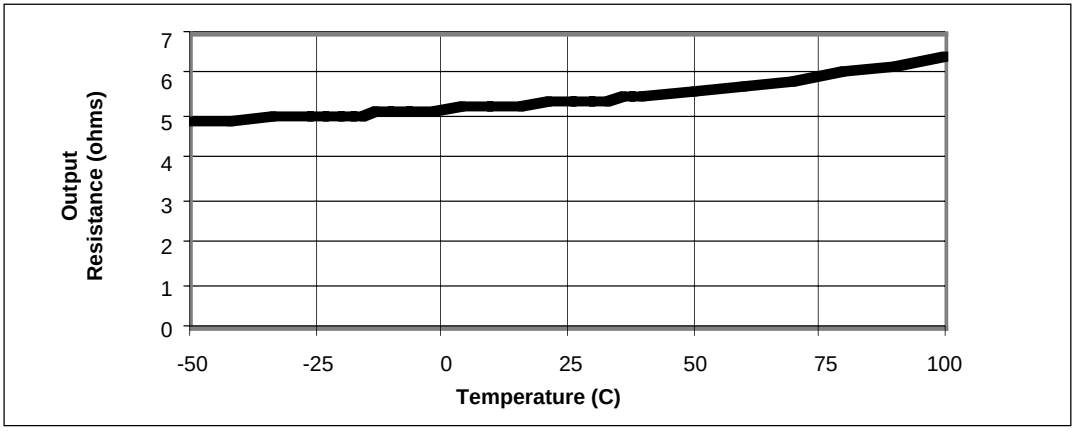


Figure 15. Output Source Resistance vs. Temperature Inverter LF

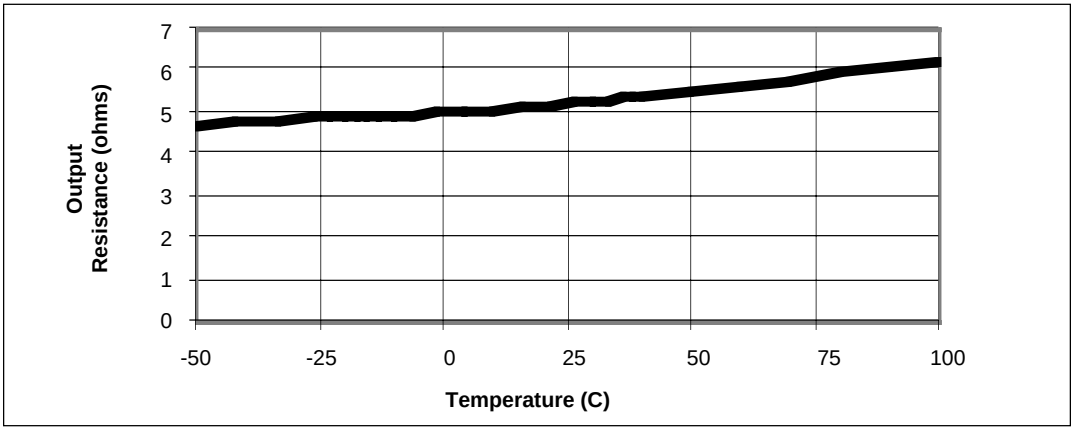


Figure 16. Output Source Resistance vs. Temperature where Inverter HF

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +3.6V, T_{AMB} = 25°C unless otherwise noted. LF = Low Frequency, FC = Open, C1 = C2 = 150µF.
HF = High Frequency, FC = V+, C1 = C2 = 22µF. Inverter Circuit use ***Figure 1***. Doubler Circuit use ***Figure 2***.

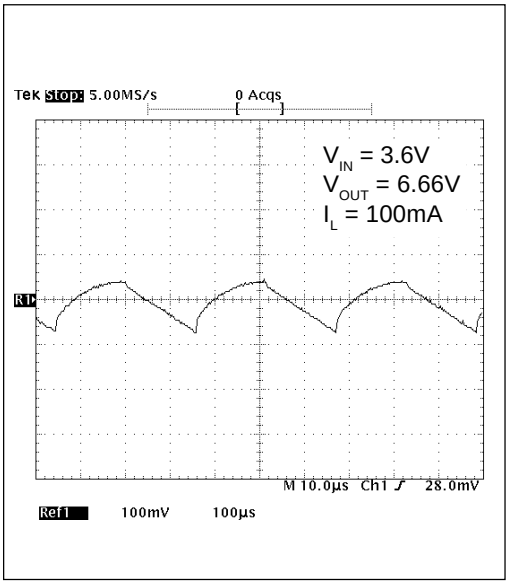


Figure 17. Output Noise and Ripple - Doubler LF

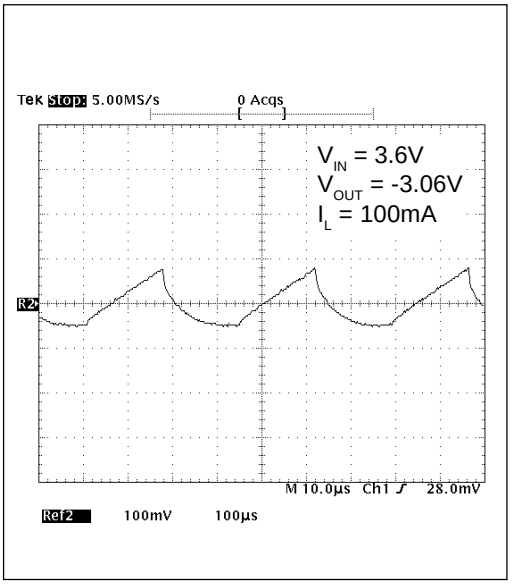


Figure 18. Output Noise and Ripple - Inverter LF

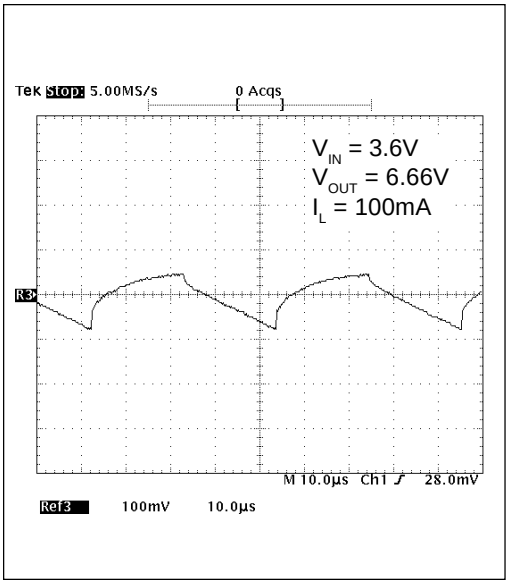


Figure 19. Output Noise and Ripple - Doubler HF

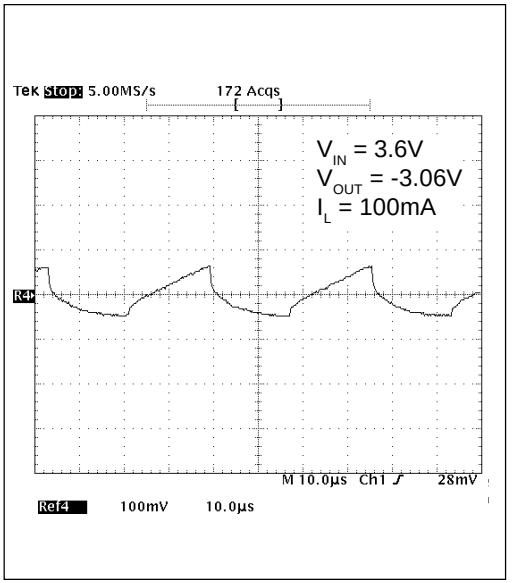


Figure 20. Output Noise and Ripple - Inverter HF

THEORY OF OPERATION

Negative Voltage Inverter

This is the most common application of the **SP6660** where a +1.5V to +4.25V input is converted to a -1.5V to -4.25V output. In the inverting mode, the **SP6660** is typically operated with LV connected to GND. Since the LV may be left open, the substitution of the **SP6660** for the ICL7660 industry standard is simplified.

The circuit for the voltage inverter mode can be found in ***Figure 21***. This operating circuit uses only two external capacitors, C1 and C2, for the internal charge pump. This allows designers to avoid any EMI concerns with the costly, space-consuming inductors typically used with switching regulators.

The **SP6660** is insensitive to load current changes. Output Source Resistance vs. Supply Voltage and Temperature curves are shown in ***Figures 14*** to ***16***. A typical output source resistance of 5.2Ω allows an output voltage of -4.25V under light load with an input of +4.25V. This output voltage decreases to only -4.0V with a load current draw of 100mA.

The peak-to-peak output ripple voltage is calculated as follows:

$$V_{RIPPLE} = \frac{I_{OUT}}{2(f_{PUMP})(C2)} + I_{OUT}(ESR_{C2})$$

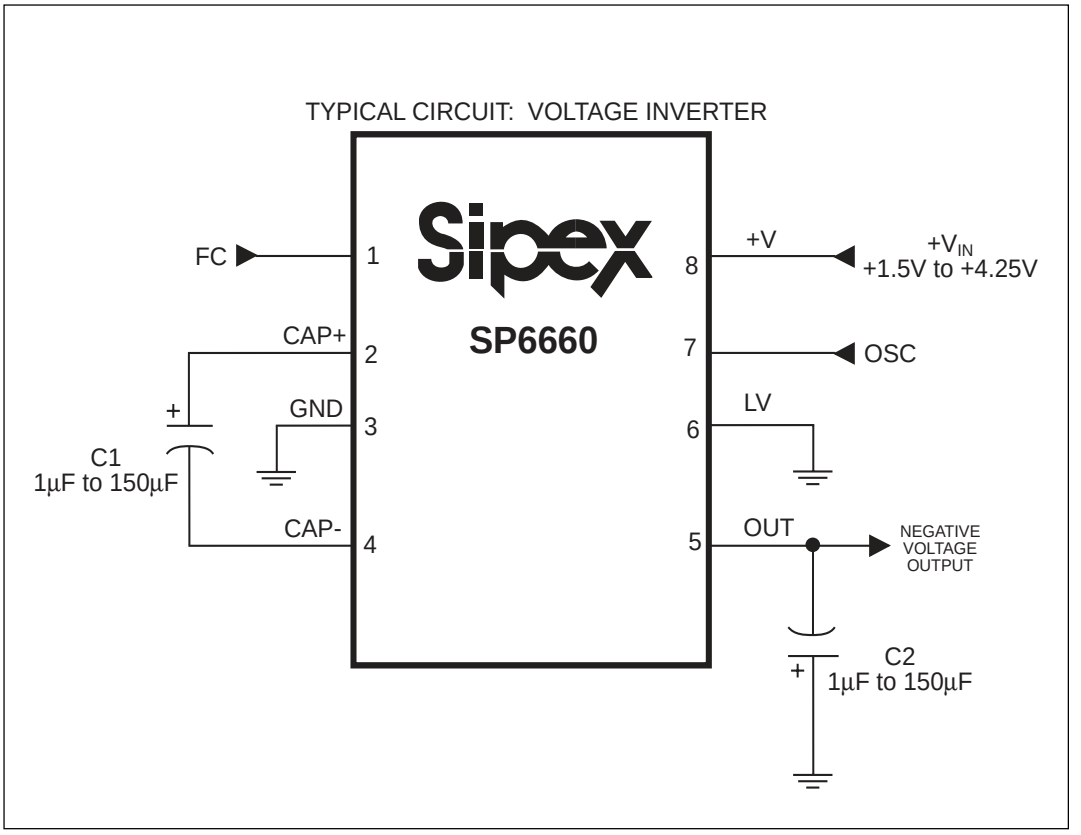


Figure 21. Typical Operating Circuit for the Voltage Inverter

For a nominal f_{PUMP} of 5kHz (where f_{OSC}=10kHz) and C2=150µF with an ESR of 0.2Ω, the ripple is approximately 90mV with a 100mA load current. If C2 is raised to 390µF, the ripple drops to 45mV. The output ripple voltage is calculated by noting that capacitor C2 supplies the output current during one-half of the charge pump cycle.

OSC is internally connected to a 15pF capacitor. An external capacitor can be added to slow the oscillator. Designers should take care to minimize stray capacitance. An external oscillator may also be connected to overdrive OSC. Refer to the **Oscillator Control** section for further details.

Positive Voltage Doubler

The **SP6660** can double the output voltage of an input power supply or battery. From a +4.25V input, the circuit in ***Figure 22*** can provide 100mA with +8.0V at V+. The no-load voltage output at V+ is $2(V_{INL})$.

LV may be tied to OUT pin for all input voltages in the positive voltage doubler mode. Connect the power-supply positive voltage input to GND pin. Connect the power-supply ground input to OUT pin. V+ is the positive voltage output in this mode.

Designers may overdrive OSC in the positive voltage doubler mode. Refer to the **Oscillator Control** section for further details.

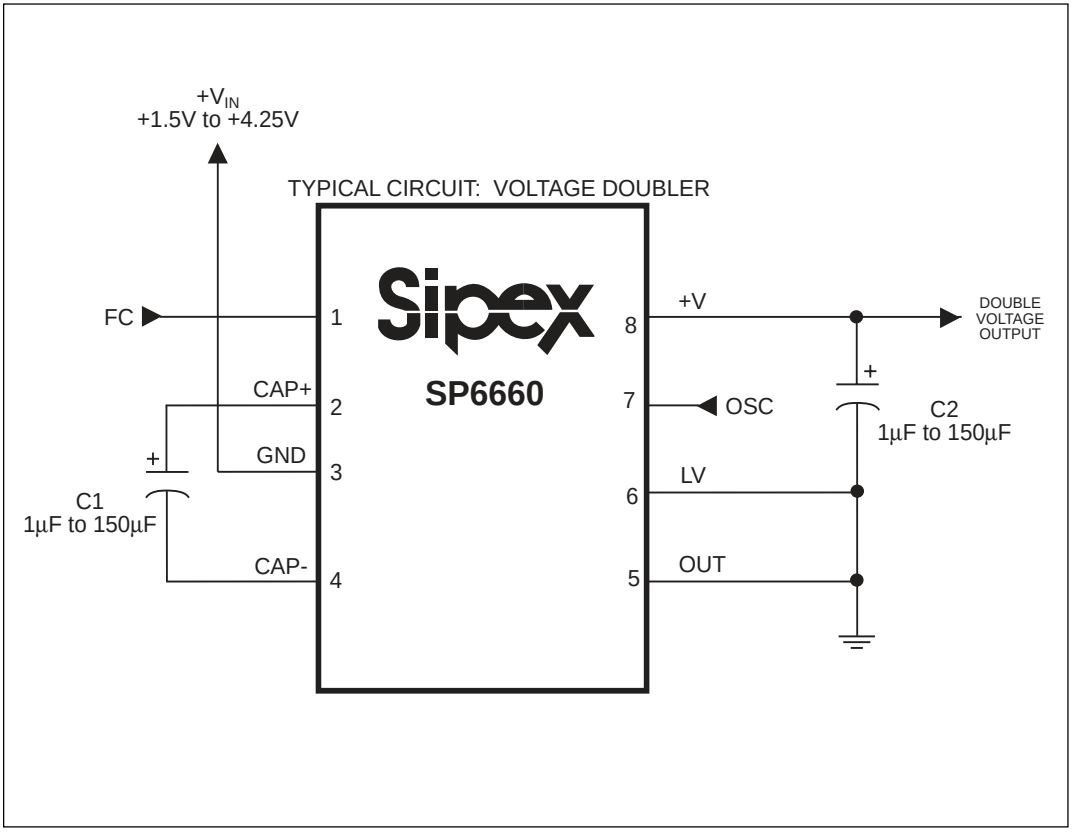


Figure 22. Typical Operating Circuit for the Positive Voltage Doubler

FC	OSC	Oscillator Frequency
open	open	10kHz typical
V+	open	80kHz typical
open or V+	external capacitor	refer to **Figure 11**
open	external clock	external clock frequency

Figure 23. Four control modes for the SP6660 Oscillator Frequency

Oscillator Control

Refer to ***Figure 23*** for a table of the four control modes of the **SP6660** internal oscillator frequencies. In the first mode, FC and OSC are open (unconnected) and the internal oscillator typically runs at 10kHz. OSC is internally connected to a 15pF capacitor.

In the second mode, FC is connected to V+. The charge and discharge current at OSC changes from 1.0µA to 8.0µA, increasing the oscillator frequency eight times to 80kHz.

In the third mode, the oscillator frequency is lowered by connecting a capacitor between OSC and GND. FC can still multiply the frequency by eight times in this mode, but for a lower range of frequencies. Refer to ***Figure 11*** for these ranges.

In the fourth mode, any standard CMOS logic output can be used to drive OSC. OSC may be overdriven by an external oscillator that swings between V_{IN} and GND. When OSC is overdriven, FC has no effect.

Unlike the 7660 and 660 industry standards, designers may overdrive the oscillator of the **SP6660** in both the inverting and the Voltage Doubling Mode.

Optimizing Loss Conditions

Losses in **SP6660** applications can be anticipated from the following:

1. Output Resistance:

$$\mathbf{V_{LOSS\Omega} = I_{LOAD} \times R_{OUT}}$$

where $V_{LOSS\Omega}$ is the voltage drop due to the **SP6660** output resistance, I_{LOAD} is the load current, and R_{OUT} is the **SP6660** output resistance.

2. Charge Pump Capacitor ESR:

$$\mathbf{V_{LOSSC1} \approx 4 \times ESR_{C1} \times I_{LOAD}}$$

where V_{LOSSC1} is the voltage drop due to the charge pump capacitor, C1, ESR_{C1} is the ESR of C1, and I_{LOAD} is the load current. The loss in C1 is larger than the loss in the reservoir capacitor, C2, because it handles a current almost four times larger than the load current during charge-pump operation. As a result of this, a change in the capacitor ESR has a much greater impact on the performance of the **SP6660** for C1 than for C2.

3. Reservoir Capacitor ESR:

$$\mathbf{V_{LOSSC2} = ESR_{C2} \times I_{LOAD}}$$

where V_{LOSSC2} is the voltage drop due to the reservoir capacitor C2, ESR_{C2} is the ESR of C2, and I_{LOAD} is the load current. Increasing the capacitance of C2 and/or reducing its ESR can reduce the output ripple that may be caused by the charge pump. A designer can filter high-frequency noise at the output by implementing a low ESR capacitor at C2. Generally, capacitors with larger capacitance values and higher voltage ratings tend to reduce ESR.

Optimizing Capacitor Selection

Refer to ***Figure 24*** for the total output resistance for various capacitance values and oscillator frequencies. The reservoir and charge pump capacitor values are equal. The capacitance values required to maintain comparable ripple and output resistance typically diminish proportionately as the pump frequency of the **SP6660** increases.

The test conditions for the curves of ***Figure 24*** are the same as for ***Figures 2*** to ***20*** for the circuits in ***Figures 1*** and ***2***; additional conditions are as follows:

C1 = C2 = 0.2Ω ESR capacitors
R_{OUT} = 4.2Ω

The flat portion of the curves shown at a 5.2Ω effective output resistance is a result of the **SP6660's** 5.25Ω output resistance where

$$\mathbf{5.2\Omega = R_{OUT(SP6660)} + (4 \times ESR_{C1}) + ESR_{C2}.}$$

Instead of the typical 5.2Ω, R_{OUT} = 4.2Ω is used because the typical specification includes the effect of the ESRs of the capacitors used in the test circuit in ***Figures 1*** and ***2***.

Refer to ***Figures 17, 18, 19*** and ***20*** for the output currents using 0.33µF to 220µF capacitors. Output currents are plotted for 3.0V and 4.5V inputs taking into consideration a 10% to 20% loss in the input voltage. The **SP6660** 5.2Ω series resistance limits increases in output current vs. capacitance for values much higher than 47µF. Larger values may still be useful to reduce ripple.

Designing a Multiple of the SP6660 Negative Inverted Output Voltage

The **SP6660** can be cascaded to allow a designer to provide a multiple of the negative inverted output voltage of a single **SP6660** device. The approximate total output resistance, R_{TOT}, of the cascaded **SP6660** devices is equal to the sum of the individual **SP6660** output resistance values, R_{OUT}. The output voltage, V_{TOT}, is a multiple of the number of cascaded **SP6660** devices and the output voltage of an individual **SP6660** device, V_{OUT}. Refer to ***Figure 25*** for the circuit cascading **SP6660** devices. Note that the capacitance value of C1 for the charge pump and C2 at V_{OUT} is multiplied respectively to the number of cascaded **SP6660** devices.

Connecting the SP6660 in Parallel

SP6660 devices can be connected in parallel to reduce the total output resistance. The approximate total output resistance, R_{TOT}, of the multiple devices connected in parallel is equal to the output resistance of an individual **SP6660** device divided by the total number of devices connected. Refer to ***Figure 26*** for the circuit connecting multiple **SP6660** devices in parallel. Note that only the charge pump capacitor value of C1 is multiplied respectively by the number of **SP6660** connected in parallel. A single capacitor C2 at the output voltage V_{OUT} of the "nth" device connected in parallel serves all devices connected.

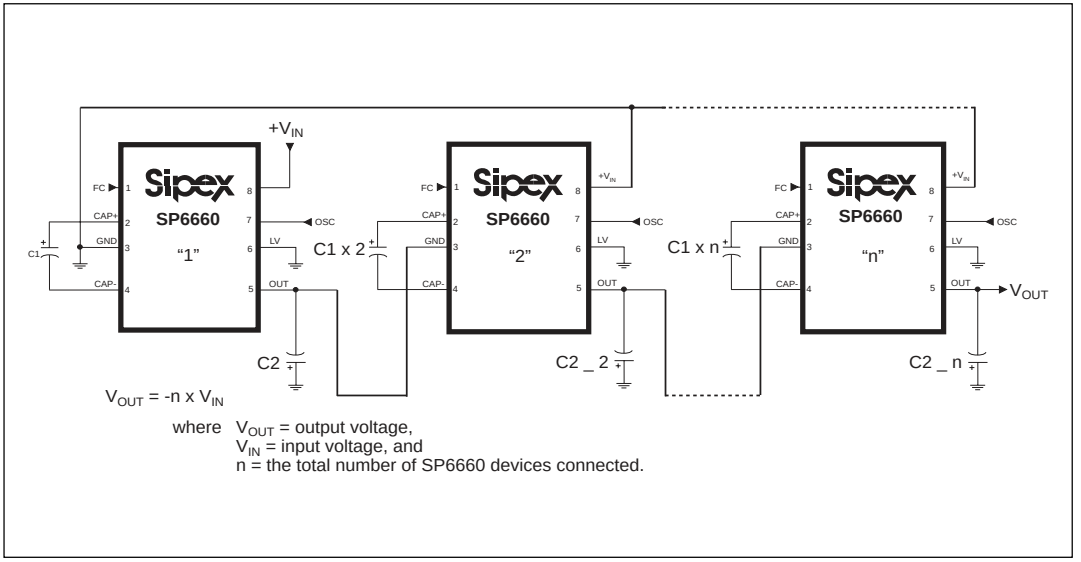


Figure 25. SP6660 Devices Cascaded to Provide a Multiple of a Negative Inverted Output Voltage

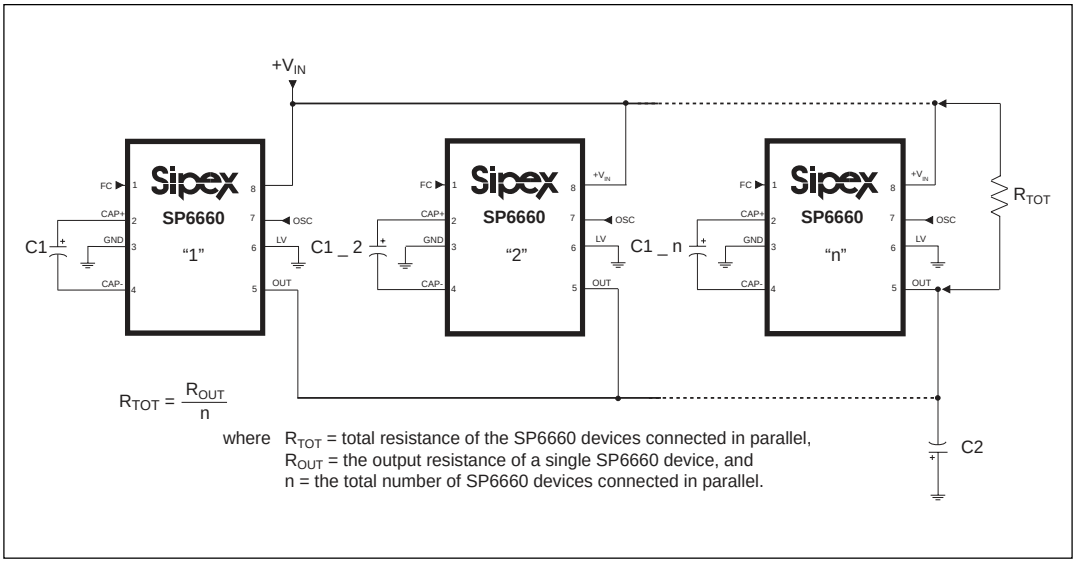


Figure 26. SP6660 Devices Connected in Parallel to Reduce Output Resistance

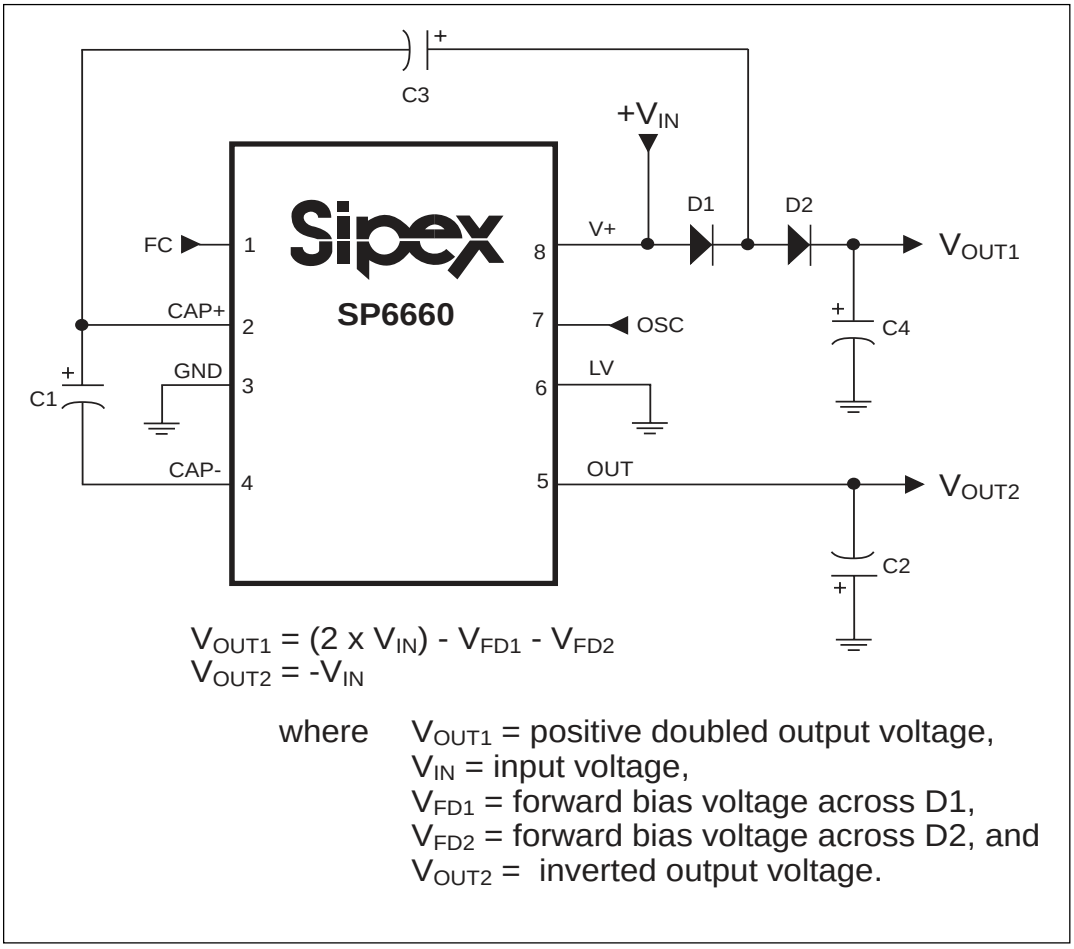


Figure 27. The SP6660 Connected for Negative Voltage Conversion with Positive Supply Multiplication

Circuit for Negative Voltage Conversion with Positive Supply Multiplication

A designer can use the circuit in ***Figure 27*** to provide both an inverted output voltage at V_{OUT1} and a positive multiple of V_{IN} at V_{OUT2} (subtracting the forward biased voltages of D1 and D2). Capacitor C1 is for the charge pump and capacitor C2 is for the reservoir function to generate the inverted output voltage at V_{OUT2}. Capacitor C3 is for the charge pump and capacitor C4 is for the reservoir function to generate the multiplied positive output voltage at V_{OUT1}. Designers should pay special attention to the possibility of higher source impedances at the generated supplies due to the finite impedance of the common charge pump driver.

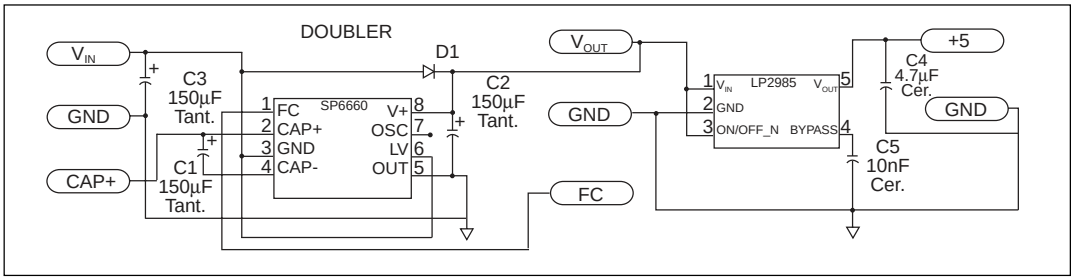


Figure 28. The SP6660 and a LDO Regulator Connected as a 3V Input to Regulated 5V Output Converter.

APPLICATIONS

The SP6660 Evaluation Board provides a 3V to 5V 160mA DC to DC Converter using the SP6660 Doubler Circuit and a 5V LDO Regulator.

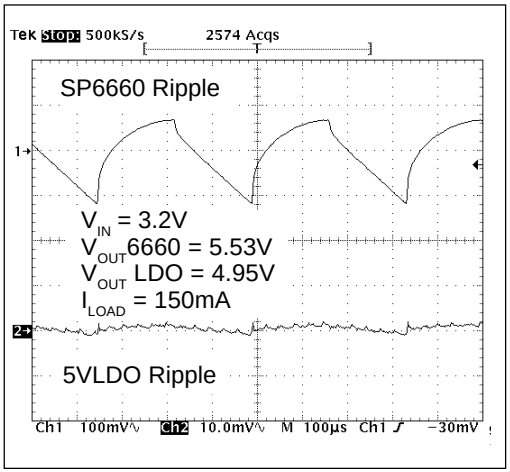


Figure 29. Ripple and Noise output of the SP6660 and a LDO Regulator with I_{LOAD} = 150mA

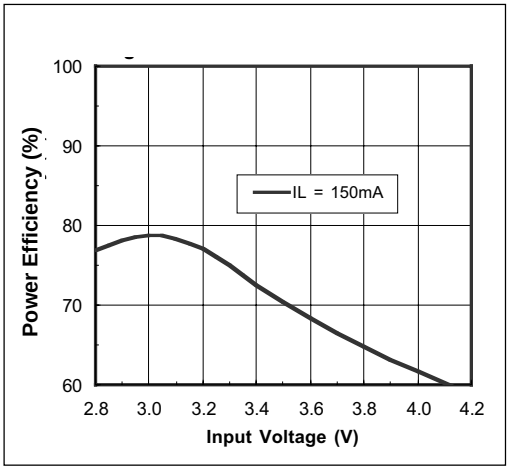


Figure 30. Power Efficiency vs Input Voltage - SP6660 Doubler with 5V LDO

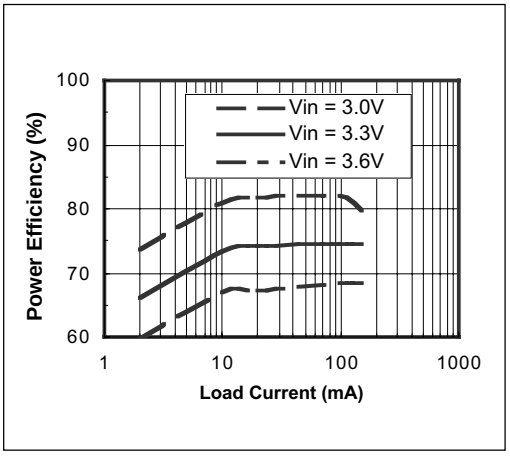


Figure 31. Power Efficiency vs Load Current - SP6660 Doubler with 5V LDO

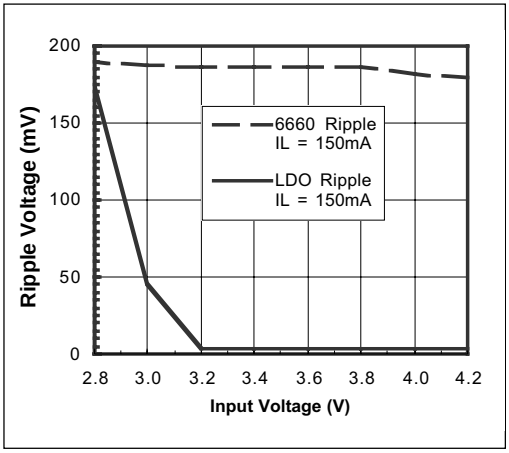
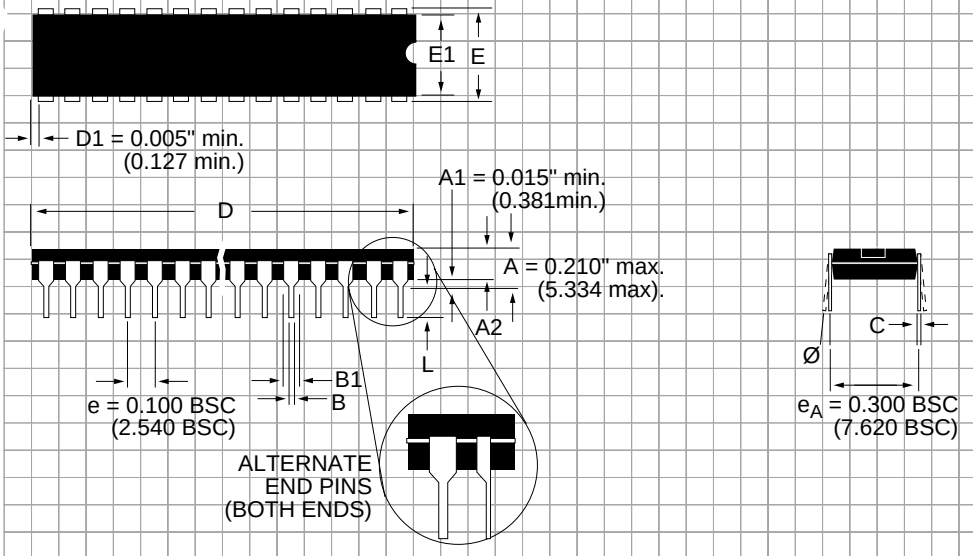


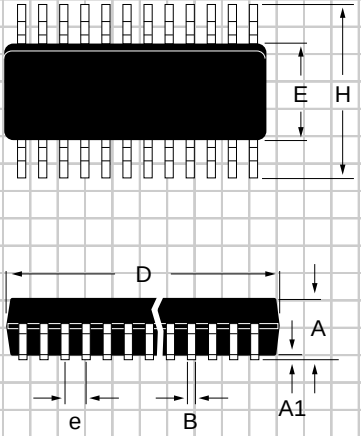
Figure 32. Ripple Voltage vs Input Voltage - SP6660 Doubler with 5V LDO

PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)



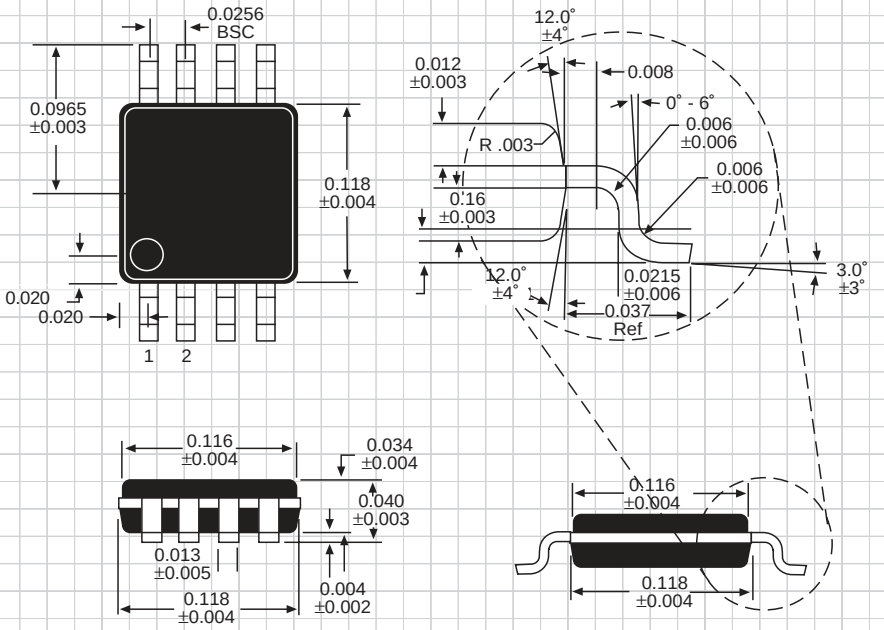
DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN	18–PIN	20–PIN	22–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)

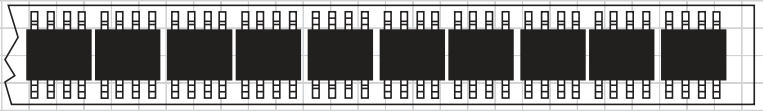


DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC MICRO SMALL OUTLINE (µSOIC)



All package dimensions in inches



50 µSOIC devices per tube

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6660CP	0˚C to +70˚C	8-Pin PDIP
SP6660EP	-40˚C to +85˚C	8-Pin PDIP
SP6660CN	0˚C to +70˚C	8-Pin NSOIC
SP6660EN	-40˚C to +85˚C	8-Pin NSOIC
SP6660CU	0˚C to +70˚C	8-Pin µSOIC
SP6660EU	-40˚C to +85˚C	8-Pin µSOIC
SP6660EB		Evaluation Board

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Available in lead free packaging. To order, add "-L" suffix to the part number.
Example: SP6660EU/TR=Tape & Reel. SP6660EU-L/TR = lead free.

SIGNAL PROCESSING EXCELLENCE

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