# HMC988LP3E

v04.1014

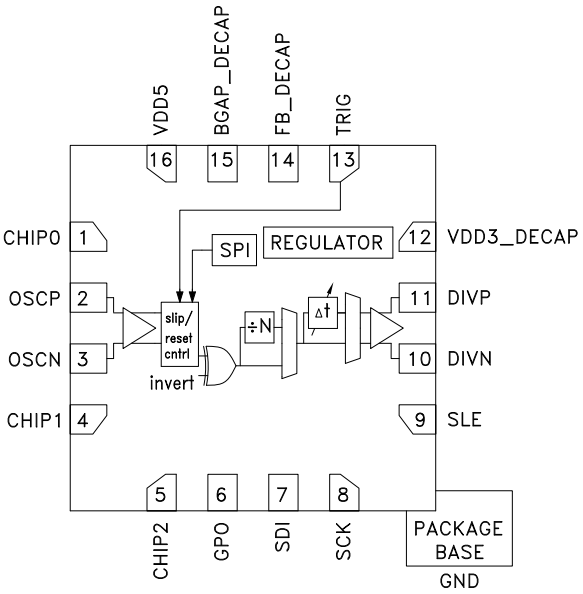
## PROGRAMMABLE CLOCK DIVIDER AND DELAY DC - 4 GHz

### Typical Applications

The HMC988LP3E is ideal for:

- Basestation Digital Pre-Distortion Paths(DPD)
- High Performance Automated Test Equipment(ATE)
- Backplane clock skew management
- Phase Coherence of multiple clock paths
- Clock Delay management to improve setup & hold time margins
- PCB signal flight time offset circuits
- Track and hold circuits for ADC/DACs

### Functional Diagram




### Features

DC - 4 GHz

-170 dBc/Hz floor @ 100 MHz output

-164 dBc/Hz floor @ 2 GHz output

Integrated Jitter 35 $fs_{RMS}$ @ 100 MHz output

13 $fs_{RMS}$ (calculated) @ 2 GHz output

Adjustable output phase with soft/hard reset sync

Adjustable output delay in 60 steps of 20 ps

Flexible Input Interface:

LVPECL,LVDS,CML,CMOS Compatible

AC or DC Coupling

On - Chip Termination 50 Ω (100 Ω Differential)

Output Driver (LVPECL):

800 mVpp LVPECL into 50 Ω Single-Ended (+3 dBm Fo)

Up to 8 addressable dividers per SPI bus

3.3 V operation or 5 V operation with Optional on-chip regulator for best performance

3 x 3 QFN Leadless SMT Package

### General Description

The HMC988LP3E is a an ultra low noise clock divider capable of dividing by 1/2/4/8/16/32. It is a versatile device with additional functionality including adjustable output phase, adjustable delay in 60 steps of ~ 20 ps, a clock synchronization function, and a clock invert option.

Housed in a compact 3x3 mm SMT QFN package, the clock divider offers a high level of functionality. The device works with 3.3 V supply or may be connected to 5 V supply and utilize the optional on-chip regulator. This on-chip regulator may be bypassed.

Up to 8 addressable HMC988LP3E devices can be used together on the SPI bus.

The HMC988LP3E is ideally suited for data converter applications with extremely low phase noise requirements.



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*Application Support: Phone: 1-800-ANALOG-D*

## Table 1. Electrical Specifications

Unless otherwise specified: T = +25 °C. Current consumptions assumes fine adjustable delay is disabled. Phase noise degrades approximately 15 dB if using fine delay adjustment.

| Parameter | Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| OSCP/N Input Frequency Range | | DC | | 4 | GHz |
| DIVP/N Output Frequency Range | | DC | | 4 | GHz |
| Divide Ratios | | | 1/2/4/8/16/32 | | |
| Maximum Fine Delay Adjust Frequency | | DC | | 1 | GHz |
| VDD | with on-chip regulator | +3.7 | +4.5 | +5.5 | V |
| VDD | bypass on-chip regulator | +3.1 | +3.3 | +3.5 | V |
| Input Swing (LVPECL or AC) | | | 0.800<br>See Figure 9 | | Vpp |
| Output Swing (LVPECL) [1] | Measured into a 50ohm Load | | 0.8 (single ended) | | Vpp |
| | Measured into a 50ohm Load | | 1.6 (differential) | | Vppd |
| Rise/Fall Time (LVPECL OUT) | 20%/80% | | 90 | | ps |
| OSCP/N Input Commom Mode DC Bias [2] | | +1.6 | +2 | +2.5 | V |
| DIVP/N Output Common Mode Voltage [1] | | | +2 | | V |
| Phase Noise (@100 MHz offset) [3]<br>@ 100 MHz output<br>@ 500 MHz output<br>@ 1 GHz output<br>@ 2 GHz output | | | <br>-170<br>-168<br>-166<br>-164 | | dBc/Hz |
| Jitter Density [4]<br>@ 100 MHz output<br>@ 500 MHz output<br>@ 1 GHz output<br>@ 2 GHz output | | | <br>7.1<br>1.8<br>1.1<br>0.7 | | asec/√Hz |
| Integrated Jitter (12k - 20MHz) [5]<br>@ 100 MHz output<br>@ 500 MHz output [6]<br>@ 1 GHz output [6]<br>@ 2 GHz output [6] | | | <br>32<br>8<br>5<br>3.2 | | fsec |
| FOM (Figure of Merit) Noise Floor | Noise Floor = FOM+10Log(Fout) | | -254 | | dBc/Hz |
| Coarse Delay Adjustment Range | | | 1/2 to ∞ *$T_{INPUT}$ | | Input Cycles |
| Fine Delay Adjustment Range [7] | 60 steps of ~ 20 ps; Delay compresses with increasing frequency. See Figure 6. With divider bypassed maximum frequency limited to 650MHz | 300 | | 1500 | ps |
| Fine Delay Adjustment Resolution | | | 20 | | ps |
| Fine Delay Adjustment Step Count | | | 60 | | |
| PSRR [8] | | | | | |
| With Regulator | AM | -70 | | -80 | dBc |
| | PM | -80 | | -92 | dBc |



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# PROGRAMMABLE CLOCK DIVIDER AND DELAY DC - 4 GHz



## Table 1. Electrical Specifications

Unless otherwise specified: T = +25 °C. Current consumptions assumes fine adjustable delay is disabled. Phase noise degrades approximately 15 dB if using fine delay adjustment.

| Parameter | Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Bypass Regulator | AM | -40 | | -50 | dBc |
| | PM | -50 | | -70 | dBc |
| Current Consumption | | | | | |
| Stand-by Current - Chip Disabled | using Regulator case | | 0.7 | | mA |
| | bypass Regulator case | | 0.01 | | mA |
| Mininum Current [9] | | | 68 | | mA |
| Additive Divider | | | 16 | 21 | mA |
| Delay Line Current | | | 12 | 44 | mA |
| LVPECL Termination Load Current | | | 26 | 40 | mA |
| Propagation Delay | Delay Line Disabled | | 210 | | ps |
| Delay vs Temp | 250 MHz (Setpoint 15) | | | 350 | fs/ °C |
| | 1 GHz (Setpoint 15) | | | 150 | fs/ °C |
| **Logic Inputs: CHIP0, CHIP1, CHIP 2, SLE,SDI, SCK, TRIG** | | | | | |
| Input Logic Low, Vil | | | | 0.9 | V |
| Input Logic High, Vih | | 2.1 | | | V |

[1] Using standard LVPECL termination as shown in Figure 9
[2] When Reg04[03]=1, Default Setting=0
[3] Phase noise performance is characterized using the HMC1034 as a source at ~2 GHz, 9 dBm differential. For sinusoidal low-frequency inputs, the phase noise may degrade. For example, a single-ended 100 MHz 9 dBm sin-wave in bypass mode produces a phase noise floor of -164 dBc/Hz as opposed to -170 dBc/Hz.
[4] To calculate Jitter Density, (√2*10^((Floor phase noise)/20)/2π)*(1/frequency) i.e jitter density@ 500 MHz = (√2*10^(-168/20)/2π)*(1/500000000)
[5] Integrated Bandwidth start from 12 KHz to 20 MHz, Jitter Density x √Desired customized BW i.e integrated jitter @ 2 GHz over a 6 GHz BW = 0.7 asec/√Hz x √6 GHz 1asec = 1/1000 of a femtosecond. Only 100 MHz number is meaured with 100 MHz Wenzel and HMC988 in bypass mode
[6] These integrated jitter number are based on calculation.
[7] The fine delay adjustment is valid up to a 1 GHz output frequency. Maximum frequency is 650MHz with divider bypassed (divide-by-1).
[8] Spur caused by 100 mVpp Agressor tone on input supply. This specification is the level of the SSB spur which appears symmetrically around the output frequency when the input supply stimulated by a 100 mVpp aggressive tone @ 30 kHz. The spur level is linearly proportional to the aggressor tone amplitude. It is relatively independent of input and output frequencies, and input power level. When regulated, at least 3.7 V must be applied to the input power supply to provide sufficient PSRR. The spur level is not appreciably different for single ended or differential operation. The frequency response to the aggressive tone is flat from 1 kHz to 50 kHz offset. Above 50 kHz the solution PSRR improves strongly, but is largely dependant on board decoupling capacitance and is not a direct indication of the raw part performance.
[9] When Divider is bypassed,no termination loads and delay line disabled case.



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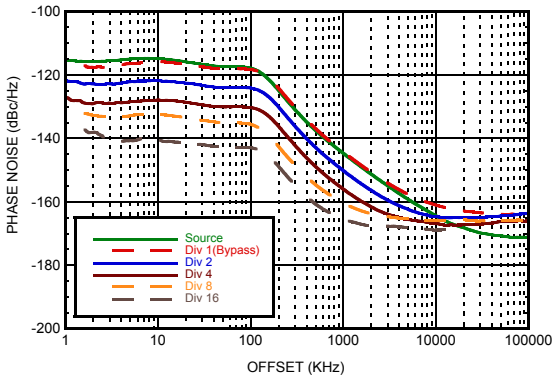
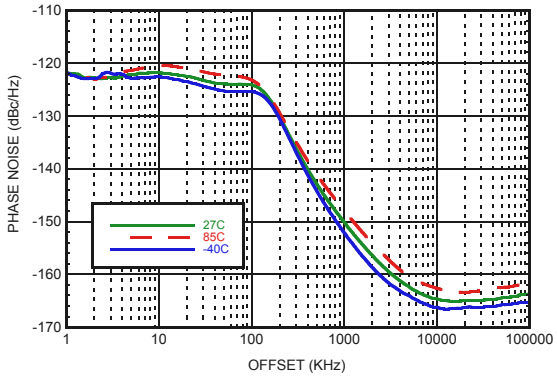
## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T = 27 °C, Regulated VDD = 3.3 V, 1.5 GHz, 6 dBm in, AC coupled single ended input and output, 120 Ω/leg DC termination, AC coupled into 50 Ω measuring load.

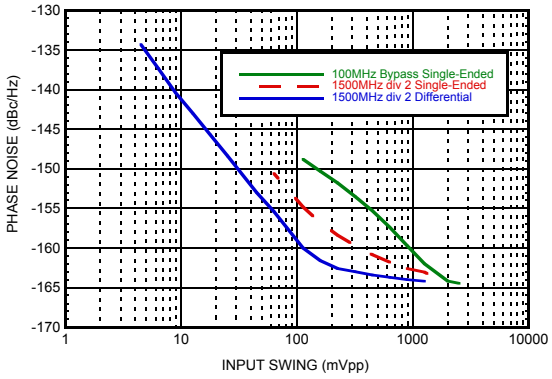
### Figure 1. Phase Noise Performance vs Divider Ratio at 1.5 GHz Div 1/2/4/8/16



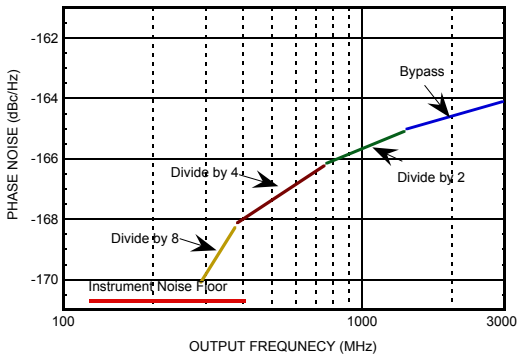

### Figure 2. Phase Noise Performance vs Temperature at 1.5 GHz Div 2



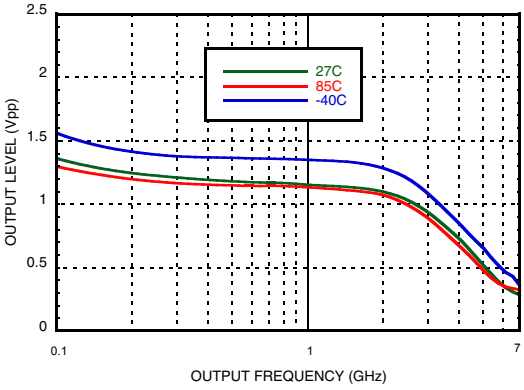

### Figure 3. Phase Noise Floor Performance Vs Input Swing



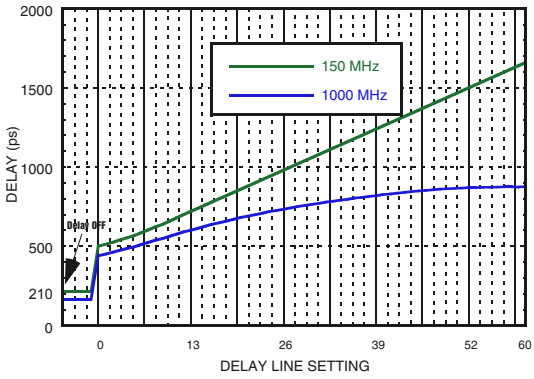

### Figure 4. Phase Noise Floor Performance Vs Output Frequency [1]




### Figure 5. VOUT Vs Frequency over Temperature [2]




### Figure 6. Delay Vs Delay line Setpoint [3]




[1] Measured Differential input and out at various frequencies. Under 300 MHz, the measurment is restricted by the instrument.

[2]Measured single-ended. 120 Ω DC termination, 3.3 V 1 +6 dBm single-ended input. HMC988LP3E AC coupled to 50 Ω instrument with divider bypass

[3]Corrected for board delay 210 ps



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**Figure 7. S-Parameters-S22 [4]**

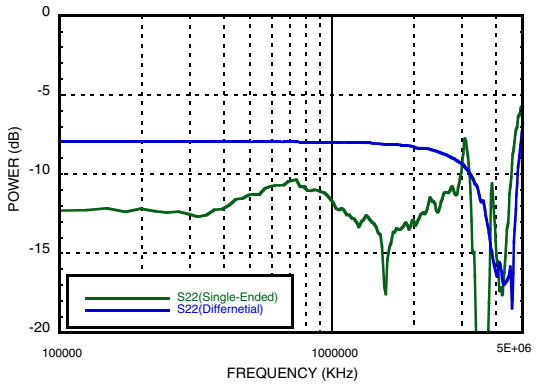



**Figure 8. S-Parameters-S11 [4]**

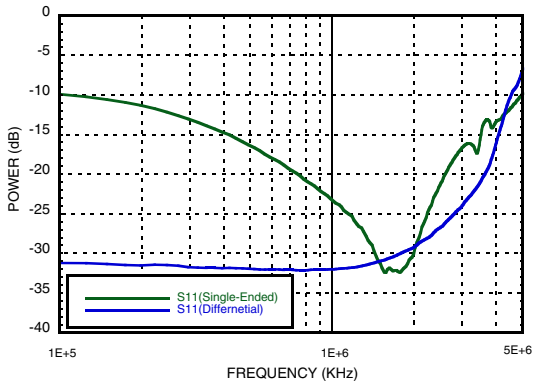



**Figure 9. Input Sensitivity[5]**

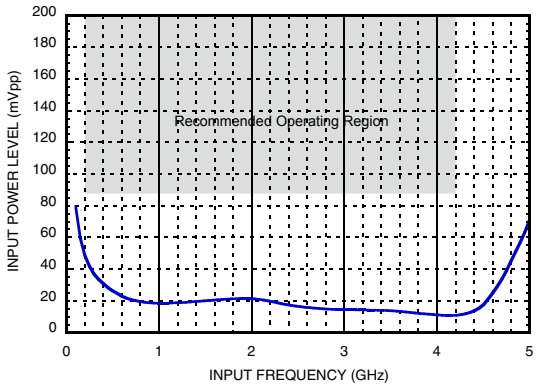



**Figure 10. Supply Voltage vs input Voltage [6]**

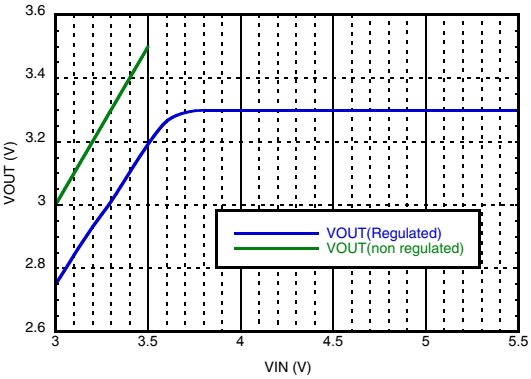
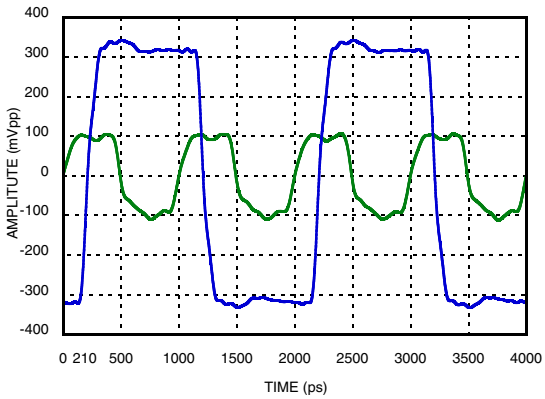



**Figure 11. Time Domain 1 GHz input, 500 MHz Output [7]**




[4] Measured with 200 Ω DC termination, 10 Ω series resistor in front, AC couple 1 nF 3.3 V
[5] Measured single-ended. 120 Ω DC termination, 3.3 V HMC988LP5E AC coupled to 50 Ω instrument(DSO8104B) with divider bypass. ESD diode will start to turn on if maximum input power exceeds 12 dBm.
[6] On Chip regulator enable mode measured at PIN CAP_3V Vs regulator bypass mode
[7] Measured with 1 GHz 400 mVpp source as single ended input, HMC988LP3E div 2. Board delay 210 ps



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**Table 2. Pin Descriptions**

| Pin Number | Function | Description |
|---|---|---|
| 1,4,5 | CHIP0, CHIP1, CHIP2 | Chip SPI Address |
| 2,3 | OSCP, OSCN | Differential Signal Input |
| 6 | GPO | General Purpose Output Pin & Serial Data Out |
| 7 | SDI | Serial Data Input |
| 8 | SCK | Serial Data Clock |
| 9 | SLE | Serial Data Latch Enable |
| 10,11 | DIVN, DIVP | Differential Output Signal |
| 12 | VDD3_DECAP | Decoupling point for internally generated supply |
| 13 | TRIG | External SYNC or SLIP Control Pin for slip/synchronization start |
| 14 | FB_DECAP | Decoupling point for regulator |
| 15 | BGAP_DECAP | Decoupling point for regulator |
| 16 | VDD5 | Regulator Input Supply Voltage |



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**Table 3. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Max Vdd to paddle on suply pin | -0.3 V to +5.5 V |
| OSCP, OSCN Max RF Power | 13 dBm |
| OSCP, OSCN Differential DC | -0.3 V to 3.6 V |
| LVPECL Min Output Load Resistor | 100 Ω to GND |
| LVPECL Output Load Current | 40 mA/leg |
| Digital Load | 1 kΩ min |
| Digital Input Voltage Range | -0.3 V to 3.6 V |
| Thermal Resistance (Jxn to Gnd Paddle) | 25 °C/W |
| Operating Temperature Range | -40 °C to +85 °C |
| Storage Temperature Range | -65 °C to + 125 °C |
| Maximum Junction Temperature | +125 °C |
| Reflow Soldering | |
| Peak Temperature | 260 °C |
| Time at Peak Temperature | 40 sec |
| ESD Sensitivity HBM | Class 1C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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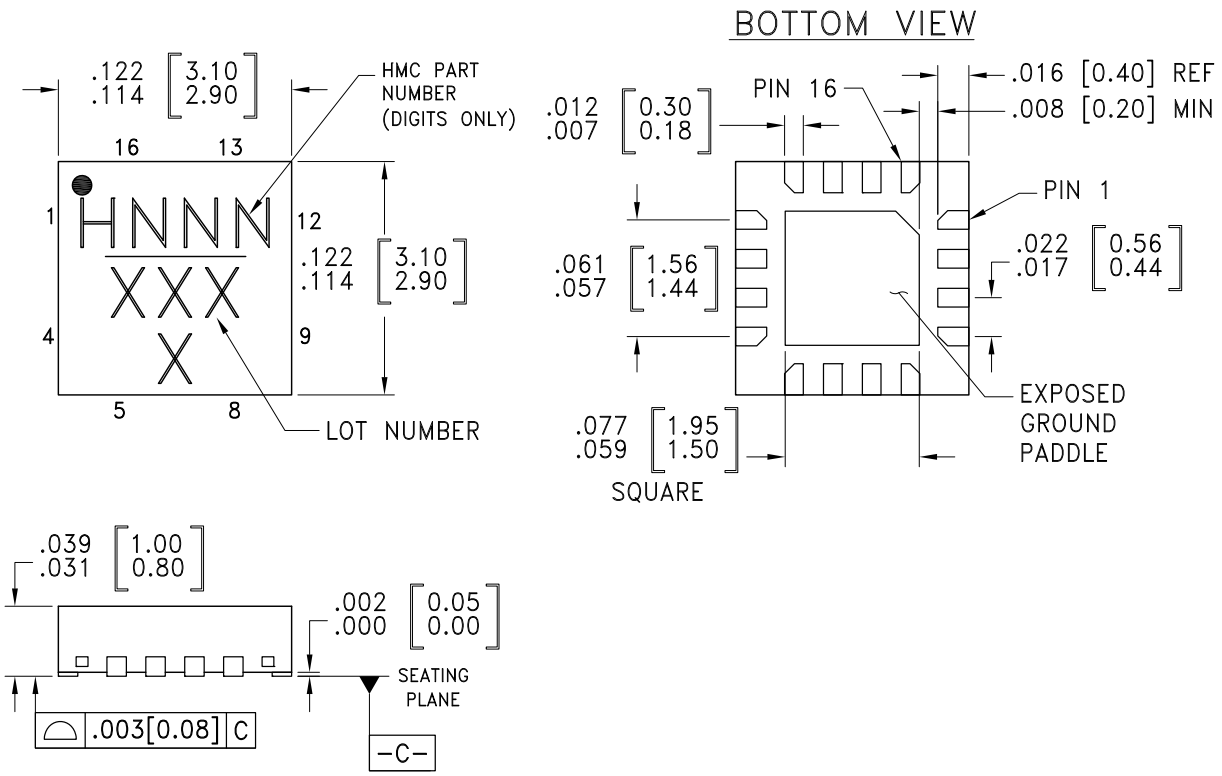
## Outline Drawing




NOTES:

[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.

[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.

[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.

[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].

[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.

[6] PAD BURR LENGTH SHALL BE 0.15 mm MAX. PAD BURR HEIGHT SHALL BE 0.05 mm MAX.

[7] PACKAGE WARP SHALL NOT EXCEED 0.05 mm

[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

**Table 4. Package Information**

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [1] |
|---|---|---|---|---|
| HMC988LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1[2] | H988<br>XXXX |

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C



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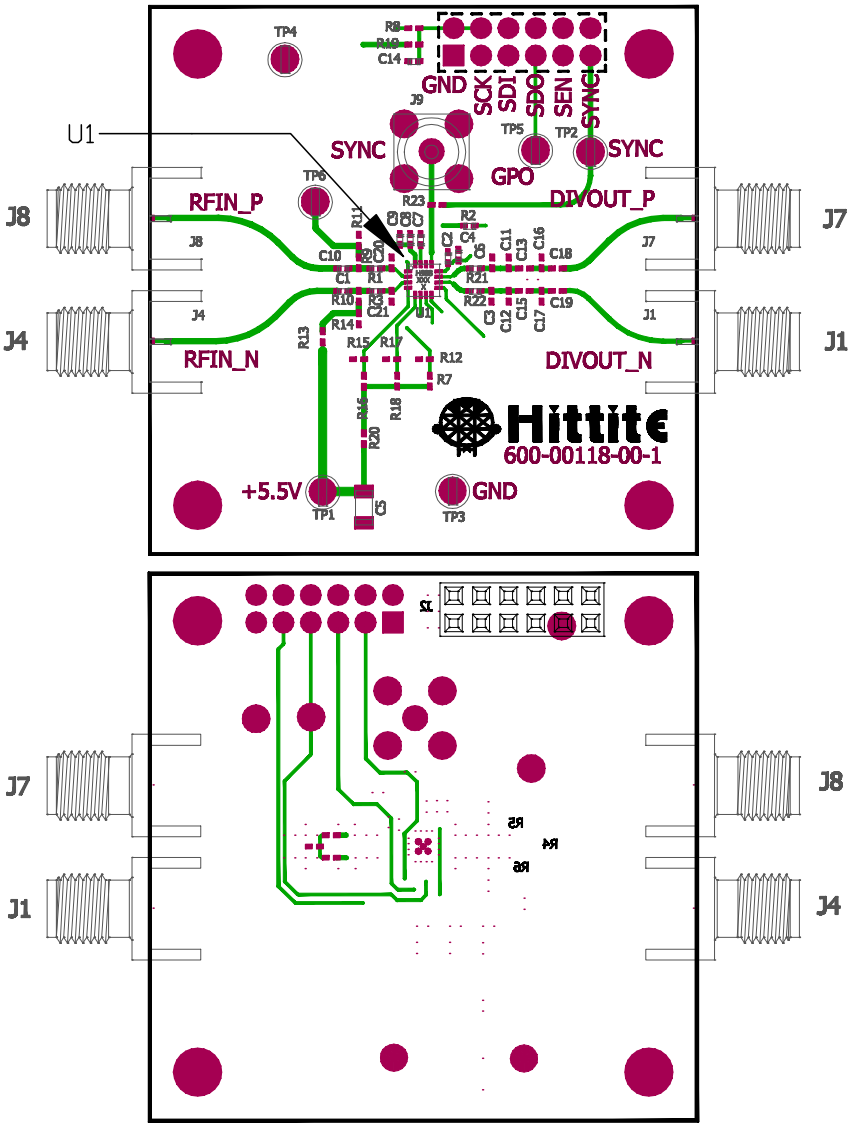
### Evaluation PCB




The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ω impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

## Evaluation PCB Schematic

*To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC988LP3E from the "Search by Part Number" pull down menu to view the product splash page.*



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**Table 5. Evaluation Order Information**

| Item | Contents | Part Number |
|---|---|---|
| Evaluation PCB Only | HMC988LP3E Evaluation PCB | EVAL01-HMC988LP3E |
| Evaluation Kit | HMC988LP3E Evaluation PCB<br>USB Interface Board<br>6' USB A Male to USB B Female Cable<br>CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software) | EKIT01-HMC988LP3E |





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## Theory of Operation

In addition to HMC988LP3E excellent low noise performance, the device offers additional functionality including:

Modular Configuration

Synchronization Function

Adjustable Fine Delay

Adjustable Coarse Delay

Trigger Options

Optional On-Chip Regulator

GPO

### Modular Configuration

The HMC988LP3E has been designed so that up to 8 devices can be placed on one SPI bus. The part has a 3-bit addressable chip addresses (CHIP0 pin, CHIP1 pin, CHIP2 pin) so that each chip can be controlled individually. In addition, HMC988LP3E has a broadcast mode which allows up to 8 HMC988LP3E devices to be simultaneously controlled, or triggered. In Broadcast mode each HMC988LP3E device will listen to the same chip address, namely "111." Typical application of HMC988LP3E is shown in Figure 1.

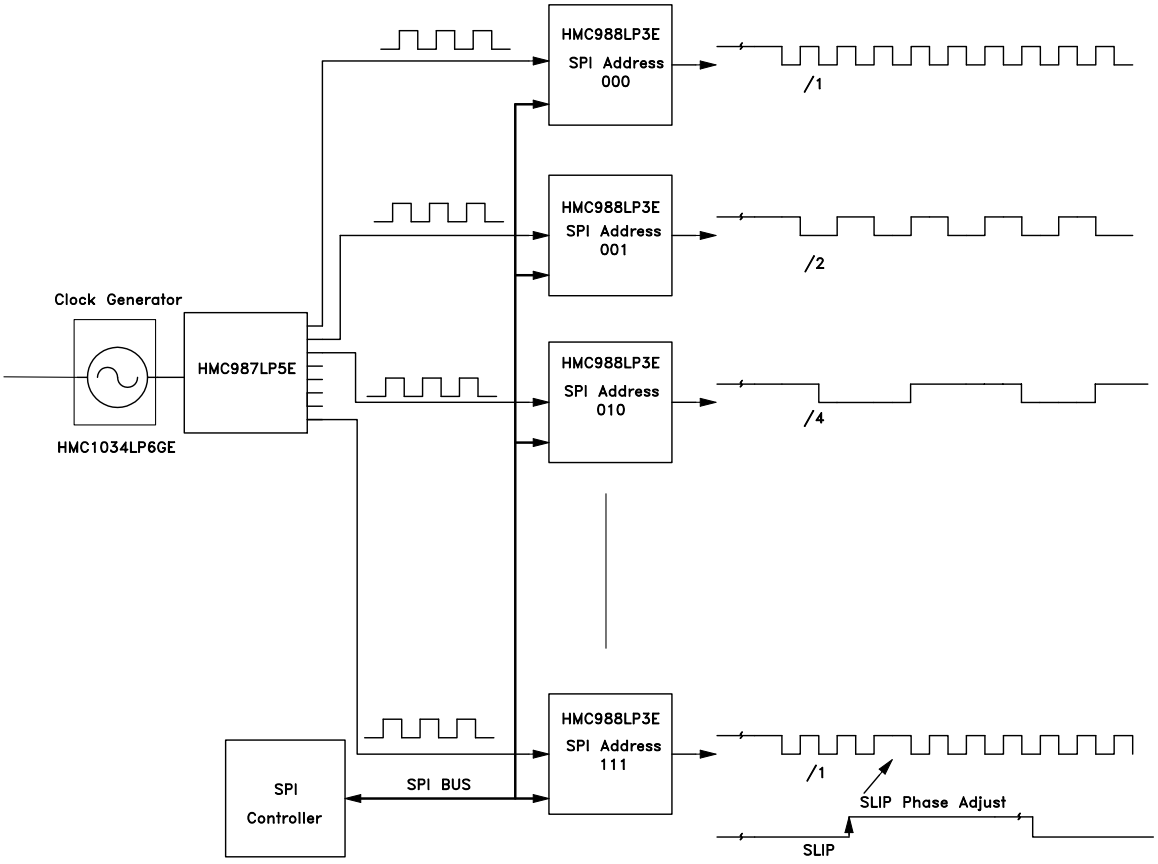


*Figure 1. Typical application of HMC988LP3E*



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Although the HMC988LP3E has only 8 SPI chip addresses, one of which ("111") is used in the broadcast mode, it is still possible to use broadcast mode and control 8 HMC988LP3E devices on one SPI bus, according to the following procedure:

Communicate with first 7 HMC988LP3E devices in a standard SPI mode. Select their chip addresses and write to the registers of interest.

1. After communicating with first 7 devices, with chip addresses ranging from ("000" to "110"), ensure that Broadcast Mode for all of them is disabled by writing to Reg04h[0] = "0" to each device.
2. Communicate with the 8th device, with Chip addresses ("111") in standard mode. The rest of the devices will not be listening because their Broadcast Mode is disabled (Reg04h[0] = "0").
3. If a broadcast to all devices on the SPI bus is required, Broadcast Mode needs to be enabled (Reg04h[0] = "1") for each device separately. After the Broadcast Mode is enabled in each device, the SPI controller can write to the SPI bus in a standard way while selecting chip address ("111"). All of the HMC988LP3E devices will be listening.

### *Synchronization Function*

If the HMC988LP3E is used in a typical application as shown in Figure 1, it may be advantageous for some or all of the outputs to be synchronized. The HMC988LP3E can accomplish this using its SYNC functionality. The SYNC feature is limited to low frequency (100MHz maximum) input clocks due to the internal rise time and delay on the internal trigger signal path.

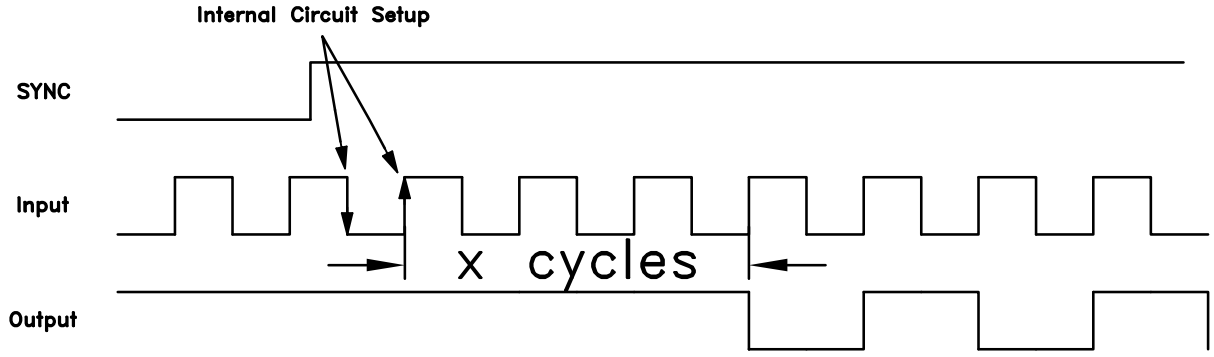


*Figure 2. HMC988LP3E SYNC Function Timing Diagram*

As shown in Figure 2, the Sync function ensures that all outputs launch synchronously, a number of input cycles after the the SYNC function is triggered. The delay, measured in the number of input cycles, is governed by equation 1 where x is the number of input cycles and N is the divide ratio selection (Reg02h[2:0]) of HMC988LP3E.

$$x = \begin{cases} \text{NA: Output disabled} & \text{if } N = 1 \\ \left(\frac{N}{2}\right) + 1 & \text{if } N > 1 \text{ and Reg06h[2]=0} \\ \left(\frac{N}{2}\right) + 2 & \text{if } N > 1 \text{ and Reg06h[2]=1} \end{cases}$$



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### Adjustable Coarse Delay

The HMC988LP3E provides the option to delay the output one cycle of the input signal using its SLIP function. This function in essence prevents the input signal from cycling for 1 period and causes a corresponding phase shift in the output signal. Timing diagram of the execution of the Slip function is show in Figure 3.

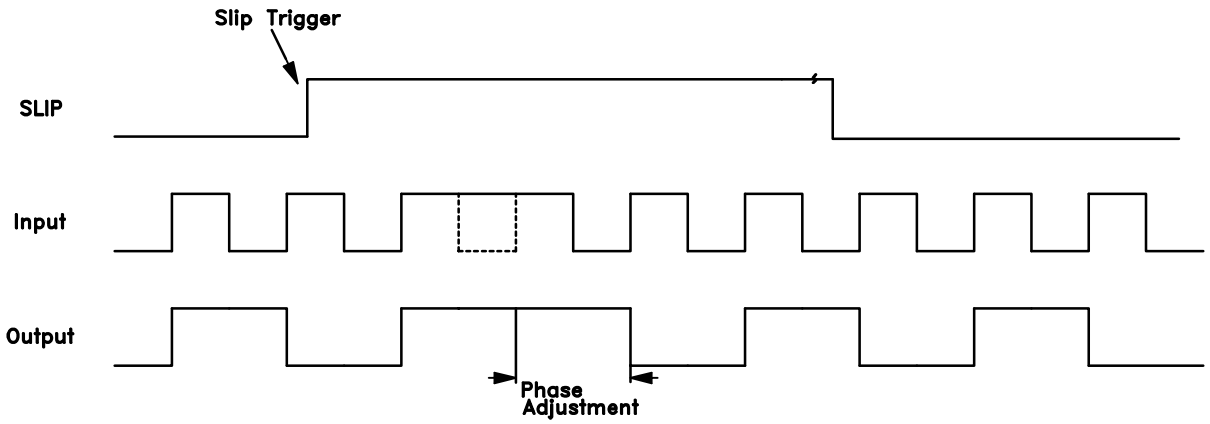


*Figure 3. HMC988LP3E's SLIP Function Timing Diagram*

In addition, the HMC988LP3E allows the user to select the launch phase of the output signal relative to the input signal by programming Reg06h[2]. When this functionality is used in conjunction with the Slip function, it allows the user to adjust the delay/phase of the output signal, in increments of half period of the input signal. Example of a half period delay is shown in.Figure 4. In order to achieve the half period delay, the HMC988LP3E delays the output by one full period of the input signal, by using the SLIP function, then Reg06h[2] value is changed from "1" (rising edge) to "0" (falling edge) and the output is effectively sped up by half cycle of the input, resulting in a total delay of one half of the period of the input signal. Similar methodology can be deployed to delay the output signal by X.5 or more cycles, in effect the user would deploy the Slip function to X+1 times and then switch the trigger from rising edge to falling edge to achieve a total delay of X.5.



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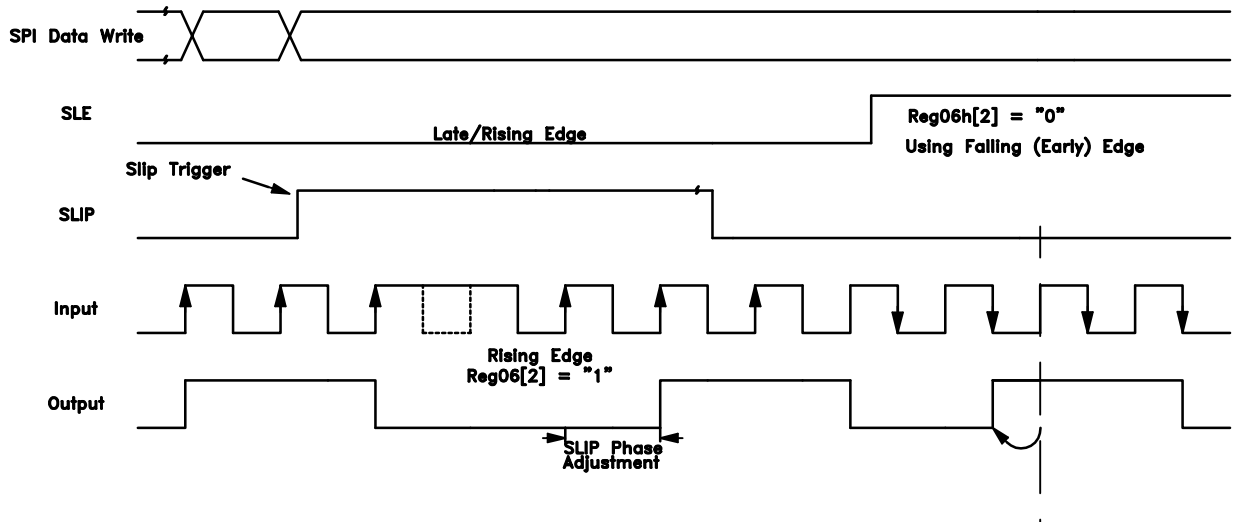


*Figure 4. Delay by 1/2 of Input Clock Cycle Timing Diagram*

### *Adjustable Fine Delay*

In addition to the 1/2 cycle delay offered by the slip function, the output of the HMC988LP3E can be delayed in ~20 ps steps, by programing Reg07h[5:0]. anywhere from 0 to 60. The delay function follows Equation 2.

$$\text{Delay} \cong (\text{Reg07h}) \times 20\text{ps} + 300\text{ps} \qquad \textbf{EQ (2)}$$

At higher frequencies (> 200 MHz), the step size compresses near the high end of the range when using the Fine Delay. See Figure 6. If Fine Delay is used when the divider is bypassed (divide-by-1) the maximum frequency is limited to 650MHz. As the frequency is increased beyond 650MHz the output amplitude will decrease when the divider is bypassed.

Please note that the phase noise can degrade by 15 dB when using Fine Delay mode.

### *Trigger Details*

In HMC988LP3E, the Sync and the Slip functions can both be implemented using the external "TRIG" pin or by using the SPI interface. The circuit diagram for SYNC and SLIP controls pins is shown in Figure 5. Note that the SYNC and SLIP should not be applied at the same time.

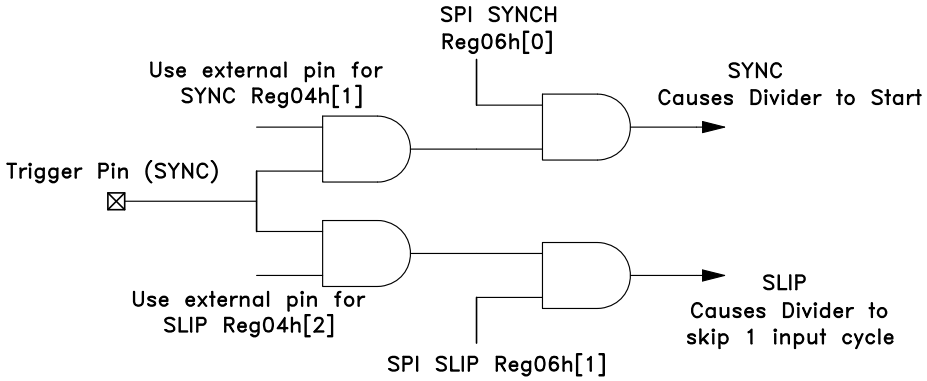


*Figure 5. SYNC/SLIP Circuit Diagram*



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### *Executing SYNC/SLIP Using External PIn*

In order to execute SYNC or SLIP function using the external pin, simply assert the external “TRIG” pin of the HMC988LP3E. The functions will trigger on the rising edge of the external SYNC or SLIP pin . Note that the corresponding SYNC or SLIP external trigger awareness function needs to be enabled in the HMC988LP3E.

Note that Reg04h[1] and Reg04h[2] should never be equal to “1” at the same time. if “1” is written to Reg04h[1], than “0” needs to be written to Reg04h[2], and vice-versa.

### *Execute SYNC/SLIP Using the SPI Interface*

Pin 9, Serial Latch Enable (SLE), of the HMC988LP3E causes SPI bits to change states and therefore acts as a trigger if the SYNC and SLIP functions are chosen to be executed using the SPI interface. Note that the SYNC signal is level sensitive, and must remain 1 in order to keep the internal divider running. The slip signal is rising-edge sensitive, and must be returned low at some point before the next trigger.

## *Optional On-Chip Regulator*

The HMC988LP3E has an optional on-chip regulator that can be used or bypassed. The regulator requires an input voltage ≥ 3.8 V. The on-chip regulator circuit is shown in Figure 6. The regulator can be bypassed by programing Reg04h[5] = “1”. In that case identical voltage should be applied to input of the regulator (VDD5) and VDD3_DECAP.

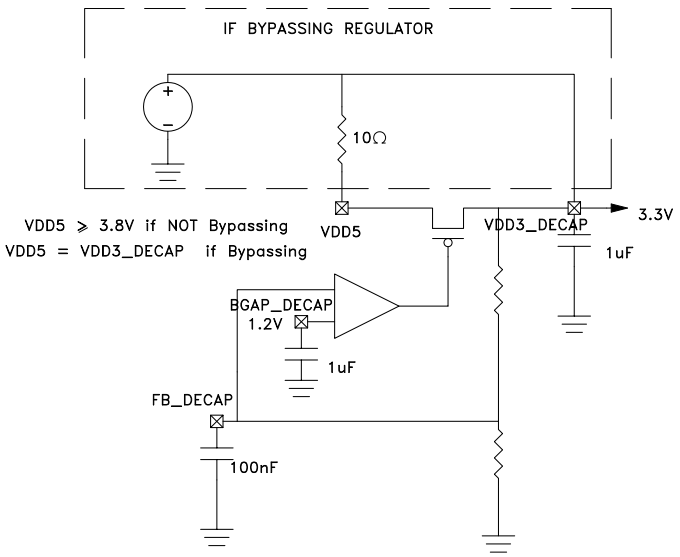


*Figure 6. Regulator Circuit Diagram*

## *GPO*

The HMC988LP3E has a GPO (General Purpose Output) pin that can be used for obtaining various internal states of the device (many of which are only used for internal testing), or as an SPI output. The function of the GPO pin is configured in Reg05h.



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### HMC988LP3E Input Stage

The HMC988LP5E input stage, Figure 7, is flexible. It can be driven single-ended or differential, with LVPECL, LVDS, or CML signals. If driven single-ended, a large AC coupling cap to ground should be used on the undriven input. The input impedance is 50 Ω single-ended (100 Ω differential). The DC bias level of 2.0 V can be generated internally by programming Reg04h[3] = 1, supplied externally, or generated via an LVPECL termination network inside the part. When Reg04h[3] = 0 internal DC bias is disabled and LVPECL termination enabled.

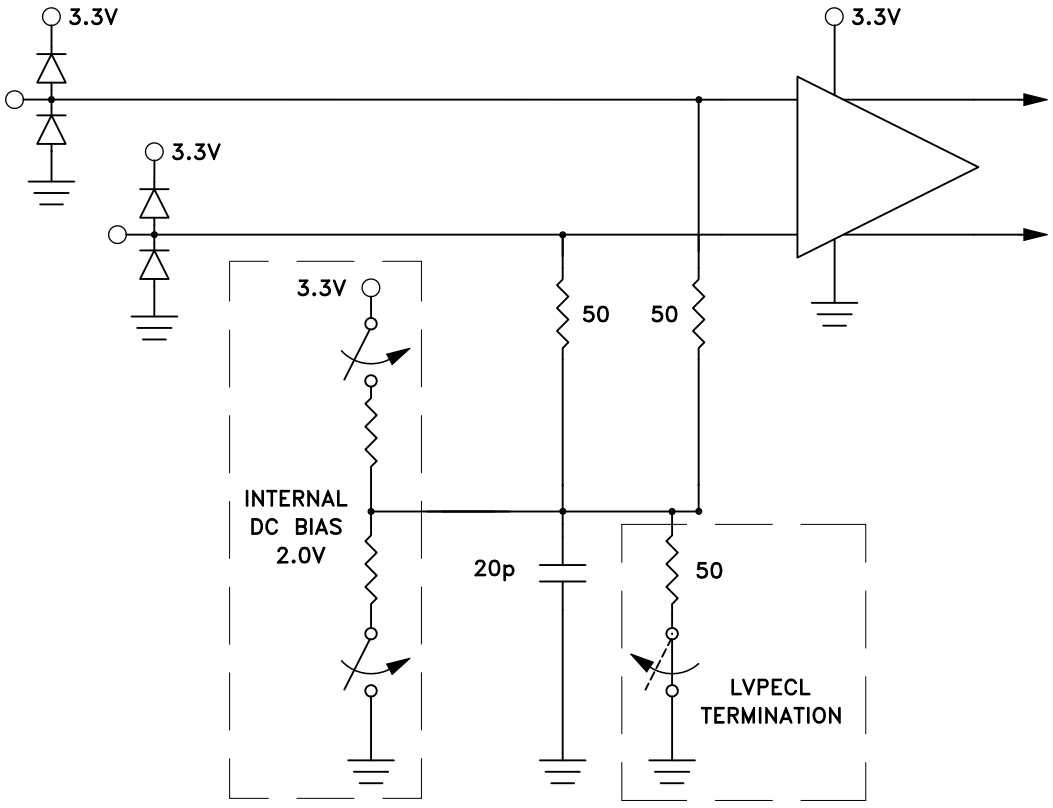


*Figure 7. HMC988LP3E Input Stage*

### HMC988LP3E Output Stage

The LVPECL output driver produces up to 1.6 Vppd swing into 50 Ω loads. LVPECL drivers are terminated with off-chip resistors that provide the DC current through the emitter-follower output stage. The output stage has a switch which disconnects the output driver from the load when not used. The switch series resistor significantly improves the output match when driving into 50 Ω transmission lines. The switch series resistor causes a small DC level shift and swing degradation, depending on the termination current.

If unused, disabled LVPECL outputs can be left floating, terminated, or grounded.



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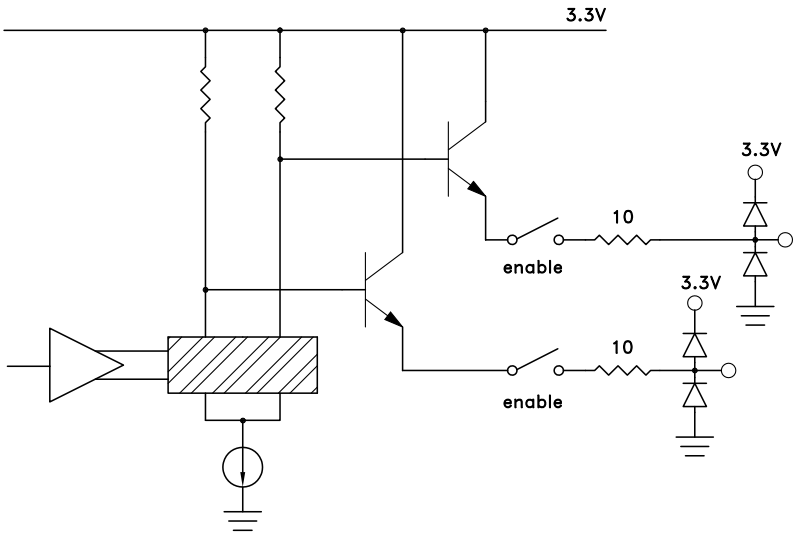


*Figure 8. HMC988LP3E Output Stage*

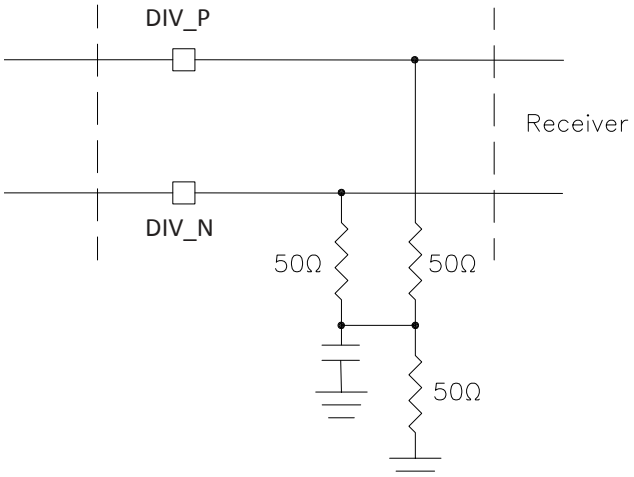


*Figure 9. Typical LVPECL Termination*



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## Serial Port Write Operation

**Table 6. SPI Open Mode - Write Timing Characteristics**

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_1$ | SDI setup time | 3 | | | ns |
| t2 | SDI hold time | 3 | | | ns |
| t3 | SLE low duration | 10 | | | ns |
| t4 | SLE high duration | 10 | | | ns |
| t5 | SCLK 9 Rising Edge to SLE Rising Edge | 10 | | | ns |
| | Serial port Clock Speed | DC | 50 | | MHz |
| $t_6$ | SLE to SCLK Recovery Time | 10 | | | ns |

A typical WRITE cycle is shown in Figure 10.

- **a.** The Master (host) places 9 bit data, d8:d0, MSB first, on SDI on the first 9 falling edges of SCLK.
- **b.** The slave () shifts in data on SDI on the first 9 rising edges of SCLK
- **c.** Master places 4 bit register address to be written to, r3:r0, MSB first, on the next 4 falling edges of SCLK (10-13)
- **d.** Slave shifts the register address bits on the next 4 rising edges of SCLK (10-13).
- **e.** Master places 3 bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (14-16).
- **f.** Slave shifts the chip address bits on the 3 rising edges of SCLK (14-16).
- **g.** Master asserts SLE after the 16th rising edge of SCLK.
- **h.** Slave registers the SDI data on the rising edge of SLE.

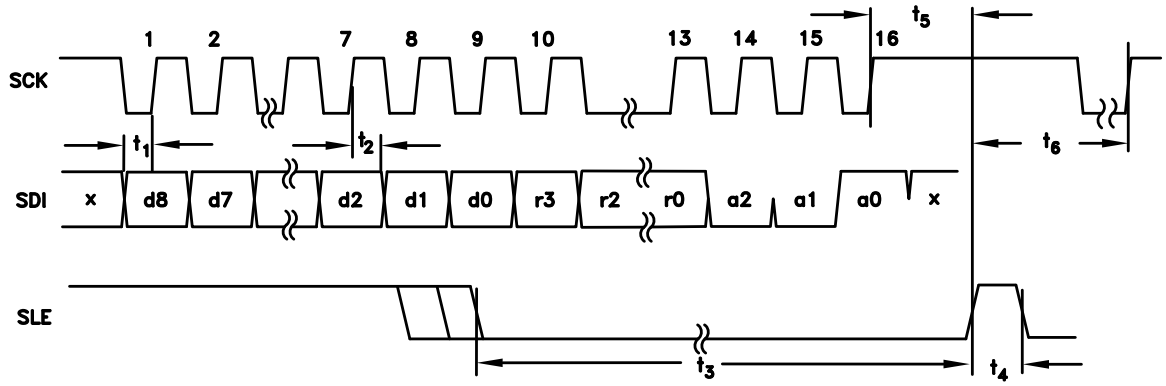


*Figure 10.* SPI Timing Diagram, Write Operation

## Serial Port Read Operation

A typical READ cycle is shown in Figure 11. In general, SDO line is always active during the WRITE cycle. SDO will contain the data from the addresses pointed to by Reg00h. If Reg00h is not changed, the same data will always be present on the SDO. If it is desired to READ from a specific address, it is necessary in the first SPI cycle to write the desired address to Reg00h, then in the next SPI cycle the desired data will be available on the SDO.

An example of the two cycle procedure to read from any random address is as follows:



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The Master (host), on the first 9 falling edges of SCLK places 9 bit data, d8:d0, MSB first, on SDI as shown in Figure 11. d8:d0 should be set to zero. d3:d0 = address of the register to be READ on the next cycle.

- **a.** The slave () shifts in data on SDI on the first 9 rising edges of SCLK
- **b.** Master places 4 bit register address , r3:r0, ( the address the WRITE ADDRESS register), MSB first, on the next 4 falling edges of SCLK (10-13). r3:r0=0000.
- **c.** Slave shifts the register bits on the next 4 rising edges of SCLK (10-13).
- **d.** Master places 3 bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (14-16).
- **e.** Slave shifts the chip address bits on the next 3 rising edges of SCLK (14-16).
- **f.** Master asserts SLE after the 16th rising edge of SCLK.
- **g.** Slave registers the SDI data on the rising edge of SLE.
- **h.** Master clears SLE to complete the address transfer of the two part READ cycle.
- **i.** If we do not wish to write data to the chip at the same time as we do the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.
- **j.** Master places the same SDI data as the previous cycle on the next 16 falling edges of SCLK.
- **k.** Slave () shifts the SDI data on the next 16 rising edges of SCLK.
- **l.** Slave places the desired data (i.e. data from address in Reg00h[3:0]) on SDO on the next 16 rising edges of SCLK.
- **m.** Master asserts SLE after the 16th rising edge of SCLK to complete the cycle.

Note that if the chip address bits are unrecognized (a2:a0), the slave will tri-state the SDO output to prevent a possible bus contention issue.

**Table 7. SPI Open Mode - Read Timing Characteristics**

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_1$ | SDI setup time | 3 | | | ns |
| t2 | SDI hold time | 3 | | | ns |
| t3 | SLE low duration | 10 | | | ns |
| t4 | SLE high duration | 10 | | | ns |
| t5 | SCLK Rising Edge to SDO time | | 8.2+0.2ns/ pF | | ns |
| t6 | SLE to SCLK Recovery Time | 10 | | | ns |
| t7 | SCLK 16 Rising Edge to SLE Rising Edge | 10 | | | ns |



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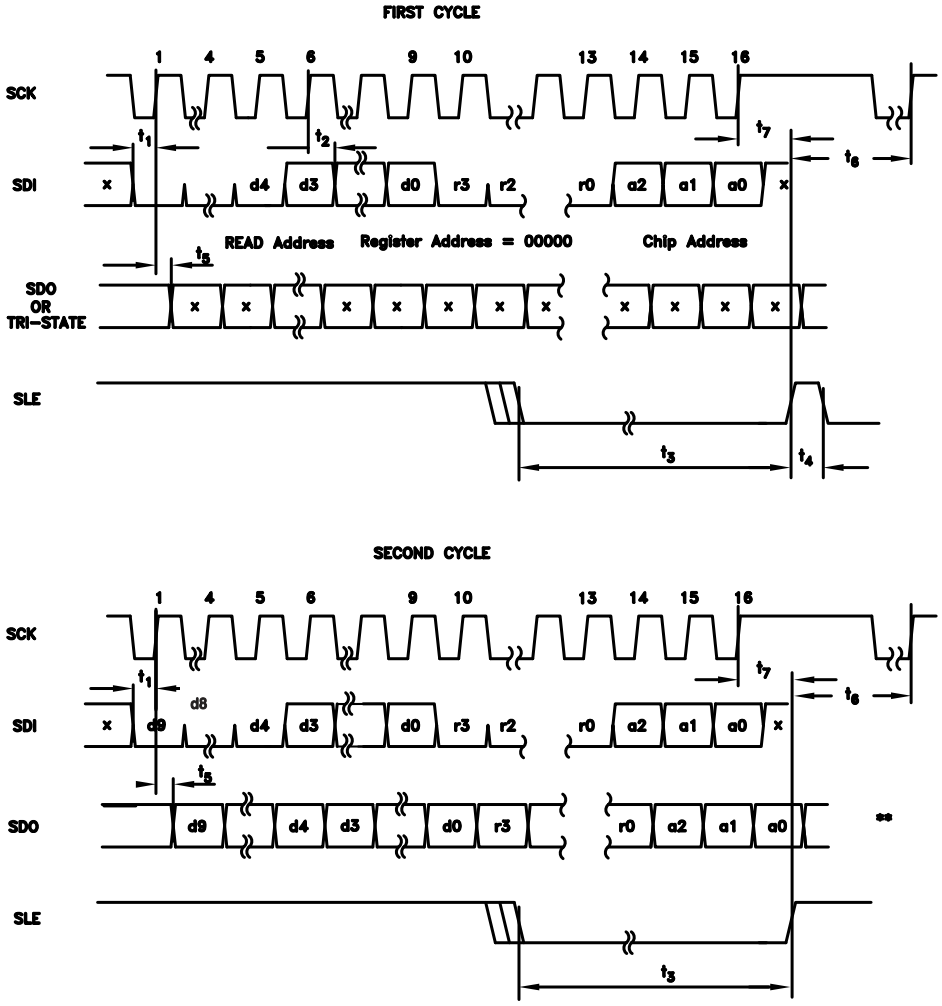


*Figure 11. SPI Diagram, Read Operation 2- Cycles*





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## Register Map

**Table 8. Reg 00h - ID and Read Register**

| Bit | Name | Width | Default | Description |
|---|---|---|---|---|
| [3:0] | Read Control | 4 | | Enter Register Address to be Read From |
| [4] | Soft Reset | 1 | 0 | 1: Reset |
| [8:0] | Chip ID | 9 | | Register 00 Contains the Chip ID (406 decimal) |

**Table 9. Reg 01h - Enables**

| Bit | Name | Width | Default | Description |
|---|---|---|---|---|
| [0] | ***Master Chip Enable*** | 1 | 1 | 1 Enables the Chip |
| [1] | Rx Buffer Enable | 1 | 1 | 1 Enables the Rx Buffer |
| [2] | Divider Core Enable | 1 | 1 | 1 Enables the Divider Core |
| [3] | Output buffer enable | 1 | 1 | 1 Enables the Output Buffer |
| [8:4] | Reserved | 5 | 0 | |

**Table 10. Reg 02h - Divide/Delay select**

| Bit | Name | Width | Default | Description |
|---|---|---|---|---|
| [2:0] | Divide Ratio Select | 2 | 2 | 0: /1<br>1: /2<br>2: /4<br>3: /8<br>4: /16<br>5: /32<br>6: N/A<br>7: N/A |
| [8:3] | Reserved | 6 | 0 | |

**Table 11. Reg 03h - Bias**

| Bit | Name | Width | Default | Description |
|---|---|---|---|---|
| [1:0] | Reserved | 2 | 2 | |
| [3:2] | Reserved | 2 | 2 | |
| [5:4] | Transmit Buffer Swing Select | 2 | 2 | 0: 600mVpp Single Ended<br>1: 700mVpp Single Ended<br>2: 800mVpp Single Ended<br>3: 900mVpp Single Ended |
| [8:6] | SYNC Delay Adjustment | 3 | 3 | Can be used to equalize SYNC delay between dividers. 1000+(0-7)*80 ps |



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### Table 12. Reg 04h - Configuration

| Bit | Name | Width | Default | Description |
|---|---|---|---|---|
| [0] | Broadcast Mode | 1 | 0 | if 1, a write to Chip Addr "111" will be listened to by all slaves.<br>Useful for synchronizing multiple dividers |
| [1] | External SYNC Pin EN | 1 | 1 | External pin can be used to start-up divider synchronously. |
| [2] | External SLIP Pin EN | 1 | 0 | External pin can be used to slip divider synchronously<br>Both ExtSLIP and ExtSYNC bits should not be '1' at the same time |
| [3] | RX Buffer DC Bias Select | 1 | 0 | Use 1 for sinusoidal / non-LVPECL AC coupled inputs |
| [4] | Delay Line Enable | 1 | 0 | Use 0 for natural low-noise path, 1 enables the fine delay |
| [5] | On-Chip Regulator Bypass | 1 | 0 | 1 bypass the on-chip regulator, 0 enable the on-chip regulator |
| [8:6] | Reserved | 3 | 0 | |

### Table 13. Reg 05h - General Purpose Output

| Bit | Name | Width | Default | Description |
|---|---|---|---|---|
| [2:0] | GPO Select | 2 | 0 | 0: 0<br>1: 1<br>2: slip req<br>3: 0<br>4: sync req<br>5: sync delayed<br>6: waiting for clock pulse (post sync)<br>7: spare |
| [3] | Force GPO Pin on GPO only | 1 | 0 | no automux to serial data output |
| [4] | Force GPO Pin on SDO only | 1 | 0 | no automux to GPO selected data PRIORITY |
| [5] | Force GPO Pin to HiZ | 1 | 0 | Force GPO pin to HiZ |
| [8:6] | Reserved | 3 | 0 | |

### Table 14. Reg 06h - SPI Triggers

| Bit | Name | Width | Default | Description |
|---|---|---|---|---|
| [0] | SPI SYNC Signal | 1 | 1 | 0 - holds divider in reset, 1 allows startup |
| [1] | SPI SLIP Signal | 1 | 0 | A 0 to 1 level change is sensed by the input clock, and causes a full input cycle-slip. The signal must be maintained for > 4 Tvco input clock cycles before brought low. |
| [2] | Output Launch Phase | 1 | 0 | 0: Falling Edge (Early)<br>1: Rising Edge (Late)<br>To delay the output by 1/2 cycle you can switch from early to late. To go back, you must force N-1 full cycle slips, and switch back from late to early. |
| [8:3] | Reserved | 6 | 0 | |

### Table 15. Reg 07 - Delay Lines

| Bit | Name | Width | Default | Description |
|---|---|---|---|---|
| [5:0] | Delay Line Setpoint | 6 | 4 | Delay = Setpoint *20 ps + 300 ps (Max of 300 -> 1500 ps) |
| [8:6] | Reserved | 3 | 0 | |





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