



# BUK9J0R9-40H

N-channel 40 V, 0.9 mΩ logic level MOSFET in LFPK56E

7 October 2019

Product data sheet

## 1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in an enhanced LFPK56E package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

## 2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower  $R_{DSon}$  in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight  $V_{GS(th)}$  limits enable easy paralleling of MOSFETs
- LFPK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPK copper clip technology:
  - Improved reliability, with reduced  $R_{th}$  and  $R_{DSon}$
  - Increases maximum current capability and improved current spreading

## 3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

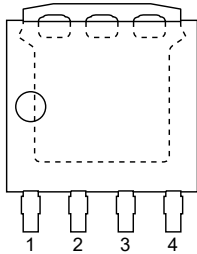
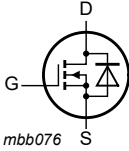
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	[1]	-	220	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	500	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a>	0.53	0.82	0.94	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	12.7	25.3	nC
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ °C}$ <a href="#">[2]</a>	-	52.6	-	nC
S	softness factor	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 17</a>	-	0.77	-	

- [1] 220A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.  
 [2] includes capacitive recovery

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9J0R9-40H	LFAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFAK56); 4 leads; 1.27 mm pitch	SOT1023

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9J0R9-40H	90H940E

## 8. Limiting values

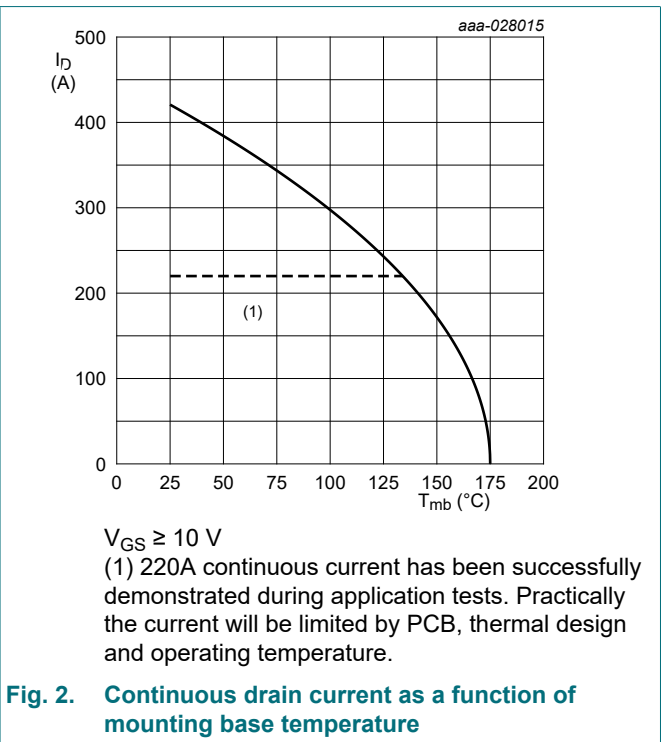
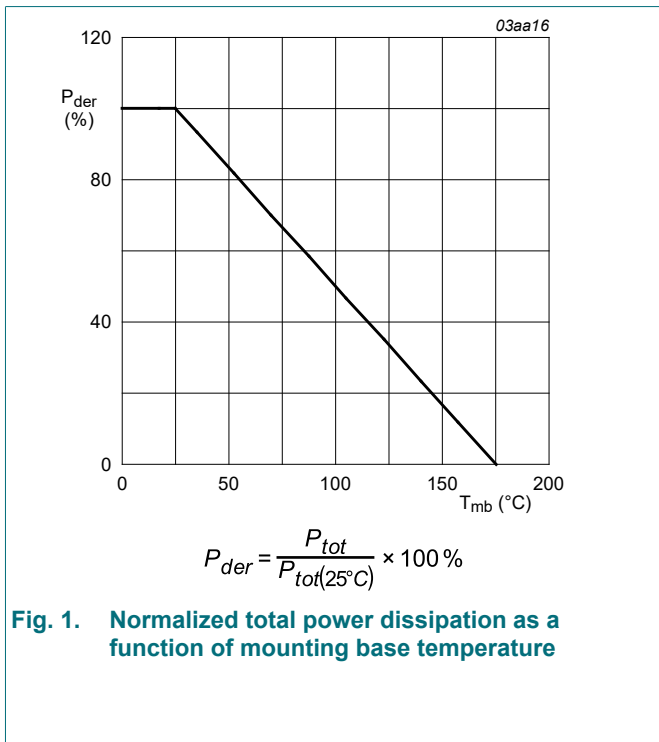
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
$V_{GS}$	gate-source voltage	DC; $T_j \leq 175\text{ °C}$	-10	16	V

Symbol	Parameter	Conditions		Min	Max	Unit
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1		-	500	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	[1]	-	220	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2	[1]	-	220	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3		-	600	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[2]	-	165	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	600	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 160\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; unclamped; Fig. 4	[3] [4]	-	290	mJ

- [1] 220A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] 165A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.



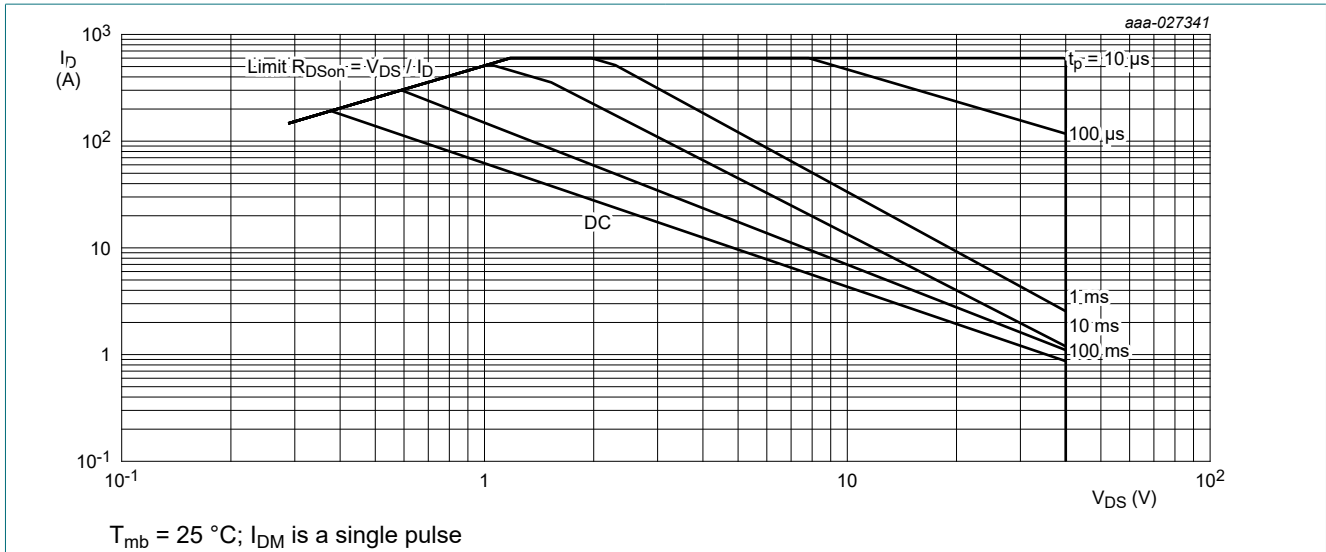


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

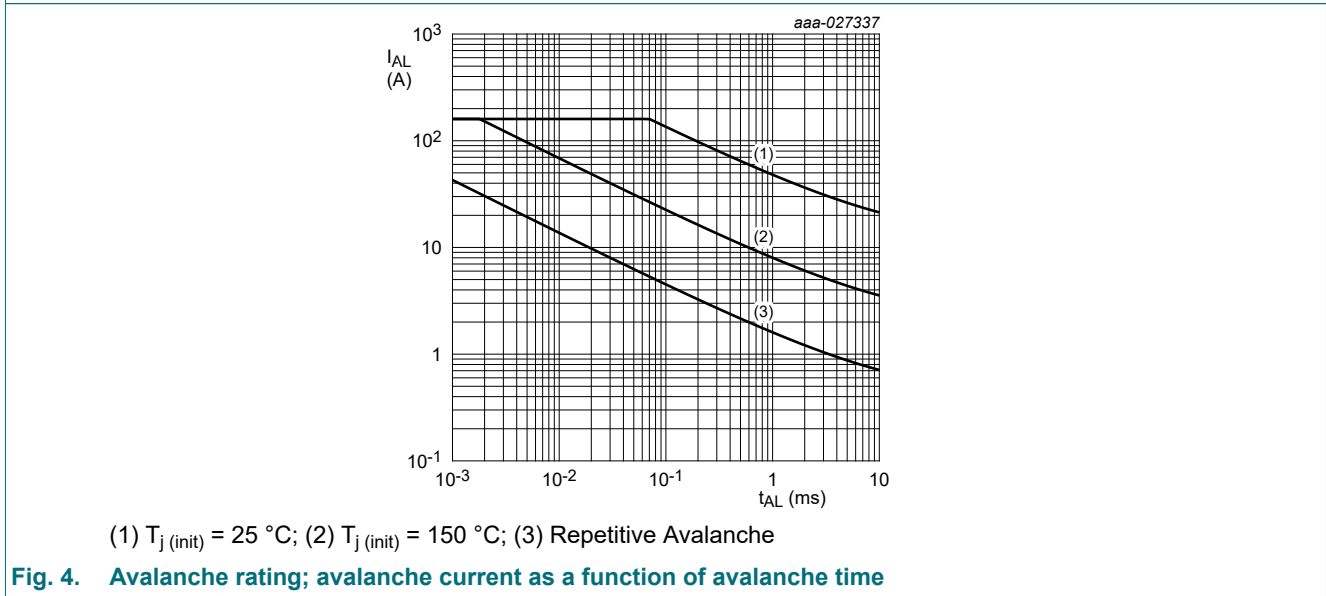


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.21	0.3	K/W

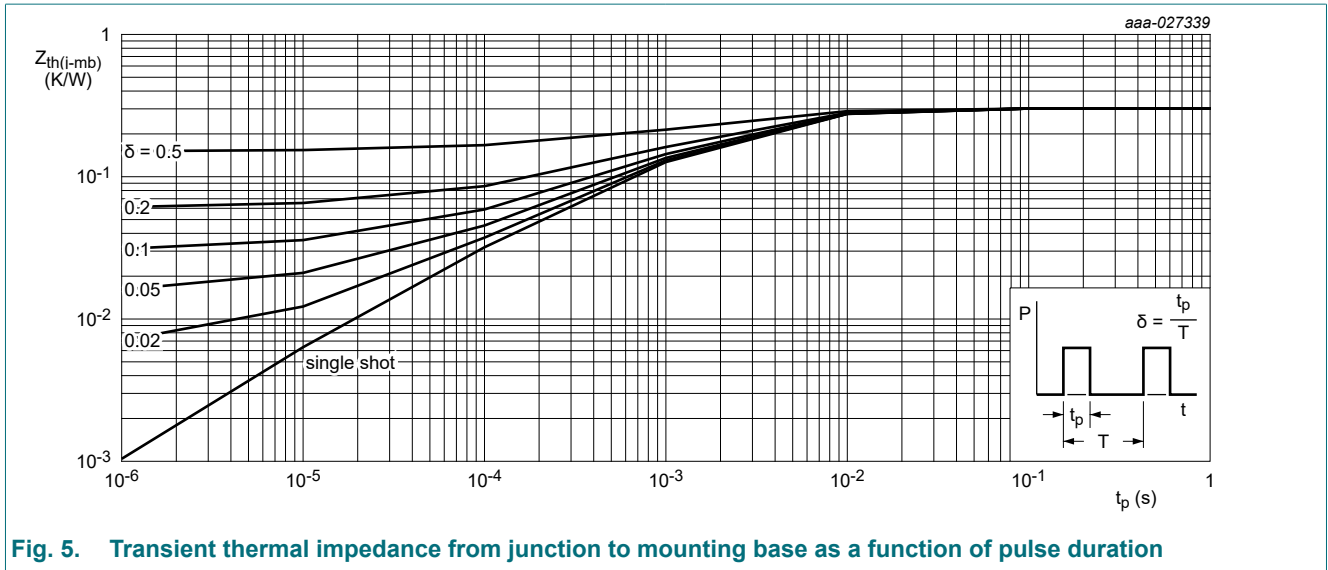


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

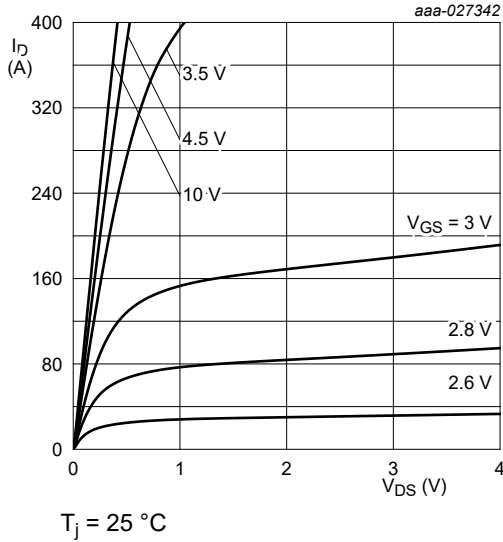
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_J = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_J = -40 \text{ }^\circ C$	-	40.5	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_J = -55 \text{ }^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_J = 25 \text{ }^\circ C; \text{ Fig. 9; Fig. 10}$	1.35	1.66	2.05	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_J = 175 \text{ }^\circ C; \text{ Fig. 10}$	0.6	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_J = -55 \text{ }^\circ C; \text{ Fig. 10}$	-	-	2.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$	-	0.4	5	$\mu A$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 125 \text{ }^\circ C$	-	3.2	25	$\mu A$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 175 \text{ }^\circ C$	-	405	1000	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$	-	2	100	nA

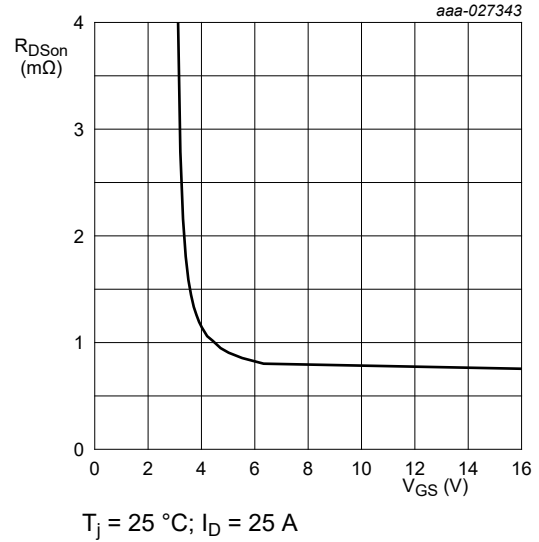
## N-channel 40 V, 0.9 mΩ logic level MOSFET in LPAK56E

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>	0.53	0.82	0.94	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 105 °C; <a href="#">Fig. 12</a>	0.79	1.17	1.48	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 125 °C; <a href="#">Fig. 12</a>	0.87	1.29	1.64	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a>	1.1	1.63	2.05	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>	0.68	0.97	1.2	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 105 °C; <a href="#">Fig. 12</a>	1	1.47	1.9	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 125 °C; <a href="#">Fig. 12</a>	1.1	1.62	2.1	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a>	1.4	2.03	2.6	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	0.42	1.04	2.6	mΩ
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	120	168	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	54.2	76	nC
Q <sub>GS</sub>	gate-source charge		-	20.2	30.2	nC
Q <sub>GD</sub>	gate-drain charge		-	12.7	25.3	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>	-	8977	12568	pF
C <sub>oss</sub>	output capacitance		-	1549	2168	pF
C <sub>rss</sub>	reverse transfer capacitance		-	346	760	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 20 V; R <sub>L</sub> = 0.8 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 5 Ω	-	45.4	-	ns
t <sub>r</sub>	rise time		-	46.2	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	59.2	-	ns
t <sub>f</sub>	fall time		-	32.6	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>	-	0.76	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C	-	44.6	-	ns
Q <sub>r</sub>	recovered charge		[1]	-	52.6	-
S	softness factor	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.77	-	
		I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -500 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.67	-	

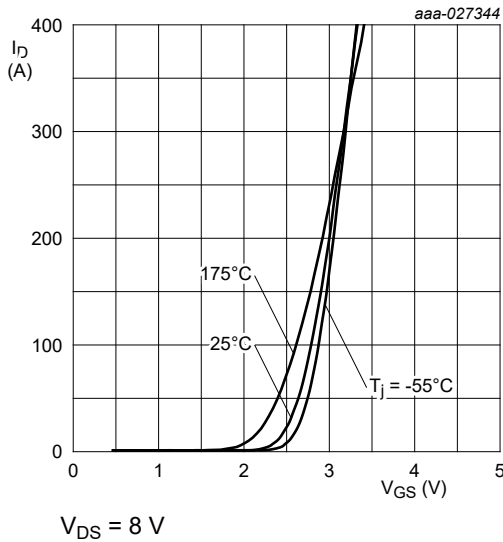
[1] includes capacitive recovery



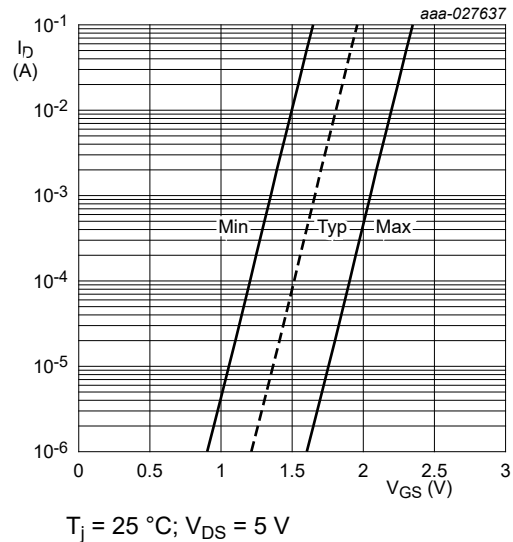
**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



**Fig. 9. Sub-threshold drain current as a function of gate-source voltage**

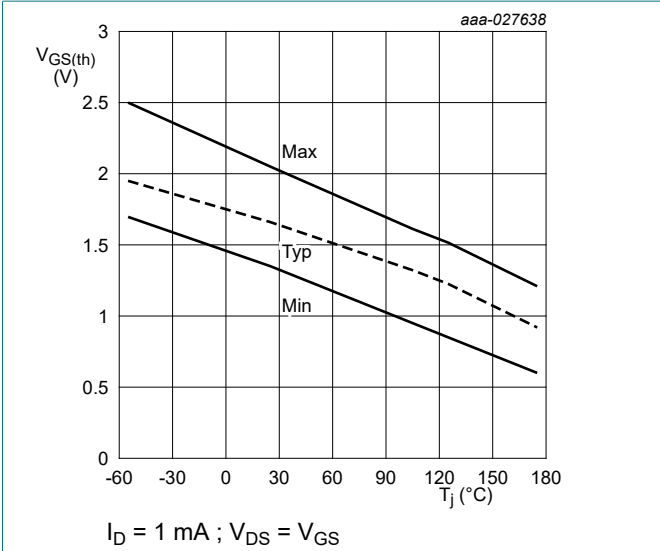


Fig. 10. Gate-source threshold voltage as a function of junction temperature

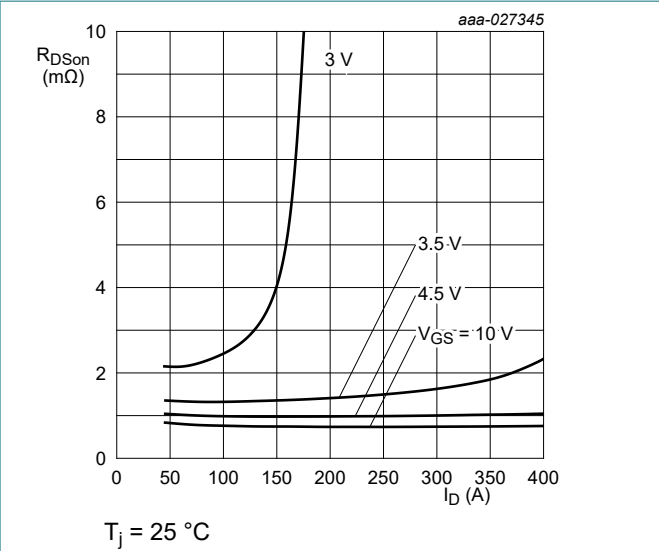


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

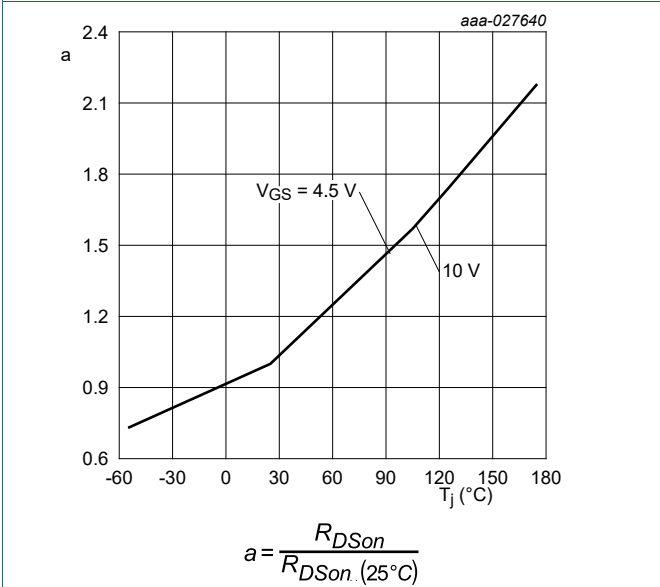


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

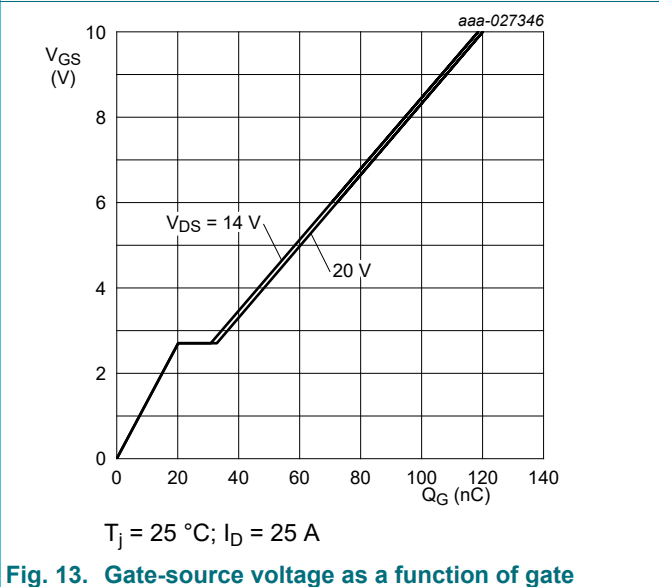


Fig. 13. Gate-source voltage as a function of gate charge; typical values



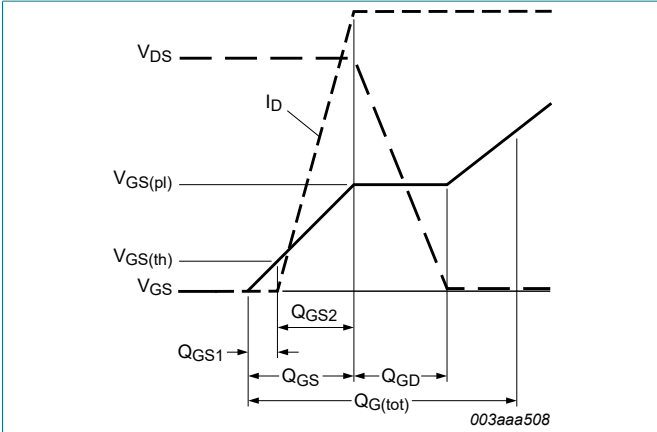
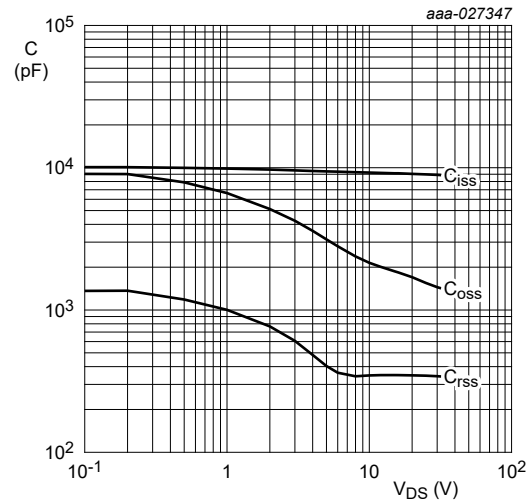
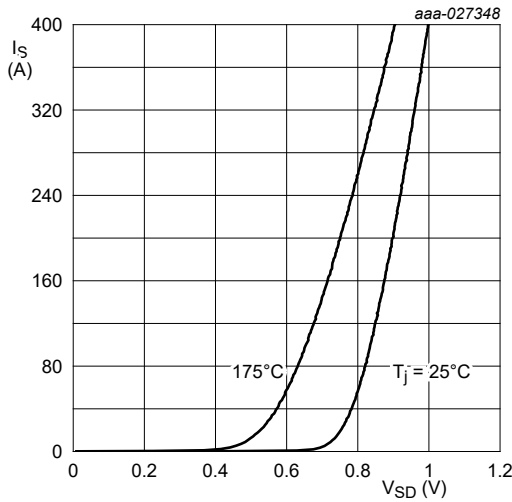


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

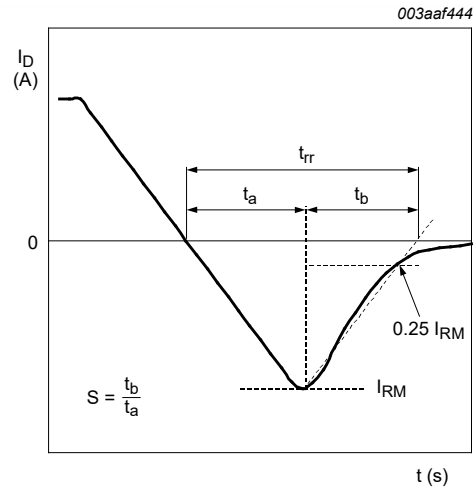


Fig. 17. Reverse recovery timing definition

11. Package outline

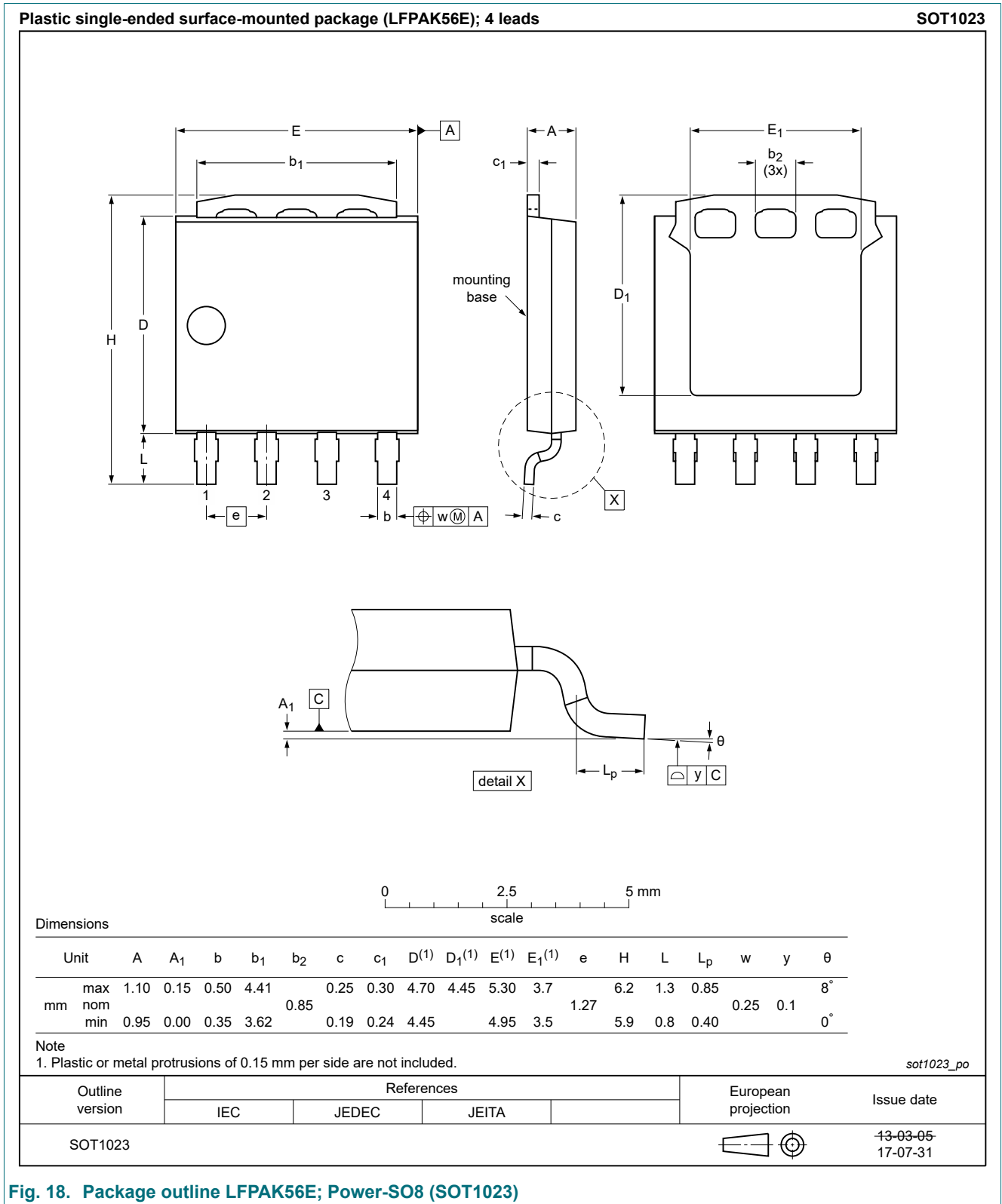


Fig. 18. Package outline LPAK56E; Power-SO8 (SOT1023)

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 7 October 2019

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