

# PHB66NQ03LT

## N-channel TrenchMOS logic level FET

Rev. 07 — 30 January 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC convertors
- General purpose switching

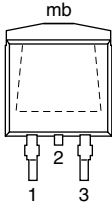
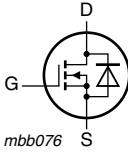
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	25	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	-	-	66	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	93	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 50\text{ A};$ $V_{DS} = 15\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 11</a>	-	3.6	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	9.1	10.5	m $\Omega$

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>SOT404 (D2PAK)</b></p>	 <p><i>mbb076</i></p>
2	D	drain <a href="#">[1]</a>		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

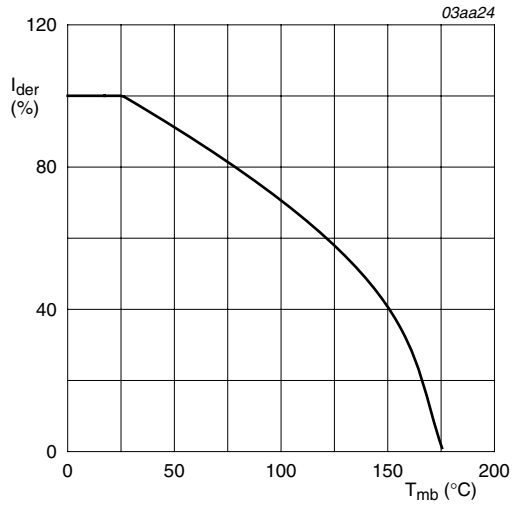
Type number	Package	Description	Version
	Name		
PHB66NQ03LT	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

**Table 4. Limiting values**

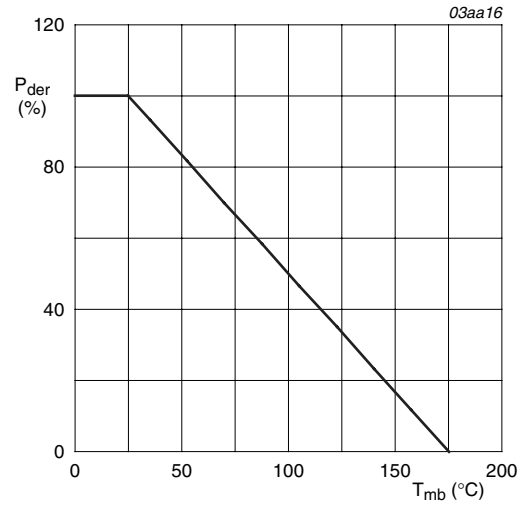
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	25	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$	-	45	A
		$V_{GS} = 5\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	40	A
		$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	57	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$	-	66	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	228	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	93	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	57	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	228	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 43\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; unclamped; $t_p = 0.15\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	90	mJ



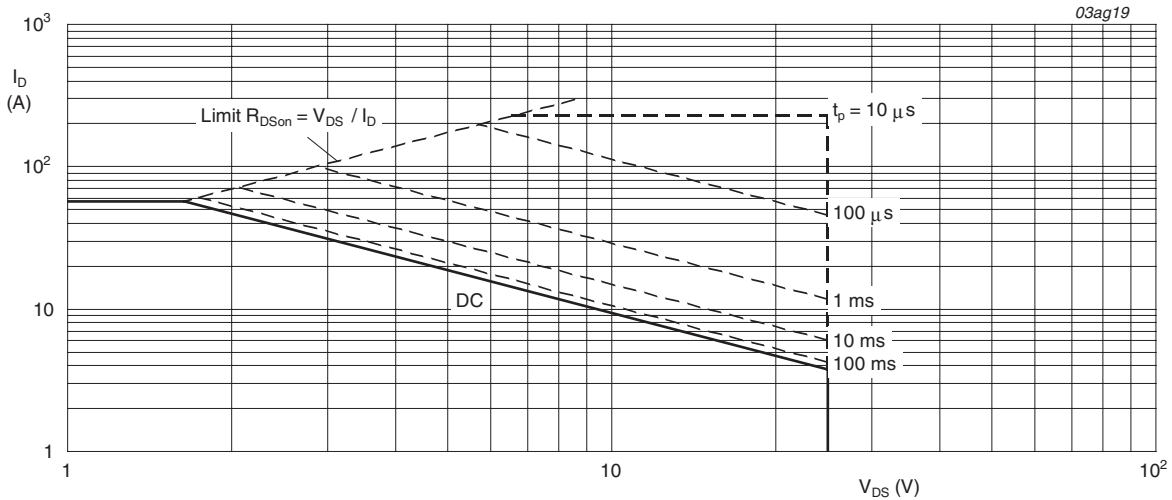
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



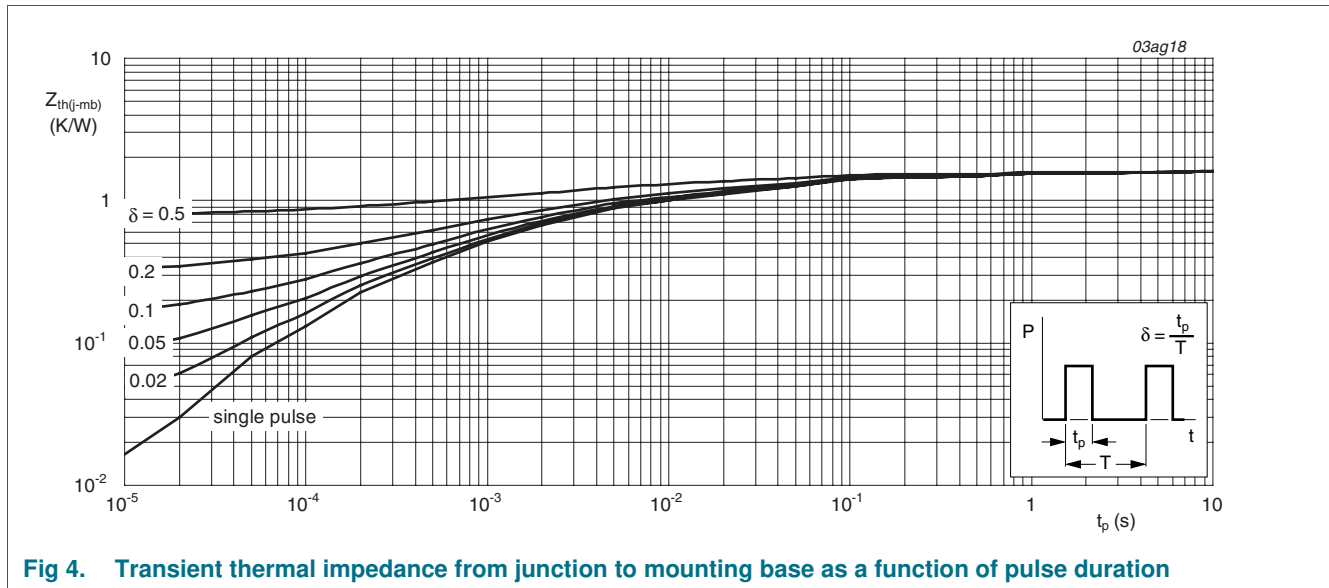
$T_{mb} = 25^\circ\text{C}; I_{DM}$  is single pulse;  $V_{GS} = 5\text{V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	1.6	K/W

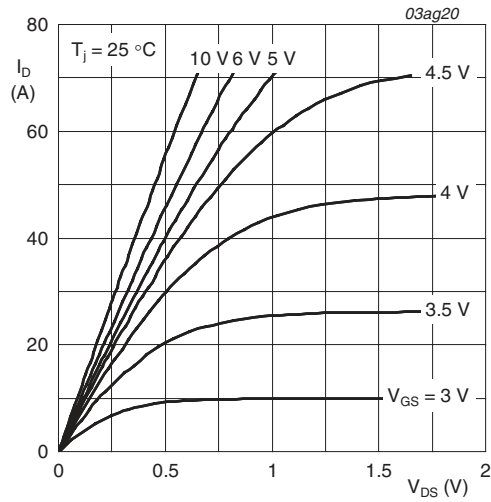


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

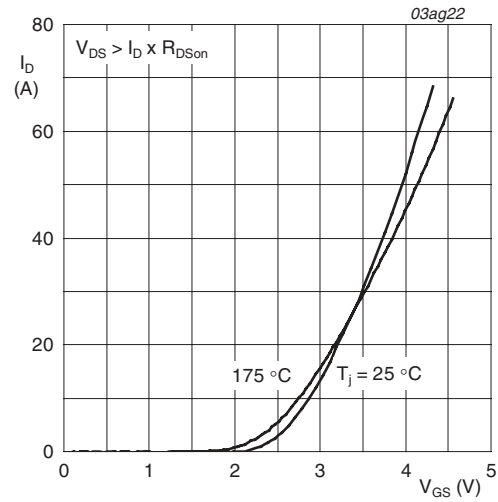
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	22	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	2.2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	16.4	18.9	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	11.2	13.6	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	9.1	10.5	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 50 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	12	-	nC
$Q_{GS}$	gate-source charge		-	4.5	-	nC
$Q_{GD}$	gate-drain charge		-	3.6	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	860	-	pF
$C_{oss}$	output capacitance		-	330	-	pF
$C_{rss}$	reverse transfer capacitance		-	145	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.6 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 5.6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	15	25	ns
$t_r$	rise time		-	90	135	ns
$t_{d(off)}$	turn-off delay time		-	25	40	ns
$t_f$	fall time		-	25	40	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	0.95	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	32	-	ns
$Q_r$	recovered charge		-	20	-	nC



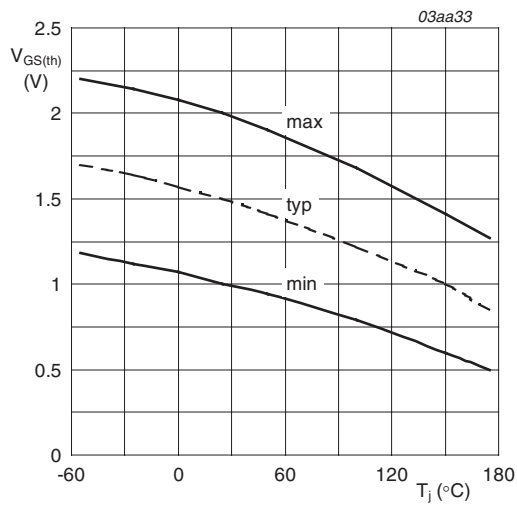
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



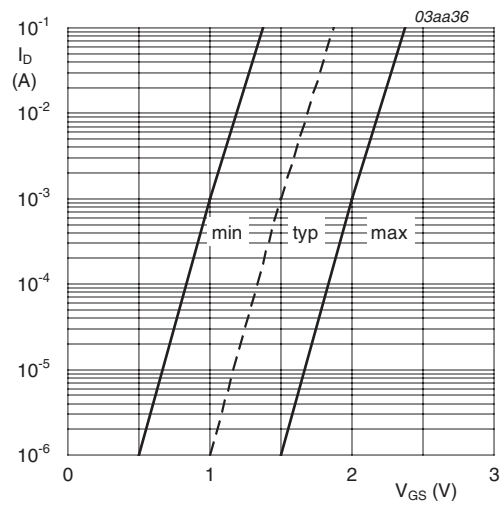
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}; V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



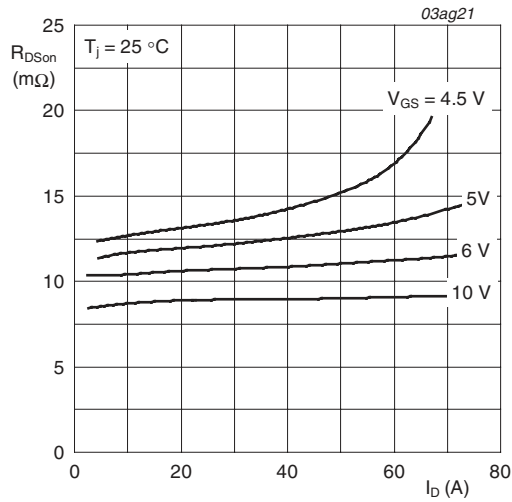
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



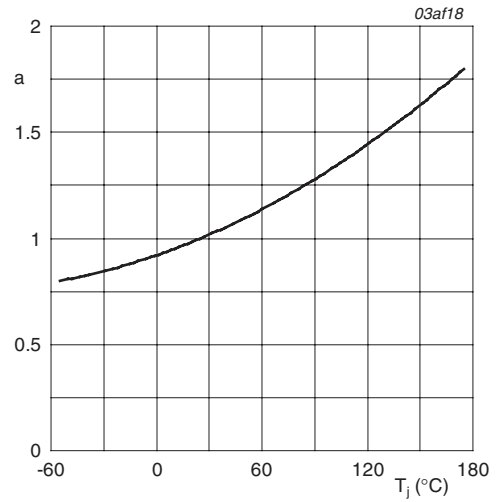
$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



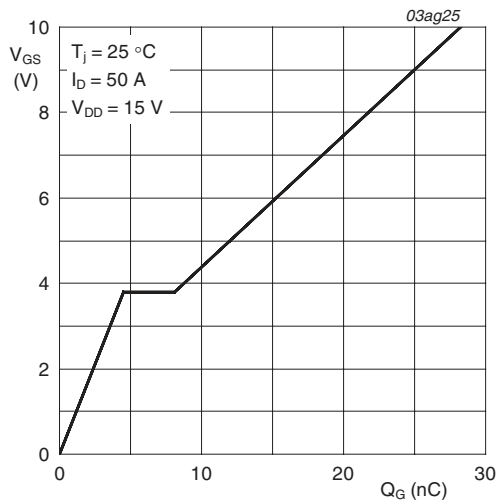
$T_j = 25\text{ }^\circ\text{C}$

**Fig 9. Drain-source on-state resistance as a function of drain current; typical values**



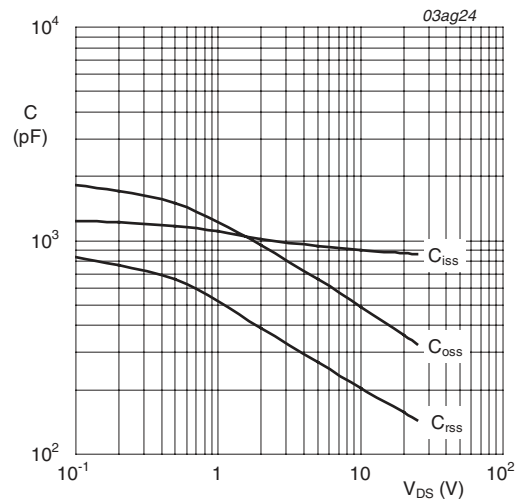
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

**Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature**



$I_D = 50\text{ A}; V_{DS} = 15\text{ V}$

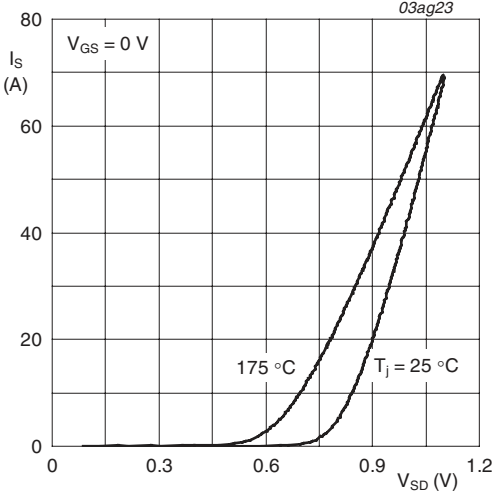
**Fig 11. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**





$T_j = 25\text{ °C}$  and  $175\text{ °C}; V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

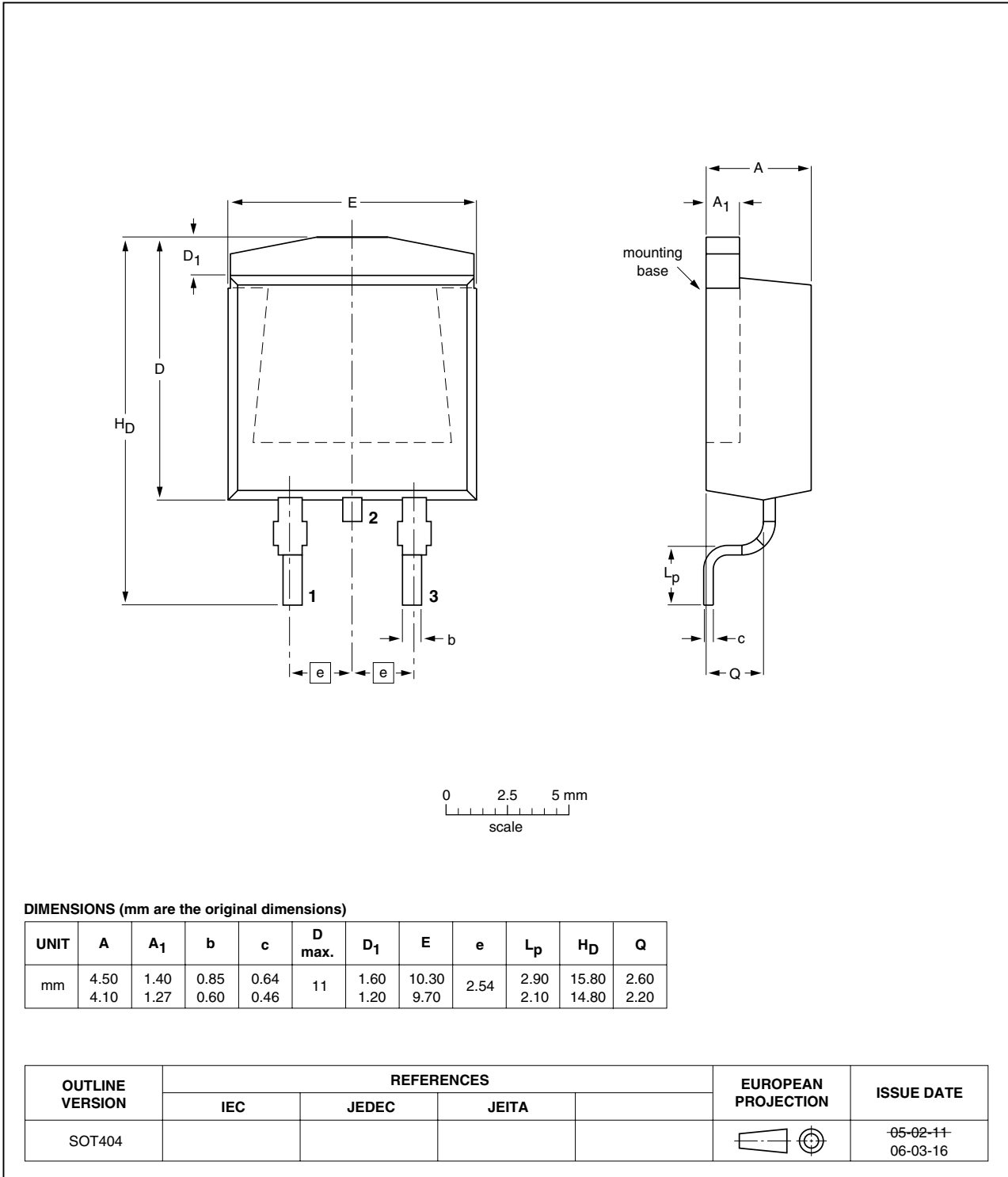


Fig 14. Package outline SOT404 (D2PAK)

## 8. Revision history

**Table 7. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHB66NQ03LT_7	20090130	Product data sheet	-	PHB_PHD66NQ03LT_6
Modifications:		<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>		
PHB_PHD66NQ03LT_6 (9397 750 13429)	20040802	Product data sheet	-	PHP_PHB_PHD66NQ03LT_5
PHP_PHB_PHD66NQ03LT_5 (9397 750 13107)	20040415	Product data sheet	-	PHP_PHB_PHD66NQ03LT_4
PHP_PHB_PHD66NQ03LT_4 (9397 750 10158)	20020909	Product data sheet	-	PHP_PHB_PHD66NQ03LT_3
PHP_PHB_PHD66NQ03LT_3 (9397 750 09284)	20020312	Product data sheet	-	PHP_PHB_PHD66NQ03LT_2
PHP_PHB_PHD66NQ03LT_2 (9397 750 09119)	20011210	Product data sheet	-	PHP_PHB_PHD66NQ03LT_1
PHP_PHB_PHD66NQ03LT_1 (9397 750 08725)	20011012	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 11. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>3</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>5</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>6</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>10</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>11</b>
<b>9</b>	<b>Legal information</b> . . . . .	<b>12</b>
9.1	Data sheet status . . . . .	12
9.2	Definitions . . . . .	12
9.3	Disclaimers . . . . .	12
9.4	Trademarks . . . . .	12
<b>10</b>	<b>Contact information</b> . . . . .	<b>12</b>

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