



STS6PF30L

P-CHANNEL 30V - 0.027 Ω - 6A SO-8 STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS6PF30L	30 V	<0.030 Ω	6 A

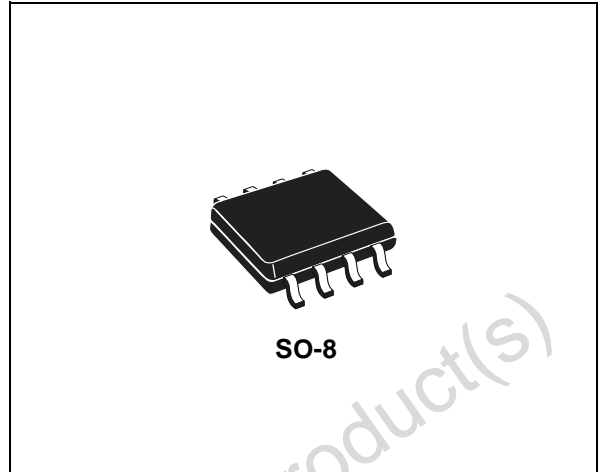
- TYPICAL R_{DS(on)} = 0.027 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

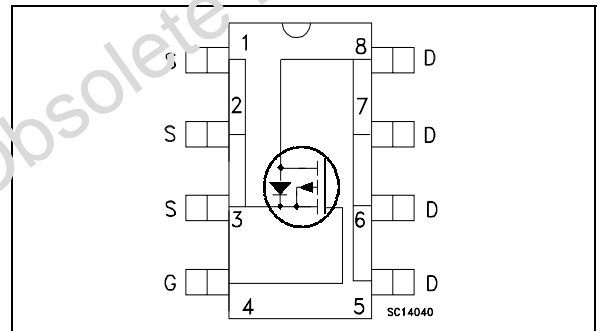
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- MOBILE PHONE APPLICATIONS
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate-source Voltage	± 16	V
I _D	Drain Current (continuous) at T _C = 25°C	6	A
I _D	Drain Current (continuous) at T _C = 100°C	3.8	A
I _{DM} (●)	Drain Current (pulsed)	24	A
P _{tot}	Total Dissipation at T _C = 25°C	2.5	W

(●) Pulse width limited by safe operating area.

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Note: For the P-CHANNEL MOSFET the actual polarity of the gate, drain and source voltages and current has to be reversed

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THERMAL DATA

Rthj-amb	Thermal Resistance Junction-ambient	Max	50	°C/W
T _j	Maximum Lead Temperature For Soldering Purpose	Typ	150	°C
T _{stg}	storage temperature		-55 to 150	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1	1.6	2.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 3 A V _{GS} = 5 V I _D = 3 A		0.027 0.034	0.030 0.042	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} =10 V I _D =3 A		12		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1670		pF
C _{OSS}	Output Capacitance			345		pF
C _{rSS}	Reverse Transfer Capacitance			120		pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON(*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 3\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 1)		62 140		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 24\text{ V}$ $I_D = 6\text{ A}$ $V_{GS} = 5\text{ V}$ (see test circuit, Figure 2)		21 3.9 8.6	28	nC nC nC

SWITCHING OFF(*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 24\text{ V}$ $I_D = 3\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 1)		57 19		ns ns

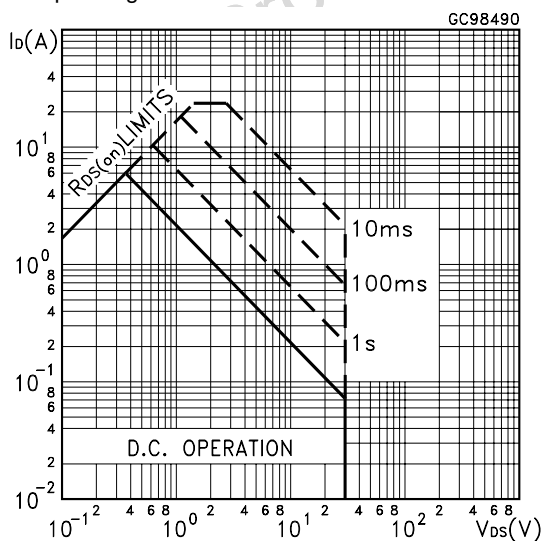
SOURCE DRAIN DIODE(*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				6 4	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 6\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 6\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		37 46.3 2.5		ns nC A

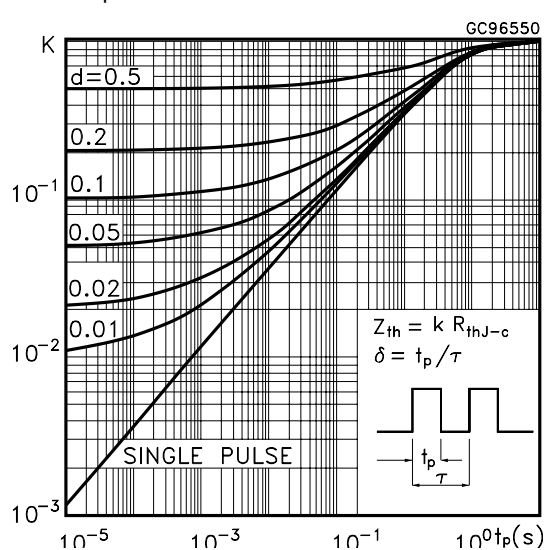
(*)Pulse width $\leq 300\ \mu\text{s}$, duty cycle 1.5 %.

(●)Pulse width limited by T_{JMAX}

Safe Operating Area

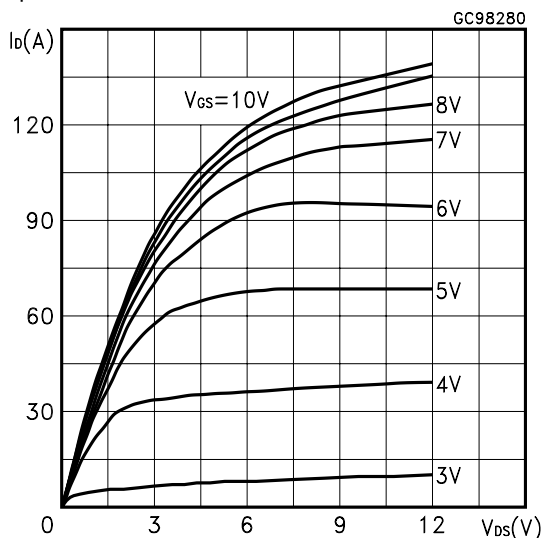


Thermal Impedance

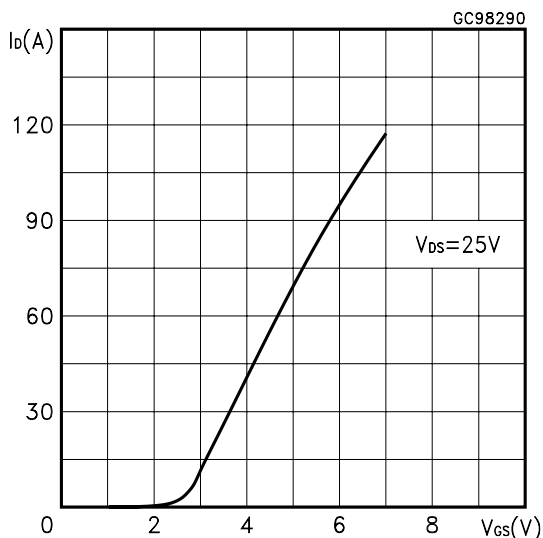


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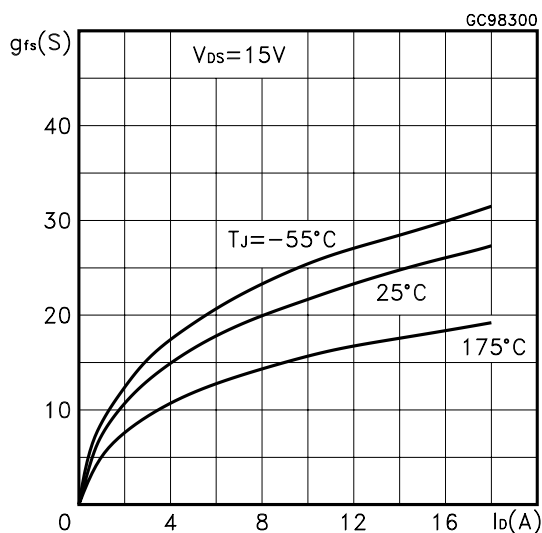
Output Characteristics



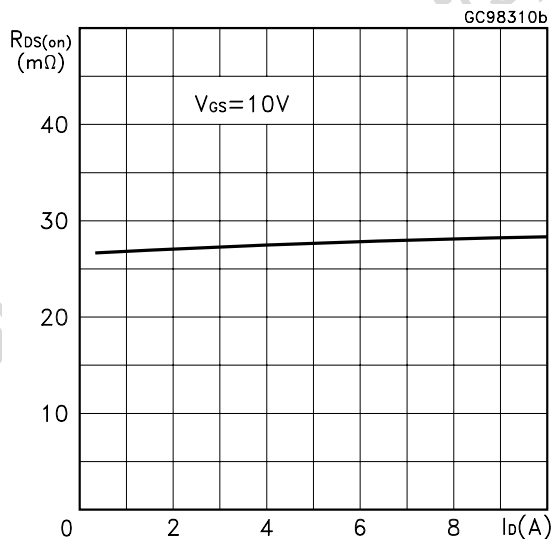
Transfer Characteristics



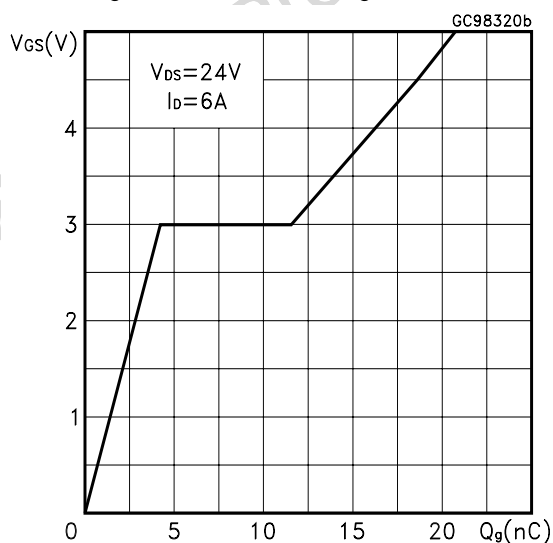
Transconductance



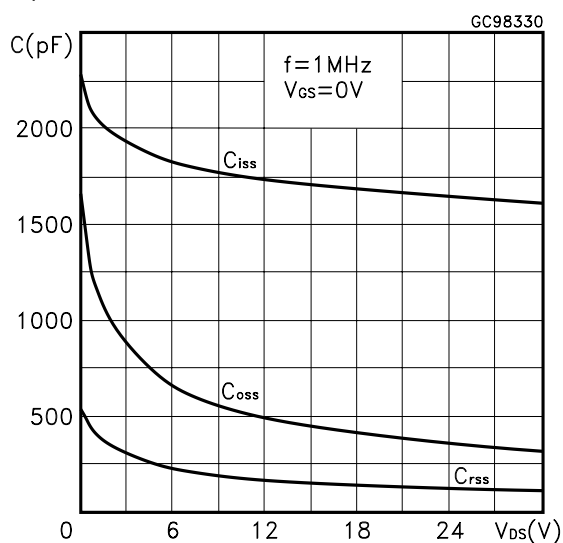
Static Drain-source On Resistance



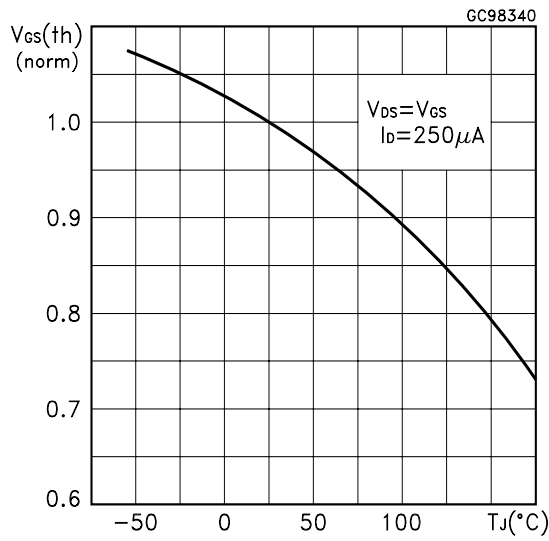
Gate Charge vs Gate-source Voltage



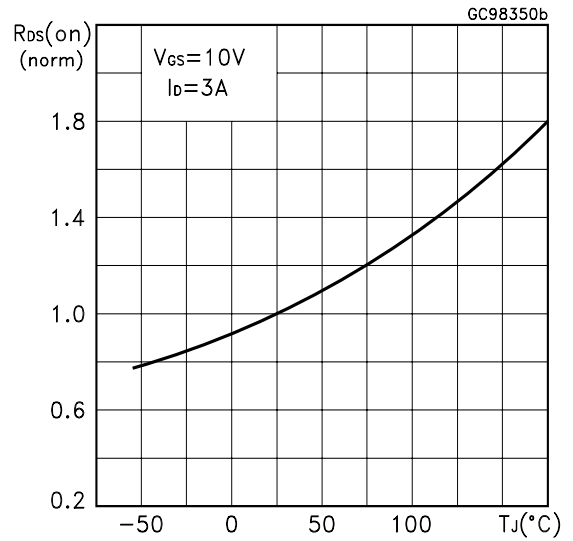
Capacitance Variations



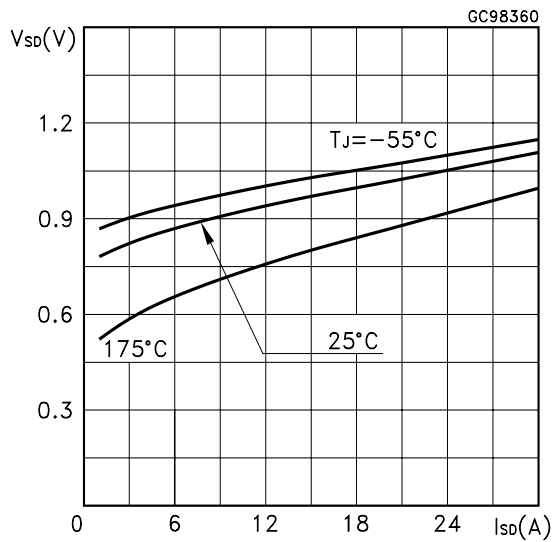
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

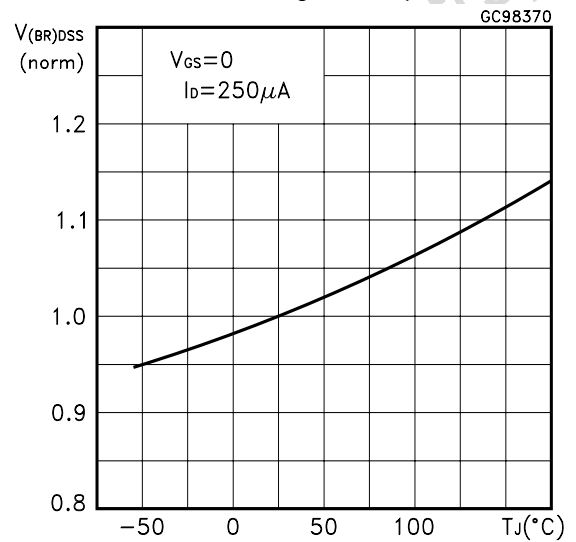


Fig. 1: Switching Times Test Circuits For Resistive Load

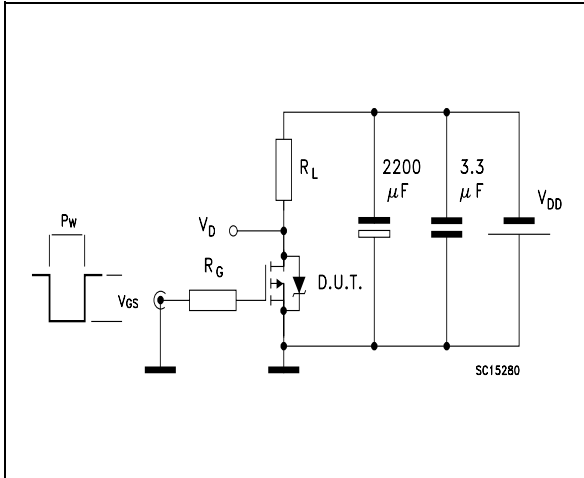


Fig. 2: Gate Charge test Circuit

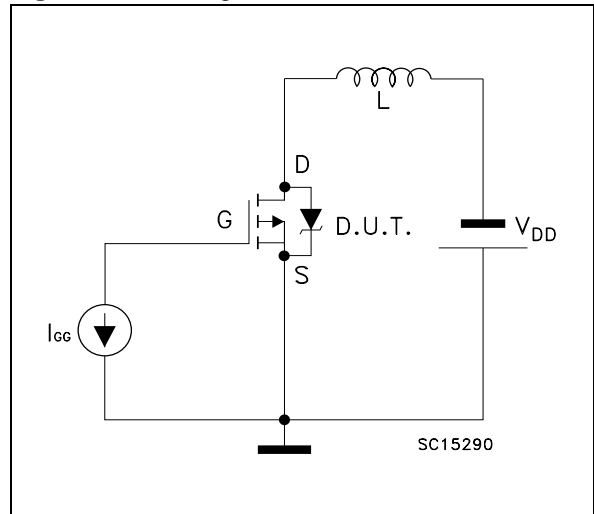
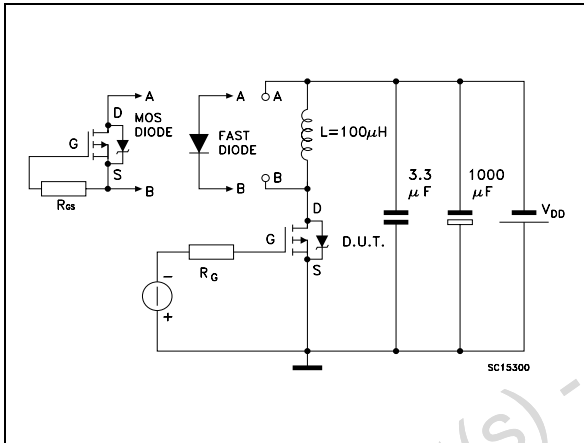


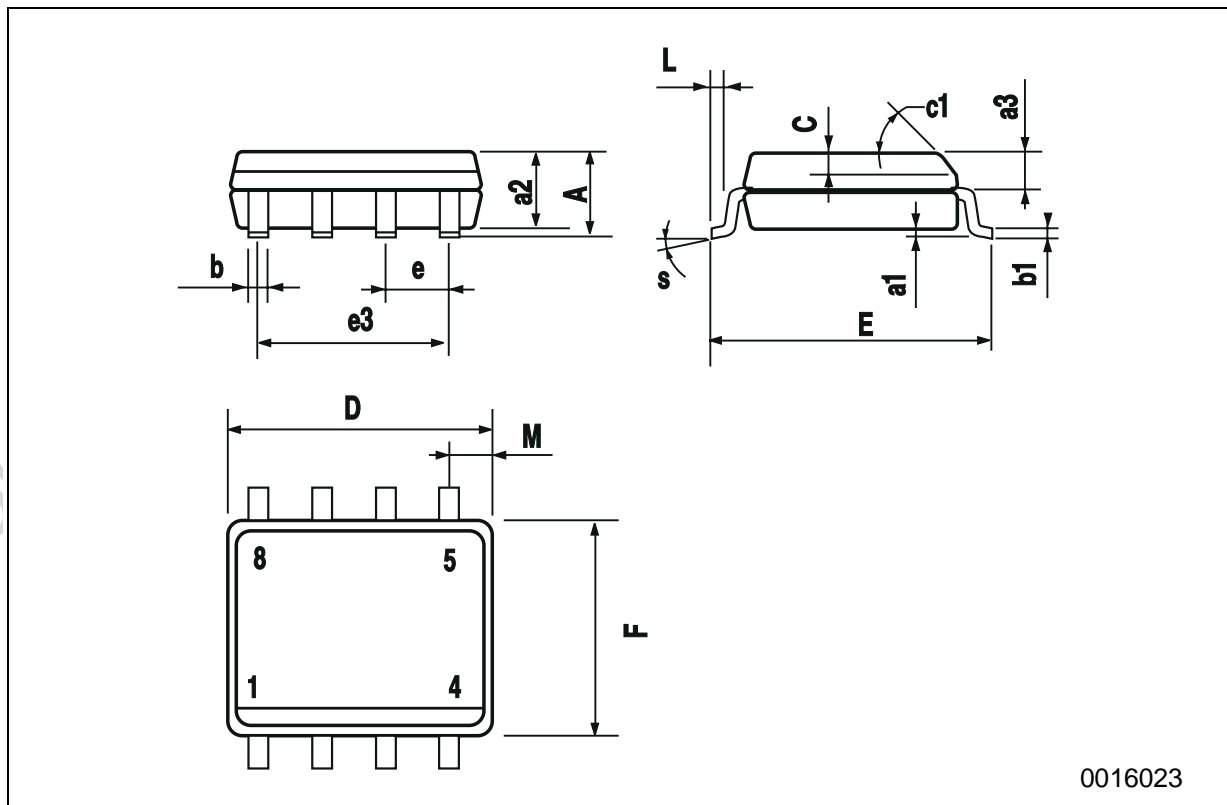
Fig. 3: Test Circuit For Diode Recovery Behaviour



Obsolete Product(s) - Obsolete Product(s)

SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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