Five-level active neutral point clamped flying capacitor inverter design based on OptiMOS™ 5 150 V

Author: Mostafa Khazraei, Peter B. Green

Get exclusive information
Register product

About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to the multilevel inverter demonstration board EVAL_4KVA_230VAC_5LINV, based on the five-level active neutral point clamped flying capacitor topology using OptiMOS™ 5 MOSFETs. The circuit functionality is discussed in detail. System implementation including converter architecture, control algorithms and firmware is also described in detail. Waveforms are shown under all operating conditions, and test measurement data is presented.

Intended audience

This application note is intended for design engineers, applications engineers and students.

Infineon components featured

- **BSC093N15NS5** OptiMOS™ 5 150 V N-channel in a SuperSO8 package
- **IPT60R022S7** 600 V CoolMOS™ S7 superjunction MOSFET in TO-Leadless (TOLL) package
- The EiceDRIVER™ **2EDF7275F** dual-channel isolated MOSFET gate-driver IC
- **XMC4700-F144F2048** 32-bit microcontroller with ARM® Cortex-M4 (XMC™)

Table of contents

1 Introduction

1.1 Switching cells

When discussing inverters, it is convenient to use the term *switching cell* to describe any combination of switches driven by a particular gate drive signal or its complement. A simple example is shown below.
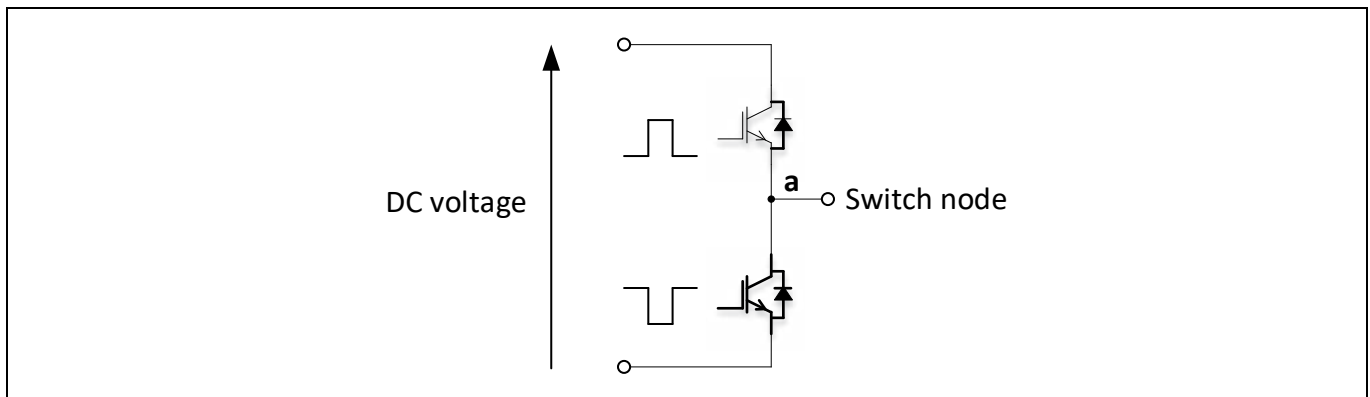

Figure 1 A simple switching cell

In practice, a switching cell can be much more complicated than this example, consisting of several series and parallel MOSFET or IGBT power device blocks, which may be placed in different locations within the topology of the inverter. When driven by the same gate drive PWM signal or its complement, these combine to form switching cells. An individual switching cell has three states – that is, one switch on and the other off, the opposite or both switches off. An inverter is said to be *multilevel* if its topology contains more than one switching cell per half-bridge.

1.2 Inverter types

A broad definition of an inverter is a power converter that converts a DC input to an AC output. For most applications, a pure sine wave output is desirable. Inverters cover many different applications, such as photovoltaic (PV) systems, energy storage systems (ESS) and motor drives covering power ratings ranging from tens of watts to megawatts and utilizing a variety of different architectures and topologies. Most PV and ESS inverters are grid-tied, requiring complex control of frequency, voltage, power factor and power flow. At higher power levels, three-phase inverters are used, which include three single-phase stages with output voltages synchronized at 120 degrees apart. This application note describes in detail the EVAL_4KVA_230VAC_5LINV multilevel inverter designed to produce a single-phase line frequency sinusoidal output for connection to standard loads. The control strategies required for grid-tied operation are not covered, though the design could be upgraded to make this possible.

Modern inverter implementations are based on several different power semiconductor technologies, including silicon MOSFETs, IGBTs and also wide bandgap technologies such as SiC and GaN to form the switching cells that make up the topology. Choice of power switch type is determined by power, voltage, type of topology and cost/performance trade-offs. Inverters can be classified by the number of switching levels implemented.

Introduction

1. *Two-level inverters*

The most basic types of inverter use classic two-level topologies, in which there are only two possible voltage levels existing at the output of the power converter switching stage that feeds the output filter. The switching voltage is pulse width modulated using bipolar modulation at switching frequency F_{sw} according to a sinusoidal reference. Frequency components of F_{sw} are filtered out by the output filter to produce a sine wave output.
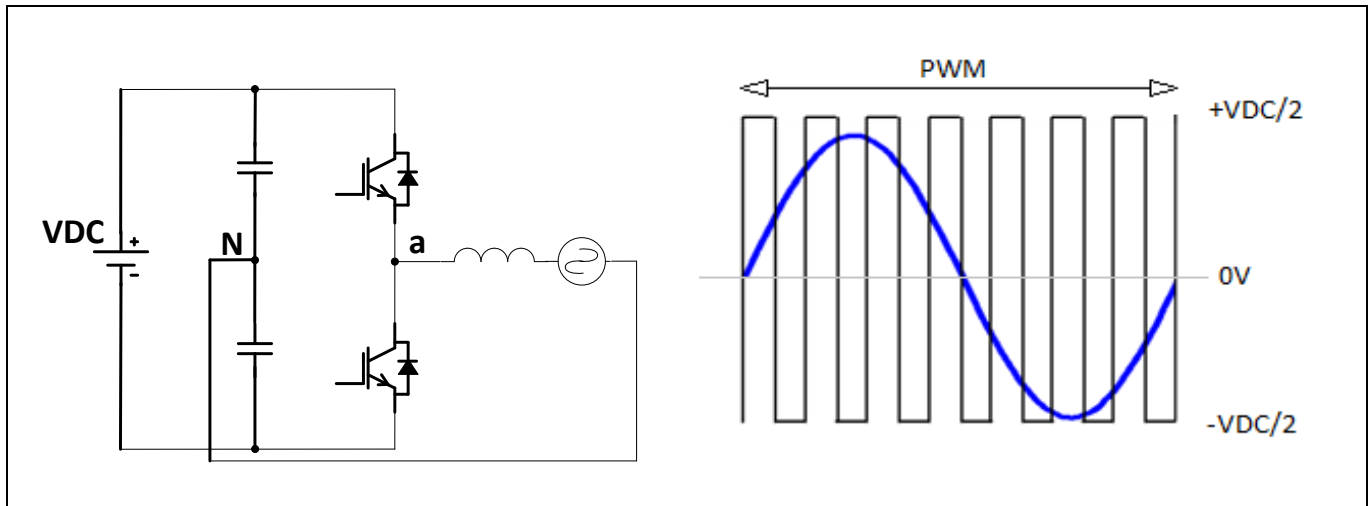

Figure 2   Two-level inverter basic schematic and operating waveforms

The figure above shows a simple half-bridge implementation of a two-level inverter containing one switching cell, where the switching node "a" can either be at +VDC/2 or -VDC/2 potential depending on which of the two switches is on. The output is returned to the mid-point of two series capacitors, which provides the 0 V neutral point. In applications like PV, ESS VDC is usually higher than 400 V. Therefore, high voltage (HV) switches must be used with their associated conduction and switching losses, which limits the overall efficiency. Furthermore, the output filter is necessarily large to remove enough of the high-frequency (HF) components to produce a clean sine wave output at the rated power.

2. *Three-level inverters*

In a three-level inverter, there are three possible voltage levels existing at the output of the power converter switching stage that feeds the output filter, which are +VDC/2, -VDC/2, and the 0 V mid-point. A bidirectional switch composed of two back-to-back power devices enables the switch node to be connected directly to 0 V again, provided by two series capacitors in the most basic implementation. This inverter still contains only a single switching cell and is not considered to be multilevel.
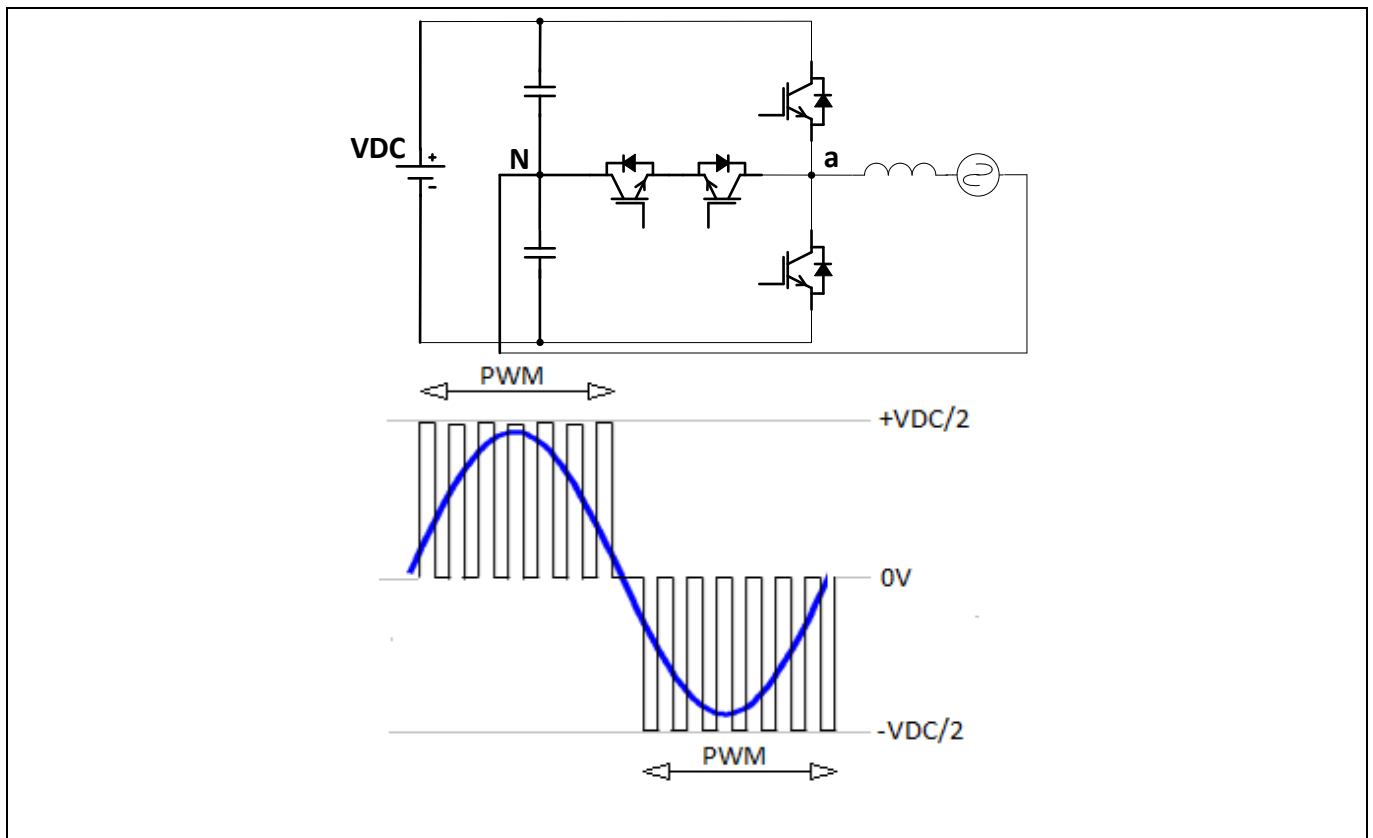
Figure 3   Three-level inverter basic schematic and operating waveforms

The figure above shows a half-bridge implementation of a three-level transistor clamped T-type inverter where the switching node "a" can either be at +VDC/2 or –VDC/2 potential if one or other of the half-bridge switches is on and the other is off. Additionally, it can be connected to 0 V with the ability to transfer current in either direction through the bidirectional back-to-back switches. The output is returned to the same 0 V mid-point of the two series capacitors, which again provides the 0 V neutral point.

There are other implementations of the three-level inverter, including H-bridge topologies that can eliminate the need for the capacitor divider at higher power levels. There are also three-level inverter topologies that include more than one switching cell, which qualifies them as multilevel.

3.   *Multilevel inverters*

In multilevel inverters, there are at least three possible voltage levels existing at the output of the power converter switching stage that feeds the output filter including the 0 V mid-point and +VDC/2 and –VDC/2. The number of levels is always an odd number, since each level is available in either polarity with the exception of 0 V. Switching occurs during different time periods between two adjacent voltage levels to create a composite waveform, which contains HF components of amplitude VDC/(N-1) that requires less filtering to provide a sine wave output.
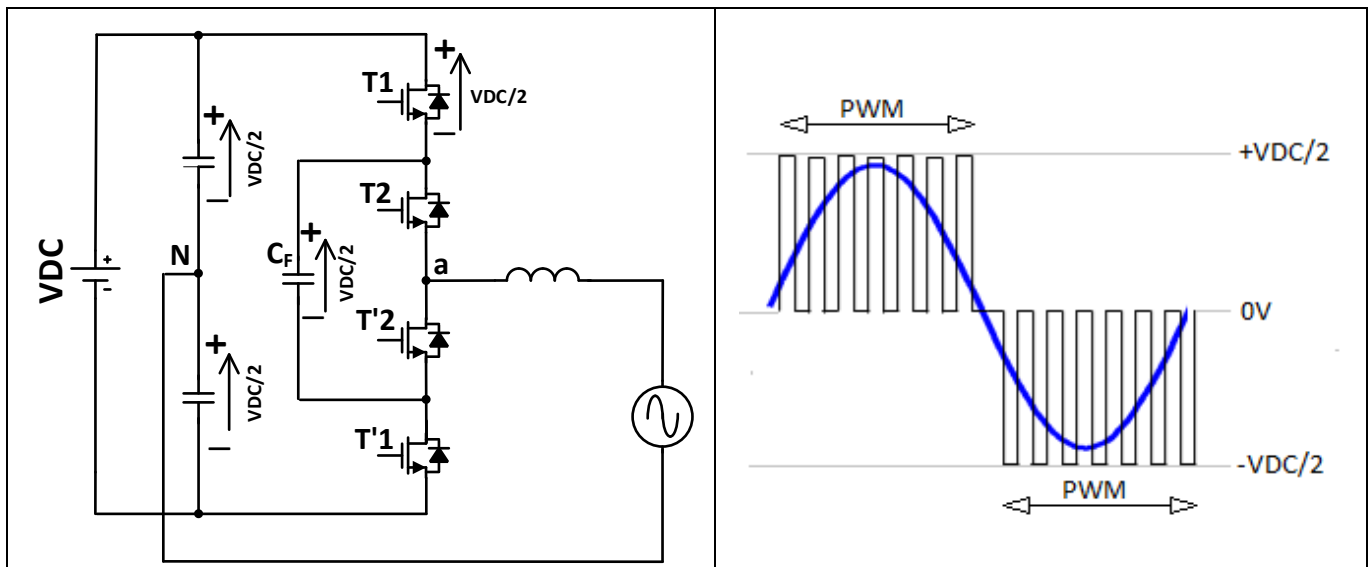
Introduction

Figure 4   **Three-level flying capacitor inverter basic schematic and operating waveforms**

Table 1   **Three-level flying capacitor inverter switching states**

Switching states	T1	T2	T'1	T'2	V_{aN}
1	1	1	0	0	+VDC/2
2	1	0	0	1	0
3	0	1	1	0	0
4	0	0	1	1	-VDC/2

The above example shows a three-level inverter that is considered multilevel because there are two switching cells, one comprising T1 and T'1 and the other comprising T2 and T'2. There are four switching states used during operation – for all of which, two MOSFETs are on and two are off, as shown in Table 1.

Multilevel inverters are able to use lower-voltage trench MOSFET switches that offer very low $R_{DS(on)}$ and body diode recovery charge Q_{rr} compared to HV superjunction MOSFETs or IGBTs. Greatly reduced conduction losses combined with reduced switching losses make it possible to reach very high efficiency. An inverter without the need for a heatsink or fan can then be designed. The multilevel inverter has become popular in medium- and high-power applications because of the reduced power dissipation of switching elements, smaller output filter size, lower harmonic content, and significantly lower EMI.

Some inverter designers may be concerned by the increased level of complexity involved in a multilevel design compared to traditional topologies, due to the higher number of switches and isolated gate drivers needed. However, above a certain power level, usually in the greater-than 3 kW range, the benefits of the multilevel approach such as reduction in size and weight combined with higher efficiency and power density can justify the additional complexity. As the power rating of power inverters increases, the share of mechanical parts such as heatsink and filter increase in size and cost compared to the semiconductor devices' portion. This is why a multilevel inverter will be even more beneficial as the power range increases.

There are several configurations of multilevel inverter, including:

      a.   Diode clamped multilevel inverters (DC-MLI)

      b.   Flying capacitor clamped multilevel inverters (FC-MLI)

      c.   Cascaded H-bridge multilevel inverters (CHB-MLI)

Introduction

A further FC-MLI example is shown in **Figure 5** – in this case a five-level flying capacitor inverter. In FC-MLI the so-called "flying capacitors" (sometimes referred to as "floating capacitors") float with respect to ground potential. In the following example the five-level inverter utilizes the intermediate voltage levels +VDC/4 and -VDC/4 as well as +VDC/2, 0 V and –VDC/2. In this case, three flying capacitors are used, with voltage balance achieved by using *redundant switching states*, meaning combinations where the capacitors may be charged or discharged while the output node remains at the same potential in both states. In the **Figure 4** example switching states 2 and 3 are redundant, either adding or removing charge from the flying capacitor C_F while the output node is held at 0 V. As will be explained later, phase-shifted pulse width modulation (PSPWM) is used to generate the switching states including the redundant switching states to balance the voltage of capacitors.
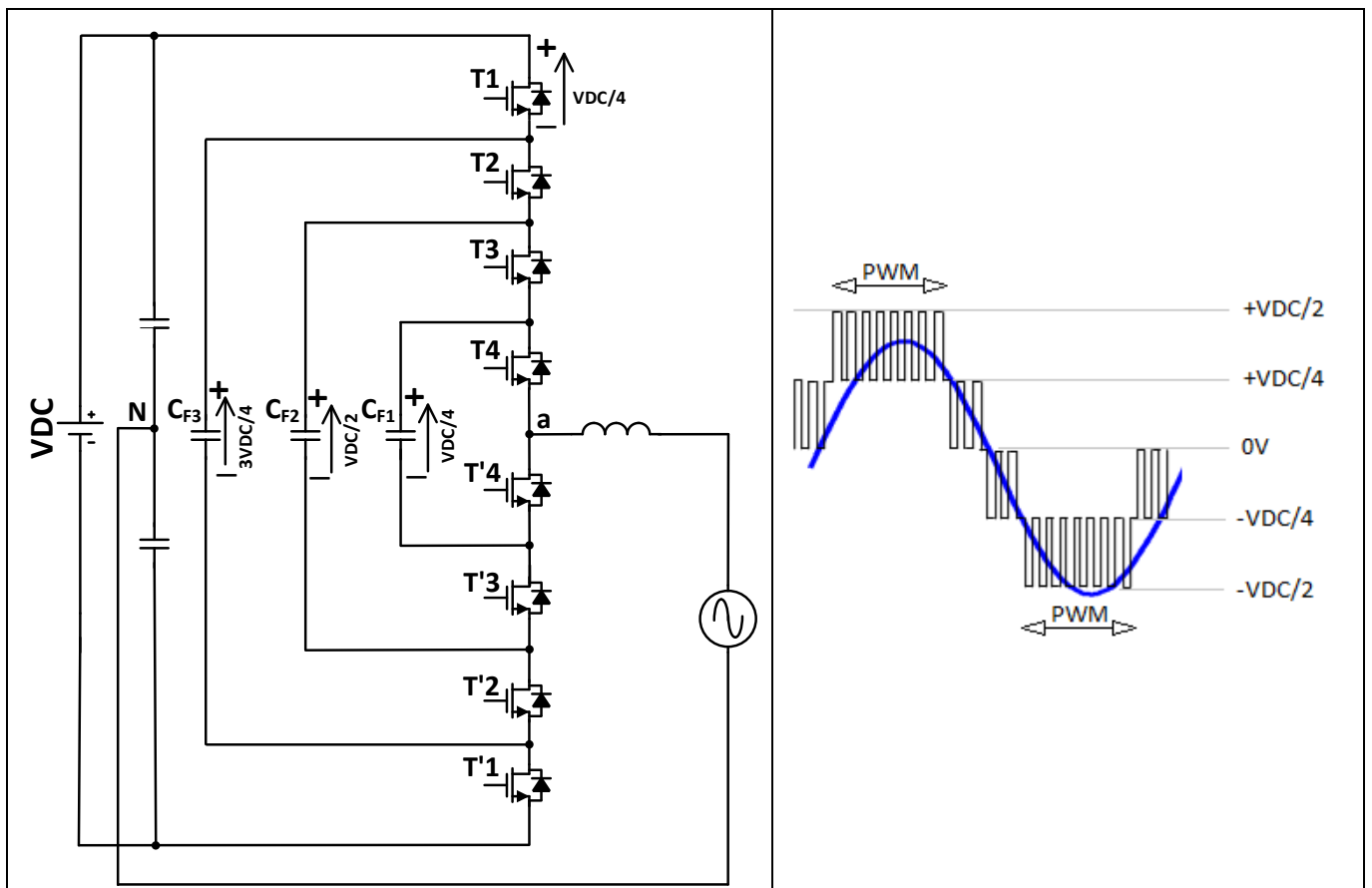

Figure 5   **Five-level flying capacitor inverter basic schematic and operating waveforms**

In the example above, there are four switching cells. The complexity has greatly increased from the three-level to the five-level implementation of the FC-MLI, which now requires three flying capacitors. The number of switching states required for operation has also increased to 16, calculated by the formula $N_s = 2^{(N-1)}$ where N is the number of levels.

The topology shown in **Figure 6** is a derivative of the five-level inverter shown in **Figure 5**, which replaces three flying capacitors with only one. This is known as a *hybrid* multilevel inverter, which allows a five-level design to be realized with only two switching cells (HF PWM switching cells) combined with other MOSFETs switching at line frequency (low-frequency PWM switching cells) for polarity toggling. This hybrid topology is called active neutral point clamped flying capacitor inverter (ANPC-FC). The evaluation board EVAL_4KVA_230VAC_5LINV described in this application note is based on this topology. The differences between two-level inverters, general multilevel inverters (Figure 5) and this hybrid multilevel inverter ANPC-FC are listed in Table 2. Please note that the information in Table 2 is based on the inverter in a half-bridge configuration.
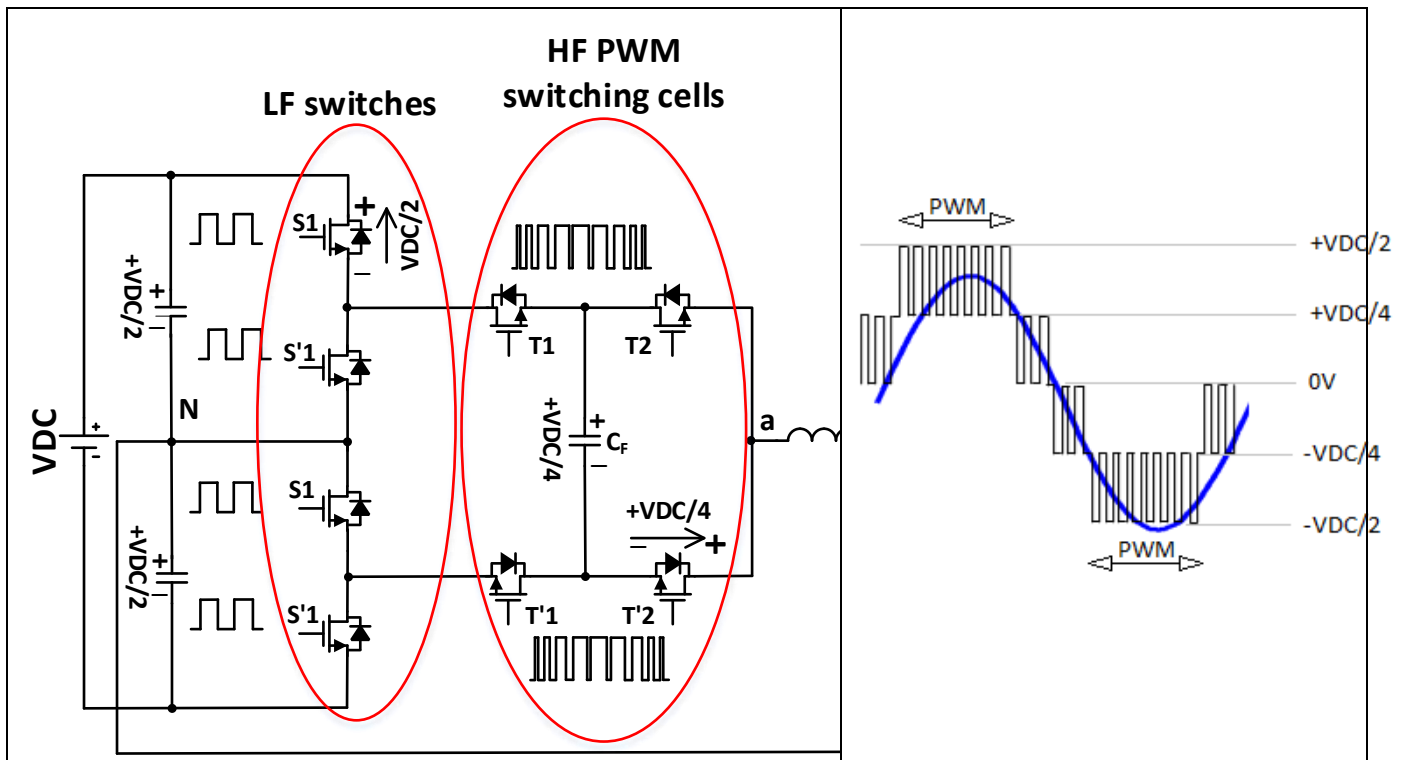
Figure 6   Five-level ANPC-FC inverter basic schematic and operating waveforms

Table 2   Comparison of key parameters for multilevel vs. two-level inverters

	Two-level	N-level	ANPC-FC	Comment
Number of HF switching cells N_{sc}	1	N-1	(N-1)/2	Lower number of N_{sc} for ANPC-FC for the same N.
FET blocking voltage	VDC	VDC/(N-1)	VDC/(N-1)	HV FET/IGBTs replaced with lower-voltage FET. Significant reduction in loss is achieved.
Effective output frequency	F_{sw}	(N-1) × F_{sw}	(N-1)/2 × F_{sw}	Higher output frequencies with lower switching losses. F_{sw} = MOSFET switching frequency.
Output inductor	L	$L/(N_{sc})^2$	$L/[N_{sc} \times (N\text{-}1)]$	Significant reduction in size and weight.
EMI	Switching at VDC	Switching at VDC/(N-1)	Switching at VDC/(N-1)	Improved due to reduced switching voltages.
Number of switches	2	2 × (N-1)	≤2 × (N-1)	Lower number of MOSFETs needed for ANPC-FC if HV MOSFETs used as LF switches.

1.3 Evaluation board description

The EVAL_4KVA_230VAC_5LINV evaluation board has a full-bridge configuration and consists of two five-level ANPC-FC half-bridge inverters operating 180 degrees out of phase with each other to provide a differential multilevel voltage output. The basic structure of this board is shown in **Figure 7**. The load is connected between points "a" and "b", via the output filter. Each half-bridge consists of 24 switches; 16 are switching at line frequency (these will be referred to as the low-frequency (LF) switches) and eight are switching at the high frequency (these will be referred to as the high-frequency (HF) switches). All these 48 MOSFETs are OptiMOS™ 5 150 V BSC093N15NS5 devices. This MOSFET has very low $R_{DS(on)}$, Q_g and Q_{rr}. In an N-level ANPC-FC multilevel inverter the voltage of the flying capacitor is VDC/(N − 1). Then for a five-level inverter operating from a 400 VDC bus, V_{FC} = 400/(5 − 1) = 100 V. That means the voltage each one of the HF switches has to withstand is only VDC/4 = 100 V. That is why 150 V MOSFETs can be used here. Also, to be able to use the same 150 V MOSFETs in LF sections, MOSFETs are installed in series, as seen in **Figure 7**. Each two MOSFETs that are in series are synchronized and only one single pulse from the microcontroller is needed to control them. When MOSFETs are installed in series, voltage sharing is a concern. However, OptiMOS™ 5 MOSFETs enjoy relatively linear output capacitance (C_{oss}), which helps significantly with voltage sharing. Also, the series MOSFETs here are only switching at line frequency, 60 Hz. As shown later in the test results, the MOSFET voltage sharing is successfully achieved.

There are 12 gate driver ICs in the board, as shown in **Figure 7**. Each gate driver has two channels, and two isolated power supplies are needed per channel (PS1, PS2, …, PS24). Later, it will be shown that these isolated power supplies can be easily implemented in a very cost effective manner using planar transformers with an integrated flyback controller. There are also two HV MOSFETs IPT60R022S7 (650 V, 22 mΩ) that have been used to bypass the inrush current control resistor. These two MOSFETs have been installed in parallel to form the DC relay switch (DRC), as shown in **Figure 7**.

While there are lot of MOSFETs and gate drivers used in this design, the overall system control is not as complicated as it may initially appear. To better understand how this system is controlled, a simplified version of **Figure 7** has been shown in **Figure 8**, which shows the PWM control signals that are needed for the system to function. Only three PWM signals, S1, T1, T2, are necessary and all of the MOSFETs are controlled either with these three signals or their complimentaries: S'1, T'1, T'2. S1 is a LF pulse 60 Hz, and T1 and T2 are HF pulses in the 16 to 20 kHz range.

The effective output frequency is twice MOSFET frequency, equivalent to ~40 kHz. In this inverter the five-level output voltage between points "a" and "b" will be the following: +VDC, +VDC/2, 0 V, -VDC/2, -VDC. Section 4 of this application note explains how the five-level output waveform is generated.
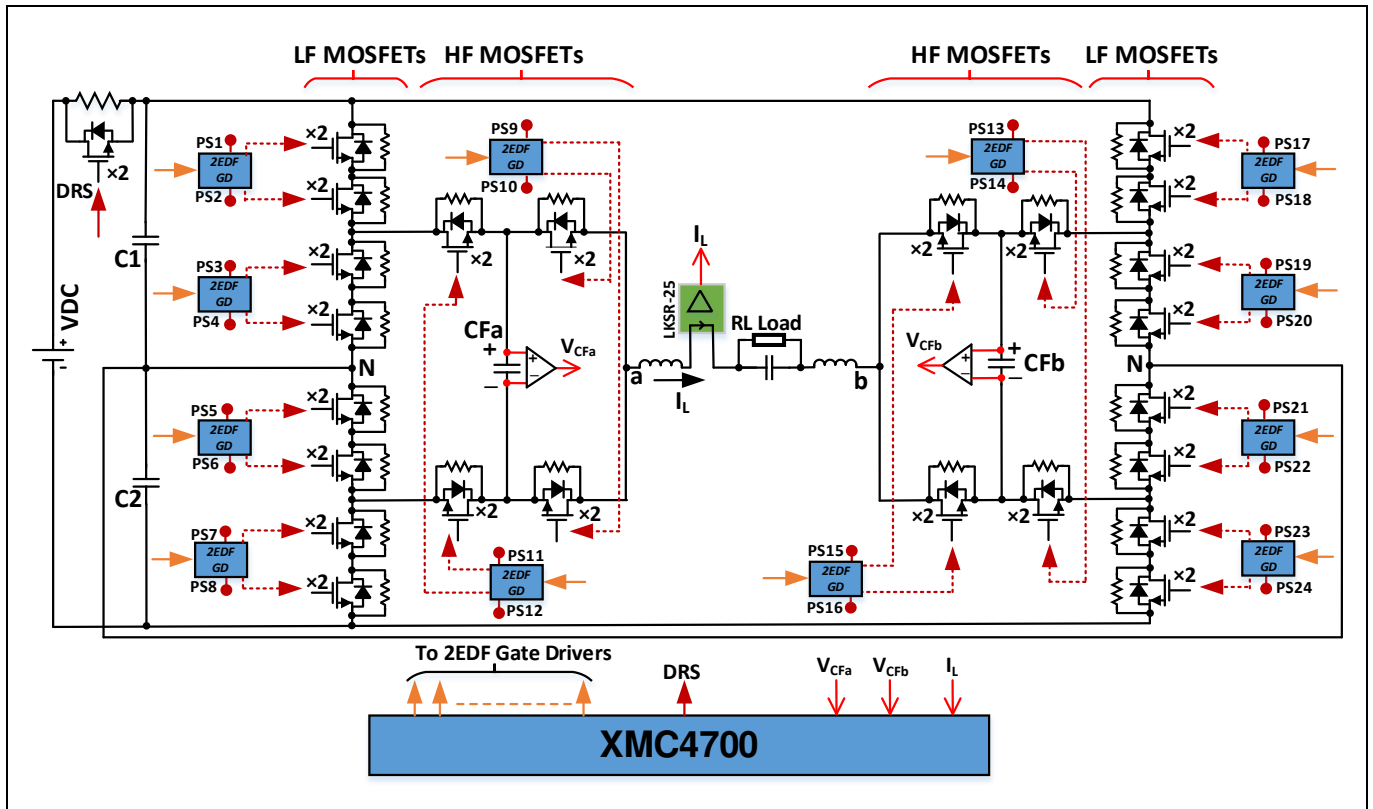
Figure 7   EVAL_4KVA_230VAC_5LINV evaluation board basic architecture
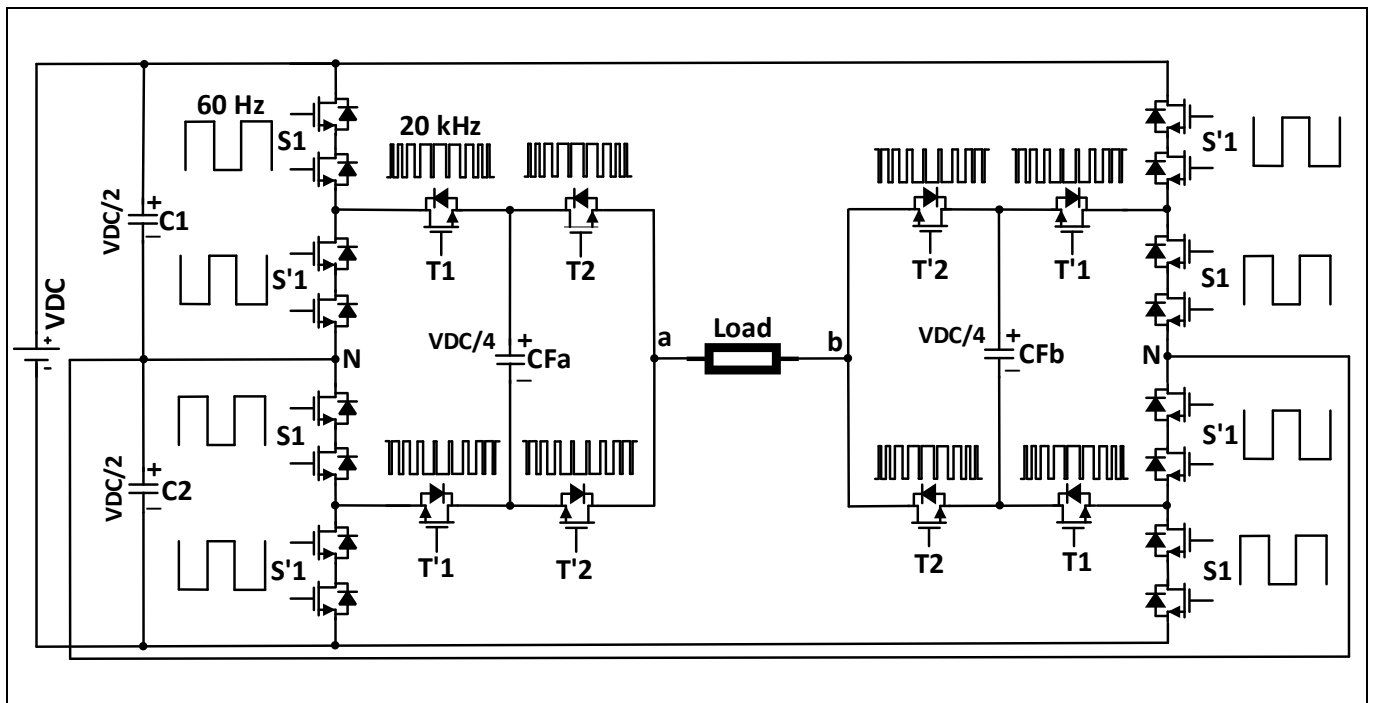
Figure 8   EVAL_4KVA_230VAC_5LINV evaluation board simplified architecture
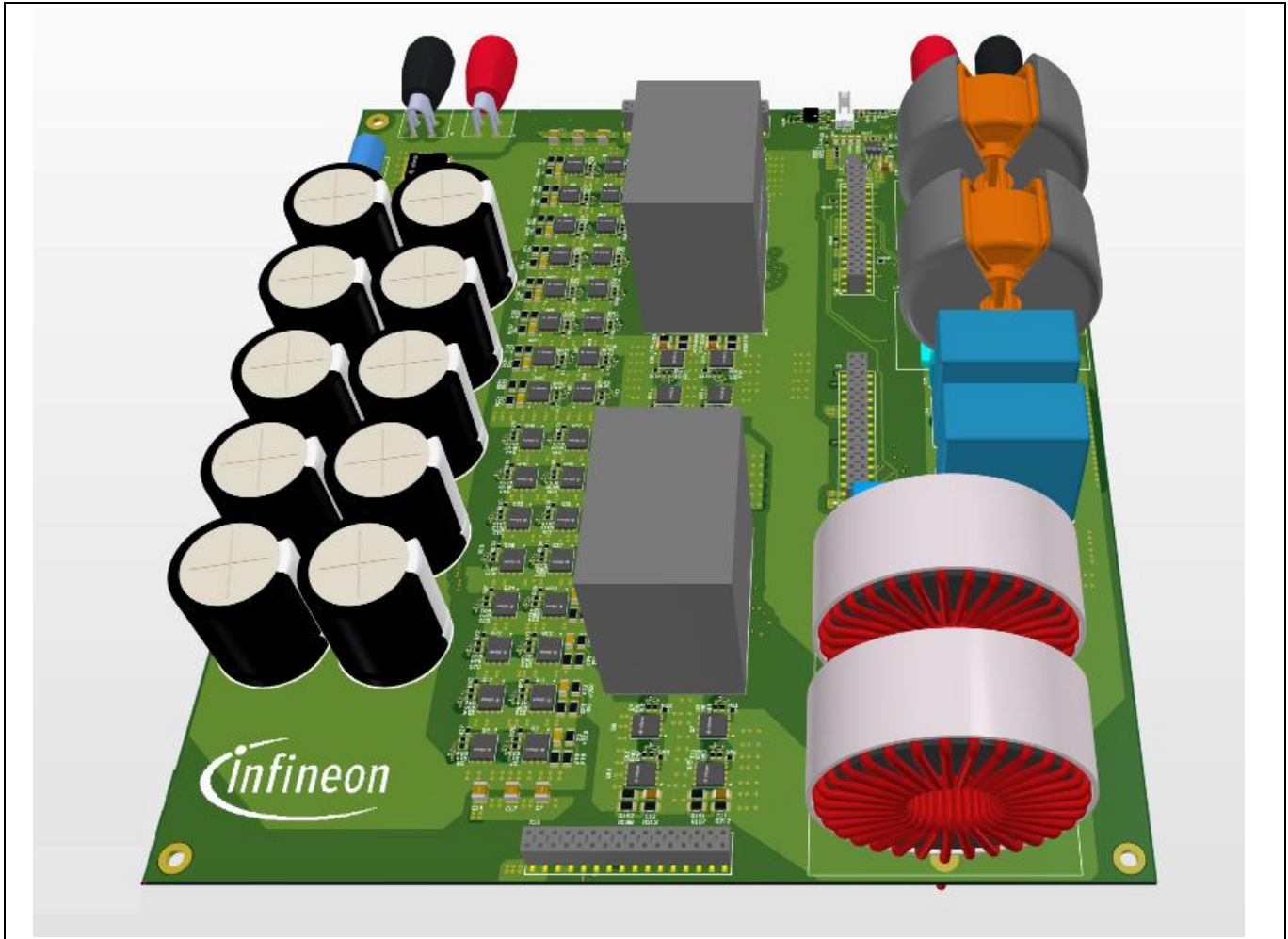
Figure 9   EVAL_4KVA_230VAC_5LINV main board
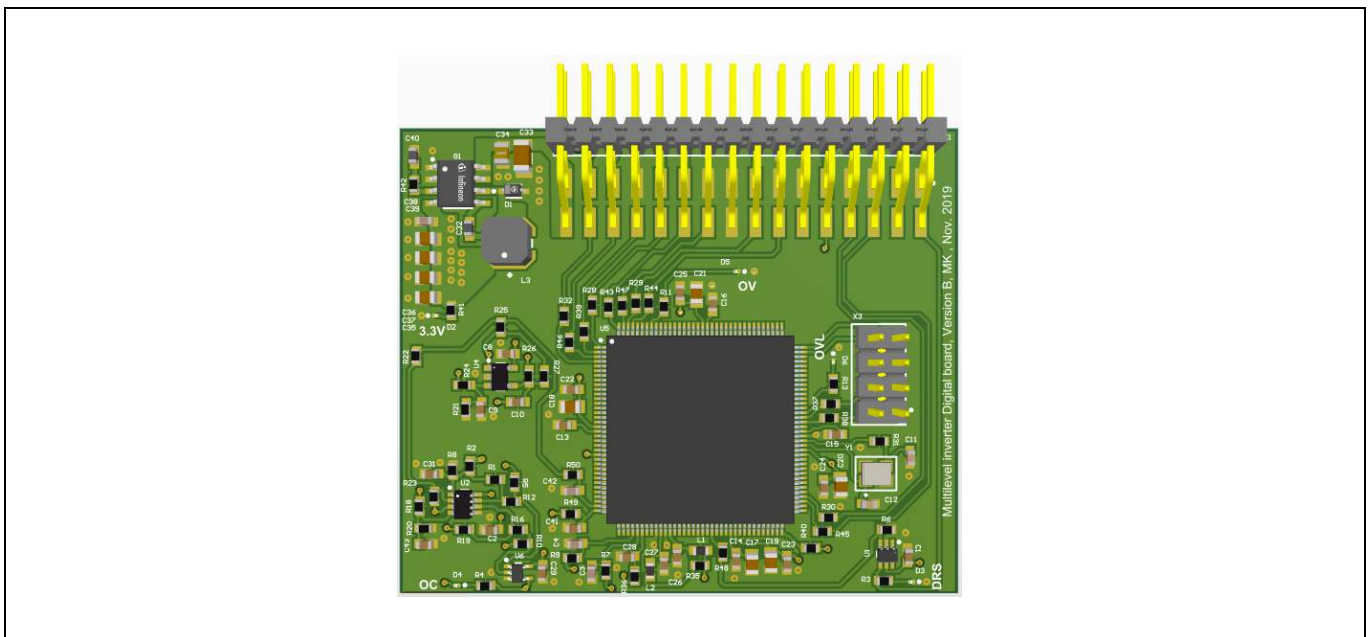
Figure 10   EVAL_4KVA_230VAC_5LINV control card

Figure 11   EVAL_4KVA_230VAC_5LINV auxiliary power – gate driver cards (center)

Figure 12   EVAL_4KVA_230VAC_5LINV auxiliary power – gate driver cards (side)

2 Evaluation board specifications

Input and output in normal operation

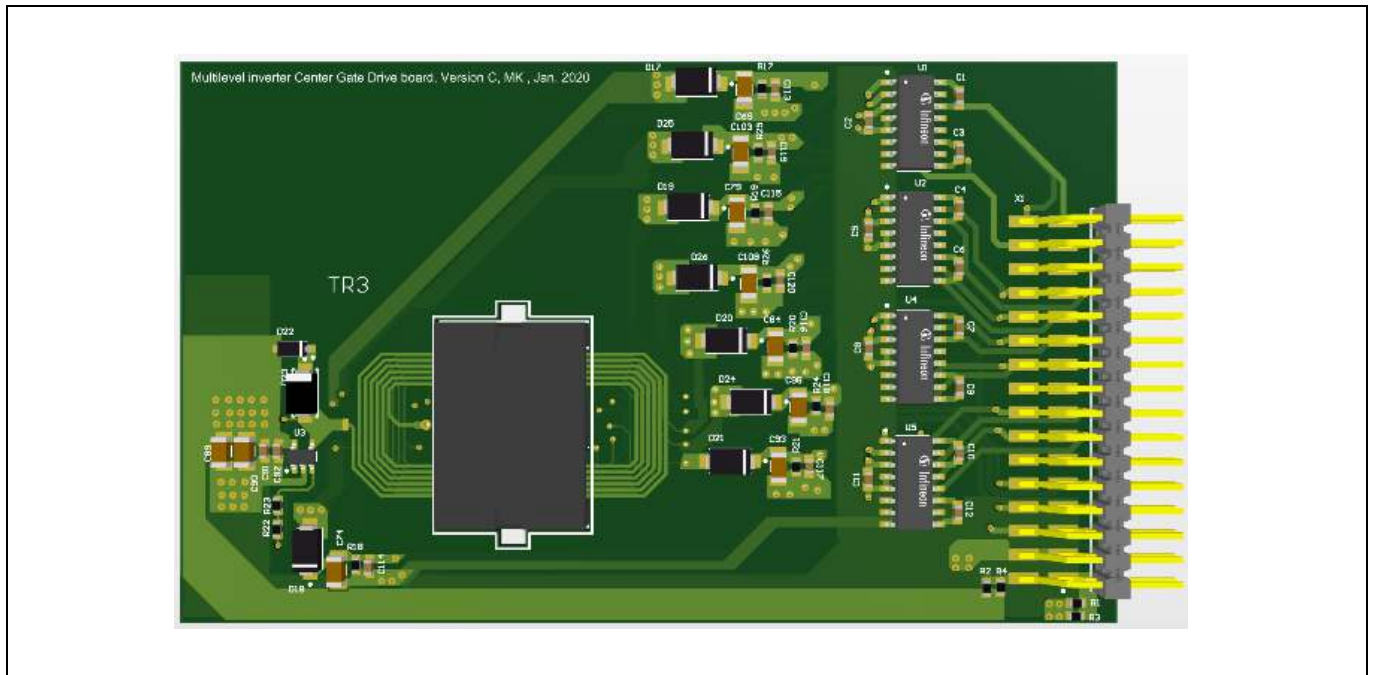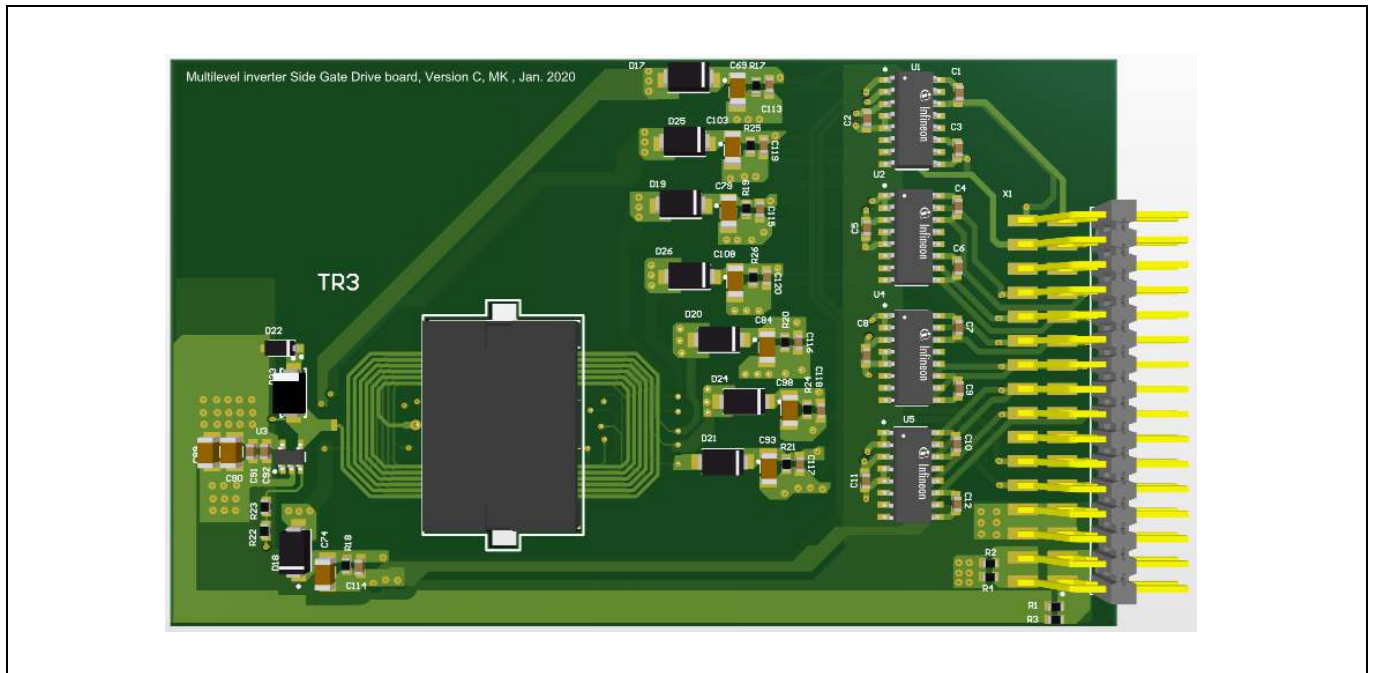- Input voltage 400 V DC nominal
- DC input voltage range: 380 V up to 420 V
- Nominal output voltage 230 V_{RMS} (60 Hz)
- Maximum continuous average input current 12 A
- Maximum output continuous power 4.0 kVA
- Normal loads supported only. No grid-tied operation![1]
- Pure sine wave output
- Inverter start-up time to reach the nominal output voltage during full-load or no-load condition less than 500 ms

Protection features

- DC input undervoltage and overvoltage protection (UVP/OVP)
- Over-load and short-circuit output protection.

Attention: *It is <u>not</u> recommended to short-circuit the output!*

Board dimensions

Main board:

- Maximum width 8.95 inches (227 mm), max. length 7.88 inches (200 mm)

Control board:

- Maximum width 2.36 inches (60 mm), max. length 1.97 inches (50 mm)

Auxiliary power boards:

- Maximum width 3.94 inches (100 mm), max. length 2.36 inches (60 mm)

Attention: *HIGH VOLTAGE OUTPUT! Risk of electric shock.*

Attention: *The board should be tested only by qualified engineers and technicians.*

---

[1] Grid-tied operation may be possible with a firmware upgrade but is NOT currently supported.

3 Evaluation board connections
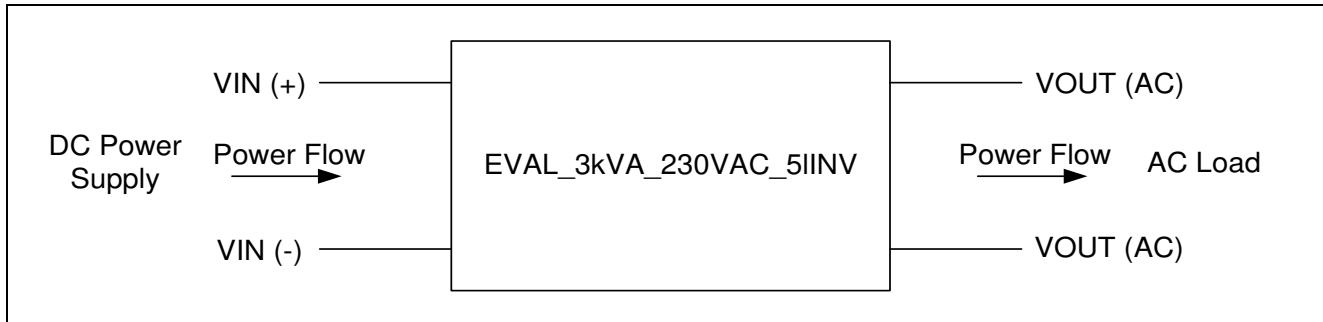
Figure 13   EVAL_4KVA_230VAC_5LINV connections
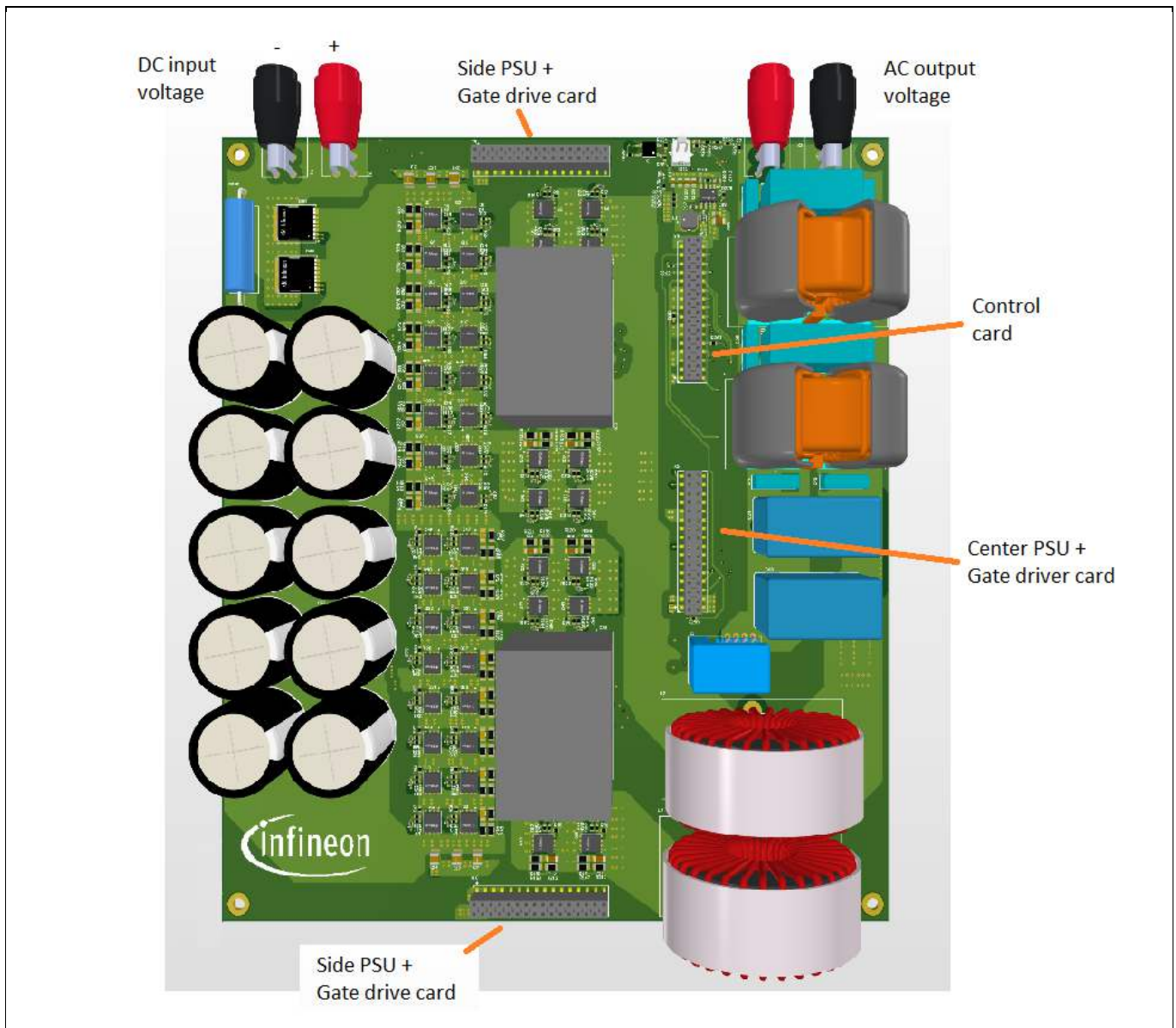
Figure 14   EVAL_4KVA_230VAC_5LINV connection diagram

4 Schematics

Figure 15   EVAL_4KVA_230VAC_5LINV – main board schematic – daughter card connectors
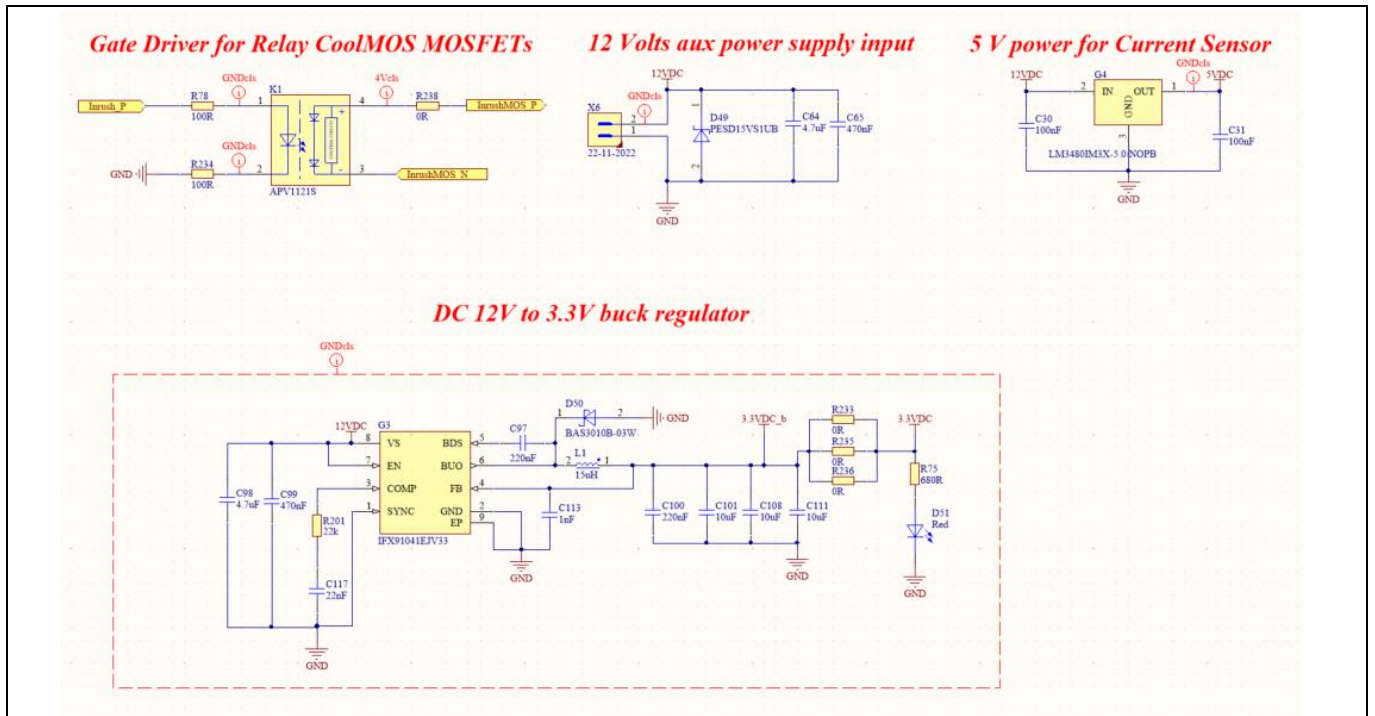
Figure 16   EVAL_4KVA_230VAC_5LINV – main board schematic – auxiliary power supplies
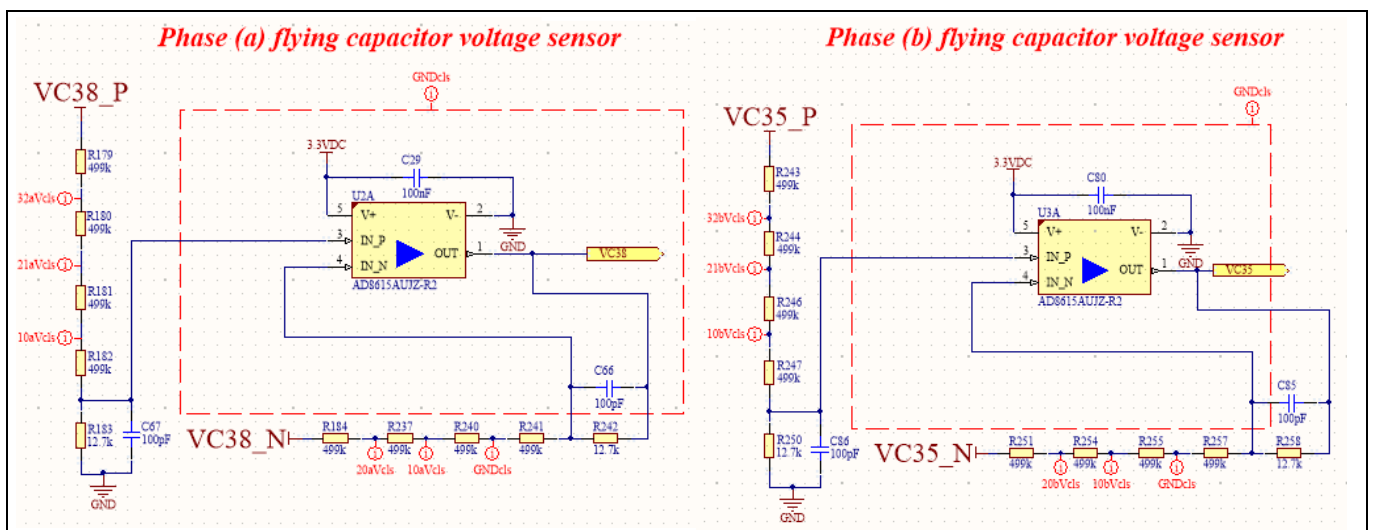
Figure 17   EVAL_4KVA_230VAC_5LINV – main board schematic – flying capacitor voltage sensing

Figure 18   EVAL_4KVA_230VAC_5LINV – main board schematic – DC input section

Figure 19   EVAL_4KVA_230VAC_5LINV – main board schematic – inverter power section (top left)

Figure 20   EVAL_4KVA_230VAC_5LINV – main board schematic – inverter power section (bottom left)

Figure 21   EVAL_4KVA_230VAC_5LINV – main board schematic – inverter power section (top right)

Five-level active neutral point clamped flying capacitor inverter
design based on OptiMOS™ 5 150 V
Schematics
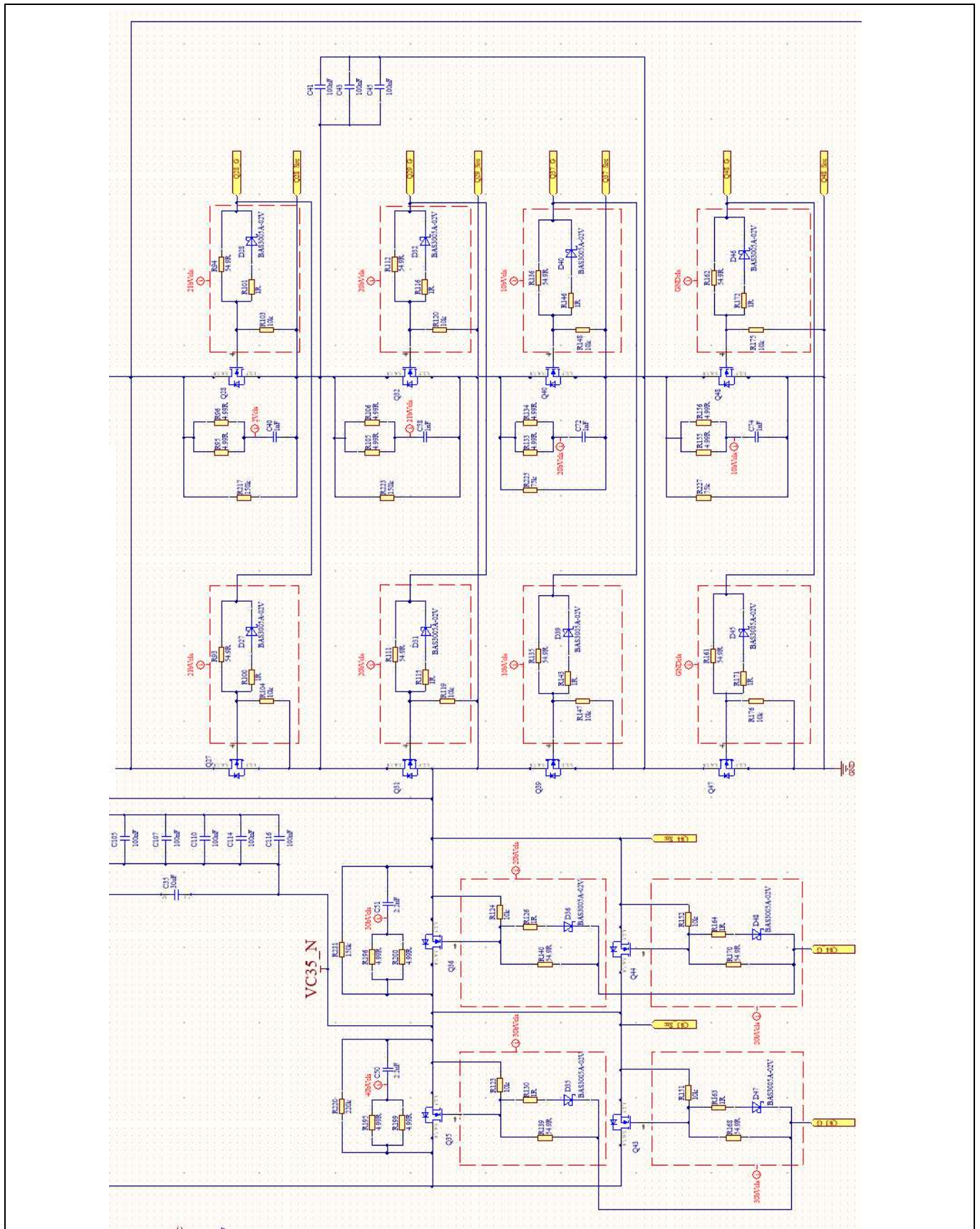
Figure 22   EVAL_4KVA_230VAC_5LINV – main board schematic – inverter power section (bottom right)
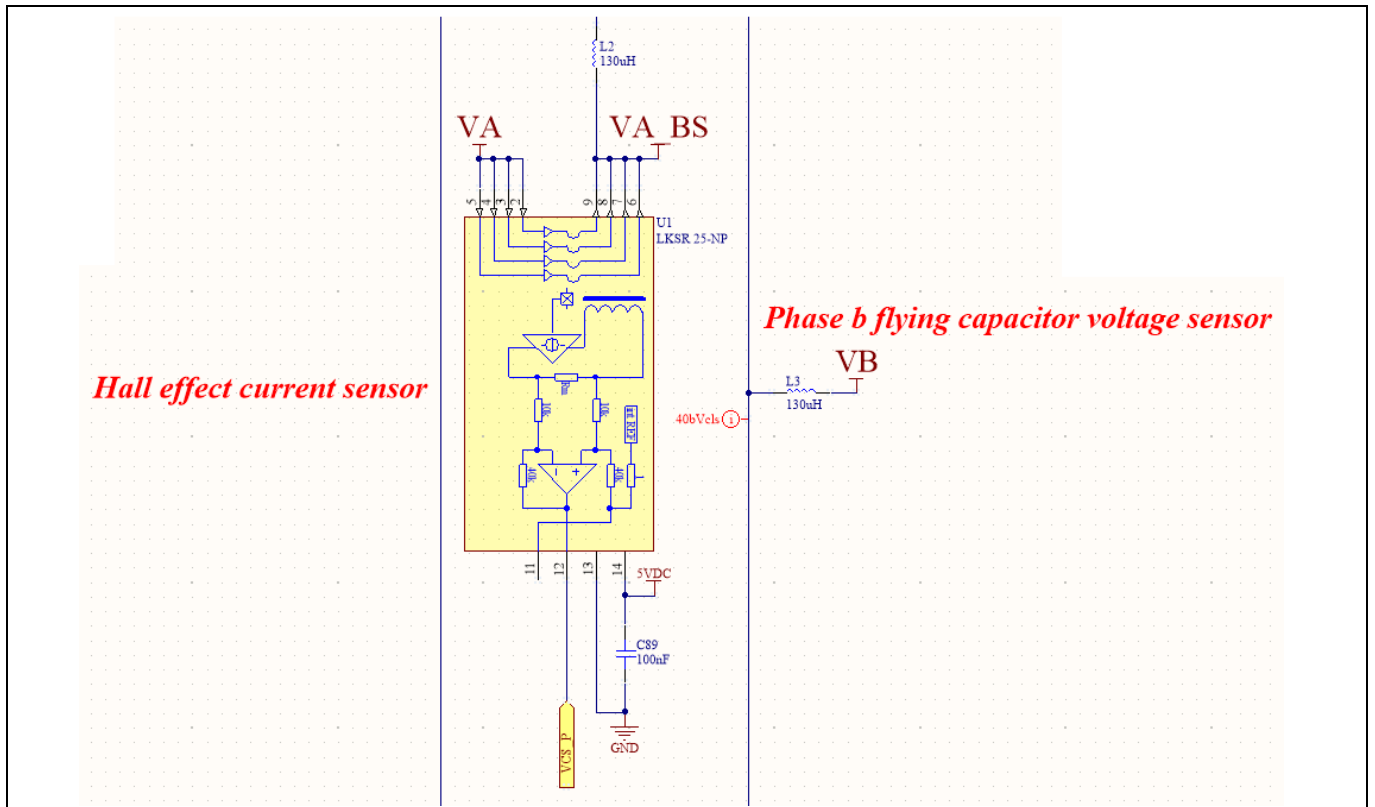
Figure 23   EVAL_4KVA_230VAC_5LINV – hall effect current sensor
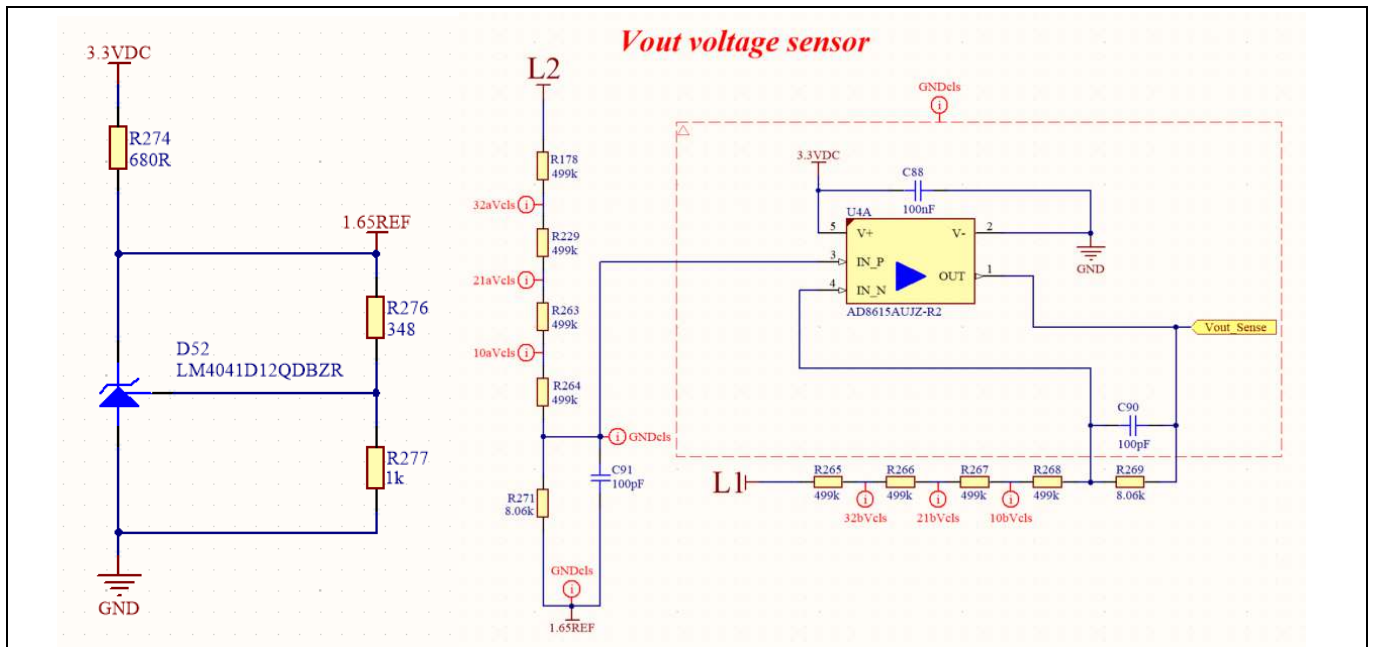
Figure 24   EVAL_4KVA_230VAC_5LINV – output voltage sensing and reference circuit
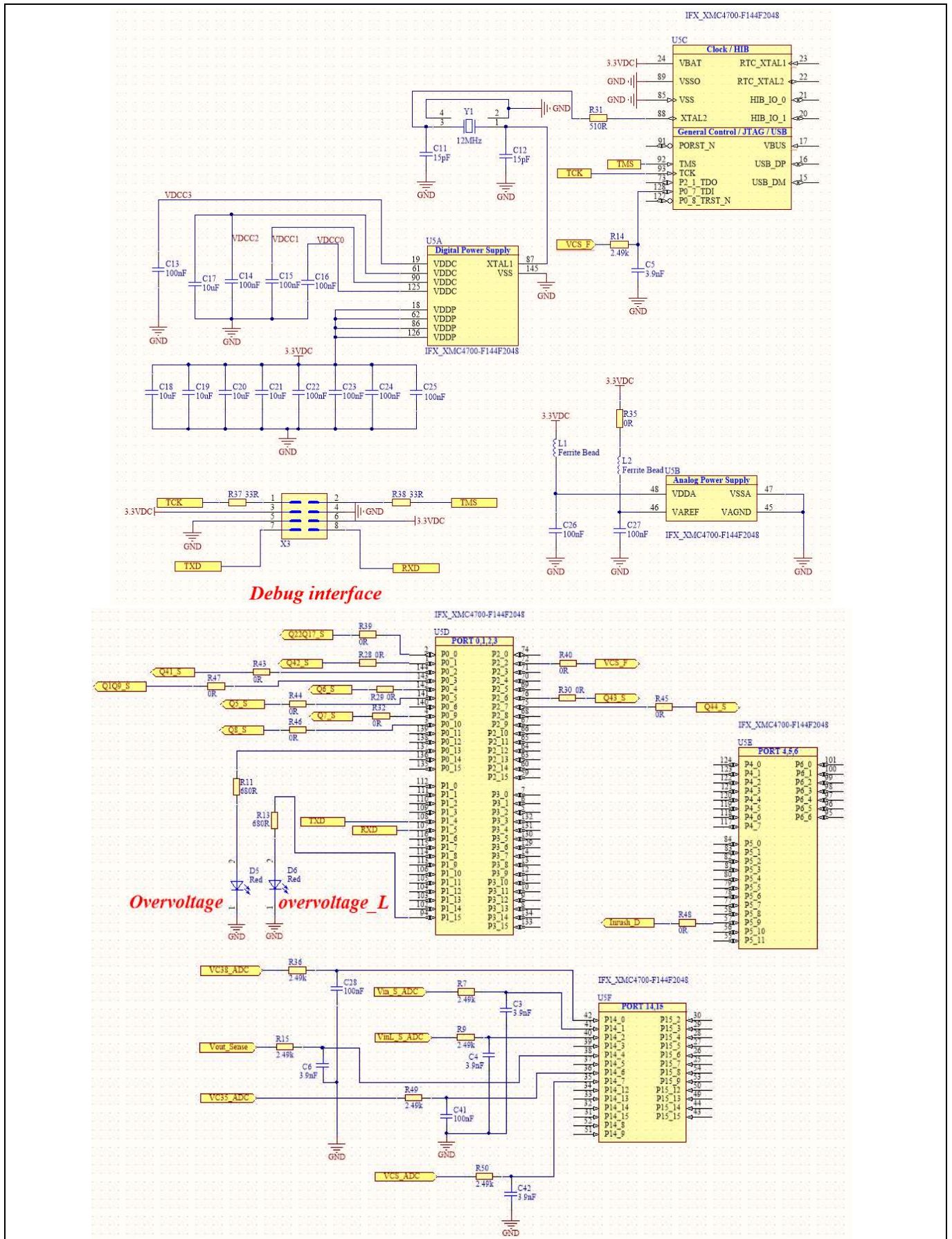
Figure 25   EVAL_4KVA_230VAC_5LINV – control card schematic (1)

Figure 26   EVAL_4KVA_230VAC_5LINV – control card schematic (2)
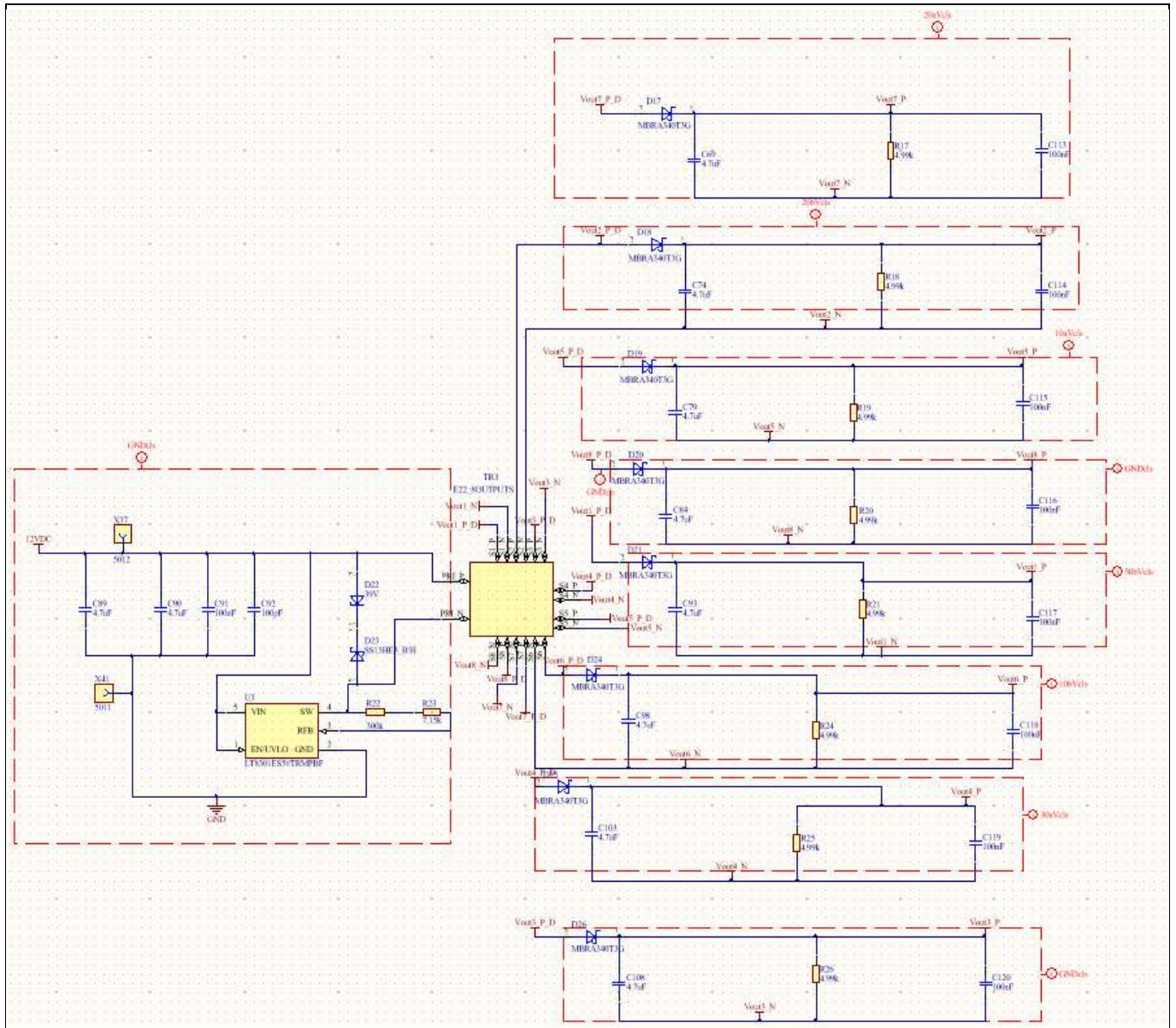
Figure 27   EVAL_4KVA_230VAC_5LINV – auxiliary power supply and gate driver schematic (center) power supply section

Figure 28   EVAL_4KVA_230VAC_5LINV – auxiliary power supply and gate driver schematic (center) gate driver section

Figure 29   EVAL_4KVA_230VAC_5LINV – auxiliary power supply and gate driver schematic (sides) power supply section

Figure 30   EVAL_4KVA_230VAC_5LINV – auxiliary power supply and gate driver schematic (sides) gate driver section

5 Functional description

5.1 Differential five-level ANPC-FC inverter operation

The main board contains the power conversion circuitry based on the circuit shown in **Figure 7**. As mentioned in section 1.2, the differential voltage between the switch nodes "a" and "b" (V_{ab}) can be any one of five distinct levels, shown below.
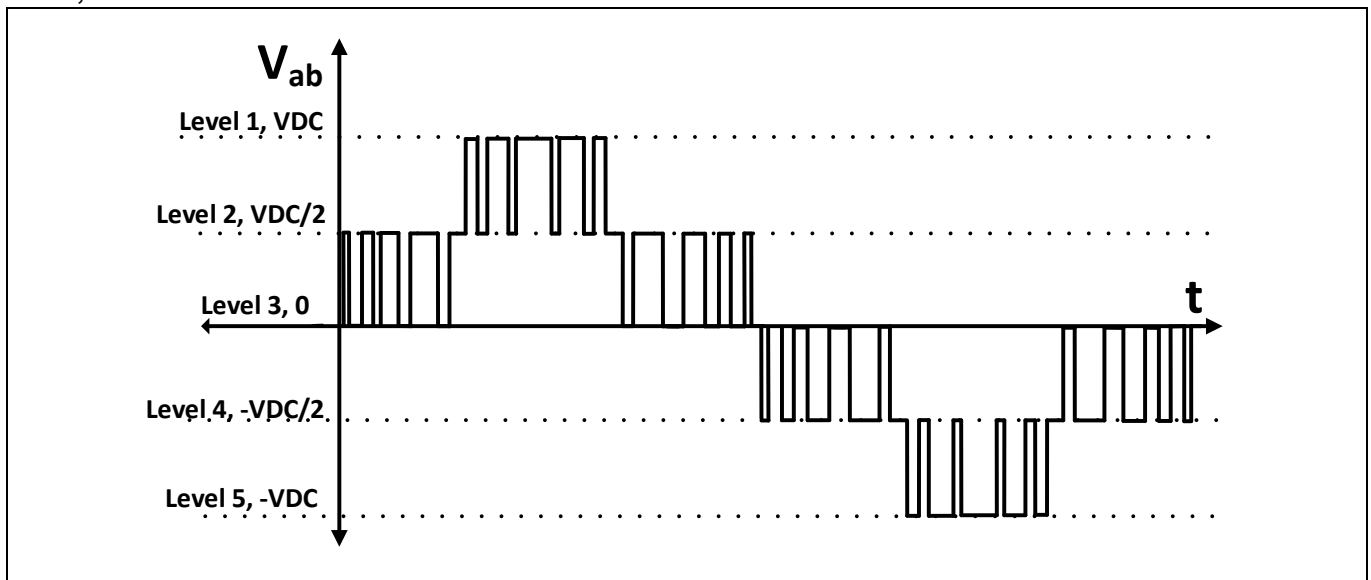
Figure 31   EVAL_4KVA_230VAC_5LINV switching node voltage

The sine wave output is constructed by various switching states, shown in Table 3. The differential voltage V_{ab} shown above is connected via an LC filter to the output, which removes the HF switching component to produce a line frequency sine wave output. Although there are five possible voltage levels available, there are actually eight switching states, as shown in the table below. Switching states 2 and 3, and 6 and 7 are redundant states, so for each of these pairs V_{ab} will be the same, but the flying capacitors C_{Fa} and C_{Fb} are either charging or discharging. By switching between redundant states, the flying capacitor charge balance is maintained. As seen in Table 3, only three independent switching signals, S1 (LF 60 Hz), T1 and T2 (HF PWM ~20 kHz) and their complements are needed to provide all the gate drive signals for this inverter. It will be explained later how by using PSPWM these eight switching states will be generated in hardware.

Table 3   Differential five-level inverter switching states

Switching states	S1	T1	T2	V_a	V_b	V_{ab}
1	1	1	1	VDC	0	VDC
2	1	1	0	3VDC/4	VDC/4	VDC/2
3	1	0	1	3VDC/4	VDC/4	VDC/2
4	1	0	0	VDC/2	VDC/2	0
5	0	1	1	VDC/2	VDC/2	0
6	0	1	0	VDC/4	3VDC/4	-VDC/2
7	0	0	1	VDC/4	3VDC/4	-VDC/2
8	0	0	0	0	VDC	-VDC

Five-level active neutral point clamped flying capacitor inverter
design based on OptiMOS™ 5 150 V
Functional description

5.1.1 Switching states of the differential five-level ANPC-FC inverter

In this section, it is explained how output waveform is generated by applying various switching states from table 3. For the sake of simplicity, it is assumed that power factor is equal to 1 (no phase shift between output voltage and current). During switching state 1, V_{ab} is equal to VDC, the output inductor current is rising (energy transfer) and flying capacitors (CFa and CFb) are bypassed, neither being charged nor discharged by the load current.
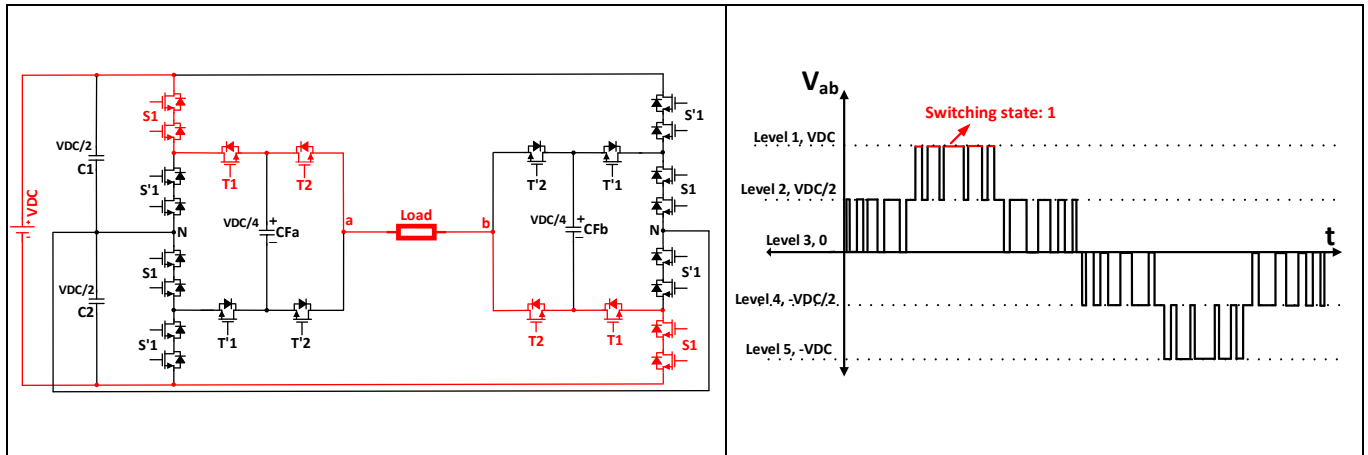
Figure 32   Switching state 1

During switching state 2, V_{ab} is equal to VDC/2 because the flying capacitors are now introduced into the circuit, each blocking VDC/4. The inductor current is rising (energy transfer) with the load current increasing the FC charge.
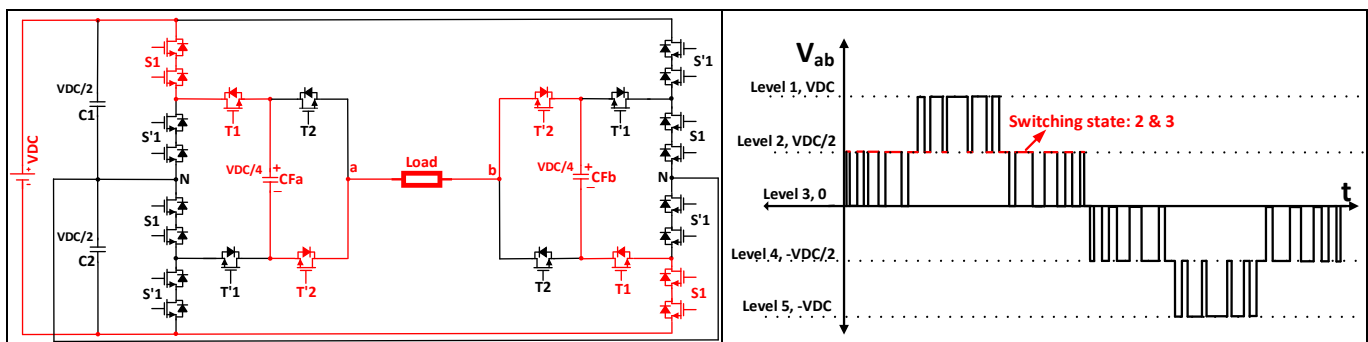
Figure 33   Switching state 2

During switching state 3, V_{ab} is also equal to VDC/2; however, in this case the flying capacitors are still blocking VDC/4. The inductor current is now falling (freewheeling) with the load current discharging both CFa and CFb.
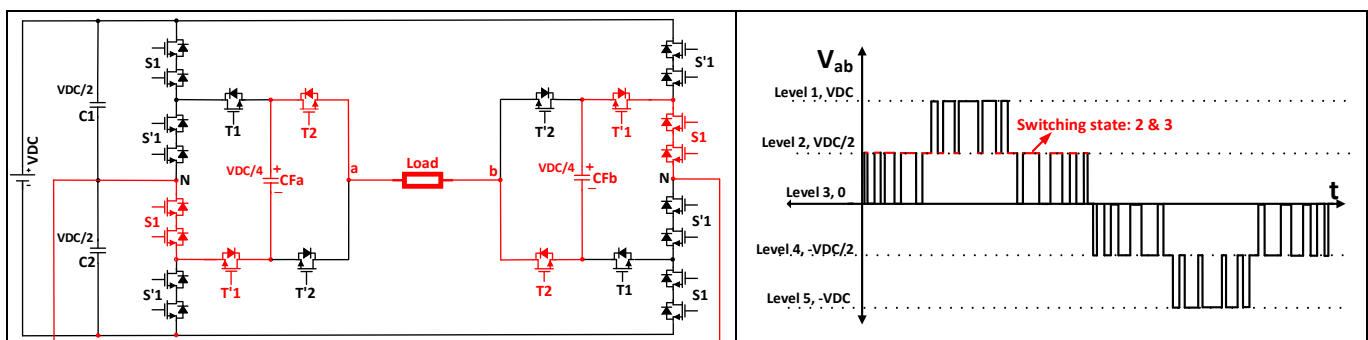
Figure 34   Switching state 3

During switching state 4, V_{ab} is equal to 0 V. In this case the flying capacitors are bypassed. The inductor current falls (freewheeling) and C_{Fa} and C_{Fb} are neither being charged nor discharged by the load current.
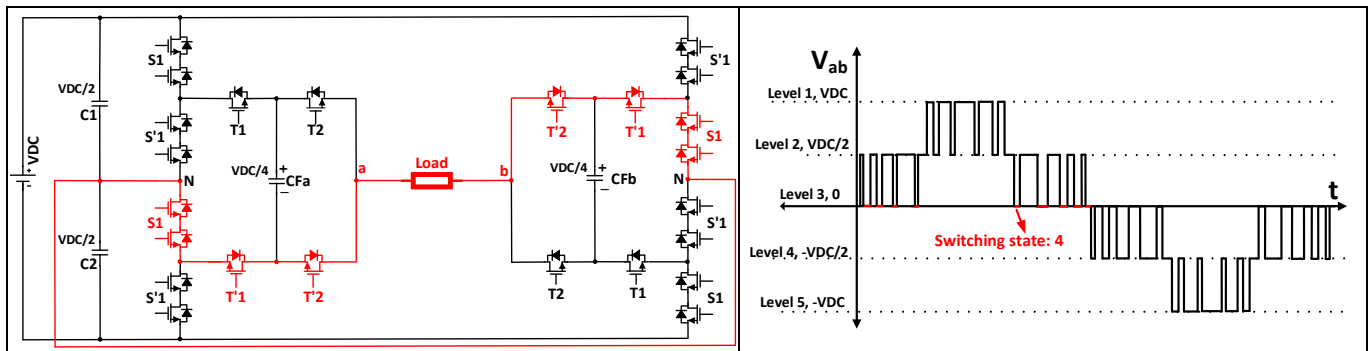
Figure 35   Switching state 4

During switching state 5, V_{ab} is also equal to 0 V. In this case the flying capacitors remain bypassed. The inductor current rises and C_{Fa} and C_{Fb} are neither being charged nor discharged by the load current.
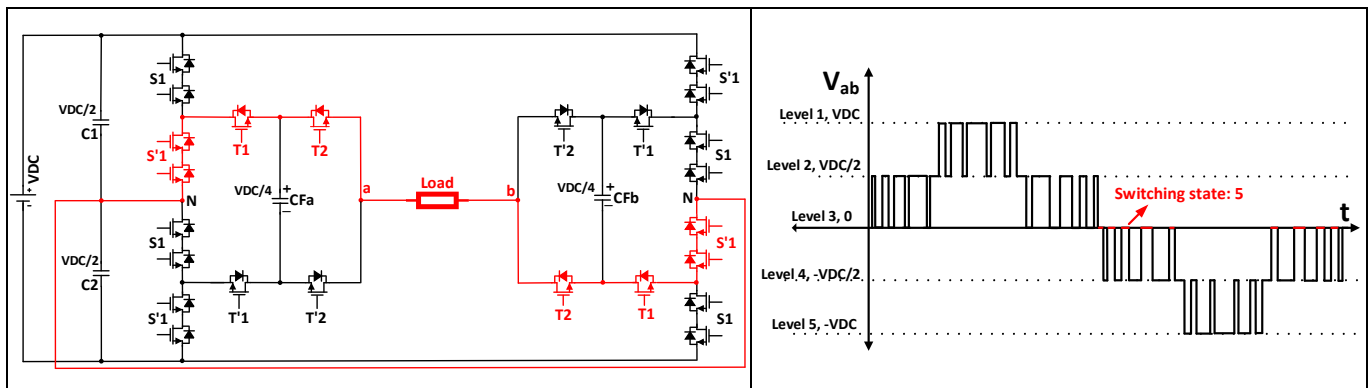
Figure 36   Switching state 5

During switching state 6, V_{ab} is equal to -VDC/2. The reverse inductor current is falling with the load current discharging C_{Fa} and C_{Fb} voltage.
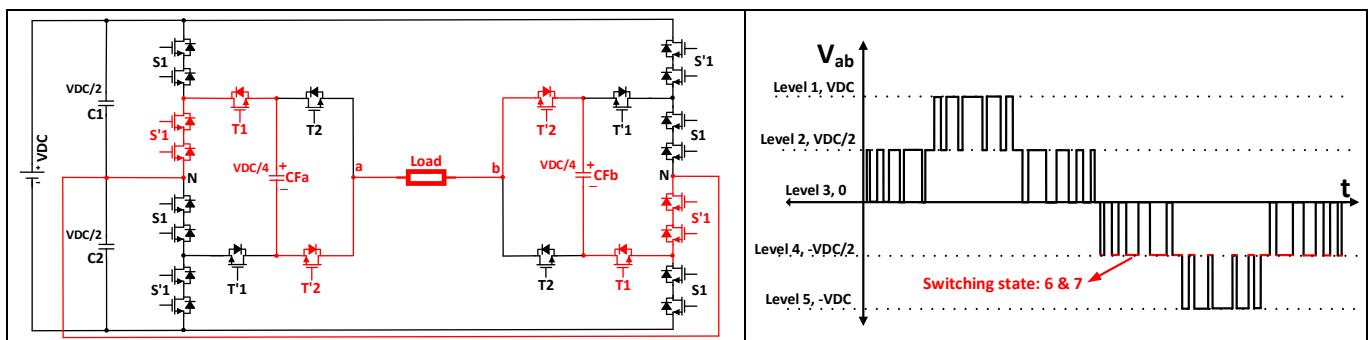
Figure 37   Switching state 6

During switching state 7, V_{ab} is equal to -VDC/2. The reverse inductor current is falling with the load current charging C_{Fa} and C_{Fb} voltage.
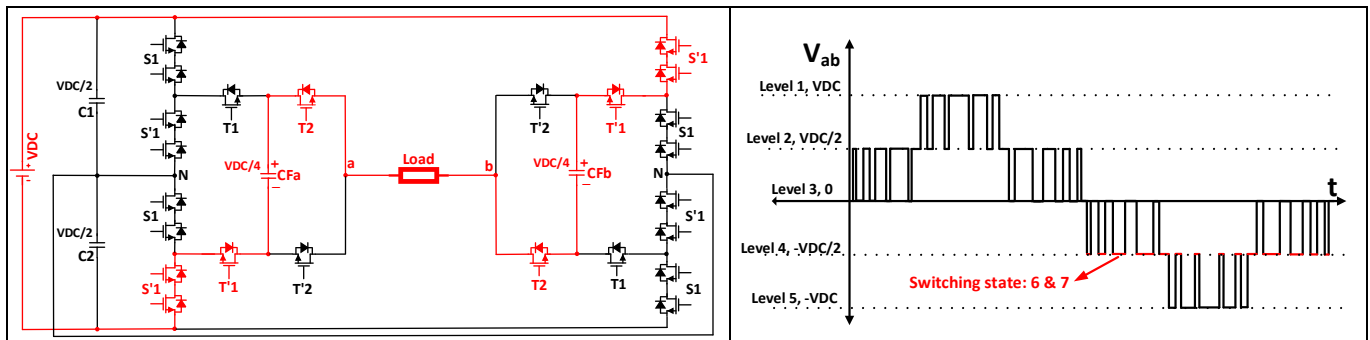
Figure 38   Switching state 7

During switching state 8, V_{ab} is equal to -VDC, the inductor current is falling and the flying capacitors C_{Fa} and C_{Fb} are neither being charged nor discharged by the load current.
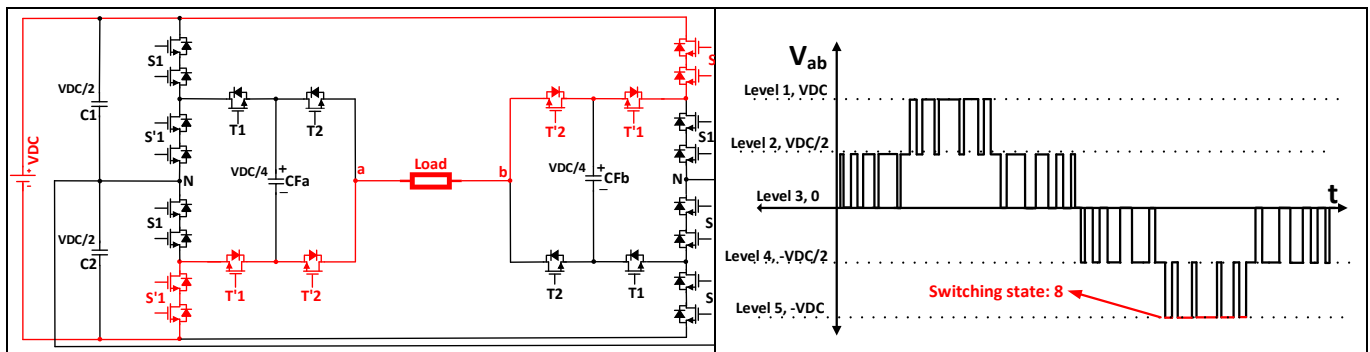
Figure 39   Switching state 8

5.1.2   Modulation scheme

In previous section, it was shown how the V_{ab} waveform is built by switching between various switching states, as listed in Table 3. In this section, it is explained how to generate the switching states using the PSPWM modulation scheme. In PSPWM, the modulation waveform described as $D_{HF}(t)$ in **Figure 40** and equation [12] is compared with carrier waveforms. In this five-level inverter there are two independent switching cells per half-bridge, so two carrier waveforms are needed with 360-degree/2 = 180-degree phase difference. **Figure 41** shows how the Q1 and Q2 PWM pulses are generated by comparing carrier and modulation waveforms. Note that here the modulation waveform has been shown for only a small-time interval during the positive half-cycle (S1 = 1), which is why it appears flat and not sinusoidal in this figure. It is illustrated here how different switching states from Table 3 are generated. For example, when T1, T2 and S1 are all one (switching state 1, see Table 3) V_{ab} = V DC. Also, the existence of redundant switching states has been shown, T1 = 1, T2 = 0, S1 = 1 (switching state 2) and T1 = 0, T2 = 1, S1 = 1 (switching state 3). Both of these switching states give the same voltage level V_{ab} = VDC/2.
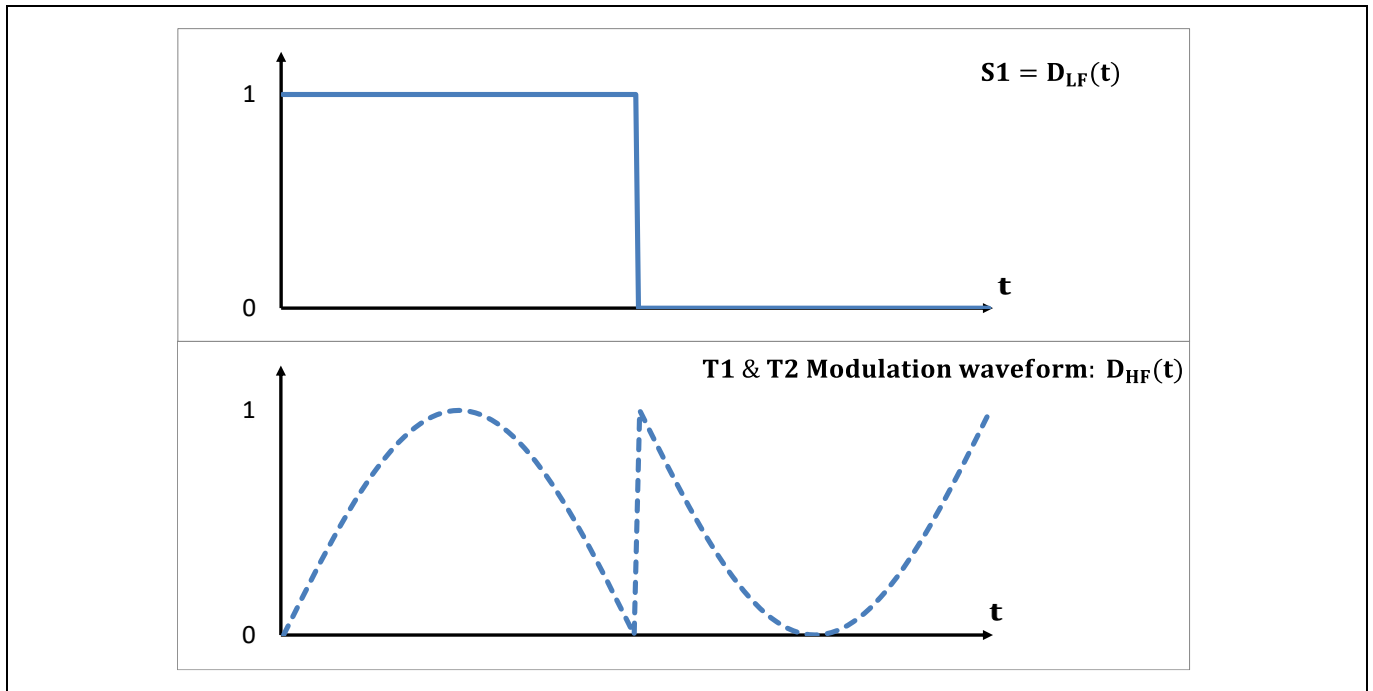
Figure 40   Slow MOSFETs S1 signal and fast switches modulation waveform
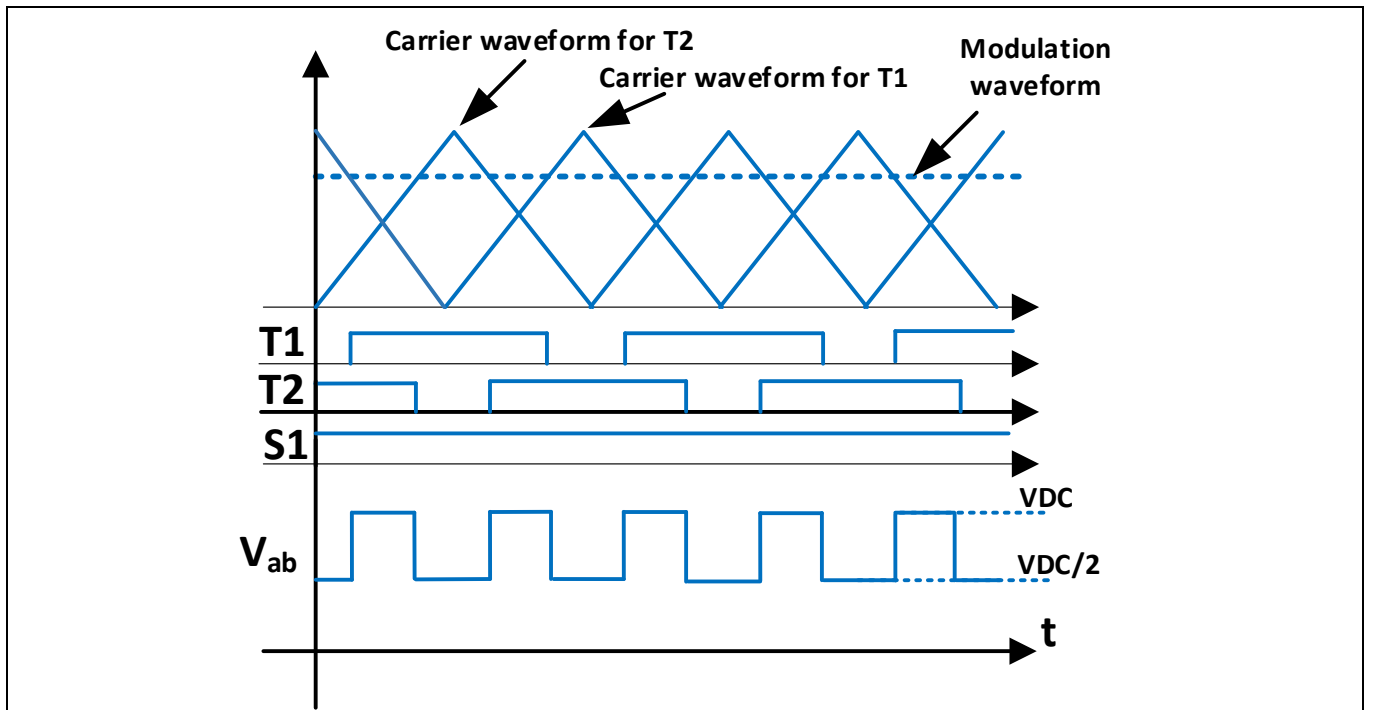
Figure 41   T1, T2 pulse generation using PSPWM

5.2 Passive component selection

In this section, it will be explained how to dimension and select major passive components in the multilevel inverter, including: output filter inductors (L_{fa} and L_{fb}), output filter capacitor (C_{out}), floating capacitors (CFa and CFb) and pre-charge resistors.

5.2.1 Output filter inductor design

To generate the pure sinusoidal output voltage V_{out} from V_{ab}, this voltage is fed to an LC filter as shown in **Figure 42**. In this section, it is explained how to calculate the values of L_{fa} and L_{fb}.
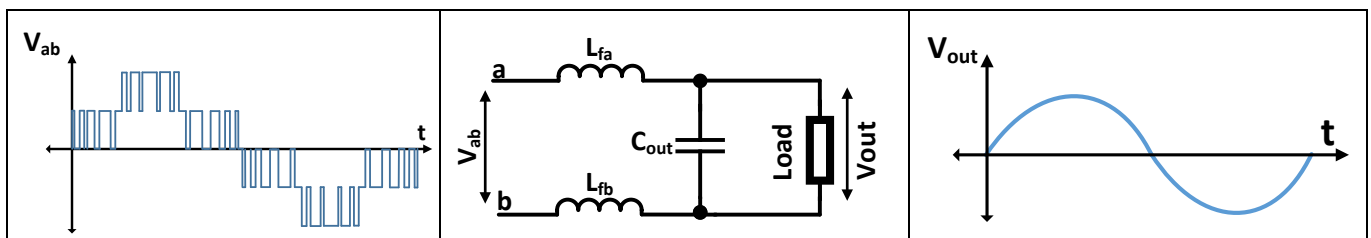
Figure 42   Output filter configuration

To limit the current ripple the inductance value L_{fa} + L_{fb} must be sufficient. For the ANPC-FC inverter here, considering the design case:

Full-load power: $S_{out} = 4000\ VA$

Output voltage: $V_{out(rms)} = 230\ V$

Switching frequency: $F_{SW} \approx 20\ kHz$

Inductor peak-to-peak ripple: $\Delta I_{pp} = 0.25 \times I_{pk}$

Where, as shown in **Figure 43**, I_{OUT} is the output (load) current, and I_L is the output filter inductor current assuming the output filter capacitor current is negligible to simplify the calculation.
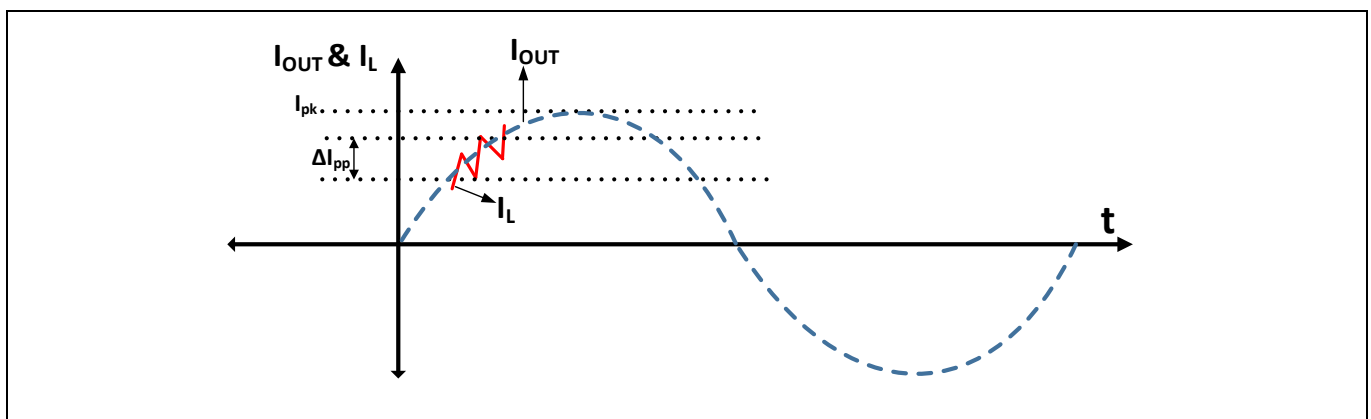
Figure 43   Output current I_{OUT}, inductor filter I_L

The inductance value is selected so that the inductor current maximum peak-to-peak ripple ΔI_{pp} is limited to $\Delta I_{pp} \leq 0.25 \cdot I_{pk}$ where I_{pk} is the peak of the sine wave output current at maximum rated load as calculated below:

$$I_{pk} = \frac{\sqrt{2}S_{out} \times \cos\varphi}{V_{out(rms)}} = \frac{\sqrt{2} \times 4000 \times \cos 0}{230} = 24.6\ A \qquad [1]$$

Where in [1] the power factor is assumed to be one (no phase shift between output current and output voltage $\varphi = 0$). The output capacitor in conjunction with the inductor needs to be large enough to filter out most of the ripple to provide a clean low frequency sine wave output. In a two-level inverter in full bridge configuration and with bipolar modulation, the output phase-to-phase voltage (V_{ab}) switches between VDC and -VDC, therefore the peak-to-peak switched voltage across the output filter inductor is 2 VDC. For the two-level inverter the minimum inductance value necessary to limit peak-to-peak ripple to ΔI_{pp} is given by:

$$L_{fil\_2level} \geq \frac{V_{DC}}{2 \times F_{sw} \times \Delta I_{pp}} \qquad [2]$$

The derivation for this formula can be found in reference [6].
In the EVAL_4KVA_230VAC_5LINV design, the effective output frequency will be twice the switching frequency because there are two switching cells. Also, while for a two-level inverter the amplitude of switched voltage is 2 VDC for a five-level inverter this value is VDC/2. Therefore, the minimum inductance will be:

$$L_{fil\_5level} = \frac{L_{fil\_2level}}{2(twice\ the\ switching\ frequncy) \times 4(lower\ switched\ voltage)} \qquad [3]$$

$$L_{fil\_5level} \geq \frac{V_{DC}}{16 \times F_{sw} \times \Delta I_{pp}} \qquad [4]$$

Therefore, in the current design:

$$L_{fil\_5level} \geq \frac{400}{16 \times 20000 \times (0.25 \times 24.6)} = 203 \times 10^{-6} = 203\ \mu H \qquad [5]$$

The output inductance will therefore be divided between two 100 μH filter inductors L_{Fa} and L_{Fb}.

5.2.2 Output filter capacitor design

Now that inductor filter value is known, output filter capacitor can be determined. The output filter cut-off frequency is set at one-tenth of effective output switching frequency. The output capacitor frequency can then be calculated as below:

$$C_{out} > (\frac{1}{2 \times \pi \times f_{cut}})^2 \times \frac{1}{L_{fil}} = (\frac{1}{2 \times \pi \times 4000\ Hz})^2 \times \frac{1}{200 \times 10^{-6} H} = 7.9\ \mu F \qquad [6]$$

10 μF is a standard value that is selected here. Two 5 μF film capacitors will be connected in parallel.

5.2.3 Flying capacitor design

Since all load currents go through flying capacitors, film-type capacitors must be used. Film capacitors have much lower ESR than electrolytic capacitors but are bulkier. The required minimum value of the flying capacitors depends on the allowed maximum voltage ripple, effective output switching frequency and capacitor current. Larger values of flying capacitors provide more robust performance but slow down the dynamic response of the system. The floating capacitor value must be large enough to limit the maximum voltage ripple that appears across it. This can be calculated as follows:

$$\Delta V_{FC\_max} = \frac{max[D_{FC} \times I_{FC}]}{C_{FC} \times 2 \times F_{sw}} \qquad [7]$$

where I_{FC} is the floating capacitor current and D_{FC} is the duty cycle of the floating capacitor current. As shown, the maximum ripple occurs at a switching period where $D_{FC} \times I_{FC}$ is maximum. The exact value of ΔV_{FC_max} can only be calculated if the instantaneous value of D_{FC} and I_{FC} as functions of time and power factor are substituted into the above equation and $\frac{d\Delta V_{FC\_max}}{dt} = 0$ is then solved. To simplify the design process, the worst-case scenario for maximum voltage ripple is considered and used to approximate the floating capacitor value.

There will be a power factor value in which the maximum voltage ripple happens, and it can be approximated as follows:

$$\Delta V_{FC\_max}(worst\ case) = \frac{max[D_{FC}] \times max[I_{FC}]}{C_{FC} \times 2 \times F_{sw}} \approx \frac{1 \times I_{pk}}{C_{FC} \times 2 \times F_{sw}} \tag{8}$$

Therefore, the minimum possible floating capacitor value is calculated as:

$$C_{FC} \geq \frac{I_{pk}}{\Delta V_{FC\_max}(worst\ case) \times 2F_{sw}} \tag{9}$$

Assuming the maximum voltage ripple to be 20 percent of the steady state value of C_{FC} voltage (100 V):

$$C_{FC} \geq \frac{24.6\ A}{0.2 \times 100\ V \times 2 \times 20000\ W} \approx 30\ \mu F \tag{10}$$

30 µF, 250 V film capacitors are selected as the floating capacitors for CFa (phase a floating capacitor) and CFb (phase b floating capacitor).

5.2.4 Pre-charging resistor selection

Once the input voltage is applied to the inverter and before the MOSFETs start switching the flying capacitor and input capacitors must have been pre-charged to a value close enough to their steady-state value. Otherwise, some of the MOSFETs may have to withstand higher voltage and experience avalanche breakdown while other MOSFETs are withstanding much less voltage. To pre-charge the flying capacitors, resistors are installed in parallel with MOSFETs. There is no specific formula to calculate these resistor values but they should be selected so that when no MOSFET is switching and the overall inverter behavior is similar to a RC network, the steady-state value of flying capacitor voltage is within 10 percent of their nominal value (100 V in this case). Too-high resistor values would result in a long pre-charging time, and too-low values would contribute to unacceptable resistive power loss. In this inverter 75 kΩ, 150 kΩ and 220 kΩ are used. Refer to the schematic to see the location of these resistors in the inverter circuit.

5.3 Power loss analysis

In this section of the application note, the major sources of power loss are identified. It will be shown using a pie chart how the total losses are distributed among all these sources. The numerical value of power loss contributed by each one of these sources is then calculated. To calculate the conduction loss of each MOSFET the RMS current value is needed, which will be analytically derived.

5.3.1 Identifying the major sources of power loss

In order to perform the power loss analysis, the major sources of loss must first be identified. These sources are shown in the figure below and listed in Table 4. MOSFETs in the system are classified as either slow (switching at line frequency, F_{line}) or fast (switching at switch cell PWM frequency, F_{sw}).
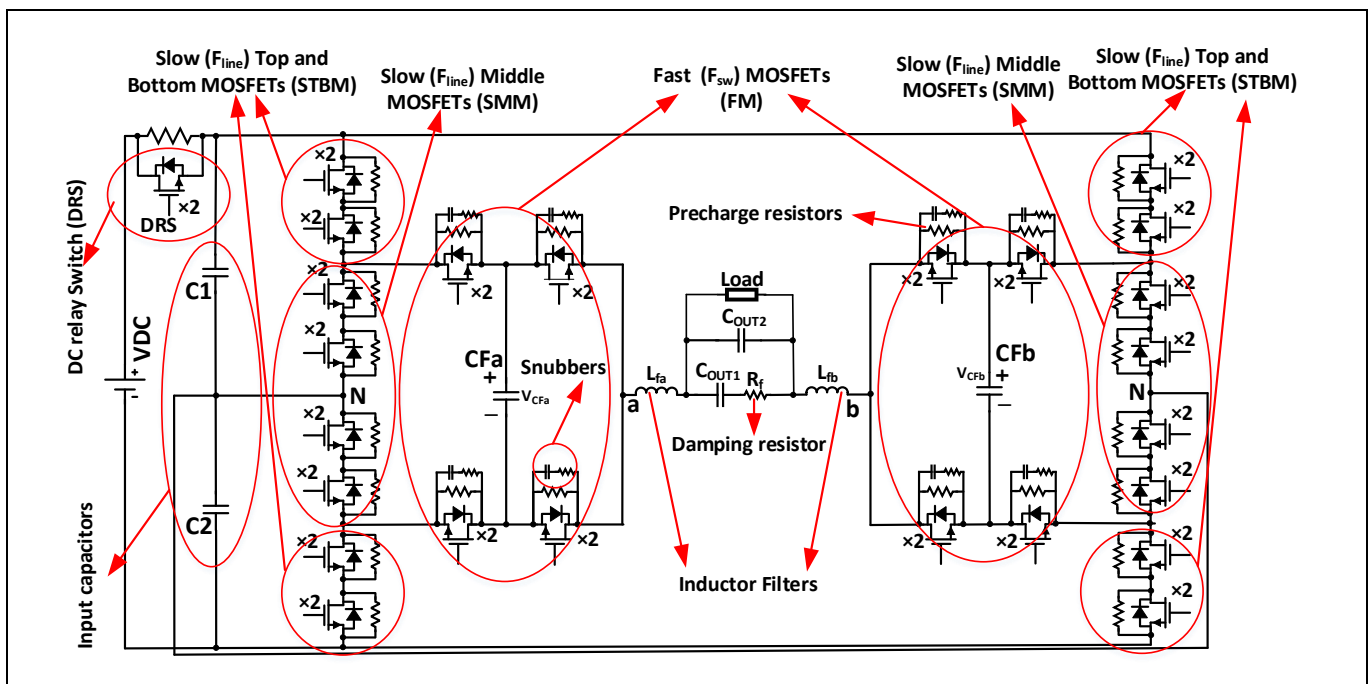
Figure 44   Main sources of inverter power loss

Table 4   Summary of power loss sources

Fast MOSFETs	Slow MOSFETs	DC relay switch	Input capacitor	Inductor filters	Pre-charge resistors	Snubbers	Damping resistors
Conduction and switching loss	Conduction loss	Conduction loss	ESR loss	Copper loss	Resistive loss	Resistive loss	Resistive loss

 It can be seen in the loss breakdown pie chart shown below that the losses are distributed among many sources of power dissipation. This is the main reason why this design doesn't need heatsink or fan for thermal management. While in a traditional two-level inverter most power dissipation is concentrated in the power semiconductors, in this design the semiconductor loss is only around 0.5 percent of total power.
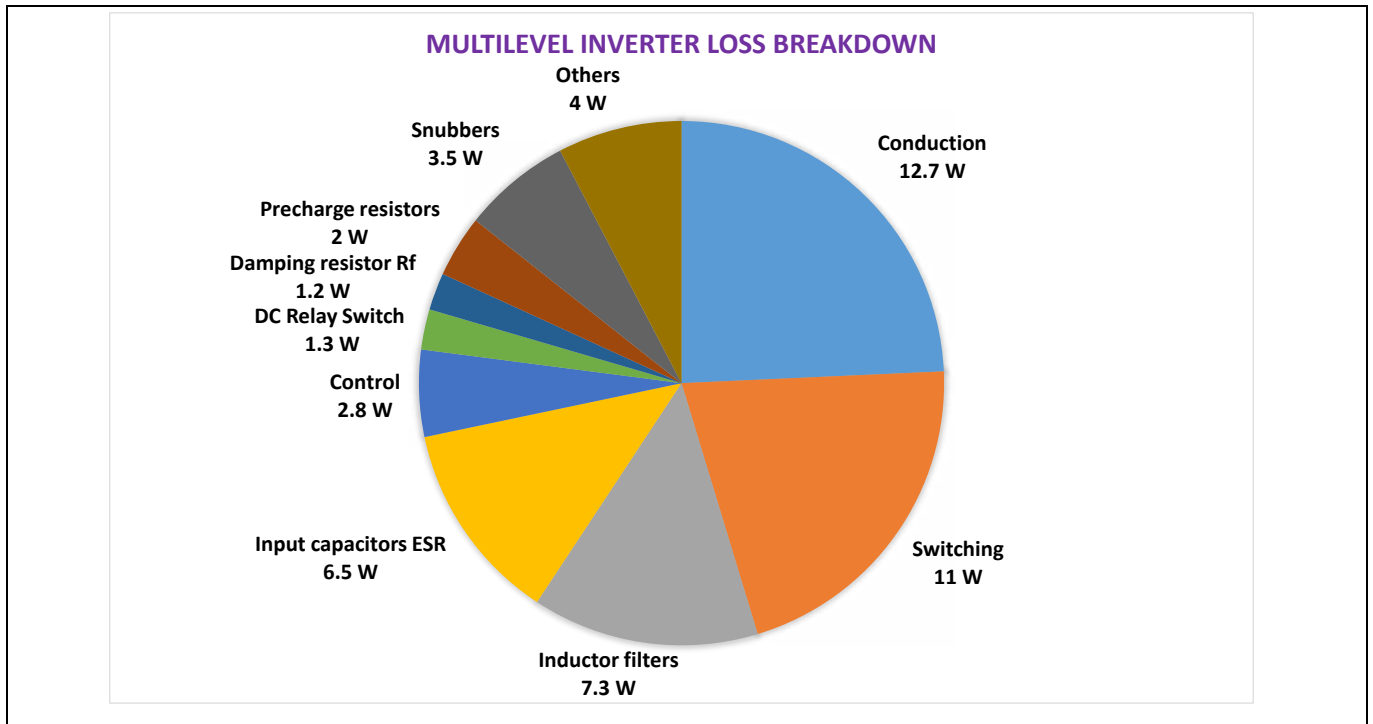
Figure 45   Multilevel inverter loss breakdown at 4 kW load

5.3.2   Analytical derivation of MOSFET RMS current

In this section, duty cycle and MOSFET RMS current are calculated for phase a. Due to the symmetrical nature of this topology the same values can also be applied to phase b.

The slow MOSFETs duty cycle D_{LF} (see **Figure 40** and **Figure 46**) is considered as an ideal square waveform.

$$D_{LF}(\theta) = \begin{cases} 1, & 0 \leq \theta < \pi \\ 0, & \pi \leq \theta < 2\pi \end{cases} \qquad [11]$$

The long-term average of fast MOSFETs duty cycle is equal to modulation waveform D_{HF} and can be written as below:

$$D_{HF}(\theta) = \begin{cases} m\sin(\theta), & 0 \leq \theta < \pi \\ 1 + m\sin(\theta), & \pi \leq \theta < 2\pi \end{cases} \qquad [12]$$

Where m is the modulation index and $\theta = \omega t$, $\omega = 2\pi \cdot F_{line}$, and F_{line} is line frequency equal to 60 Hz.

The output load current and output voltage are assumed to be fully sinusoidal and can be described using the below equations:

$$I_{out}(t) = I_{pk}\sin(\theta - \varphi) \qquad [13]$$

$$V_{out}(t) = V_m\sin(\theta) \qquad [14]$$

For simplicity, the output current I_{OUT} is assumed to be equal to inductor filter current, disregarding the filter capacitor current.

There are 48 MOSFETs in the EVAL_4KVA_230VAC_5LINV inverter design (other than the inrush current resistor bypass HV MOSFET). The RMS current value of all the fast MOSFETs is identical. However, the slow MOSFETs are divided into two separate groups:

1. The slow MOSFETs in top and bottom position (STBM).

2. The slow MOSFETs in the middle position (SMM).

The current values of all MOSFETs in STBM positions are equal to each other. The same is true for all the MOSFETs in SMM positions. However, the current value of STBM MOSFETs is different from SMM MOSFETs.
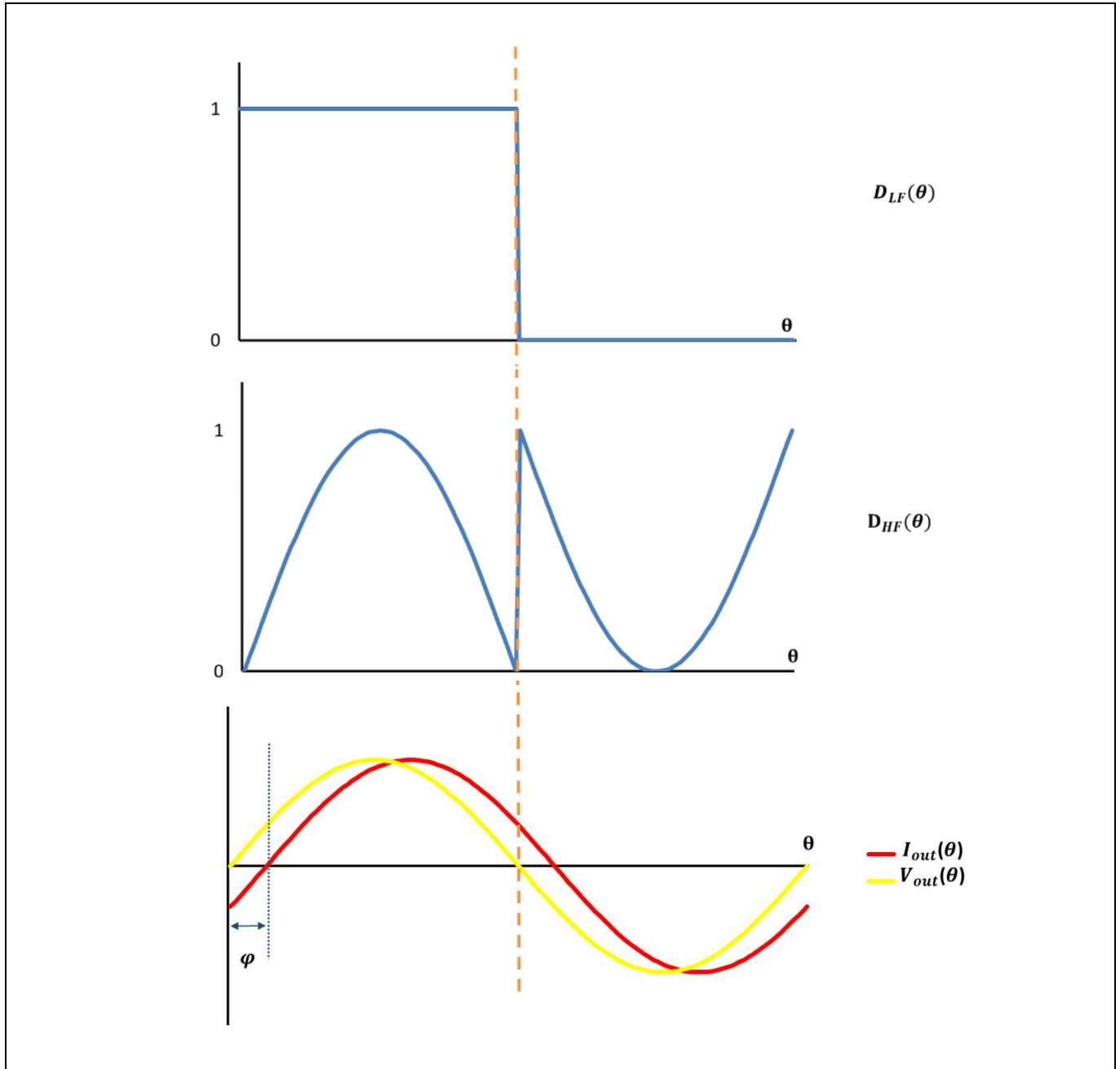
Figure 46   a) Slow MOSFET duty cycle, b) fast MOSFETs duty cycle, c) output load current and voltage

In a simple buck converter or a two-level inverter, the RMS current of each MOSFET depends only on the load current and duty cycle of that specific MOSFET. However, in the multilevel inverter the current that is passing through each MOSFET not only depends on the load current and duty cycle of that specific MOSFET but also the duty cycle of all the other MOSFETs in the current path. The term "effective duty cycle" is used here to account for this. The effective duty cycle of one the fast MOSFETs, (D_{FM}) T_1 (see **Figure 8**) is derived here. The amplitude of effective duty cycle of all other fast MOSFETs are the same as T_1. The effective duty cycle of T_1 can be calculated as below: as below [8]:

$$D_{FM}(\theta) = \begin{cases} D_{HF}(\theta) \times D_{LF}(\theta), & 0 \le \theta < \pi \\ D_{HF}(\theta) \times (1 + D_{LF}(\theta)), & \pi \le \theta < 2\pi \end{cases} \tag{15}$$

By applying equations [11] and [12]:

$$D_{FM}(\theta) = \begin{cases} m\sin(\theta), & 0 \le \theta < \pi \\ 1 + m\sin(\theta), & \pi \le \theta < 2\pi \end{cases} \tag{16}$$

The effective duty cycle of slow top MOSFETs (D_{STM}) can be written as below:

$$D_{STM}(\theta) = \begin{cases} D_{HF}(\theta) \times D_{LF}(\theta), & 0 \le \theta < \pi \\ D_{HF}(\theta) \times D_{LF}(\theta), & \pi \le \theta < 2\pi \end{cases} \tag{17}$$

By applying equations [11] and [12]:

$$D_{STM}(\theta) = \begin{cases} m\sin(\theta), & 0 \le \theta < \pi \\ 0, & \pi \le \theta < 2\pi \end{cases} \tag{18}$$

The effective duty cycle of slow middle MOSFETs (D_{SMM}) can be written as below:

$$D_{SMM}(t) = \begin{cases} (D_{HF}(\theta))' \times D_{LF}(\theta), & 0 \le \theta < \pi \\ 0, & \pi \le \theta < 2\pi \end{cases} \tag{19}$$

By applying equations [11] and [12]:

$$D_{SMM}(t) = \begin{cases} 1 - m\sin(\theta), & 0 \le \theta < \pi \\ 0, & \pi \le \theta < 2\pi \end{cases} \tag{20}$$

The fast MOSFET RMS current equation is derived as follows:

$$I_{FM(RMS)} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}[I_{FM}(\theta)]^2 d\theta} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}[I_{out}(\theta)]^2 D_{FM}(\theta) dt} \tag{21}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_{pk}{}^2(\sin(\theta - \varphi))^2\, m\sin(\theta)d\theta + \frac{1}{2\pi}\int_\pi^{2\pi} I_{pk}{}^2(\sin(\theta - \varphi))^2\,(1 + m\sin(\theta))d\theta} = \frac{I_{pk}}{2}$$

For slow top and bottom MOSFETs the current value is [8]:

$$I_{STM(RMS)} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}[I_{STM}(\theta)]^2 d\theta} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}[I_{out}(\theta)]^2 D_{STM}(\theta) dt} \tag{22}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_{pk}{}^2(\sin(\theta - \varphi))^2\, m\sin(\theta)d\theta} = \sqrt{\frac{m I_{pk}{}^2(\cos^2\varphi + 1)}{3\pi}}$$

$$I_{SMM(RMS)} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}[I_{SMM}(\theta)]^2 dt} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_{pk}{}^2(\sin(\theta - \varphi))^2\,(1 - m\sin(\theta))d\theta} \tag{23}$$

$$= \sqrt{\frac{I_{pk}^2}{4} + \frac{mI_{pk}^2(\sin^2\varphi - 2)}{3\pi}}$$

Note that as can be seen in the multilevel inverter schematic, each MOSFET is paralleled with another MOSFET. The derived MOSFET equations therefore represent the total current shared between two parallel MOSFETs. All information needed to calculate conduction loss is now available. The equations above will be used in the following section to determine conduction loss.

5.3.3 Conduction loss calculation

Now that MOSFETs RMS current expressions are available, the corresponding conduction losses can be calculated. First modulation index is calculated as shown below:

$$m = \frac{\sqrt{2}\times V_{out(rms)}}{V_{DC}} = \frac{\sqrt{2}\times 230\,V}{400\,V} = 0.81 \tag{24}$$

The fast MOSFET RMS current is therefore:

$$I_{FM(RMS)} = \frac{I_{pk}}{2} = \frac{24.6\,A}{2} = 12.3\,A \tag{25}$$

Now assuming the power factor is ($\varphi = 0$), then for the top and bottom MOSFETs the RMS current is:

$$I_{STM(RMS)} = \sqrt{\frac{mI_{pk}^2(\cos^2\varphi + 1)}{3\pi}} = \sqrt{\frac{0.81\times(24.6\,A)^2(\cos^2 0 + 1)}{3\pi}} = 10.2\,A \tag{26}$$

The slow middle MOSFET RMS current is:

$$I_{SMM(RMS)} = \sqrt{\frac{I_{pk}^2}{4} + \frac{mI_{pk}^2(\sin^2\varphi - 2)}{3\pi}} = \sqrt{\frac{(24.6\,A)^2}{4} + \frac{0.81\times(24.6\,A)^2(\sin^2 0 - 2)}{3\pi}} = 6.87\,A \tag{27}$$

Now to calculate total conduction loss, remember the following points:
- The calculated RMS values in equations (25), (26) and (27) give the current through one pair of parallel MOSFETs.
- As can be seen in the thermal image shown in the results section, the slow MOSFET steady-state temperature at full power reaches 70°C and the fast MOSFET temperature reaches 85°C. Therefore, it is necessary to use the corresponding drain-to-source on-resistance at those temperatures to calculate conduction loss.
  From the datasheet $R_{ds(on)@85°C} = 11\,m\Omega$ and $R_{ds(on)@70°C} = 10\,m\Omega$.
- There are 16 fast MOSFETs, 16 slow MOSFETs in the top and bottom positions, and 16 slow MOSFETs in middle positions.

Considering the above mentioned points, total MOSFET-related conduction loss is given by:

$$P_{CON} = 16 \times \left[R_{ds(on)@85°C} \times \left(\frac{I_{FM(RMS)}}{2}\right)^2 \right] + 16 \times \left[R_{ds(on)@70°C} \times \left(\frac{I_{STBM(RMS)}}{2}\right)^2 \right]$$

$$+ 16 \times \left[R_{ds(on)@70°C} \times \left(\frac{I_{SMM(RMS)}}{2}\right)^2 \right] \tag{28}$$

$$= 16 \times \left[11 \, m\Omega \times \left(\frac{12.3 \, A}{2}\right)^2\right] + 16 \times \left[10 \, m\Omega \times \left(\frac{10.2 \, A}{2}\right)^2\right] + 16 \times \left[10 \, m\Omega \times \left(\frac{6.87 \, A}{2}\right)^2\right] = 12.7 \, W$$

5.3.4 Switching loss calculation

Calculation of switching loss is more challenging than conduction loss. Layout design heavily affects switching loss, and circuit parasitic cannot be easily quantified. Also, unlike conduction loss where the RMS value of MOSFET current suffices for the calculations, for switching loss the instantaneous current value is needed. Therefore, it would be very difficult to accurately calculate switching loss values. In this section the goal is to show how to obtain reasonable estimates of the switching loss. For more detailed and more accurate measurement of switching loss in a multilevel inverter (or a general inverter), see reference [9].

As stated, there are 48 MOSFETs in this inverter. 32 of these are switching at line frequency with negligible switching loss (slow MOSFETs). In this section the focus is therefore on calculating the switching loss contributed by the 16 fast MOSFETs.

To calculate the switching loss, gate driver IC, MOSFET and gate driving circuit parameters need to be considered. The 2EDF7275F gate driver IC parameters are as follows:

$R_{dr\_on} = 0.85 \, \Omega$ Gate driver IC internal resistor, source path
$R_{dr\_off} = 0.35 \, \Omega$ Gate driver IC internal resistor, sink path
$V_{dri} = 12 \, V$ Driving voltage

From the BSC093N15NS5 datasheet, the following parameters are extracted:

$V_{plateau} = 5.7 \, V$ Plateau voltage
$Q_{sw} = 13.4 \, nC$ Switching charge; this is the amount of charge needed to be transferred during switching transient
$R_{g\_internal} = 0.9 \, \Omega$ Internal MOSFET gate resistance

From the multilevel inverter circuit:

$R_{gon} = 54.6 \, \Omega$ Gate driving resistor in the turn-on path. This resistor is selected to be large enough to mitigate ringing and improve EMI.
$R_{goff} = 1 \, \Omega$ Gate driving resistance in the turn-off path. This resistor is selected to be small enough to minimize turn-off switching loss.

MOSFET turn-on time can be calculated as follows:

$$I_{g\_on} = \frac{V_{dri} - V_{plateau}}{R_{gon} + R_{dr\_on} + R_{g\_internal}} = \frac{12 \, V - 5.7 \, V}{54.6 \, \Omega + 0.85 \, \Omega + 0.9 \, \Omega} = 0.11 \, A \tag{29}$$

$$t_{on} = \frac{Q_{sw}}{I_{g\_on}} = \frac{13.4 \, nC}{0.11 \, A} = 122 \, ns \tag{30}$$

Turn-off time can be calculated as follows:

$$I_{g\_off} = \frac{V_{plateau}}{R_{g_{off}} + R_{dr\_off} + R_{g\_internal}} = \frac{5.7\ V}{1\ \Omega + 0.35\ \Omega + 0.9\ \Omega} = 2.5\ A \qquad [31]$$

2EDF7275F gate driver sink capability is 4 A. Since one gate driver channel drives two MOSFETs in parallel, sink capability per MOSFET will be capped at 2 A.

$$t_{off} = \frac{Q_{sw}}{I_{g\_off}} = \frac{13.4\ nC}{2\ A} = 6.7\ ns \qquad [32]$$

Note that due to the existence of parasitic inductance the real t_{off} is most likely higher than 6.7 ns. To calculate switching loss, other than calculating turn-on and turn-off time, Q_{oss} and Q_{rr} parameters also need to be estimated. From the datasheet $Q_{oss}(@75V) = 91\ nC$. Assuming the C_{oss} curve in the 75 V to 100 V region is approximately linear:

$$Q_{oss}(@100\ V) \approx Q_{oss}(@75\ V) \times \frac{100\ V}{75\ V} \approx 121\ nC \qquad [33]$$

Also from the datasheet: $Q_{rr}\left(@I_F = 44\ A, @\frac{dI_F}{dt} = 100\ \frac{A}{\mu s}\right) = 58\ nC$.

In the datasheet, the Q_{rr} value is given only at this specific test condition. However, the value of di/dt is highly dependent on circuit and layout parameters like R_{gon} and parasitic inductance. Furthermore, note that in an inverter the body diode current (I_F) is not a constant DC value but follows a sinusoidal form. This means at each switching instance depending on the value of load current the Q_{rr} value is going to be different. This makes the accurate calculation of Q_{rr}-related loss in inverters somewhat challenging. However, since the switching frequency is relatively low (20 kHz), and R_{gon} is high (so dIF/dt is low) the Q_{rr}-related loss is not a significant portion of the overall loss. As a result, error in loss calculation due to the rough approximation of Q_{rr} is not substantial. Therefore, the datasheet value of Q_{rr} = 58 nC may be used in the loss calculation.

To simplify switching loss calculation the 16 fast MOSFETs are considered as four identical HF switching cells. Since MOSFETs have been used in parallel, each cell consists of two synchronous MOSFET pairs, as shown in **Figure 47**. To calculate the total switching loss the switching loss of a synchronous MOSFET pair is calculated similar to the way it is done in a synchronous buck converter. The results can then be multiplied by 8 (4 cells × 2 synchronous pairs).
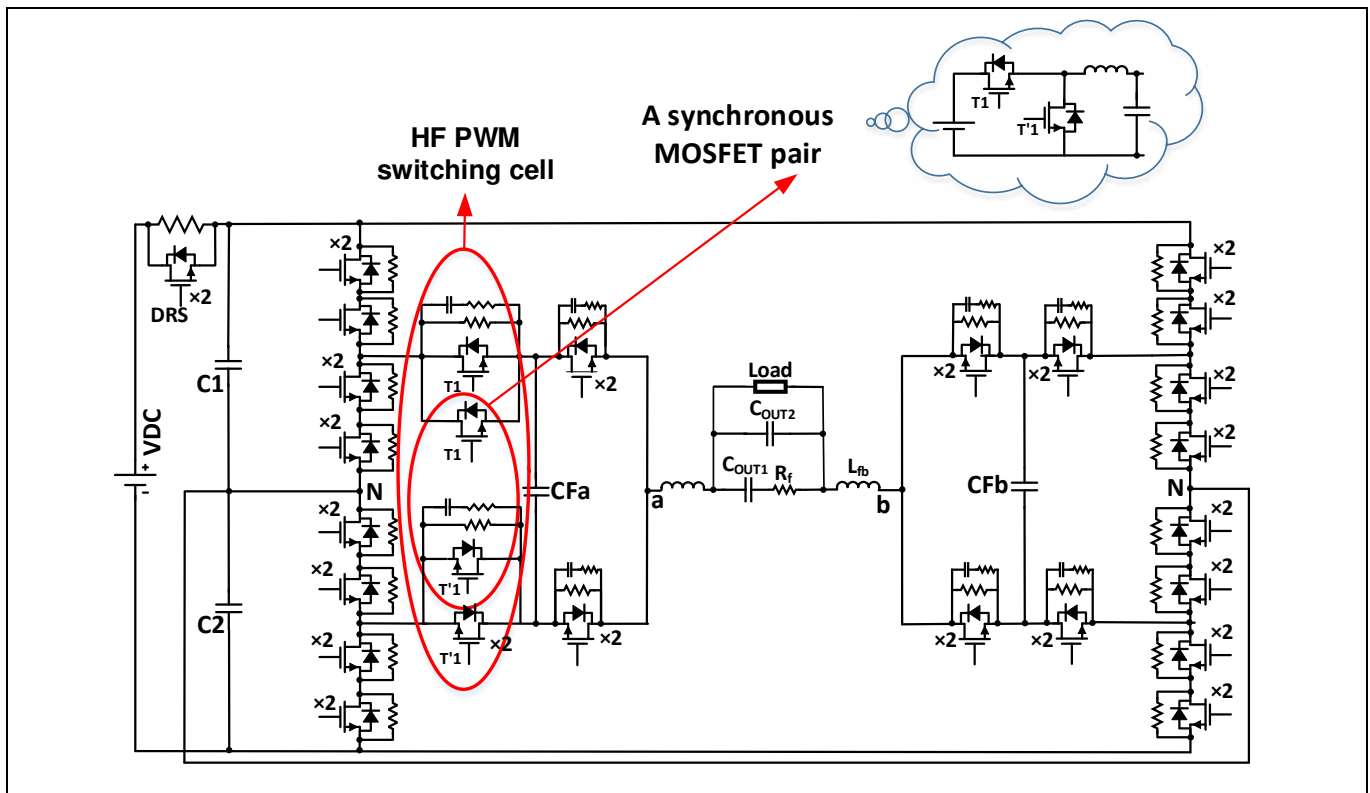
Figure 47   Demonstration of cells and synchronous MOSFET pairs

The top MOSFET in the synchronous pair at the positive half-cycle of load current experiences a hard-switching turn-on transient while the bottom MOSFETs turn on and off with its body conducting. That means the bottom MOSFET overlap switching loss (overlap of current and voltage) is negligible due to zero voltage switching (ZVS). However, the bottom MOSFET body diode experiences hard commutation and its Q_{rr} is dissipated in the top MOSFET. During the negative half-cycle of load current, the bottom MOSFET experiences hard-switching and the top MOSFET enjoys ZVS. However, due to the symmetrical structure of the inverter the switching loss calculations can be written with the assumption that current is always in the positive half-cycle. The table below summarizes the switching loss calculations for a synchronous pair, assuming the current is positive:

Switching loss	Formula	Calculation	Comment
$P_{SW\_TOP\_ON\_overlap}$	$V_{ds}\dfrac{\left(\dfrac{2I_{pk}}{\pi}\right)}{2}\dfrac{t_{on}}{2}F_{sw}$	$100\,V\dfrac{\left(\dfrac{2\times24.6\,A}{\pi}\right)}{2}\dfrac{122\,ns}{2}\times20000\,Hz$ $= 0.96\,W$	To consider the shape of current which is sinusoidal its average value $\frac{2I_{pk}}{\pi}$ is used. Also, a division by 2 is needed since there are two MOSFETs in parallel.
$P_{SW\_TOP\_OFF\_overlap}$	$V_{ds}\dfrac{\left(\dfrac{2I_{pk}}{\pi}\right)}{2}\dfrac{t_{off}}{2}F_{sw}$	$100\,V\dfrac{\left(\dfrac{2\times24.6\,A}{\pi}\right)}{2}\times\dfrac{6.7\,ns}{2}\times20000\,Hz$ $= 0.05\,W$	Turn-off loss due to overlap of voltage and current is much smaller then turn-on overlap loss
$P_{SW\_TOP\_Qoss}$	$\dfrac{Q_{oss}V_{ds}F_{sw}}{2}$	$\dfrac{121\,nC\ \times100\,V\ \times20000\,Hz}{2}$ $= 0.12\,W$	C_{oss}-related charge for top MOSFET

$P_{SW\_BOT\_Qoss}$	$\dfrac{Q_{oss}V_{ds}F_{sw}}{2}$	$\dfrac{121\ nC\ \times 100\ V\ \times 20000\ Hz}{2}$ $= 0.12\ W$	C_{oss}-related charge for bottom MOSFET
P_{SW_Qrr}	$Q_{rr}V_{ds}F_{sw}$	$58\ nC \times 100\ V\ \times 20000\ Hz$ $= 0.12\ W$	Q_{rr} of the bottom MOSFET is dissipated in the top MOSFET
P_{SW_Gate}	$Q_g V_{dri}F_{sw}$	$33\ nC \times 12\ V\ \times 20000\ Hz$ $= 0.008\ W$	This is per MOSFET loss, not per synch pair.

The total switching loss per synchronous pair is:

$$P_{SW\_one\_pair} = P_{SW\_TOP\_ON\_overlap} + P_{SW\_TOP\_OFF\_overlap} + P_{SW\_TOP\_Qoss} + P_{SW\_BOT\_Qoss}$$
$$+ P_{SW\_Qrr} + 2 \times P_{SW\_Gate} = 1.38\ W \tag{34}$$

There are eight pairs, therefore the total switching loss of the inverter is:

$$P_{SW\_total} = 8 \times P_{SW\_one\_pair} = 11\ W \tag{35}$$

Also note that due to the small dead-time and relatively low switching frequency the body diode conduction loss is insignificant and is not calculated here.

5.3.5 Input capacitor ESR loss calculation

One major source of loss is the input capacitor ESR loss. To determine this loss first the input capacitor RMS current is calculated as follows, see reference [10]:

$$I_{Cin(RMS)} = \sqrt{m I_{pk}^2 \left(\left(\frac{3 + \cos 2\varphi}{3\pi} \right) - \left(\frac{m \cos^2 \varphi}{4} \right) \right)} \qquad [36]$$

$$= \sqrt{0.81 \times (24.6\ A)^2 \left(\left(\frac{3 + \cos 0}{3\pi} \right) - \left(\frac{0.81 \times \cos^2 0}{4} \right) \right)} = 10.43\ A$$

The capacitor ESR calculated from the datasheet yields a very conservative value. To acquire more realistic ESR values, a network analyzer should be used. Using a network analyzer, the ESR value for the LGW2E391MELA30 390 µF, 250 V electrolytic capacitor from Nichicon is measured to be approximately 150 mΩ. There are a total of ten electrolytic capacitors at the input of the EVAL_4KVA_230VAC_5LINV inverter, installed in parallel and series as shown in the schematic. Hence, the total ESR is:

$$ESR_{eqv} = \frac{2 \times ESR}{5} = 0.06\ \Omega \qquad [37]$$

From equations [36] and [37], the total ESR loss at the input electrolytic capacitors is calculated as:

$$P_{ESR(Cin)} = ESR_{eqv} \times (I_{Cin(RMS)})^2 = 6.52\ W \qquad [38]$$

5.3.6 Output inductor filter losses

The power loss at the filter inductors consists of copper loss and core loss. The core loss is much smaller than copper loss and is not calculated here. The DC series resistance of inductors R_L is around 12 mΩ per inductor at 70°C (70°C is the inductor winding temperature at steady-state full power, as displayed in the thermal picture in **Figure 79**). To calculate the inductor copper loss, the output filter capacitor current can be neglected so that the inductor current can be assumed equal to the output current.

$$I_{out(rms)} = \frac{I_{pk}}{\sqrt{2}} = 17.4\ A \qquad [39]$$

Total copper loss in inductor filters is therefore:

$$P_L = 2 \times R_{L@70°C} \times (I_{out(rms)})^2 = 2 \times 12\ m\Omega \times (17.4\ A)^2 = 7.3\ W \qquad [40]$$

5.3.7 Output capacitor damping resistor losses

As explained in the passive component selection section, two 5 µF film capacitors are used in parallel at the output. A resistor (R_f = 6.6 Ω) is included in series with one of these 5 µF capacitors (C_{OUT1}) to dampen the resonance effect of the output filter. The conduction loss due to this resistor is calculated as follows:

$$I_{R\_damp} = \frac{V_{out}}{\left(\frac{1}{C_{out1} \times 2 \times \pi \times f_{line}} \right)} = V_{out} \times C_{out1} \times 2 \times \pi \times f_{line} = 0.43\ A \qquad [41]$$

$$P_{R\_damp} = R_f \times (I_{R\_damp})^2 = 6.6 \ \Omega \times (0.43 \ A)^2 = 1.2 \ W \qquad [42]$$

5.3.8 Pre-charging resistor losses

There are 24 pre-charging resistors in this inverter. Eight are 75 kΩ, 12 are 150 kΩ and four are 220 kΩ. Total resistive loss due to pre-charge resistors is calculated as:

$$P_{pre\_charge} = \sum_{i=1}^{i=24} \frac{(V_{ds})^2}{R_{pre(i)}} = 8 \times \frac{(100 \ V)^2}{75 \ k\Omega} + 12 \times \frac{(100 \ V)^2}{150 \ k\Omega} + 4 \times \frac{(100 \ V)^2}{220 \ k\Omega} = 2.05 \ W \qquad [43]$$

5.3.9 Snubber resistor losses

There are eight snubbers installed in parallel with the 16 fast MOSFETs. The corresponding power loss is:

$$P_{Snubber} = 8 \times C_{snub}(V_{ds})^2 F_{sw} = 8 \times 2.2 \ nF \times (100)^2 \times 20000 \ Hz = 3.52 \ W \qquad [44]$$

5.3.10 DCR switching losses

The DC relay switch (DCR) is used to bypass the inrush current limiting resistor. It also contributes to inverter total power loss. Because this switch turns off only infrequently the contributed losses are only conductive. To calculate this loss the inverter input current is first calculated:

$$I_{in\_DC} = \frac{S_{out} \times \cos \varphi}{V_{DC}} = \frac{4000 \ W \times \cos 0}{400 \ V} = 10 \ A \qquad [45]$$

There are two IPT60R022S7 MOSFETs installed in parallel to form the DRC switch. From the datasheet: $R_{ds\_DRS(on)@25°C} = 20 \ m\Omega$ and $R_{ds\_DRS(on)@60°C} = 26 \ m\Omega$, where 60°C is the steady-state temperature of these two MOSFETs at full power. Also, it is assumed that the input current is pure RMS, $I_{in\_DC} = I_{in\_rms}$. Now the conduction loss can be calculated as follows:

$$P_{DRS} = \frac{R_{ds\_DRS(on)@60°C}}{2} \times (I_{in\_}rms)^2 = \frac{26 \ m\Omega}{2} \times (10 \ A)^2 = 1.3 \ W \qquad [46]$$

5.4 Gate driver card design

Designers may be concerned by the need for a high number of isolated gate drivers in multilevel inverters and the fact that for each isolated gate driver channel one isolated power supply is required. However, in this section it is explained how a cost effective simple flyback-based power supply (less than 1 W) with eight outputs is used to power four dual-channel isolated gate drivers. This eight-output power supply is incorporated with four isolated gate driver 2EDF7275F ICs on one single daughter board. For the complete system, three daughter boards are needed. **Figure 48** shows the basic schematic of the eight-output auxiliary power supply. **Figure 29** shows the detailed schematic. A planar transformer simplifies the design, reducing cost and improving manufacturability.

To accommodate the eight outputs for creepage and clearance, the flyback power supply is laid out on a six-layer PCB. On each middle layer the secondary windings for two outputs are placed. The primary winding is located on the top layer. The primary winding has six turns, while each one of the secondary windings has three turns. The LT8301 is used as for the flyback switch. More detailed information on designing this flyback power supply can be found in reference [11].
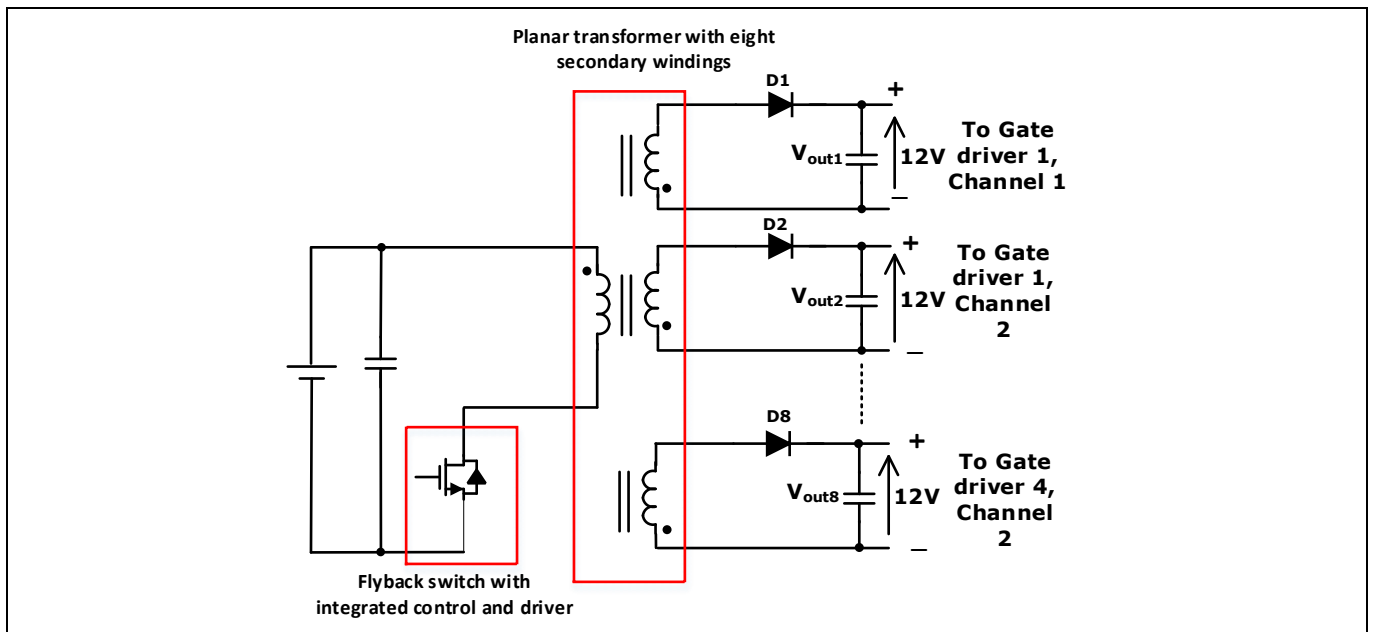
Figure 48   Flyback-based less-than 1 W power supply with eight outputs on gate driver board

5.5   Supervisory functions

5.5.1   DC input voltage sensing

The inverter is designed to operate over a specified DC input range indicated in section 2. It is therefore necessary to monitor the input voltage to prevent operation outside of these limits by disabling all PWM gate drives and waiting until the correct voltage input is available. The DC bus is capacitively divided to provide the neutral point for each side of the multilevel inverter. Two separate resistor dividers monitor the total input bus DC voltage to provide input Vin_S to the U5 and the split rail DC voltage from 0 V to the neutral point to provide VinL_S. The firmware is therefore able to monitor the input voltage and neutral point. LEDs located on the control card indicate if either of these voltages are outside the correct range.

5.5.2   AC output voltage sensing

The AC output of the inverter appears after LC filter and EMI filter stage between the node L1 and L2, as shown in **Figure 49**. Resistor dividers referenced to 0 V are used to scale down these two voltages (L1 and L2), which are then fed to a differential amplifier based around U4A to produce a differential signal with a 1.65 V offset, scaled so as not to exceed 0 V or 3.3 V. This signal Vout_Sense is fed to an ADC input of U5 so that the firmware is able to periodically sample this LF sine wave signal. The results can be used to calculate the inverter RMS output voltage and also determine phase shift. This could be used to regulate AC real and reactive power components in a grid-tied scenario; however, the basic firmware installed in the inverter does NOT support this.
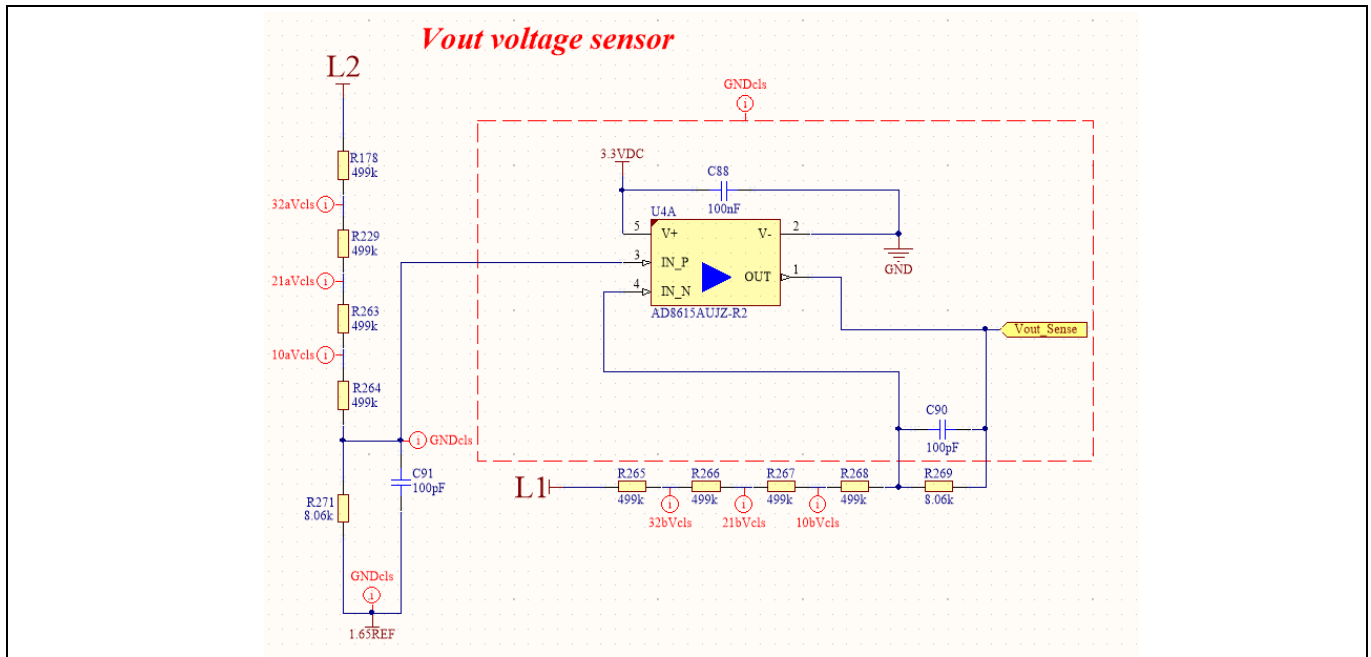
Figure 49   AC output voltage monitoring circuit

5.5.3   Output current sensing

The EVAL_4KVA_230VAC_5LINV uses a Hall sensor U1 (LKSR 25-NP) to detect the AC output current, which is nominally rated at 25 A_{RMS} but can measure up to +/-85 A and withstand up to 20 x 25 A_{RMS} before sustaining damage. The number of primary turns is one, since all of the four primary windings are connected in parallel to support maximum current. The secondary supply voltage is 5 V with a 2.5 V internal reference so that the galvanically isolated output voltage will be 2.5 V at zero input current. The sensitivity is of 25 mV/A, which allows sensing of more than 50 A_{RMS} without reaching the upper and lower voltage limits 0 V and 5 V.

The output from U1 (shown as VCS_P on the schematics) is connected from the power board to the control card through connector X8, where it is then connected to an amplifier circuit that scales it down through U4A to shift the offset down to 1.675 V, which is half the 3.3 V supply voltage of the microcontroller U5 that sets the maximum limit for analog inputs. The firmware samples the output current periodically, performing analog to digital conversions so that the instantaneous current can be sampled.

The scaled output current feedback signal to U5 is also fed to the dual comparator U2. One of the comparators detects a high positive peak and the other detects a high negative peak, with each output transitioning negative rapidly in the event of a high current peak. The two outputs (OC_POS and OC_NEG) are fed to an AND gate, whose output transitions low if either of the two signals goes low to provide a fast fault indication to U5. A high-to-low transition at this input triggers the U5 to shut off all of the PWM gate drive outputs much more rapidly than the time it would take for an analog to digital conversion and result check to take place.
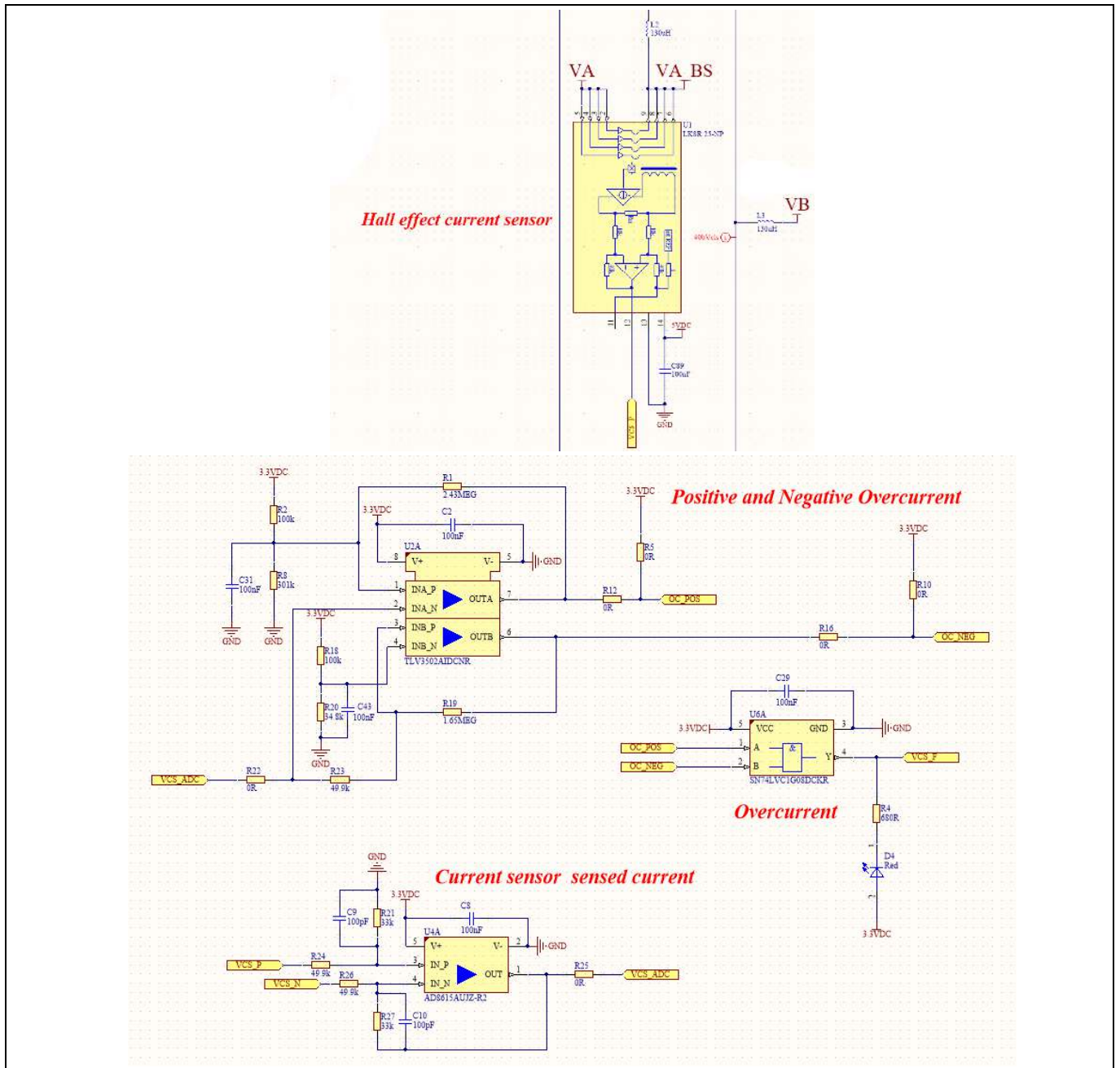
Figure 50   Output current sensing circuits

6 Embedded firmware

6.1 XMC™ 4000 series microcontroller

The XMC™ microcontroller family based on ARM® Cortex®-M cores, is suitable for real-time critical applications where an industry-standard core is needed. It is dedicated to applications in the segments of power conversion, factory and building automation and transportation, as well as home appliances. All XMC4000 devices are powered by ARM® Cortex®-M4 with a built-in DSP instruction set. The single precision floating point unit, direct memory access (DMA) feature and memory protection unit (MPU) are state-of-the-art for all devices. XMC4000 series processors run with clock speeds ranging from 80 to 144 MHz for the core and a comprehensive set of common, fast, and precise analog/mixed-signal, timer/PWM and communication peripherals.

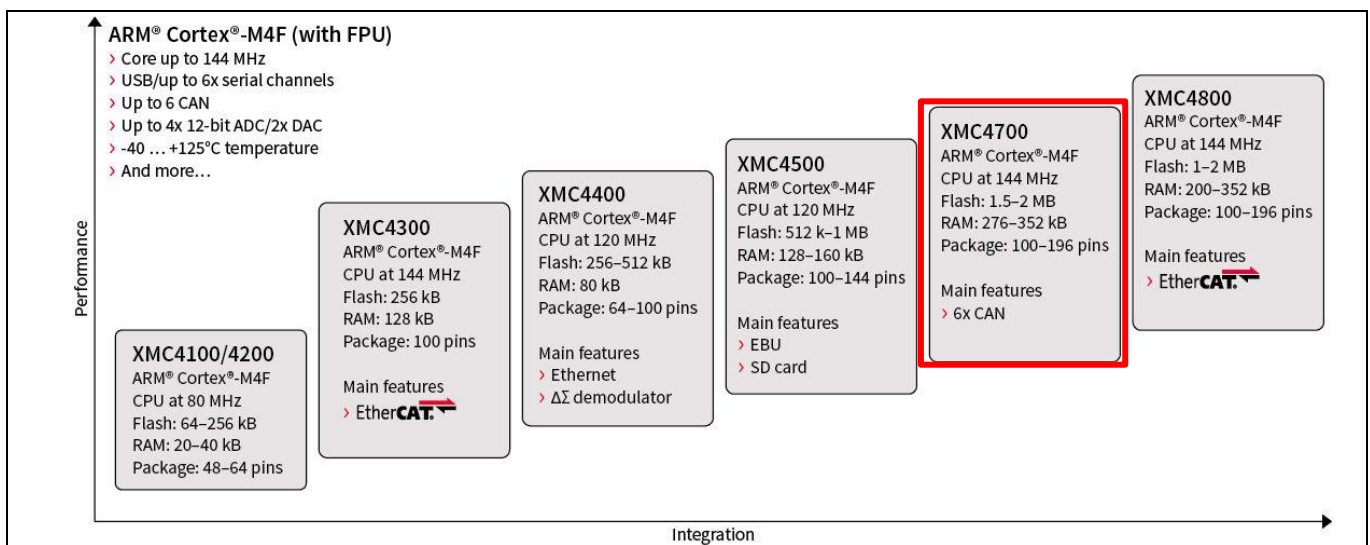There are several variants of the XMC4000 series, shown below:

Figure 51   XMC4000 series sub-groups

The growing complexity of today's energy-efficient embedded control applications demands microcontroller solutions with higher-performance CPU cores featuring DSP and FPU capabilities. Power converter designs are subject to ever-increasing requirements fueled by customer demands or industry association guidelines (such as higher power density, communication, modularity or the 80 Plus Titanium efficiency standard). Semiconductor technology advances have allowed MCU manufacturers to develop a new class of MCUs, optimized for digital power conversion applications in terms of features and price point, motivating power supply designers to use digital control for SMPS. The XMC4700 family of microcontrollers takes advantage of Infineon's decades of experience in the industrial market to provide an optimized solution to meet the performance challenges of today's embedded control applications, which is why it is has been selected for this application.

Summary of features:

- 1536 to 2048 kB Flash, 276 to 352 kB RAM

- Supply voltage range: 3.13 to 3.63 V

- USIC 6-channel [quad SPI, SCI/UART, I²C, I²S, LIN]

- 2x PWM timers (CCU8), 16 to 64-bit 8-channel+ dead-time

- 6x CAN, 256 MO

- Peripherals clock: 144 [MHZ]

- Core frequency: 144 [MHZ]

- 4x ΔΣ-demodulator

- External memory interface (EBU)

- Package: LQFP144/LQFP100/LFBBGA196

- Temperature range: -40°C…85°C/125°C

- 10/100 Ethernet MAC (/w IEEE 1588)

- SDIO/SD/MMC interface

- Safety package supporting SIL-2/3

- Rich connectivity: 2x CAN nodes, 4-channel serial COM unit (configurable to SPI, I²C, I²S, UART), USB FS

- Up to 4 x 12-bit ADC with a sample time of 70 ns ensures fast reaction times and tighter control loops
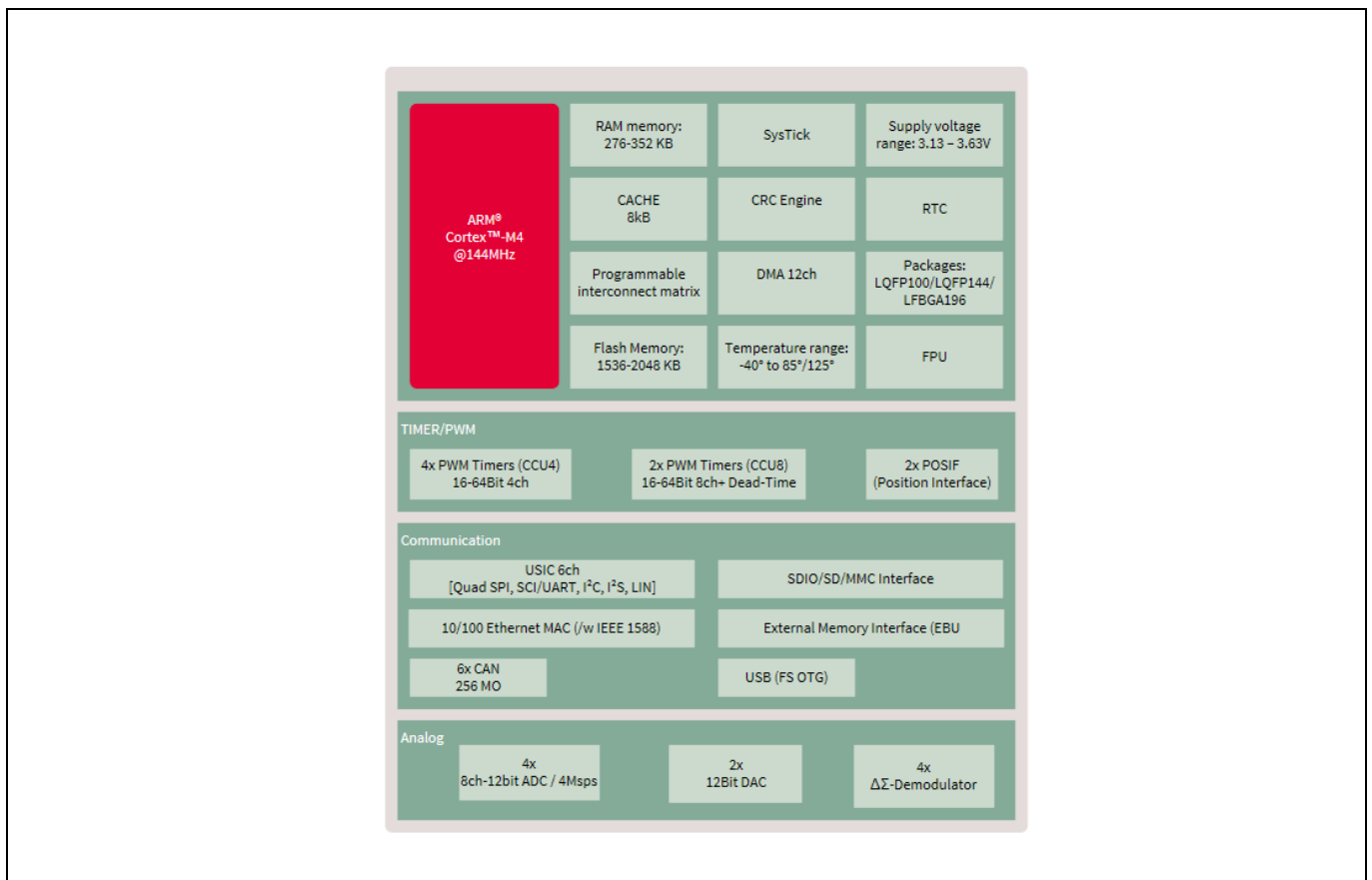
- 4-channel 150 ps HRPWM timer (XMC4200/4400 series)

Figure 52   XMC4700 core and peripherals

6.2 Digital control implementation

The digital control daughter card designed for the five-level inverter provides the PWM signals to the gate drivers. These are derived from three of the PWM modules of the XMC4700. Analog inputs are used for sensing the DC input voltage and flying capacitor voltages. The output voltage is sensed via a differential amplifier and the output current is sensed via the hall effect current sensor located on the main power board, whose output is fed to the digital control board. Comparators are used to detect positive and negative over-currents, which are signaled to the microcontroller to trigger a rapid shutdown. The microcontroller also operates the inrush current bypass circuit.

The XMC4700 option was chosen because the functionality of the PWM modules is necessary to provide the required gate-drive signals. A clock speed of 144 MHz provides sufficient granularity of adjustment for the PWM outputs switching at 20 kHz or higher.

The 144-pin PG-LQFP-144 packaged XMC4700-F144F2048 variant has 32 kB of Flash memory and 2048 kB of SRAM, and more than enough I/O pins to support the required functions.
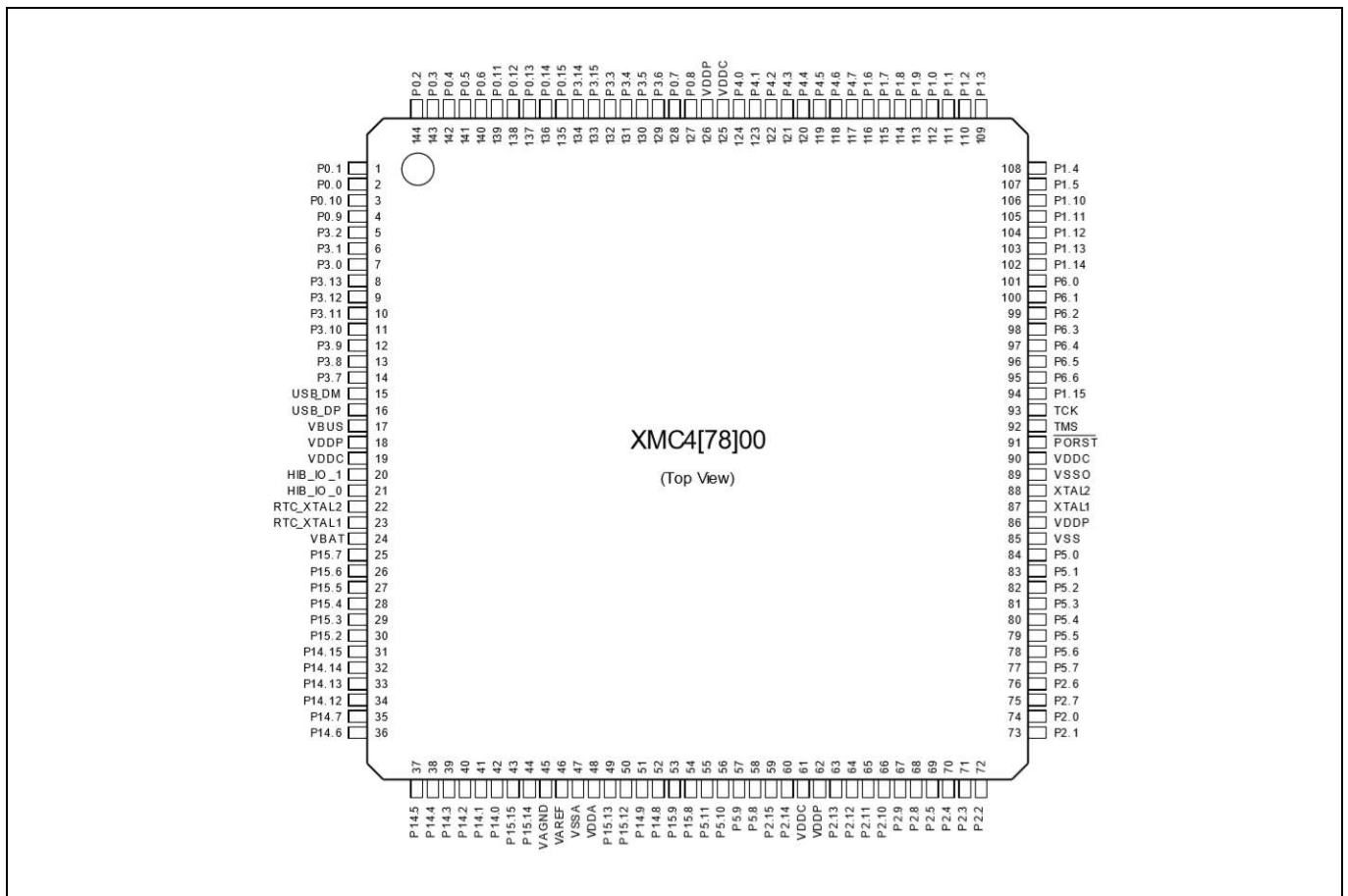

Figure 53   XMC4700 PG-LQFP-144 pin configuration (top view)

The diagram above shows the input and output connections listed in the following table:

Table 5   XMC4700-F144F2048 I/O functions (unconnected pins are not included)

Pin	Name	Function	Description
18, 62, 86, 126	VDDP		3.3 V DC regulated
19, 61, 90, 125	VDDC		1.3 V DC regulated
46	VDDA		3.3 V DC regulated
48	VAREF		3.3 V DC regulated
45	VAGND		0 V
85	VSS		0 V
47	VSSA		0 V
89	VSSO		0 V
87	XTAL1	External clock	Crystal oscillator
88	XTAL2	External clock	Crystal oscillator
92	TMS		
93	TCK		
2	P0.0	Digital output/PWM	S'1 (Q17, Q22) LF gate drive (see Table 2)
1	P0.1	Digital output/PWM	T'2 (Q42) HF gate drive (see Table 2)
144	P0.2	Digital output/PWM	T'1 (Q41) HF gate drive (see Table 2)
143	P0.3	Digital output/PWM	S1 (Q1, Q9) LF gate drive (see Table 2)
142	P0.4	Digital output/PWM	T2 (Q6) HF gate drive (see Table 2)
141	P0.5	Digital output/PWM	T1 (Q5) HF gate drive (see Table 2)
128	P0.7	Digital input	Output over-current positive or negative (active low)
4	P0.9	Digital output/PWM	T'2 (Q7) HF gate drive (see Table 2)
3	P0.10	Digital output/PWM	T'1 (Q8) HF gate drive (see Table 2)
137	P0.13	Digital output	Overvoltage warning LED
108	P1.4	Digital output	TXD
107	P1.5	Digital input	RXD
94	P1.15	Digital output	Overvoltage warning LED
72	P2.2	Analog input	Output current sense
76	P2.6	Digital output/PWM	T2 (Q43) HF gate drive (see Table 2)
75	P2.7	Digital output/PWM	S1 (Q44) LF gate drive (see Table 2)
57	P5.9	Digital output	Inrush limiter bypass
42	P14.0	Analog input	Phase "a" flying capacitor voltage (VC38)
41	P14.1	Analog input	Input DC bus full voltage
40	P14.2	Analog input	Split-rail DC voltage (center-negative side)
36	P14.6	Analog input	Phase "b" flying capacitor voltage (VC35)
35	P14.7	Analog input	Output current sense

6.3 DAVE™ IDE

The firmware controlling this demo board was developed using the DAVE™ IDE, which can be downloaded free of charge from the Infineon website. Programming and debugging was carried out via the XMC™ Link isolated debug probe, which is connected to the daughter card through the larger ribbon cable to header P1 and to a computer via a USB cable (the smaller ribbon cable is not used).

Figure 54   XMC™ Link isolated debugger probe

A project was created within the DAVE™ IDE containing the device definition, settings and source files required to compile and build the executable code, which can be downloaded into the Flash program memory of the XMC™ controller. There are several programming/debugging protocols available, which can be selected when first setting up the DAVE™ IDE to connect the daughter card before programming.

The I/O ports are configured for analog or digital input or output and mapped to the peripherals required by selecting the required DAVE™ apps and configuring these to provide the functions required for the application. These include analog inputs, digital inputs and outputs, and functions such as the PWM generators and timers.

The apps are listed in the app dependency tree window in the DAVE™ CE screen and displayed graphically in the app dependency window. Double-clicking on any app opens up a menu allowing the programmer to configure the app. The manual pin allocator is used to select which I/O pins are mapped to each of the app inputs and outputs.

When configuration is complete the corresponding ".c" and ".h" source code files are generated by clicking the "Generate code" button normally located on the command bar located below the menu bar at the top of the DAVE™ CE screen shown below. For more complex functionality, it is necessary to obtain the necessary functions from the DAVE™ library, which is also available to download.
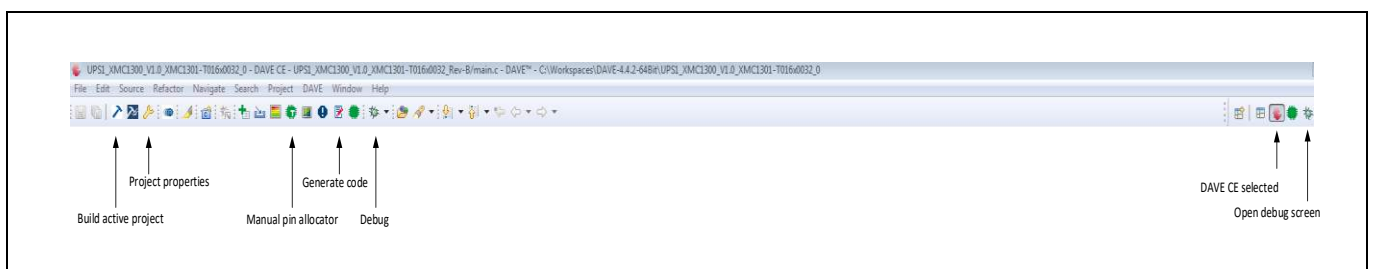

Figure 55   DAVE™ IDE main commands

6.4 Control algorithms

The firmware operates as a state machine in which a main program loop runs continuously, executing different sections of code depending on the current state. In the meantime, a number of background processes are also running, which in this case are executed at timed intervals to coincide with the switching waveforms. At the beginning of each switching cycle the analog values are transferred to the appropriate registers and then re-scaled and filtered as needed. In addition, the PWM duty cycles are updated according to the next sine value in a set stored in a reference table.
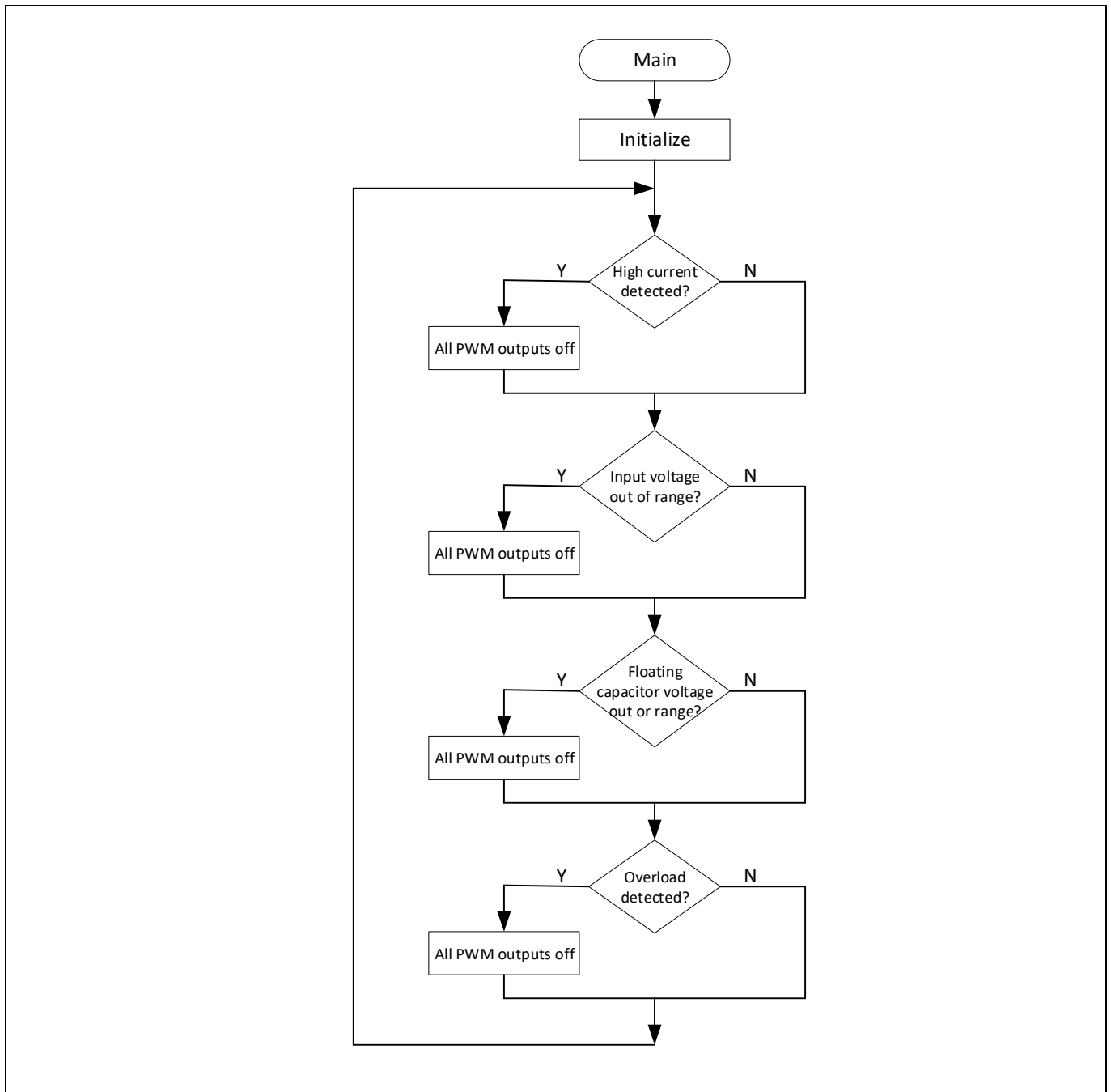
Figure 56   Main program loop

After initialization of the peripherals and variables, the main program runs in an endless loop from which the PWM period match interrupt is called at the start of each new switching cycle. During the main loop the output current signal from the fast over-current detection circuit is monitored to force a rapid switch-off of all gate

drive signals if a fault condition is detected. The input DC voltage and flying capacitor voltages are also checked in this loop, triggering a shutdown if detected to be out of range.
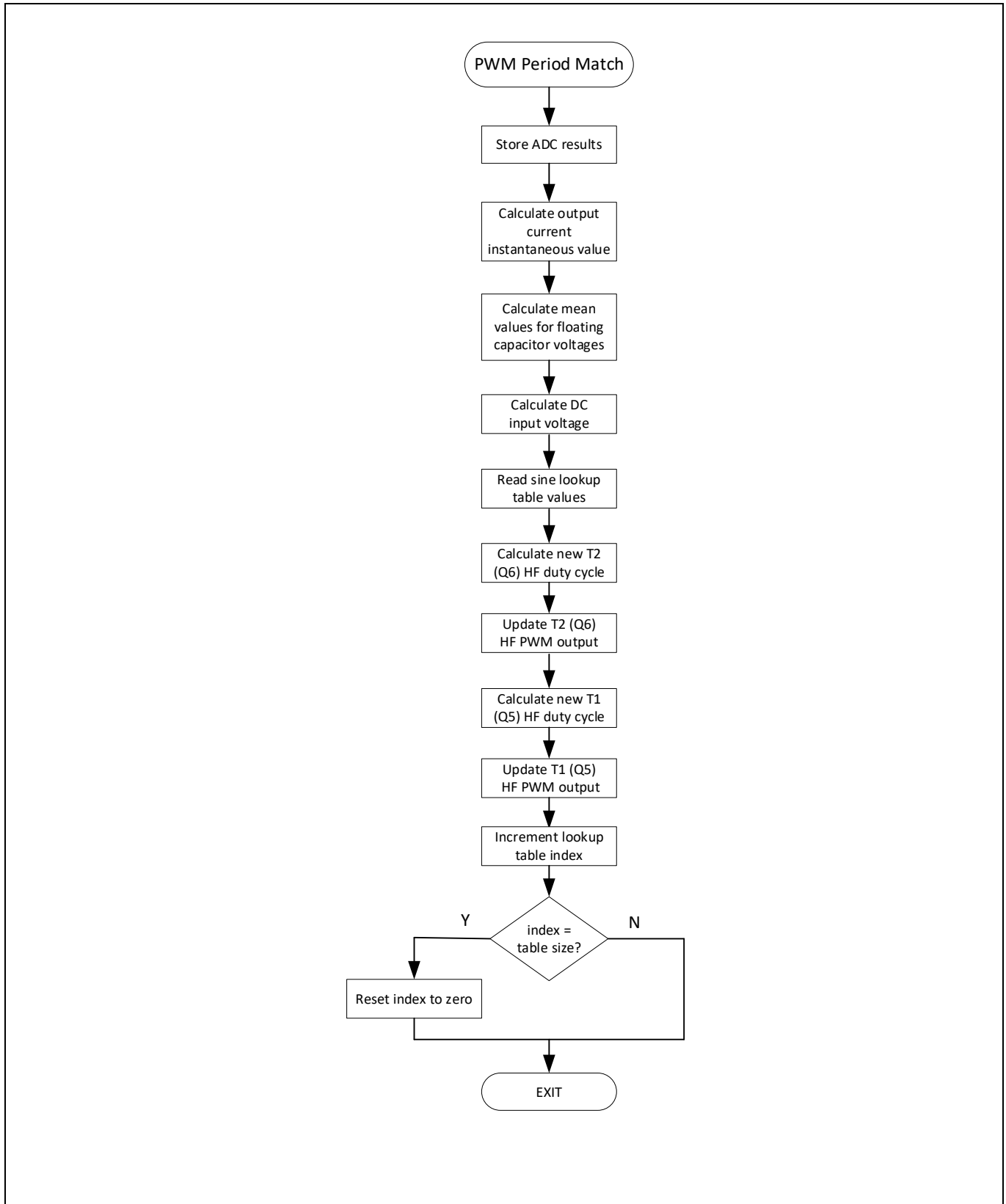

Figure 57   PWM match ISR

7 Bill of Materials (BOM)

7.1 Power board

Designator	Manufacturer	Part number	Quantity	Value/Rating
C1, C2, C18, C19, C32, C33, C36, C37, C39, C40, C57, C58, C69, C72, C73, C74	Kemet	C1206C102J2GACTU	16	1 nF
C3, C4, C5, C6, C7, C8, C14, C17, C20, C21, C22, C34, C41, C42, C43, C44, C45, C46, C47, C53, C56, C59, C60, C61, C75, C76, C77, C78, C81, C82, C83, C84, C92, C93, C94, C95, C96, C102, C103, C104, C105, C106, C107, C109, C110, C112, C114, C115, C116, C118	Kemet	C1210C104KCRACTU	50	100 nF
C9, C10, C11, C12, C48, C49, C50, C51	Yageo	CC1206KRX7RABB222	8	2.2 nF
C13, C15, C16, C52, C54, C55, C119, C120	Nichicon	LGW2E391MELA30	8	390 µF
C23, C121	Murata	GRM1885C1H392JA01	2	3.9 nF
C24, C68	TDK Corporation	B32754C2505K000	2	5 µF
C25, C26, C62, C63, C71, C79	TDK Corporation	B32021A3102K000	6	1 nF
C27, C70	TDK Corporation	B32923C3105M000	2	1 µF
C29, C30, C31, C80, C89	AVX	06035C104KAT2A	5	100 nF
C35, C38	Kemet	C4ATDBW5300A30J	2	30 µF
C64, C98	Kemet	C1206C475M3RAC	2	4.7 µF

Bill of Materials (BOM)

C65, C99	Kemet	C0805C474K5RACTU	2	470 nF
C66, C67, C85, C86	AVX	06035A101FAT2A	4	100 pF
C97	Kemet	C0603C224J8RAC	1	220 nF
C100	Murata	GRM21BR71H224KA01	1	220 nF
C101, C108, C111	Murata	GRM21BR61C106KE15	3	10 µF
C113	Murata	GRM1885C1H102JA01	1	1 nF
C117	Kemet	C0603C223K5RACTU	1	22 nF
D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48	Infineon Technologies	BAS3005A-02V	48	BAS3005A-02V
D49	Nexperia	PESD15VS1UB	1	PESD15VS1UB
D50	Infineon Technologies	BAS3010B-03W	1	BAS3010B-03W
D51	SunLED	XZMDR155W	1	Red
D52	Texas Instruments	LM4041D12QDBZR	1	Voltage reference
D53	Vishay	VS-HFA16TB120S-M3	1	VS-HFA16TB120S-M3
G3	Infineon Technologies	IFX91041EJV33	1	IFX91041EJV33
G4	Texas Instruments	LM3480IM3X-5.0/NOPB	1	LM3480IM3X-5.0/NOPB
K1	Panasonic	APV1121S	1	APV1121S

Bill of Materials (BOM)

L1	Coilcraft	LPS5030-153MRB	1	15 µH
L2, L3	MPS Industries	P15005	2	100 µH +/- 10 percent, 18 A_{RMS}, 13 mΩ
L4, L5	TDK Corporation	B82726E6243A041	2	1 mH
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q29, Q30, Q31, Q32, Q33, Q34, Q35, Q36, Q37, Q38, Q39, Q40, Q41, Q42, Q43, Q44, Q45, Q46, Q47, Q48	Infineon Technologies	BSC093N15NS5	48	OptiMOS™ 5 150 V/87 A/9.3 mΩ/ PG-TDSON-8 SuperSO8/
Q49, Q50	Infineon Technologies	IPT60R022S7	2	600 V/23 A/22 mΩ/ PG-HSOF-8/ CoolMOS™ SJS7
R1, R2, R5, R6, R7, R8, R13, R14, R33, R34, R35, R36, R37, R38, R39, R40, R59, R60, R63, R64, R76, R79, R80, R89, R90, R93, R94, R109, R110, R111, R112, R131, R132, R135, R136, R137, R138, R139, R140, R157, R159, R161, R162, R165, R166, R168, R170, R177	Vishay	CRCW060329R4FK	48	29.4 R
R3, R4, R15, R18, R19, R20, R23, R24, R41, R42, R43, R44, R45, R46, R47, R50, R65, R66, R67, R68, R81, R82, R83, R84, R97, R98, R100, R101, R113, R114, R115, R116, R125,	Vishay	CRCW06031R00FK	48	1 R

R126, R129, R130, R141, R142, R143, R146, R158, R160, R163, R164, R167, R169, R171, R172				
R9, R10, R16, R17, R29, R30, R31, R32, R57, R58, R61, R62, R73, R74, R77, R78, R91, R92, R95, R96, R105, R106, R107, R108, R127, R128, R133, R134, R153, R154, R155, R156, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200	Vishay	CRCW12064R99FK	48	4.99 R
R11, R12, R21, R22, R25, R26, R27, R28, R48, R49, R51, R52, R53, R54, R55, R56, R69, R70, R71, R72, R85, R86, R87, R88, R99, R102, R103, R104, R117, R118, R119, R120, R121, R122, R123, R124, R144, R145, R147, R148, R149, R150, R151, R152, R173, R174, R175, R176	Vishay	CRCW060310K0FK	48	10 k
R75, R274	Vishay	CRCW0603680RFK	2	680 R
R78, R234	Vishay	CRCW0603100RFK	2	100 R
R179, R180, R181, R182, R184, R237, R240, R241, R243, R244, R246, R247,	Yageo	RT0603BRD07499KL	16	499 k

R251, R254, R255, R257				
R183, R242, R250, R258	Yageo	RT0603BRD0712K7L	4	12.7 k
R201	Vishay	CRCW060322K0FK	1	22 k
R202	Ohmite	35J12RE	1	12 R
R203, R204, R207, R224, R225, R226, R227, R256	Vishay	CRCW120675K0FK	8	75 k
R205	Vishay	CRCW060321K0FK	1	21 k
R206, R228, R231, R239	Vishay	RCV12062M00FKEA	4	2 M
R208, R209, R210, R213, R214, R215, R216, R217, R219, R221, R222, R223	Vishay	RCV1206150KFKEA	12	150 k
R211, R212, R218, R220	Vishay	RCV1206220KFKEA	4	220 k
R230, R245, R248, R249, R252, R253, R270, R272, R273, R275, R279, R280	Vishay	CRCW251220R0FK	12	20 R
R232	Vishay	CRCW060342K2FK	1	42.2 k
R276	Vishay	CRCW0603348RFKEA	1	348 R
R277	Vishay	CRCW06031K00FK	1	1 k
R233, R235, R236, R238, R259, R260, R261, R262	Vishay	CRCW06030000Z0	8	0 R
U1	LEM	LKSR 25-NP	1	LKSR 25-NP
U2, U3	Analog Devices	AD8615AUJZ-R2	2	AD8615AUJZ-R2

X1, X2	Cal Test Electronics	CT3151SP-2	2	Socket 1 4p
X3, X4	Cal Test Electronics	CT3151SP-0	2	Socket 1 4p
X5, X8, X9, X10	Samtec	SSM-116-L-DV	4	Socket 16 x 2
X6	Molex	22-11-2022	1	KK 254 solid header, vertical, with friction lock, 2 circuits, gold (Au) plating
X7	Keystone Electronics Corp.	3513	1	3513

7.2 Control card

Designator	Manufacturer	Part number	Quantity	Value/Rating
C1, C2, C8, C13, C14, C15, C16, C22, C23, C24, C25, C26, C27, C28, C29, C31, C41, C43	AVX	06035C104KAT2A	18	100 nF
C3, C4, C6, C42	Murata	GRM1885C1H392JA01	4	3.9 nF
C9, C10	AVX	06035A101FAT2A	2	100 pF
C11, C12	Würth Elektronik	885012006003	2	15 pF
C17, C18, C19, C20, C21, C36, C37, C39	Murata	GRM21BR61C106KE15	8	10 µF
C32	Kemet	C0603C224J8RAC	1	220 nF
C33	Kemet	C1206C475M3RAC	1	4.7 µF
C34	Kemet	C0805C474K5RACTU	1	470 nF
C35	Murata	GRM21BR71H224KA01	1	220 nF
C38	Murata	GRM1885C1H102JA01	1	1 nF
C40	Kemet	C0603C223K5RACTU	1	22 nF

D1	Infineon Technologies	BAS3010B-03W	1	BAS3010B-03W
D2, D3, D4, D5, D6	SunLED	XZMDR155W	5	Red
G1	Infineon	IFX91041EJV33	1	IFX91041EJV33
L1, L2	TDK Corporation	MPZ1608S600ATAH0	2	Ferrite bead
L3	Coilcraft	LPS5030-153MRB	1	15 µH
R1	Vishay	CRCW06032M43FK	1	2.43 M
R2, R18	Vishay	CRCW0603100KFK	2	100 k
R3, R4, R11, R13, R41	Vishay	CRCW0603680RFK	5	680 R
R5, R10, R12, R16, R22, R25, R28, R29, R30, R32, R35, R39, R40, R43, R44, R45, R46, R47, R48	Vishay	CRCW06030000Z0	19	0 R
R6	Vishay	CRCW060310K0FK	1	10 k
R7, R9, R15, R36, R49, R50	Vishay	CRCW06032K49FK	6	2.49 k
R8	Vishay	CRCW0603301KFK	1	301 k
R19	Vishay	CRCW06031M65FK	1	1.65 M
R20	Yageo	RC0603FR-0734K8L	1	34.8 k
R21, R27	Yageo	RT0603BRD0733KL	2	33 k
R23	Vishay	CRCW060349K9FK	1	49.9 k
R24, R26	Yageo	RT0603BRD0749K9L	2	49.9 k
R31	Vishay	CRCW0603510RFK	1	510 R
R37, R38	Vishay	CRCW060333R0FK	2	33 R
R42	Vishay	CRCW060322K0FK	1	22 k

U1	Texas Instruments	SN74LVC2G14DCKR	1	SN74LVC2G14DCKR
U2	Texas Instruments	TLV3502AIDCNR	1	TLV3502AIDCNR
U4	Analog Devices	AD8615AUJZ-R2	1	AD8615AUJZ-R2
U5	Infineon Technologies	XMC4700-F144F2048	1	IFX_XMC4700-F144F2048
U6	Texas Instruments	SN74LVC1G08DCKR	1	SN74LVC1G08DCKR
X1	Samtec	TSM-116-01-F-DH-A	1	Header 16X2
X3	Samtec	TSW-104-07-L-D	1	Header 4X2-0
Y1	Nihon Dempa Kogyo	NX3225SA-12.000M-STD-CRS-2	1	12 MHz

7.3   Aux supply and gate driver card (center)

Designator	Manufacturer	Part number	Quantity	Value/Rating
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C91, C113, C114, C115, C116, C117, C118, C119, C120	AVX	06035C104KAT2A	21	100 nF
C69, C74, C79, C84, C89, C90, C93, C98, C103, C108	Kemet	C1206C475M3RAC	10	4.7 µF
C92	AVX	06035A101FAT2A	1	100 pF
D17, D18, D19, D20, D21, D24, D25, D26	ON Semiconductor	MBRA340T3G	8	MBRA340T3G
D22	ON Semiconductor	MMSZ5259BT1G	1	39 V
D23	Vishay	SS13HE3_B/H	1	SS13HE3_B/H
R1, R2, R3, R4	Vishay	CRCW06030000Z0	4	0 R
R17, R18, R19, R20, R21, R24, R25, R26	Vishay	CRCW06034K99FK	8	4.99 k
R22	Vishay	CRCW0603300KFK	1	300 k
R23	Vishay	CRCW06037K15FK	1	7.15 k
TR3	Yageo	E22_8OUTPUTS	1	E22_8OUTPUTS

U1, U2, U4, U5	Infineon Technologies	2EDF7275F	4	2EDF7275F
U3	Analog Devices	LT8301ES5#TRMPBF	1	LT8301ES5#TRMPBF
X1	Samtec	TSM-116-01-F-DH-A	1	Header 16X2
X37	Keystone Electronics Corp.	5012	1	5012
X41	Keystone Electronics Corp.	5011	1	5011

7.4 Aux supply and gate driver card (sides)

Designator	Manufacturer	Part number	Quantity	Value/Rating
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C91, C113, C114, C115, C116, C117, C118, C119, C120	AVX	06035C104KAT2A	21	100 nF
C69, C74, C79, C84, C89, C90, C93, C98, C103, C108	Kemet	C1206C475M3RAC	10	4.7 µF
C92	AVX	06035A101FAT2A	1	100 pF
D17, D18, D19, D20, D21, D24, D25, D26	ON Semiconductor	MBRA340T3G	8	MBRA340T3G
D22	ON Semiconductor	MMSZ5259BT1G	1	39 V
D23	Vishay	SS13HE3_B/H	1	SS13HE3_B/H
R1, R2, R3, R4	Vishay	CRCW06030000Z0	4	0 R
R17, R18, R19, R20, R21, R24, R25, R26	Vishay	CRCW06034K99FK	8	4.99 k
R22	Vishay	CRCW0603300KFK	1	300 k
R23	Vishay	CRCW06037K15FK	1	7.15 k
TR3	Yageo	E22_8OUTPUTS	1	E22_8OUTPUTS

U1, U2, U4, U5	Infineon Technologies	2EDF7275F	4	2EDF7275F
U3	Analog Devices	LT8301ES5#TRMPBF	1	LT8301ES5#TRMPBF
X1	Samtec	TSM-116-01-F-DH-A	1	Header 16X2
X37	Keystone Electronics Corp.	5012	1	5012
X41	Keystone Electronics Corp.	5011	1	5011

8 Inductor specifications

Figure 58   Output inductor specification

9 PCB layout

9.1 Main power board PCB design
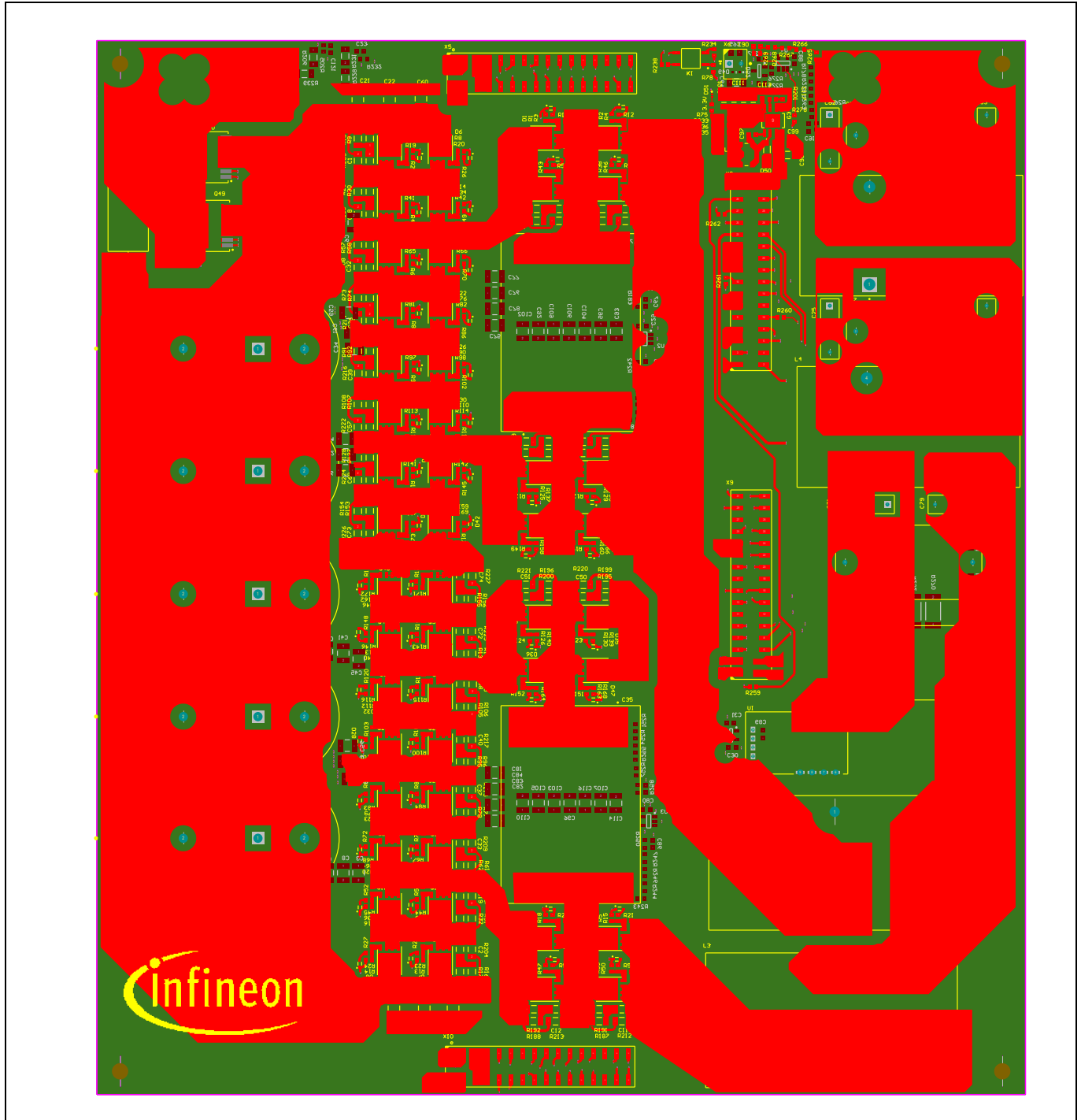
Figure 59   **Main power board top layer**
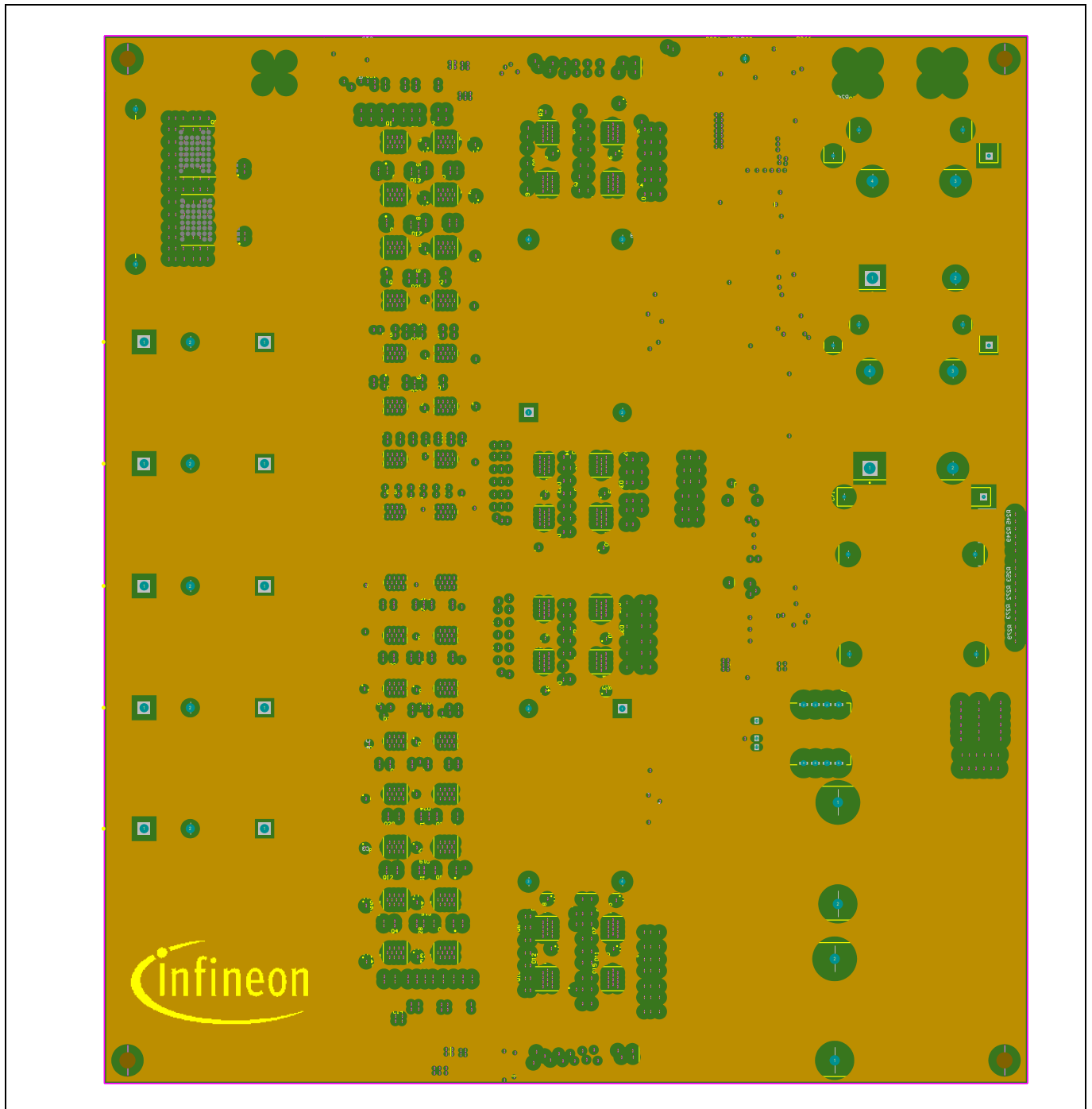
Figure 60   Main power board inner layer 1 (ground)
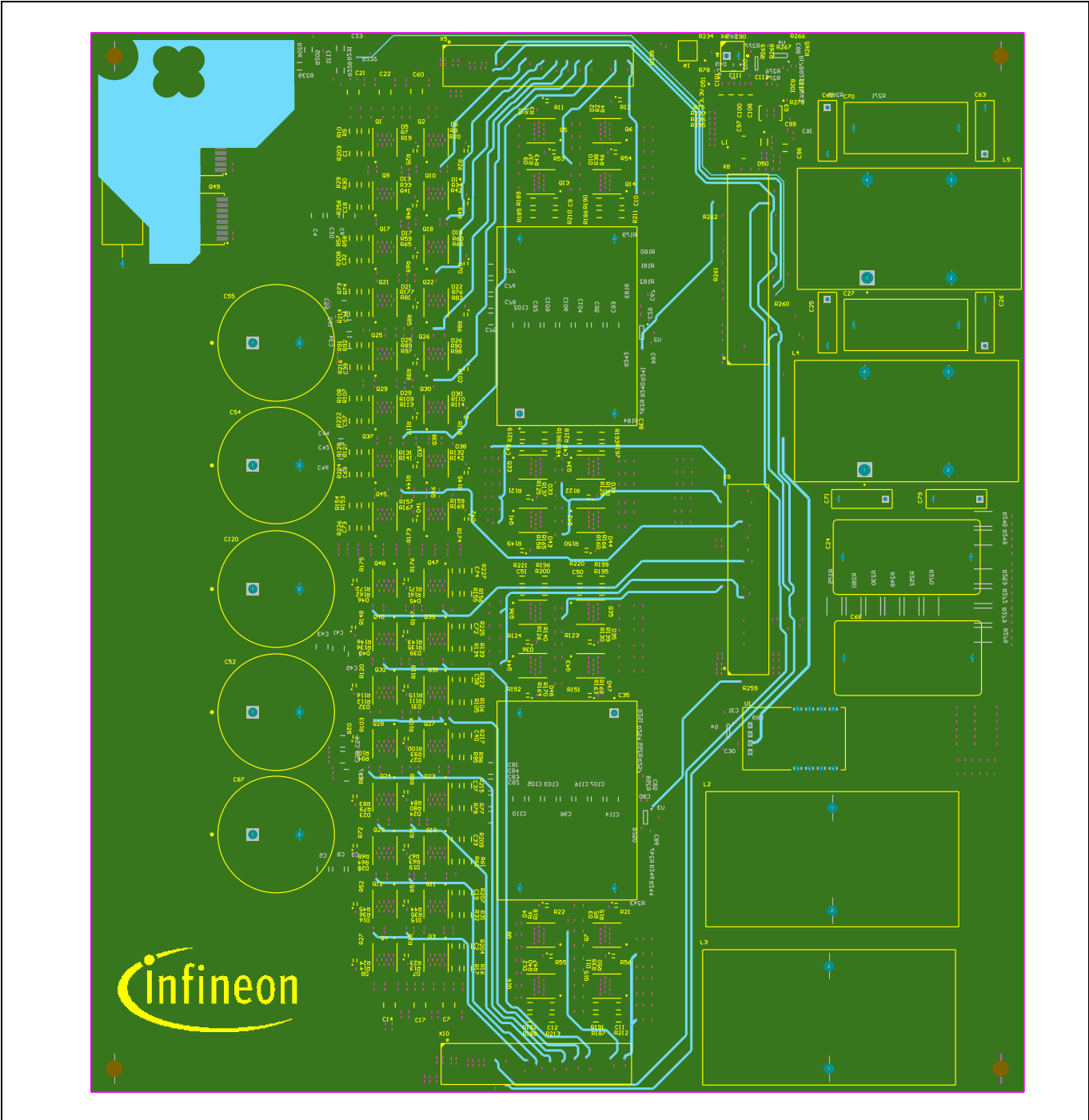
Figure 61   Main power board inner layer 2 (signal)
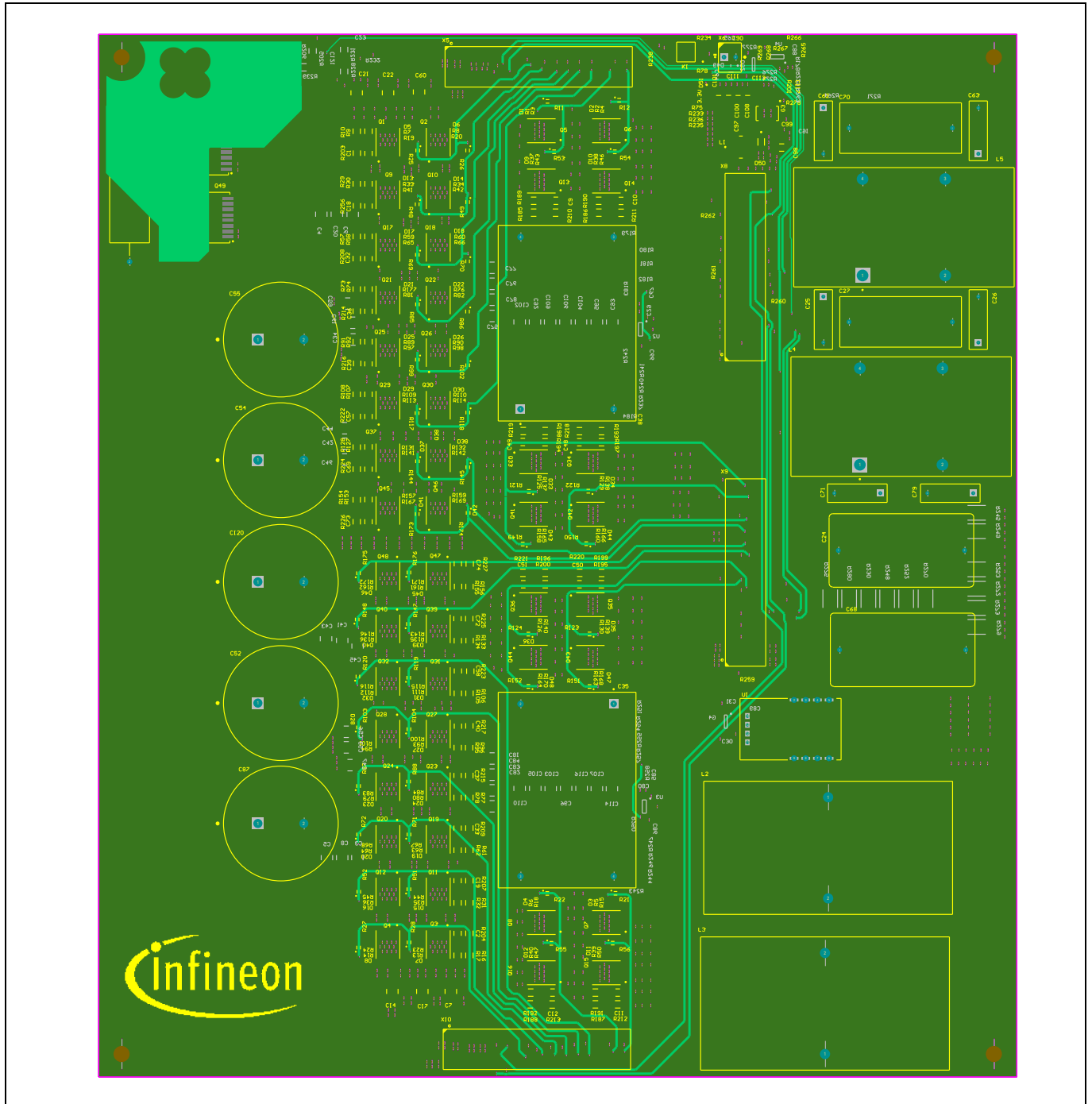
Figure 62   Main power board inner layer 3 (signal)
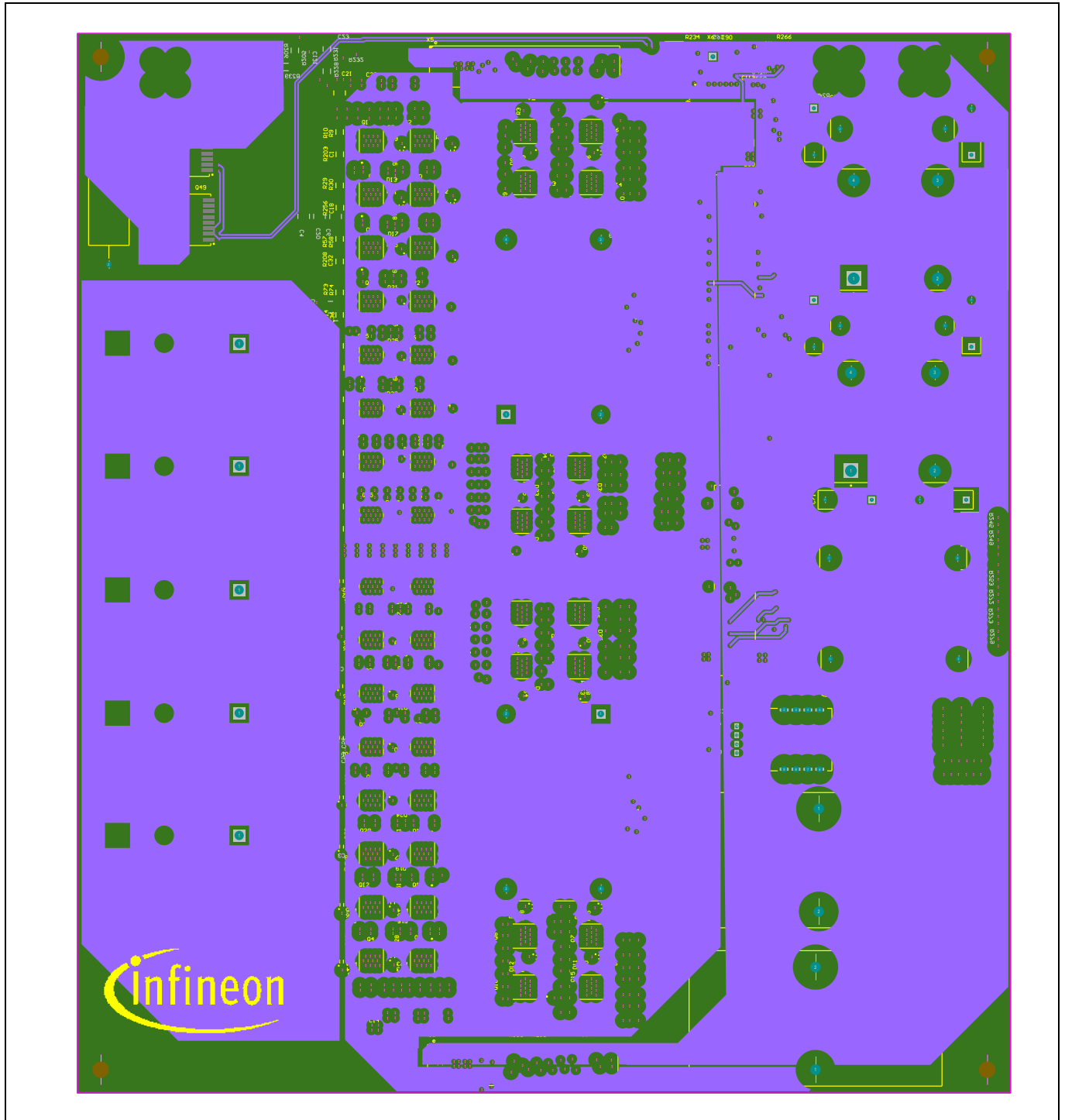
Figure 63   Main power board inner layer 4 (auxiliary power)
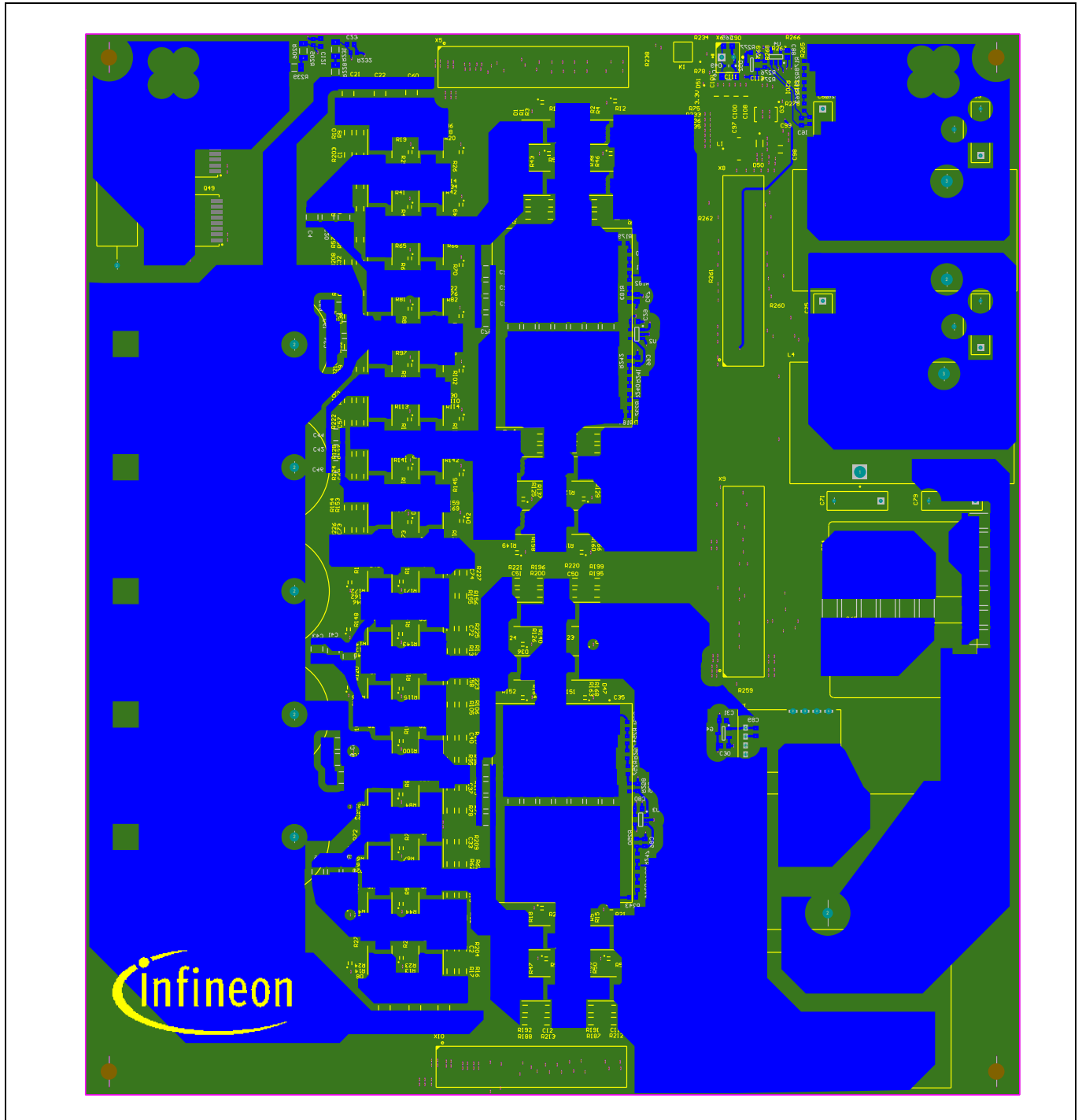
Figure 64   Main power board bottom layer

The main power board has six copper layers all with thicknesses of 2 oz. per square foot, which corresponds to 70 μm or 2.8 mils. This is necessary to carry the currents without introducing unacceptable PCB losses and also to be able to make the necessary connections in a manner that will not introduce any problems due to parasitic inductance, non-optimum signal grounding, cross-coupling or noise.

The DC bus input voltage is routed through the top layer with the mid-point being routed on the bottom layer. The ground return is routed through layer 1, which also forms the ground plane. Layers 2 and 3 are used to route gate drive signals to the various MOSFETs located in different parts of the board. Power interconnections are purposely made on the top and bottom layers with many vias connecting them. These outside conductor layers are used to carry high current so that heat can be dissipated more effectively. Layer 4 is used mainly to carry auxiliary power, including +12 V, +3.3 V and additional ground connections between the DC bus input capacitors as well as connections to the inrush current limit circuit MOSFETs Q49 and Q50.

It can also be seen that many local decoupling capacitors have been placed around different switching cells in the circuit. These consists of banks of 100 nF, 500 V rated ceramic capacitors paralleled for minimum ESR and ESL. These capacitors reduce EMI and ringing by minimizing HF loops. An example consisting of C42, C44 and C46 is shown below:
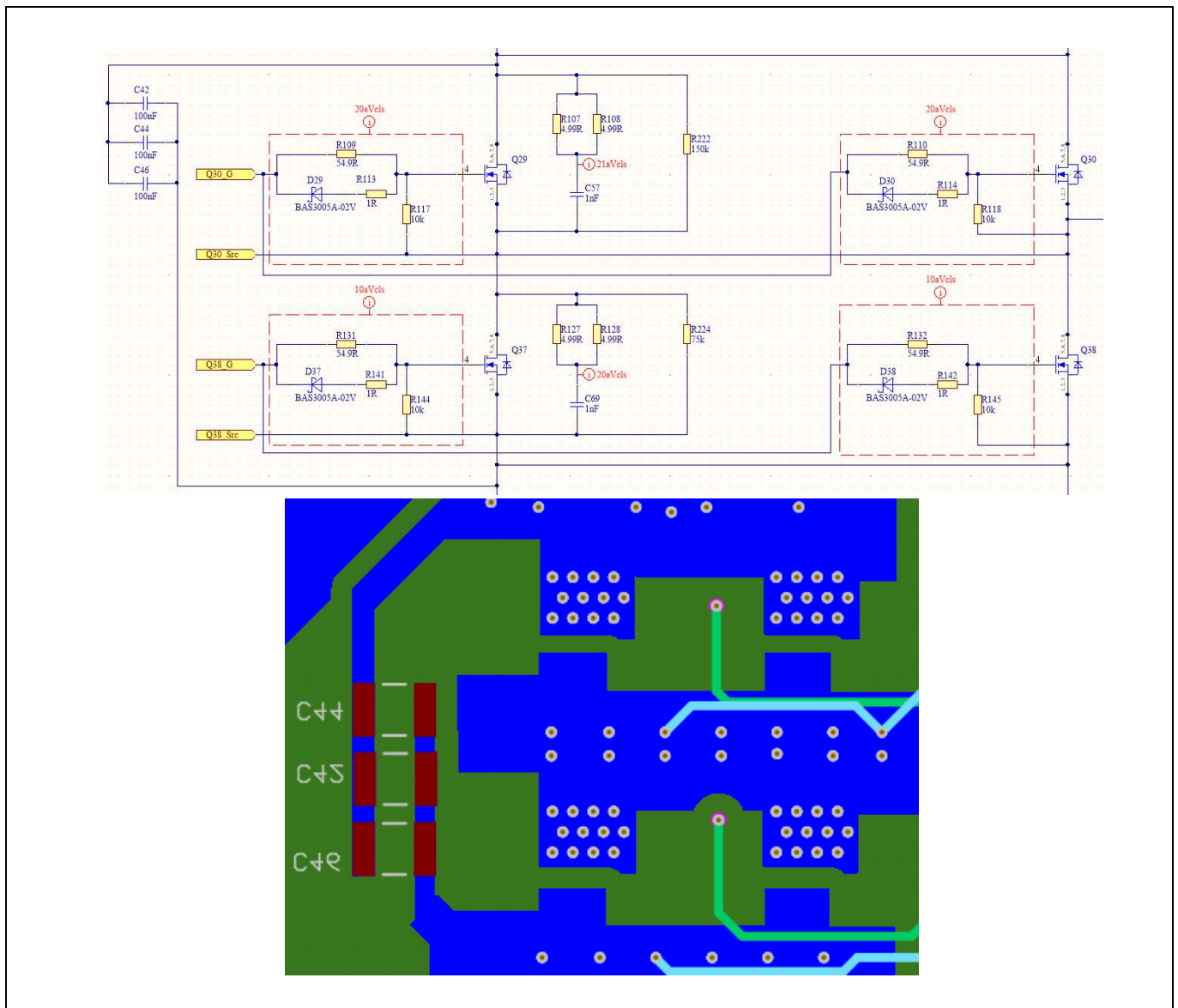
Figure 65   Ceramic capacitors added for local decoupling

10 Test results

10.1 Efficiency measurements

Table 6   **Test measurements**

V$_{IN}$	I$_{IN}$	P$_{IN}$	P$_{AUX}$	V$_{OUT}$	I$_{OUT}$	P$_{OUT}$	P$_{LOSS}$	Efficiency
(V$_{DC}$)	(I$_{DC}$)	(W)	(W)	(V$_{RMS}$)	(A$_{RMS}$)	(W)	(W)	(%)
399.40	1.26	503.64	3.1	237.18	2.11	500.45	6.29	98.76
399.30	2.52	1006.64	3.1	236.20	4.23	999.13	10.61	98.95
399.20	3.78	1510.17	3.1	235.75	6.36	1499.37	13.90	99.08
399.10	5.05	2015.46	3.1	235.38	8.50	2000.73	17.83	99.12
399.00	6.32	2521.28	3.1	235.03	10.64	2500.72	23.66	99.06
398.90	7.59	3029.25	3.1	234.69	12.79	3001.69	30.66	98.99
398.80	8.87	3537.36	3.1	234.32	14.94	3500.74	39.72	98.88
398.80	10.15	4049.42	3.1	233.85	17.11	4001.17	51.34	98.73

Figure 66   Efficiency over load

Test results
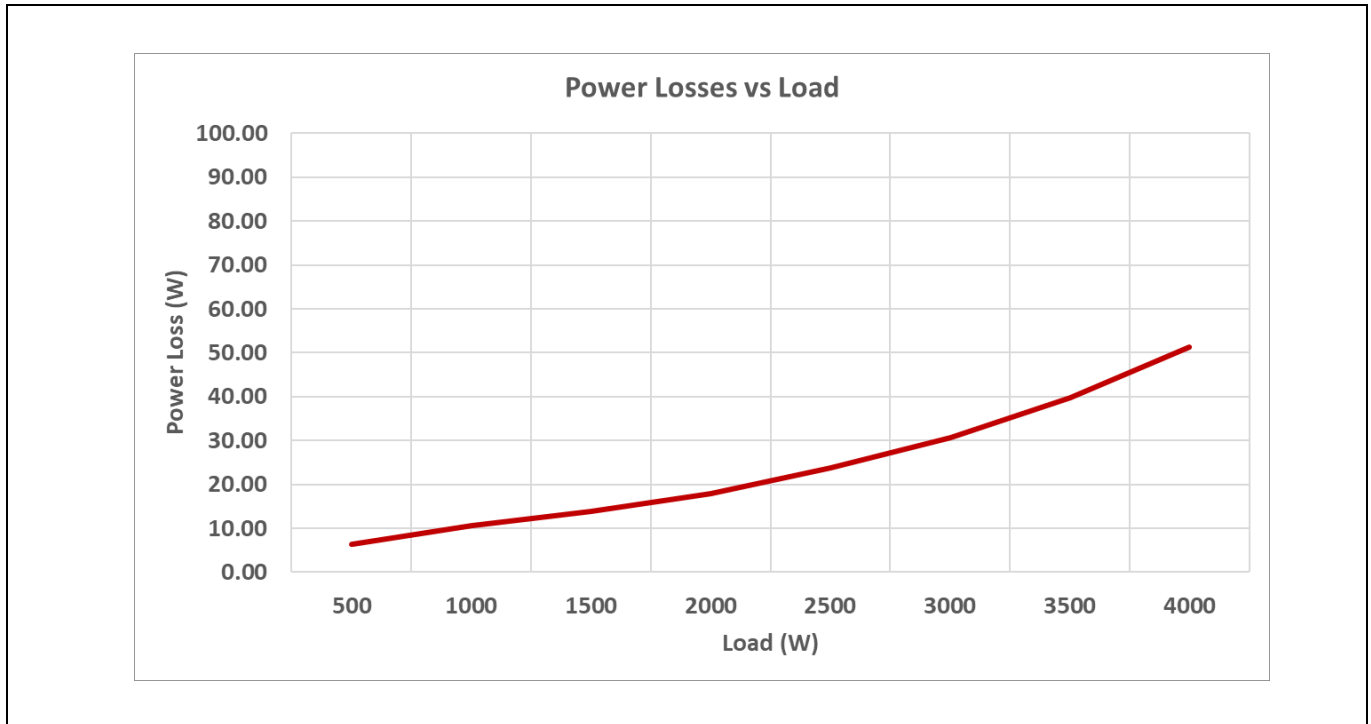
Figure 67   Power losses
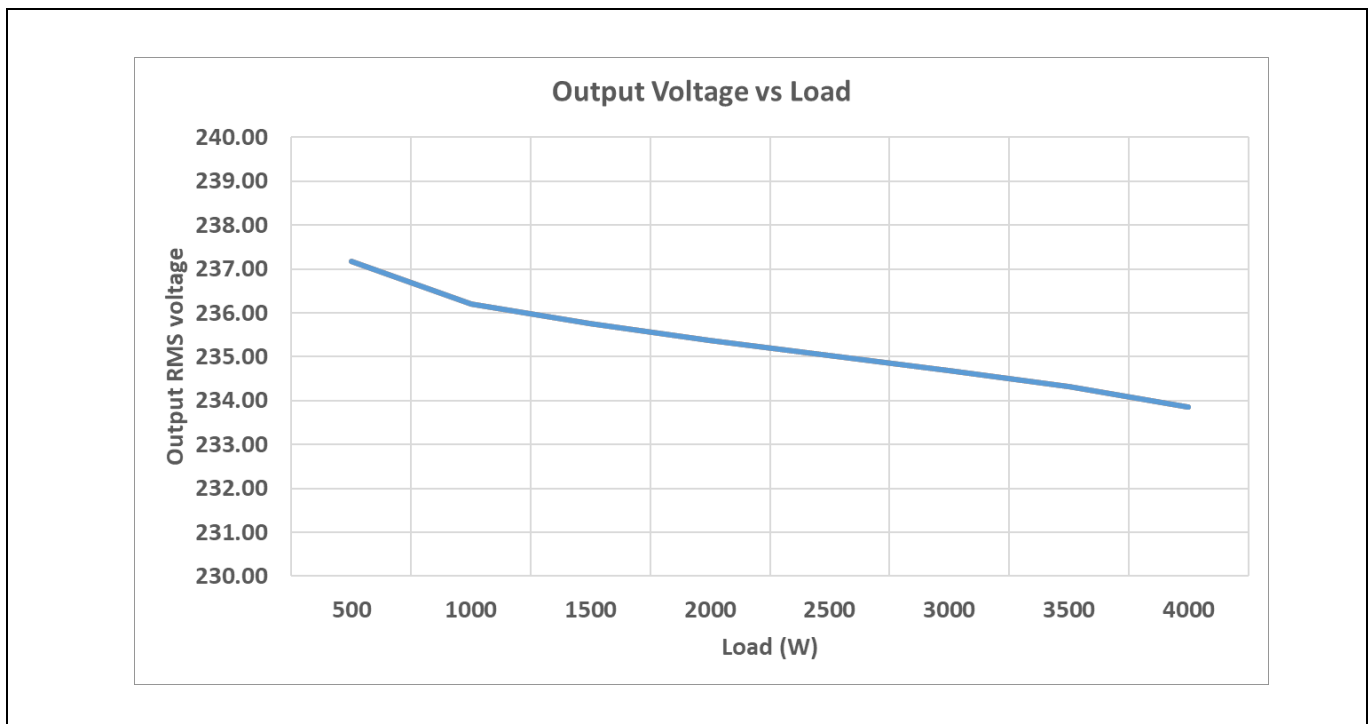
Figure 68   Load regulation

10.2 Operating waveforms

10.2.1 Inverter steady-state output voltage
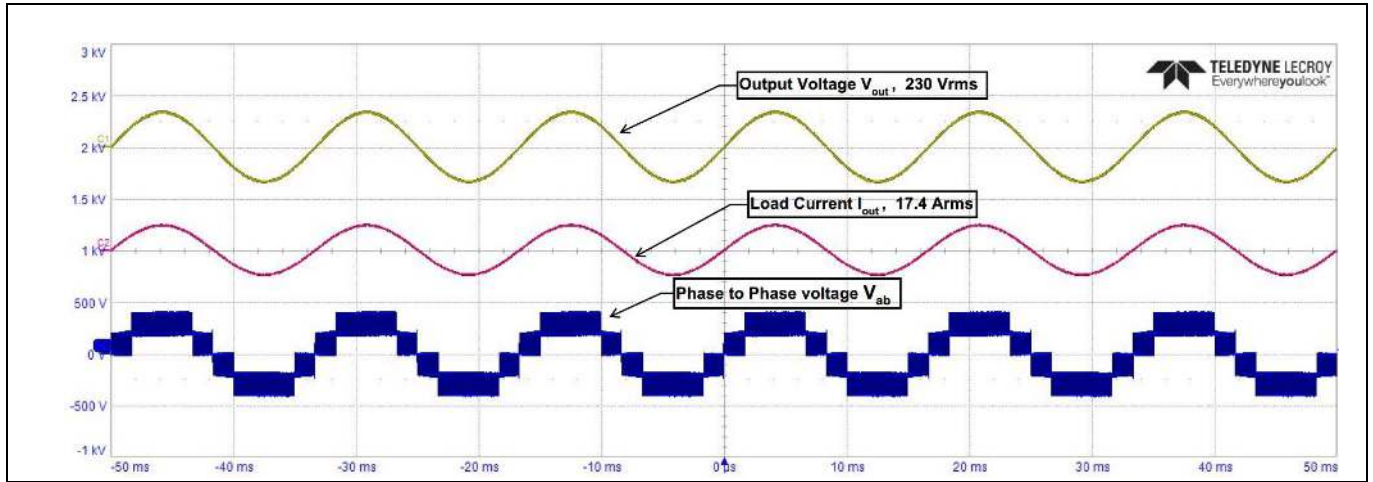
Figure 69 Output voltage V_{out}, output load current I_{OUT}, phase-to-phase voltage V_{ab} at 4 kW
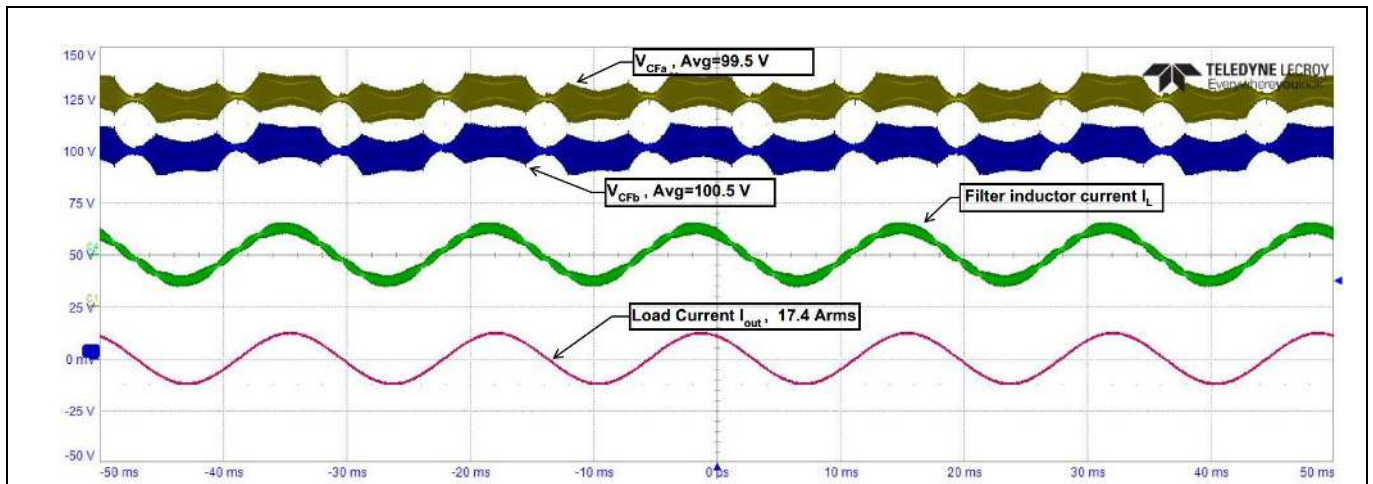
Figure 70 Filter inductor current I_L, output load current I_{OUT}, flying capacitors voltage at 4 kW

10.2.2 Inverter start-up and flying capacitor pre-charge
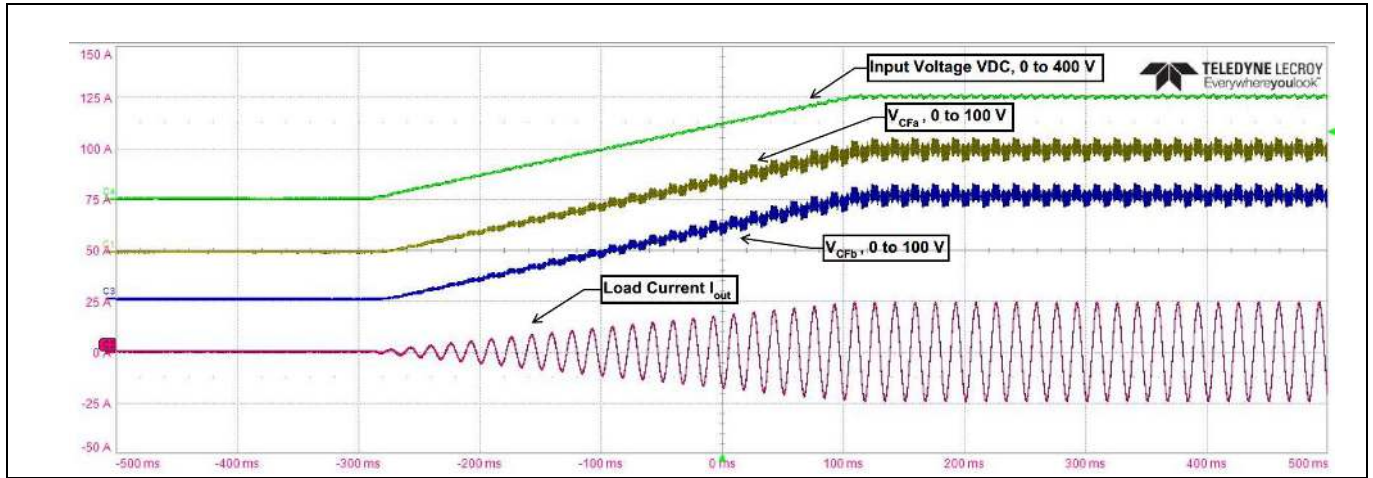
Figure 71   Input voltage V DC and flying capacitors at start-up with 4 kW load connected
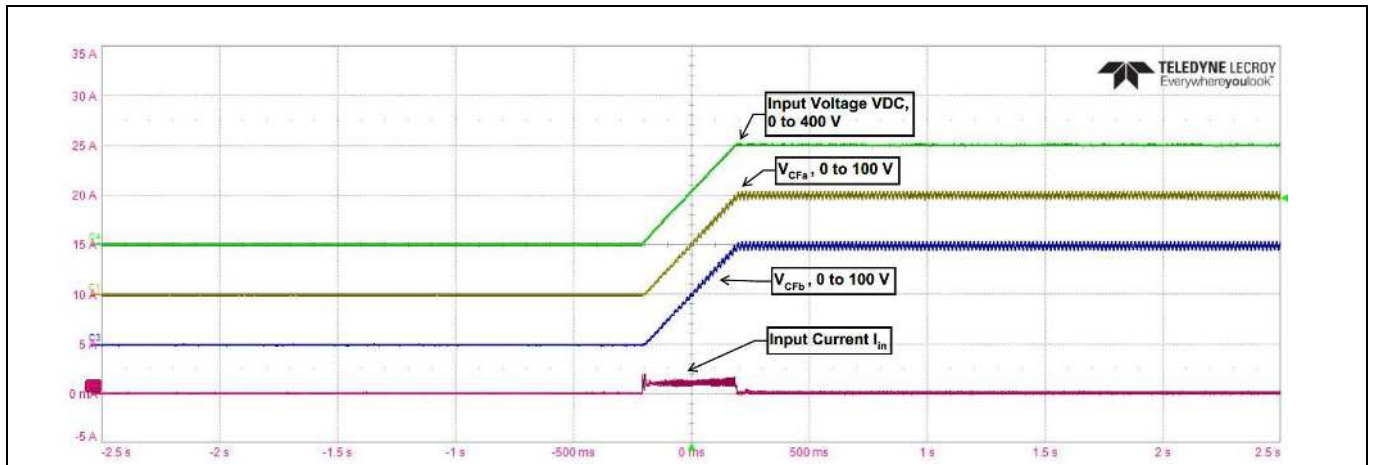
Figure 72   Input voltage V DC and flying capacitor voltages at start-up while no load is connected

10.2.3   Step-change in load
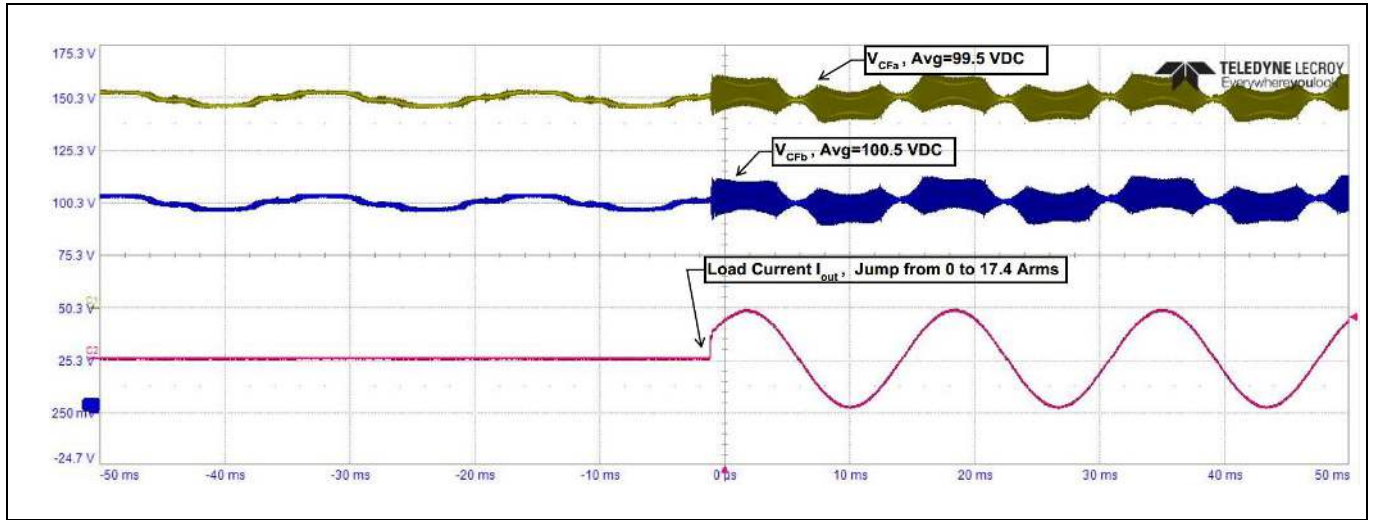
Figure 73   Output load current I_OUT and flying capacitor voltages when load steps from zero to 4 kW
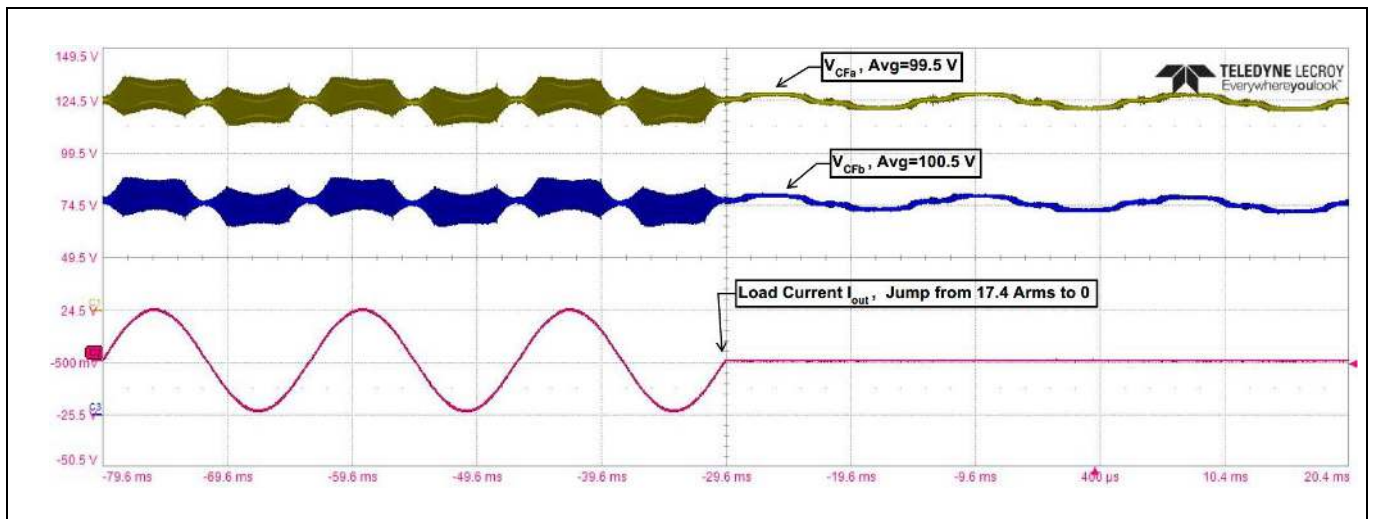
Figure 74   Output load current I_OUT and flying capacitor voltages when load steps from 4 kW to zero

10.2.4 Overload
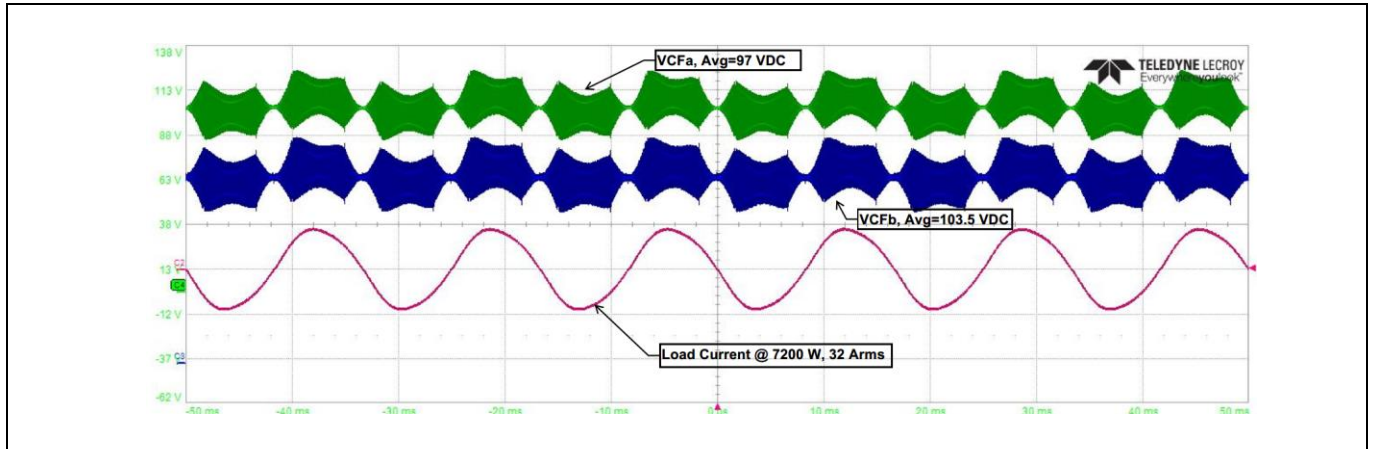
Figure 75 Output load current I$_{OUT}$ and flying capacitors voltages at overload condition 7.2 kW
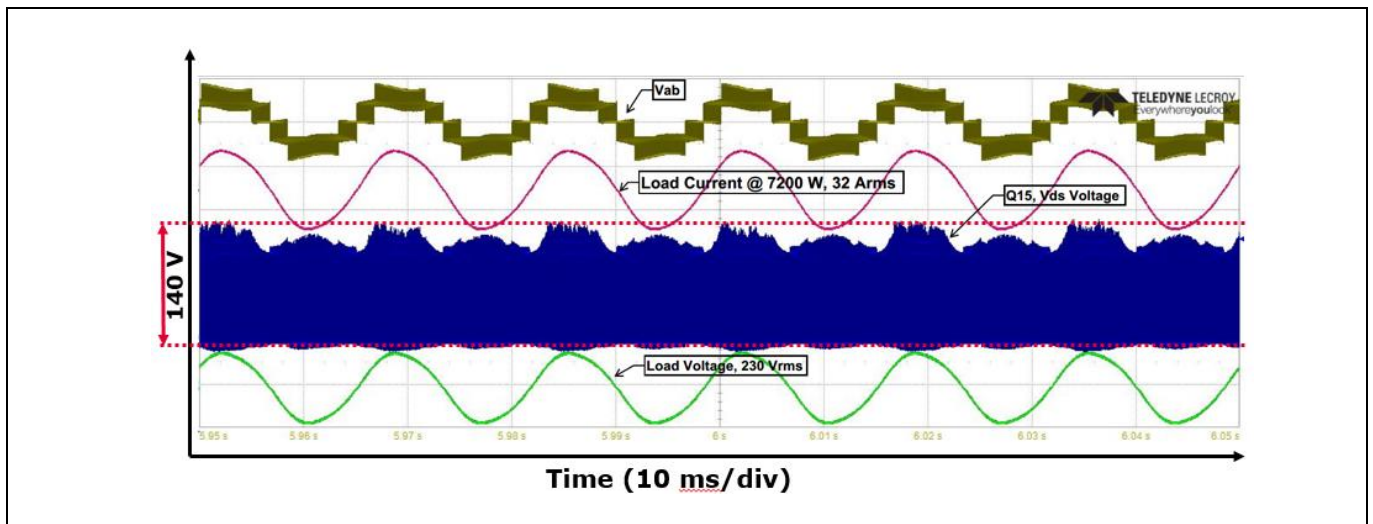
Figure 76 Output load current I$_{OUT}$, output load voltage V$_{out}$, phase-to-phase V$_{ab}$ voltage and Q15 drain-to-source voltage at overload condition 7.2 kW
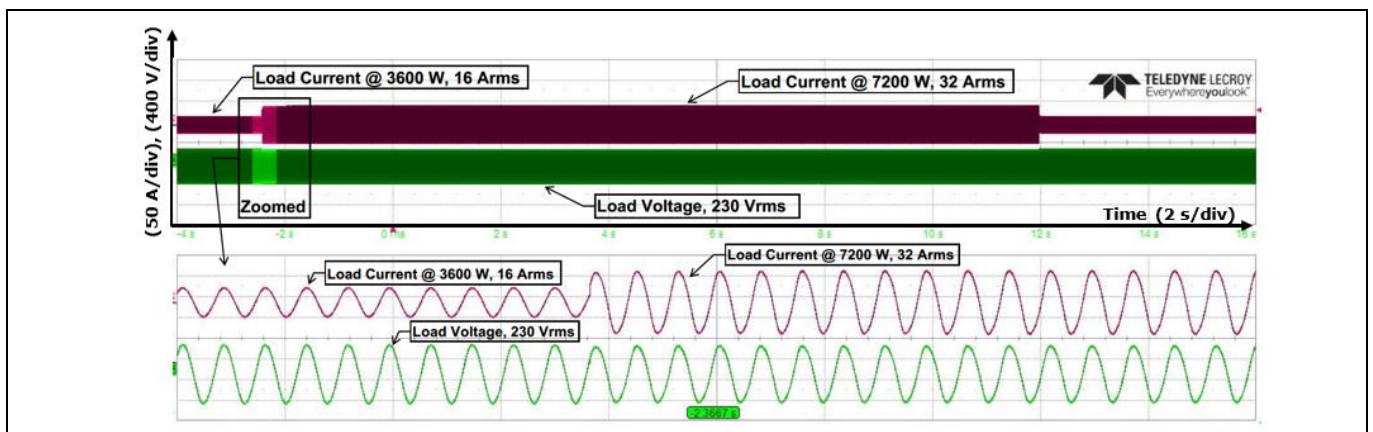
Figure 77 Output load current I$_{OUT}$, output load voltage V$_{out}$ when load steps from 3.6 kW to 7.2 kW for approximately 14 s

10.2.4.1 Non-unity power factor test result
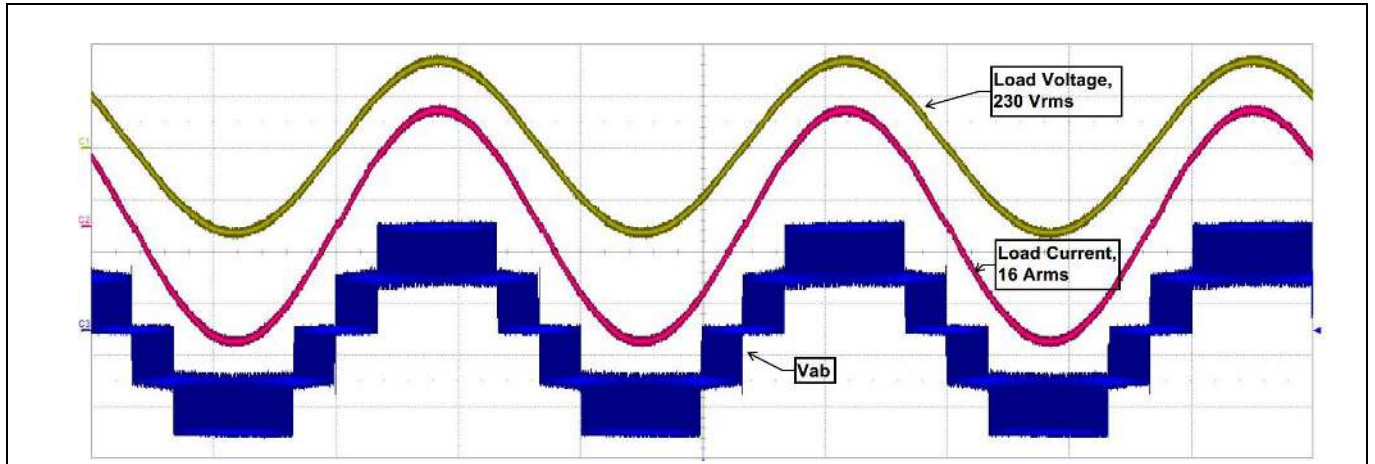
Figure 78   Output load voltage V_{out}, output load current I_{OUT}, phase-to-phase voltage V_{ab} at 3.7 kW
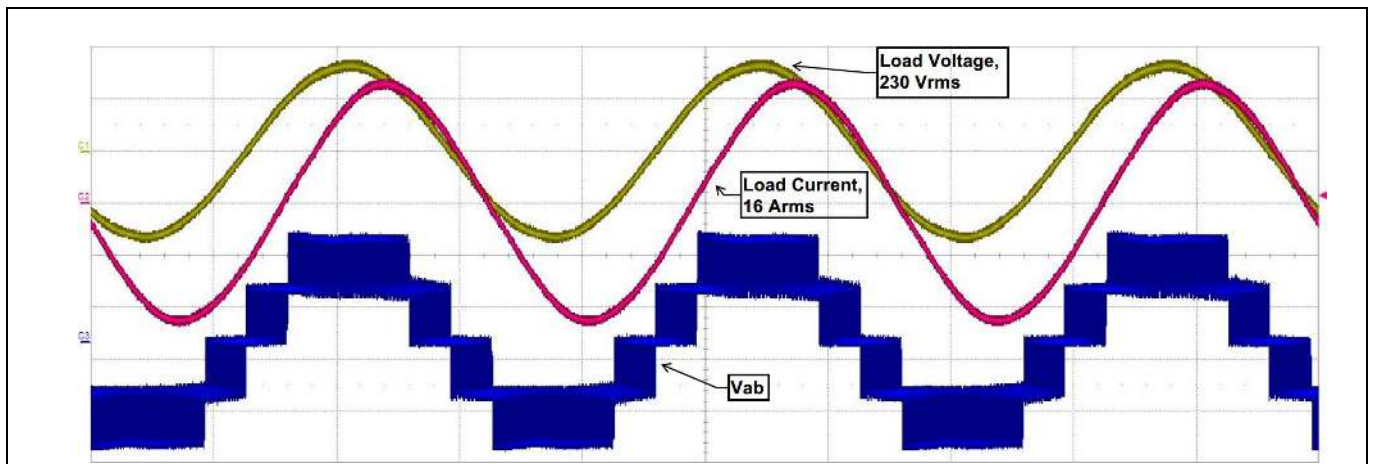
Figure 79   Output load voltage V_{out}, output load current I_{OUT}, phase-to-phase voltage V_{ab} at 3.7 kVA, power factor = 0.85

10.3 Thermal performance

10.3.1 Component temperatures at maximum load

The following results were obtained with no forced air cooling:
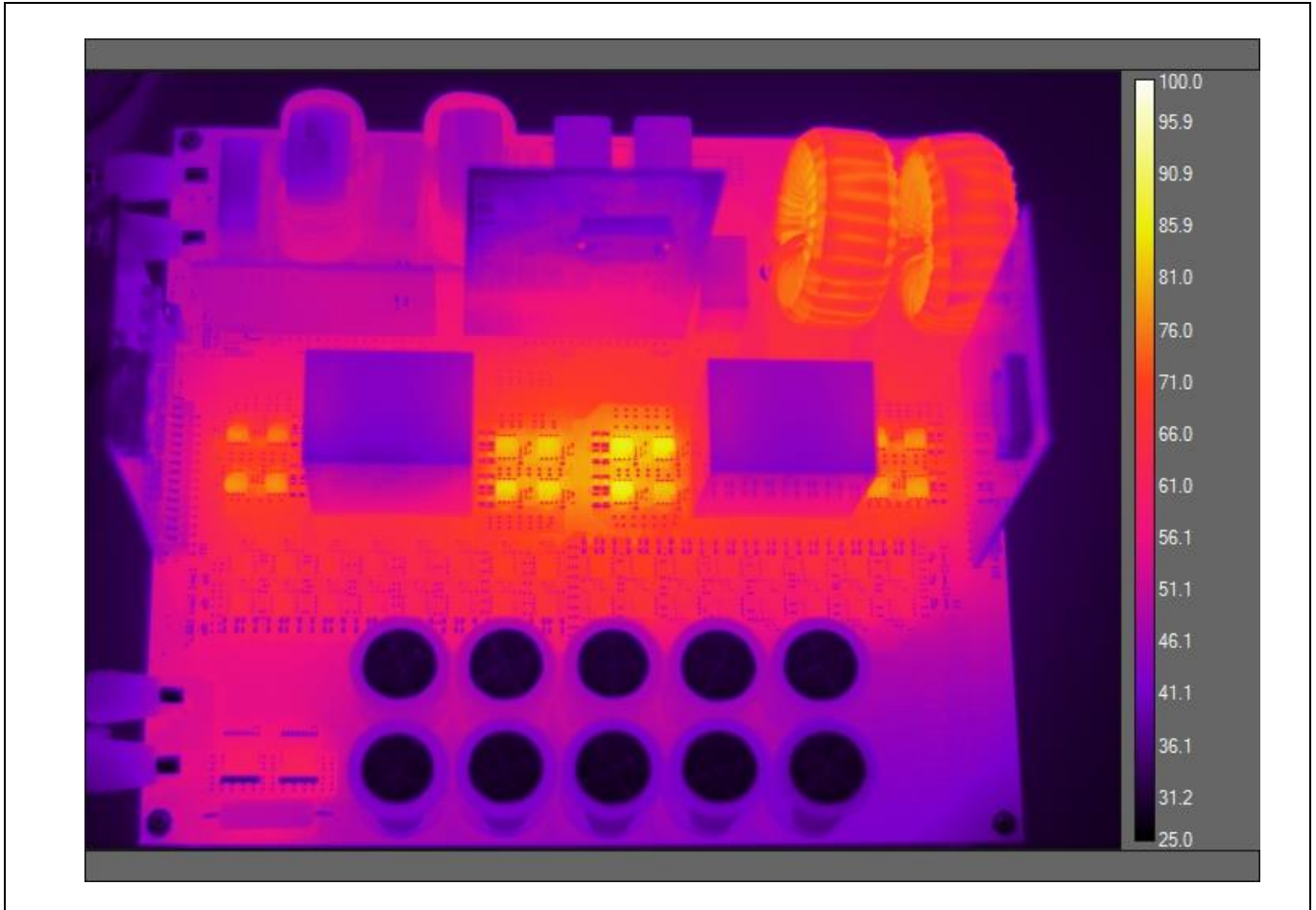
Figure 80   Top-side thermal image after 2 hours of operation at 400 V input and 4 kW load

10.3.2   Component temperature rise at twice maximum load
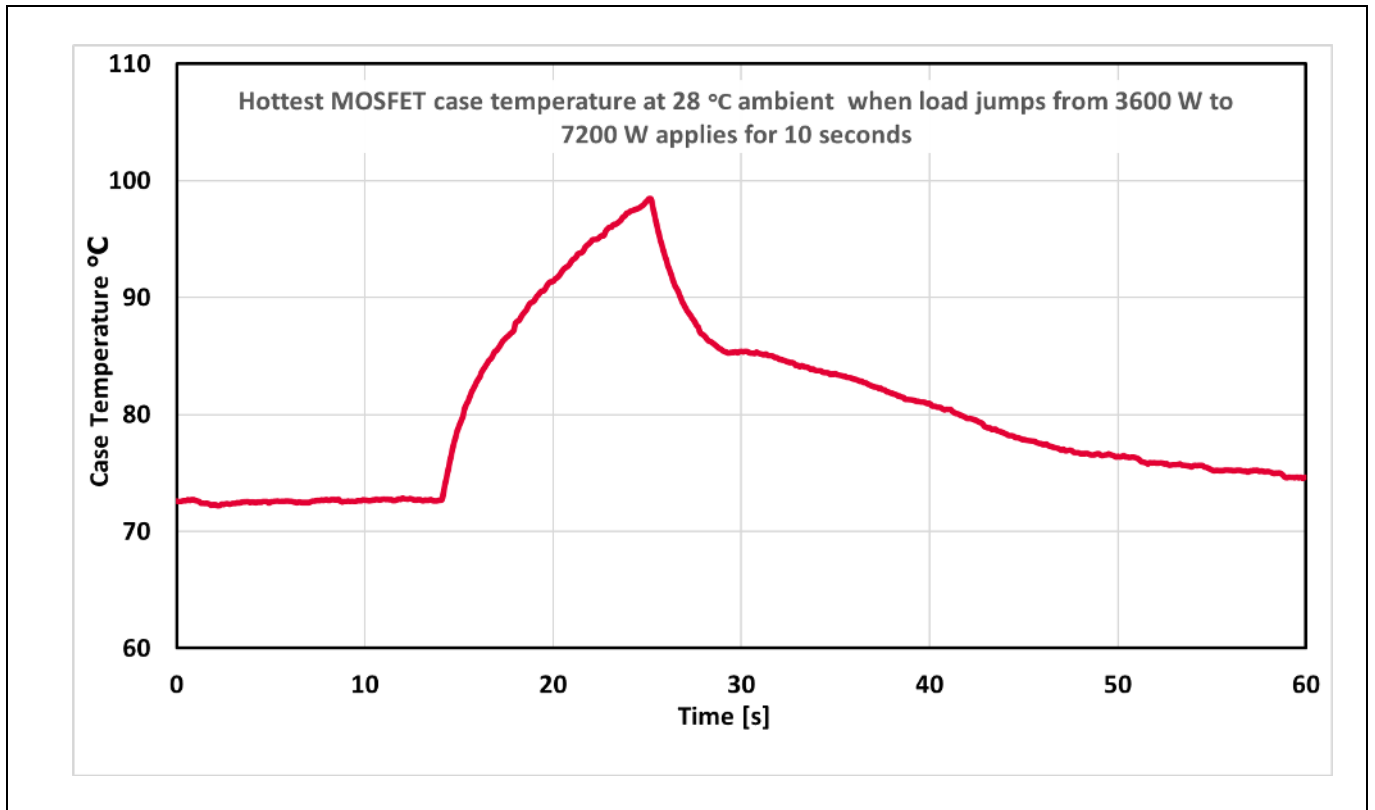
Figure 81   Temperature of the hottest MOSFET when 2 x full load is applied for 10 s

11 Conclusion

The five-level active neutral point clamped flying capacitor inverter design presented here demonstrates excellent efficiency over the load range, exceeding 98.7 percent from 500 W to 4000 W and peaking at 99.1 percent at 2000 W. The power losses are therefore approximately 50 W at full load, and around half the amount of this loss is semiconductor loss distributed over 48 MOSFETs over the area of the board. The system works at any power factor and the total harmonic distortion is under 5 percent at full load.

The RMS output voltages changes by less than 4 V from 500 W to 4 kW load in open-loop operation. This is due to the minimal losses in the system, which means that provided the input DC bus is regulated there is no need for closed-loop regulation in the inverter.

The thermal image shows that after operating at maximum load of 4 kW for two hours in open air with no forced air-cooling or heatsinking the component temperatures remained at safe operating levels, with the hottest MOSFETs not exceeding 80°C.

The inverter was also tested under an overload condition of around twice the maximum rated load for more than 14 s during which time it was able to operate without suffering any damage.

12　　References

[1] A Practical Study on Three-Level Hybrid SiC/Si Inverters – Fabio Brucchi, Klaus Sobe and Davide Chiola, Infineon Technologies

[2] A 5-Level Single Phase Flying Capacitor Multilevel Inverter – Sayli Khadse, Rohini Mendole, Amarjeet Pandey, Dept. of Electrical Engineering, S.B.J.I.T.M.R, Nagpur, Maharashtra, India

[3] Review of Multilevel Voltage Source Inverter Topologies and Analysis of Harmonics Distortions in FC-MLI – Ronak A. Rana (1), Sujal A. Patel (1), Anand Muthusamy (1), Chee woo Lee (2), Hee-Je Kim (2),
1. School of Electrical Engineering, Pusan National University, Busandaehak-ro 63 beongil 2, Busan 46241, Korea

2. Department of Electrical Engineering and Electrical Engineering Management, University of Technology Sydney, 15 Broadway Ultimo, Sydney, NSW 2007, Australia

[4] Alaa Hilal, Bernardo Cogo. Optimal inductor design and material selection for high power density inverters used in aircraft applications. International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS 2016), November 2016, Toulouse, France. ff10.1109/ESARS-ITEC.2016.7841359ff. ffhal-01532242f

[5] Infineon Technologies – XMC1300 AB-Step, XMC1000 family

[6] Texas Instruments – Design Guide: TIDM-HV-1PH-DCAC, Grid Connected Inverter Reference Design

[7] Arash Khoshkbar-Sadigh, Vahid Dargahi, Ketan Lakhera, Keith Corzine "Analytical Design of LC Filter Inductance for Two-Level Inverters Based on Maximum Ripple Current", IECON 2019 – 45th Annual Conference of the IEEE Industrial Electronics Society

[8] A.K. Sadigh, V. Dargahi, K.A. Corzine, "Analytical determination of conduction and switching power losses in flying-capacitor-based active neutral-point-clamped multilevel converter", IEEE Trans. Power Electron., vol. 31, no. 8, pp. 5473–5494, Aug. 2016

[9] J.A. Anderson, E.J. Hanak, L. Schrittwieser, M. Guacci, J.W. Kolar, G. Deboy, "All-silicon 99.35 percent efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter", CPSS Trans. Power Electron. Appl., vol. 4, no. 1, pp. 50–61, March 2019

[10] S. Abdel Rahman, Franz Stückler, Ken Siu, Infineon Technologies Application Note: "PFC boost converter design guide", February 2016

[11] Analog devices-LT8301 – Design Guide: 42 V_{IN} Micropower No-Opto Isolated Flyback Converter with 65 V/1.2 A Switch

13 Revision history

Document version	Date of release	Description of changes
V 1.0	25-06-2020	First release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.