

High-performance Regulator IC Series for PCs

100mA Linear Regulators for Note PC



BD35602F/HFN/HFV, BD35603F/HFN/HFV, BD35605F/HFN/HFV

●Description

BD3560□ series is a LDO regulator with output current 100mA. The output accuracy is ± 1% of output voltage. BD3560 □ series have some kinds of output voltage line-up and package line-up. Thus, it is used for the wide applications of digital appliances. Over current protection (for protecting the IC destruction by output short circuit), shutdown ON/OFF switch (for setting the circuit current 0 μA at shutdown mode), and thermal shutdown circuit (for protecting ICs from heat destruction by over load condition) are all built in.

●Features

- 1) Output current 100mA
- 2) Output voltage accuracy : ± 1%
- 3) Built-in Over Current Protection circuit (OCP)
- 4) Built-in Thermal Shut Down circuit (TSD)
- 5) With shut down switch
- 6) Rich package line-up : HVSO6, HSON8, SOP8

●Line-up

Product name	1.8V	5.0V	3.3V	Package
BD3560□HFV	○	○	○	HVSO6
BD3560□HFN	○	○	○	HSON8
BD3560□F	○	○	○	SOP8

Product name : BD3560□ □□□
↑ ↑
a b

Symbol			
a		b	
0□	Output Voltage (V)	□□□	Package
02	1.8V typ.	HFV	HVSO6
05	5.0V typ.	F	SOP8
03	3.3V typ.	HFN	HSON8

● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	Vcc	30.0 * ¹	V
EN Voltage	VEN	30.0	V
Power Dissipation	HVSOF6	Pd	mW
	HSON8		
	SOP8		
Operating Temperature Range	Topr	-10~+100	°C
Storage Temperature Range	Tstg	-55~+150	°C
Junction Temperature	Tjmax	+150	°C

*1 Not to exceed Pd

*2 Reduced by 6.8mW for each increase in Ta of 1°C over 25°C.

(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB.(copper foil area:100mm²))

*3 Reduced by 10.8mW for each increase in Ta of 1°C over 25°C.

(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB, 1 layer(copper foil density : 7%))

*4 Reduced by 5.52mW for each increase in Ta of 1°C over 25°C.(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB.)

● Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Max.	Unit
Input Power Supply Voltage	VCC	Vo+1.2	25	V
EN Voltage	VEN	-	25	V
Output Current	Io	-	100	mA

★This product should not be used in a radioactive environment.

● ELECTRICAL CHARACTERISTICS

BD3560□HFV/HFN/F (Unless otherwise noted, Ta=25°C, EN=3V, Vcc=16V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output Voltage 1	Vo1	Vo(T) × 0.99	Vo(T)	Vo(T) × 1.01	V	Io=0mA→100mA
Output Voltage 2	Vo2	Vo(T) × 0.985	Vo(T)	Vo(T) × 1.015	V	Tj=0 to 100°C Io=0mA→100mA
Circuit Current at shutdown mode	I _{sd}	-	0	1	μA	EN=0V, @OFF mode
Bias Current	I _{cc}	-	120	200	μA	
Output Current Ability	Io	100	-	-	mA	
Line Regulation	Reg.I	-	25	50	MV	Vcc=(Vo+1.2V)→25V, Io=100mA
EN Low Voltage	VEN (Low)	0	-	0.8	V	
EN High Voltage	VEN (High)	2.4	-	25	V	
EN Bias Current	I _{EN}	0.5	1.0	2.0	μA	

● Reference Data

BD35605HFN (Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{EN}=3\text{V}$, $V_{CC}=16\text{V}$)

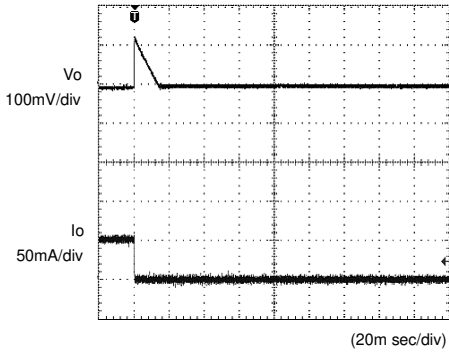


Fig.1 Transient Response
(50→0mA)
 $C_o=1\ \mu\text{F}$

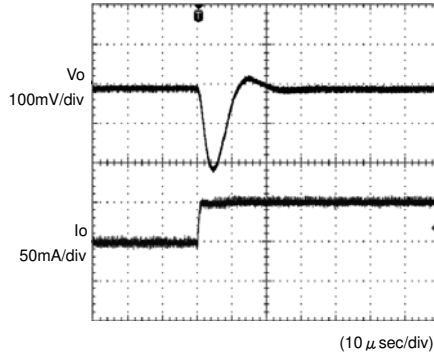


Fig.2 Transient Response
(0→50mA)
 $C_o=1\ \mu\text{F}$

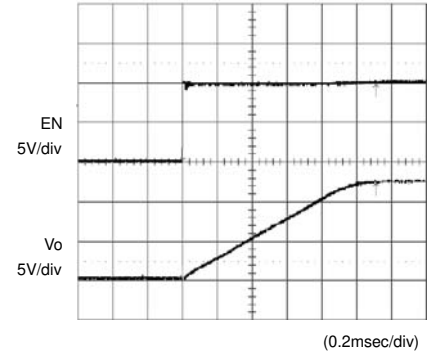


Fig.3 Waveform at output start
 $C_o=1\ \mu\text{F}$

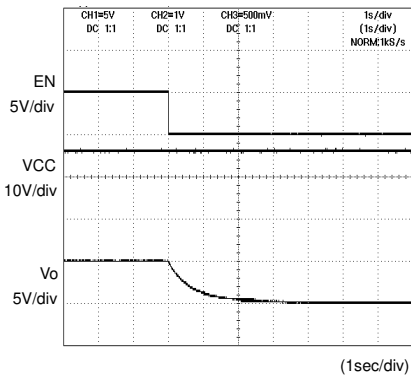


Fig.4 Waveform at output OFF
 $C_o=1\ \mu\text{F}$

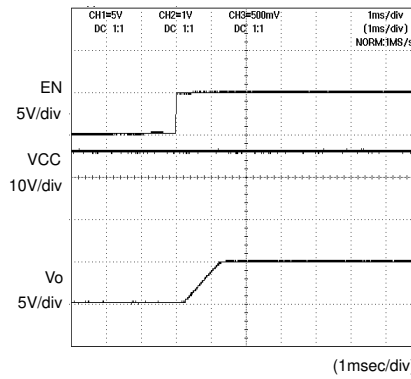


Fig.5 Input sequence 1
 $C_o=1\ \mu\text{F}$

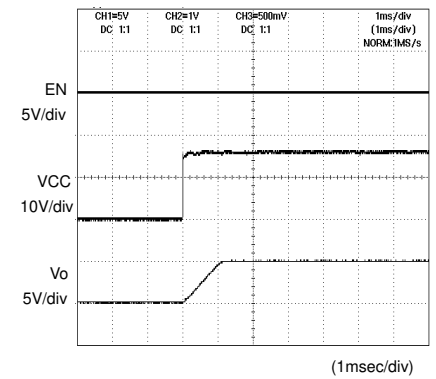


Fig.6 Input sequence 2
 $C_o=1\ \mu\text{F}$



Fig.7 T_a - V_o ($I_o=0\text{mA}$)

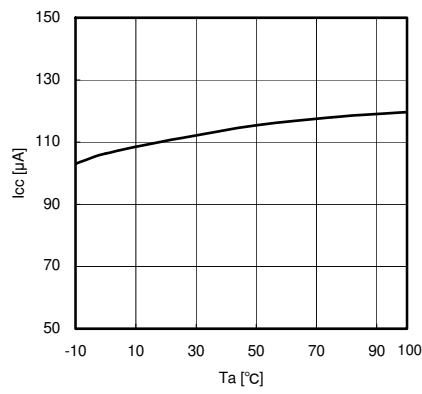


Fig.8 T_a - I_{cc}
($V_{EN}=12\text{V}$)

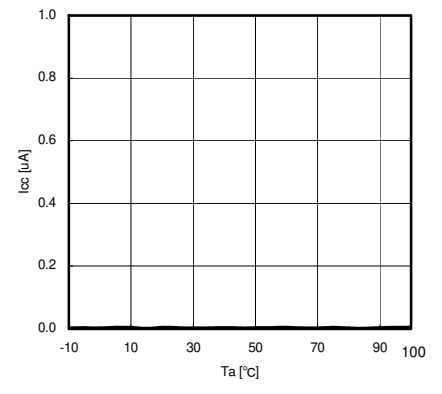


Fig.9 T_a - I_{cc}
($V_{CC}=16\text{V}$, $V_{EN}=0\text{V}$)

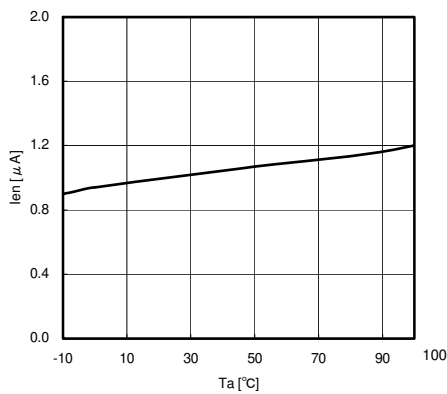


Fig.10 T_a - I_{EN}
($V_{CC}=16\text{V}$, $V_{EN}=3\text{V}$)

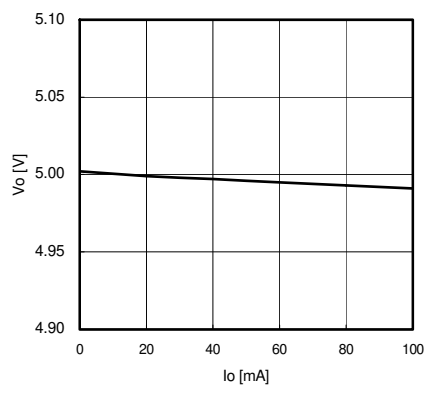


Fig.11 I_o - V_o
($V_{EN}=3\text{V}$)

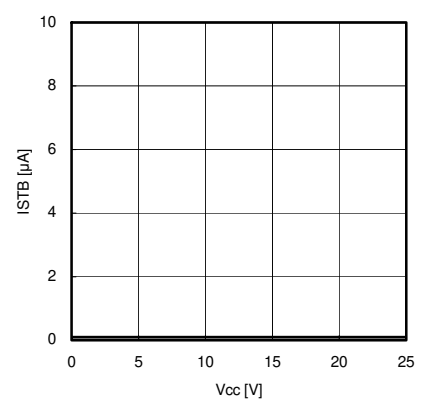


Fig.12 V_{CC} - I_{STB}

●Reference Data

BD35605HFN (Unless otherwise specified, Ta=25°C, EN=3V, Vcc=16V)

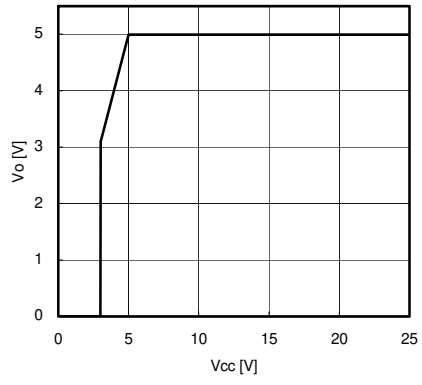
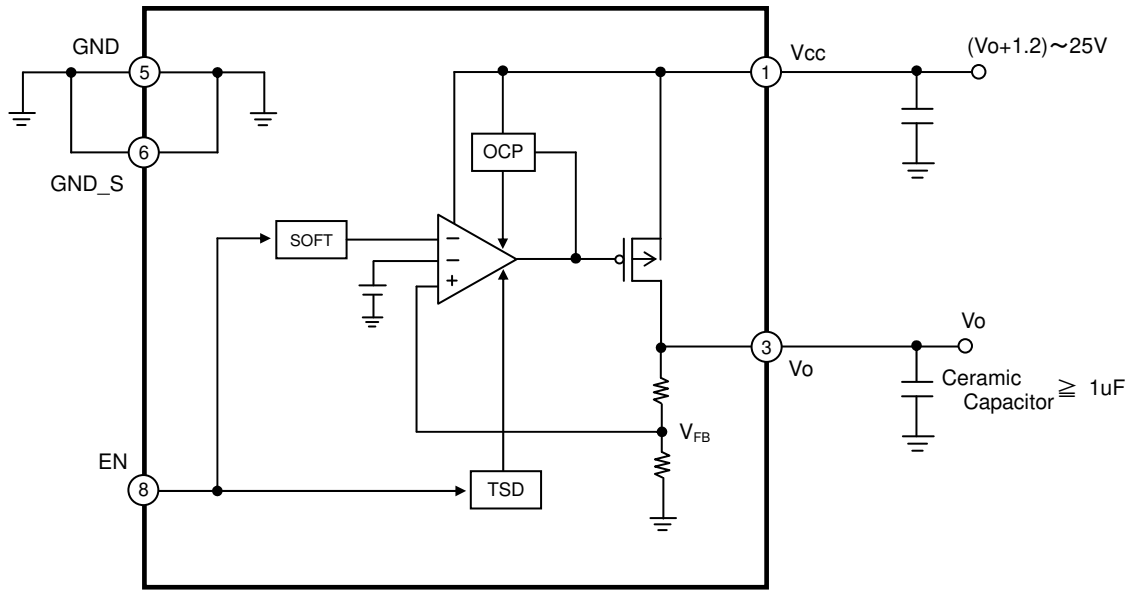


Fig.13 Vcc-Vo

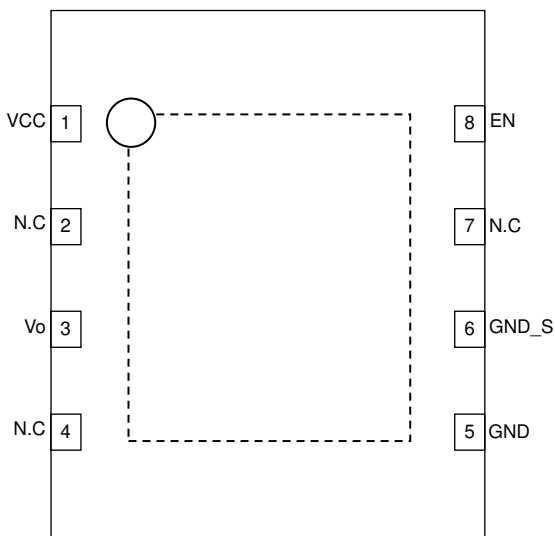
●Block Diagram (HSON8·SOP8)



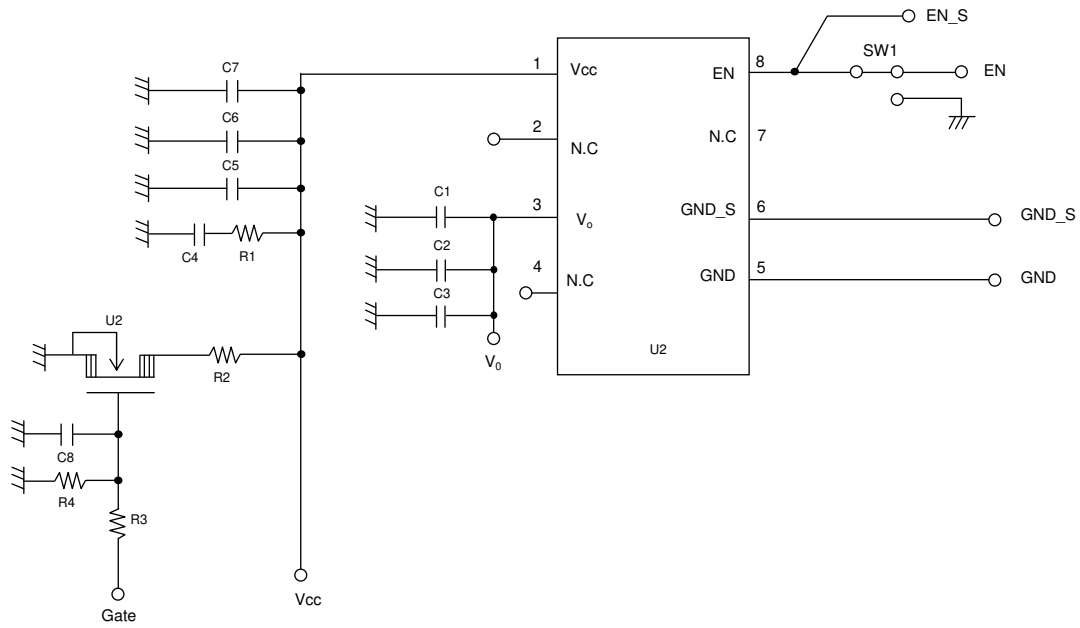
●Pin Function Table (HSON8·SOP8)

Pin No.	Pin Name	Pin Function
1	VCC	Input Voltage Pin
2	N.C.	Open
3	Vo	Output Voltage Pin
4	N.C.	Open
5	GND	GND Pin
6	GND_S	GND Sense Pin
7	N.C.	Open
8	EN	Enable Pin

●Pin Layout (HSON8·SOP8)



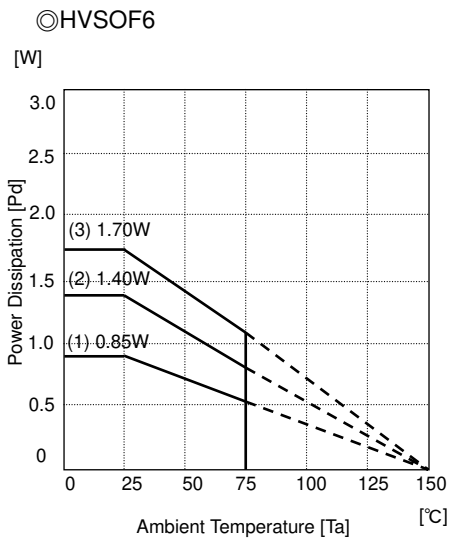
●Evaluation Board Circuit (Vo=3.3V)



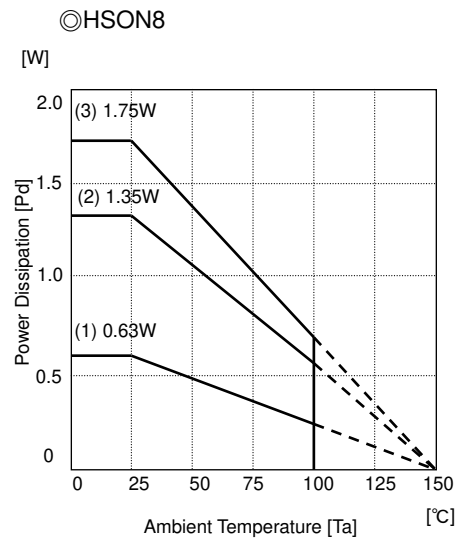
●Evaluation Board Parts List

Designation	Value	Part No.	Company
R1	-	-	-
R2	-	-	-
R3	-	-	-
R4	-	-	-
C1	-	-	-
C2	1uF	CM105B105K06A	KYOCERA
C3	-	-	-
C4	-	-	-
C5	-	-	-
C6	1uF	CM21X5R105K25A	KYOCERA
C7	-	-	-
C8	-	-	-
U1	-	BD3560XHFN	ROHM
U2	-	-	-

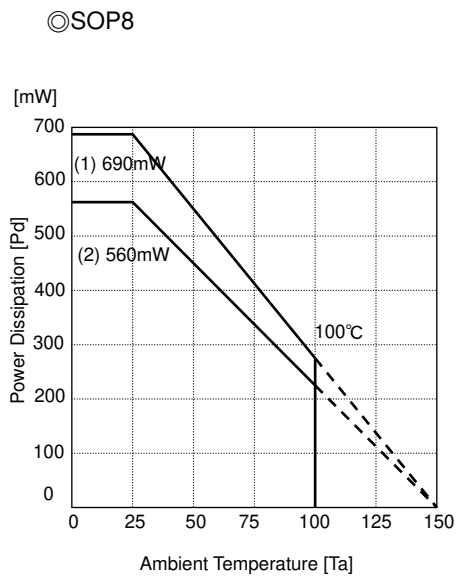
● Heat Dissipation Characteristics



PCB size : 70mm×70mm×1.6mm
 (1) 1 layer (Copper foil area : 100mm²)
 $\theta_{j-a}=147.1^{\circ}\text{C/W}$
 (2) 1 layer (Copper foil area : 90 mm²)
 $\theta_{j-a}=89.3^{\circ}\text{C/W}$
 (3) 1 layer (Copper foil area : 2500mm²)
 $\theta_{j-a}=73.5^{\circ}\text{C/W}$

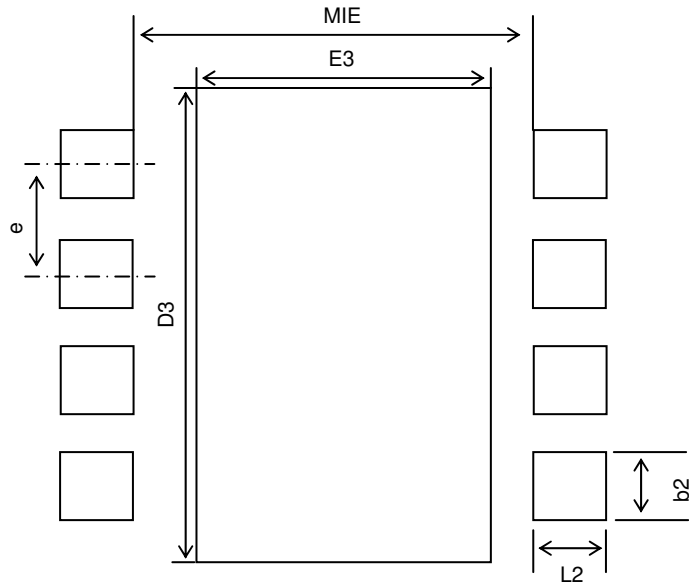


(1) 1 layer (copper foil area : less than 0.2%)
 $\theta_{j-a}=198.4^{\circ}\text{C/W}$
 (2) 1 layer (copper foil area : less than 7%)
 $\theta_{j-a}=92.4^{\circ}\text{C/W}$
 (3) 1 layer (copper foil area : less than 65%)
 $\theta_{j-a}=71.4^{\circ}\text{C/W}$



(1) 70mm×70mm×1.6mm Glass-epoxy PCB
 $\theta_{j-c}=181^{\circ}\text{C/W}$
 (2) With no heat sink
 $\theta_{j-a}=222^{\circ}\text{C/W}$

●Reference landing pattern



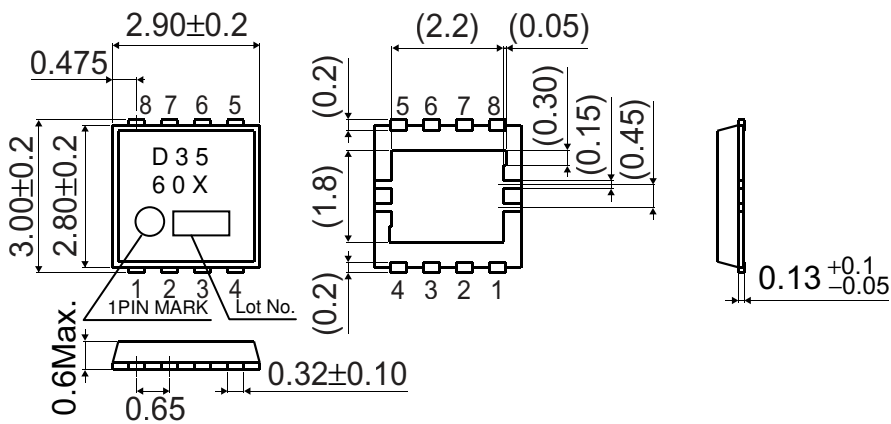
(Unit : mm)

Lead pitch	landing pitch	landing length	landing pitch
e	MIE	≥ 12	$b2$
0.65	2.50	0.40	0.35
central pad length	central pad pitch		
$D3$	$E3$		
2.90	1.90		

*It is recommended to design suitable for the actual application.

●Dimension

◎HSN8



(Unit : mm)

● Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
BD3560XHFV/HFN/F	175	15

10. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

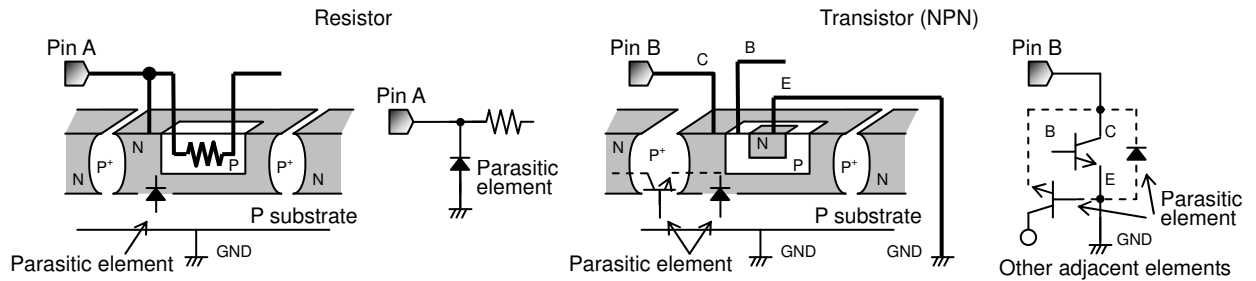
11. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

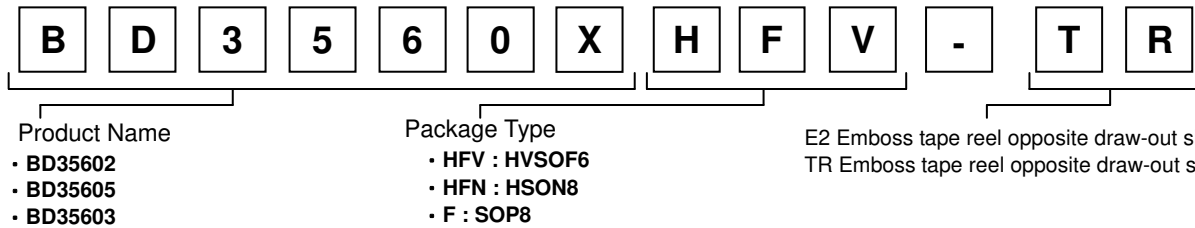
Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



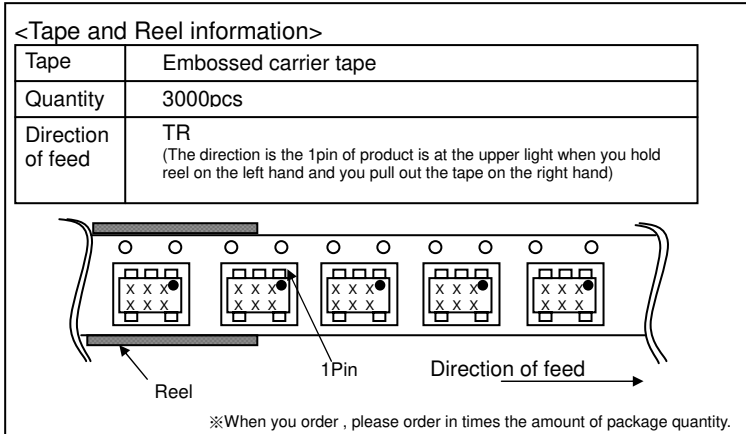
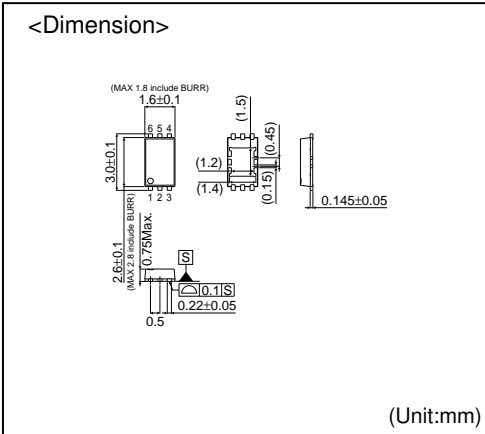
12. Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

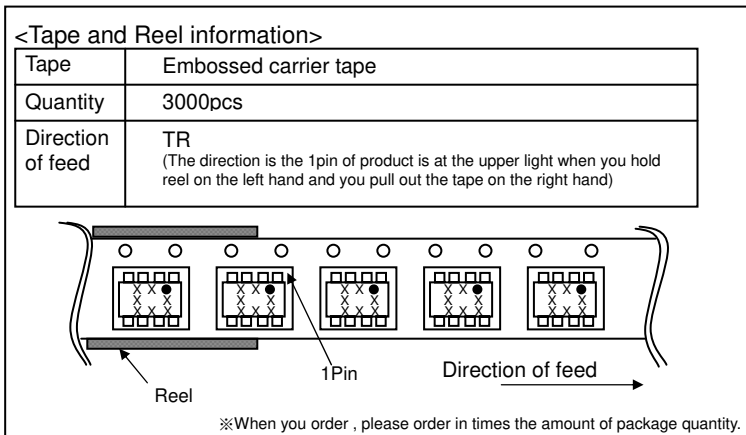
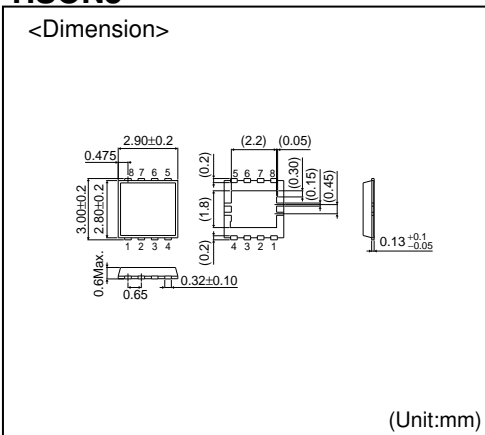
●Type Designations (Ordering Information)



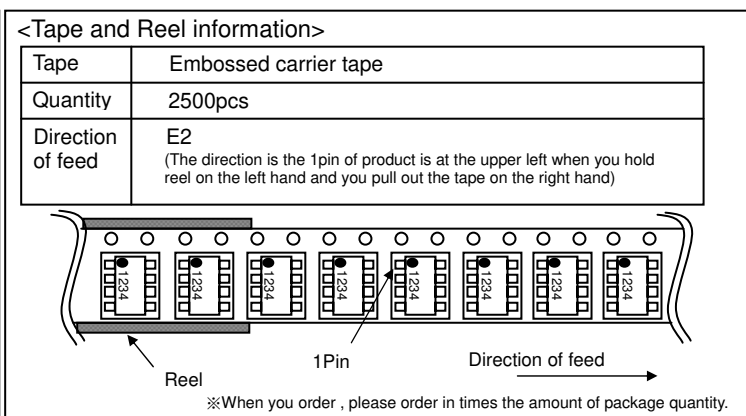
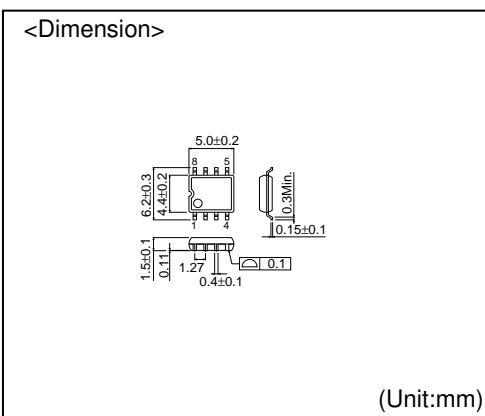
HVSOFF6



HSON8



SOP8



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