S-19518 Series

AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, 250 mA, BUILT-IN WINDOW WATCHDOG TIMER VOLTAGE REGULATOR WITH RESET FUNCTION

www.ablic.com

Rev.1.4_00

The S-19518 Series, developed by using high-withstand voltage CMOS technology, is a low dropout positive voltage regulator with the window watchdog timer and the reset function, which has high-withstand voltage. The monitoring time of watchdog timer can be adjusted by an external capacitor. Moreover, a voltage detection circuit which monitors the output voltage is also prepared.

ABLIC Inc. offers a "thermal simulation service" which supports the thermal design in conditions when our power management ICs are in use by customers. Our thermal simulation service will contribute to reducing the risk in the thermal design at customers' development stage.
ABLIC Inc. also offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
Contact our sales representatives for details.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

Regulator block

- Output voltage: 3.3 V, 5.0 V
- Input voltage: 3.0 V to 36.0 V
- Output voltage accuracy: ±2.0% (T_j = −40°C to +150°C)
- Dropout voltage: 100 mV typ. (5.0 V output product, I_{OUT} = 100 mA)
- Output current: Possible to output 250 mA (V_{IN} = $V_{OUT(S)}$ + 1.0 V)*1
- Input and output capacitors: A ceramic capacitor of 1.0 μF or more can be used.
- Built-in overcurrent protection circuit: Limits overcurrent of output transistor.
- Built-in thermal shutdown circuit: Detection temperature 170°C typ.
- Built-in ON / OFF circuit: Ensures long battery life.

Detector block

- Detection voltage: 2.6 V to 4.7 V, selectable in 0.1 V step
- Detection voltage accuracy: ±2.0% (T_j = −40°C to +150°C)
- Hysteresis width: 0.12 V min.
- Release delay time is adjustable*2: 20 ms typ. (C_{DLY} = 10 nF)

Watchdog timer block

- Watchdog activation current: 1.5 mA typ.
- Watchdog trigger time is adjustable*2: 46 ms typ. (C_{DLY} = 10 nF)
- Autonomous watchdog operation function: Watchdog timer operates due to detection of load current.
- Watchdog mode: Window mode

Overall

- Current consumption: 3.2 μA typ. (During regulator operation, during watchdog timer deactivation)
  0.1 μA typ. (During regulator stop)
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*3

***1.** Please make sure that the loss of the IC will not exceed the power dissipation when the output current is large.
***2.** The release delay time and the watchdog trigger time can be adjusted by connecting C_{DLY} to the DLY pin.
***3.** Contact our sales representatives for details.

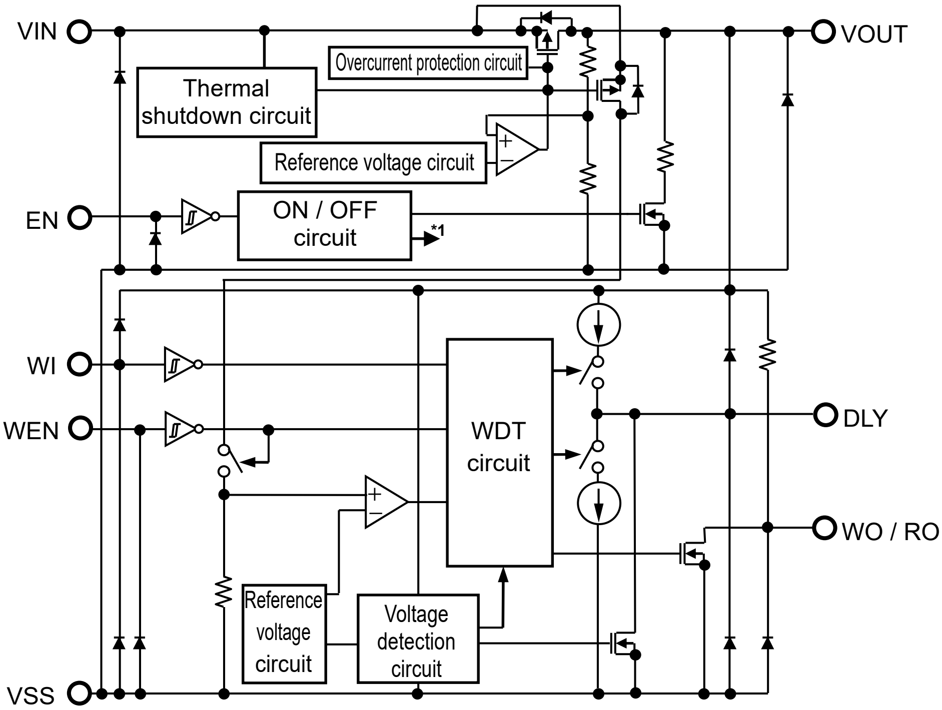
■ Applications

- Constant-voltage power supply for automotive electric component, monitoring of microcontroller

■ Packages

- TO-252-9S
- HSOP-8A

■ Block Diagram



***1.** The ON / OFF circuit controls the internal circuit and the output transistor.

Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for the operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-19518 A x x A - xxxx U 4

- U — Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- xxxx — Package abbreviation and IC packing specifications*1
  - V9T1: TO-252-9S, Tape
  - E8T1: HSOP-8A, Tape
- A — Operation temperature
  - A: Ta = −40°C to +125°C
- x (second) — Detection voltage*2
  - J to Z, 0 to 5
- x (first) — Output voltage*2
  - F, Y

***1.** Refer to the tape drawing.
***2.** Refer to "**2. Product option list**".

2. Product option list

Table 1 Output Voltage

Set Output Voltage	Symbol
5.0 V	F
3.3 V	Y

Table 2 Detection Voltage

Set Detection Voltage	Symbol	Set Detection Voltage	Symbol
4.7 V	J	3.6 V	V
4.6 V	K	3.5 V	W
4.5 V	L	3.4 V	X
4.4 V	M	3.3 V	Y
4.3 V	N	3.2 V	Z
4.2 V	P	3.1 V	0
4.1 V	Q	3.0 V	1
4.0 V	R	2.9 V	2
3.9 V	S	2.8 V	3
3.8 V	T	2.7 V	4
3.7 V	U	2.6 V	5

Remark Set output voltage ≥ Set detection voltage + 0.3 V

3. Packages

Table 3 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TO-252-9S	VA009-A-P-SD	VA009-A-C-SD	VA009-A-R-SD	VA009-A-L-SD
HSOP-8A	FH008-A-P-SD	FH008-A-C-SD	FH008-A-R-SD	FH008-A-L-SD

4. Product name list

Table 4

Output Voltage (V_{OUT})	Detection Voltage ($-V_{DET}$)	TO-252-9S	HSOP-8A
3.3 V ± 2.0%	2.8 V ± 2.0%	S-19518AY3A-V9T1U4	S-19518AY3A-E8T1U4
3.3 V ± 2.0%	2.9 V ± 2.0%	S-19518AY2A-V9T1U4	S-19518AY2A-E8T1U4
3.3 V ± 2.0%	3.0 V ± 2.0%	S-19518AY1A-V9T1U4	S-19518AY1A-E8T1U4
5.0 V ± 2.0%	4.2 V ± 2.0%	S-19518AFPA-V9T1U4	S-19518AFPA-E8T1U4
5.0 V ± 2.0%	4.6 V ± 2.0%	S-19518AFKA-V9T1U4	S-19518AFKA-E8T1U4

Remark Please contact our sales representatives for products other than the above.

■ Pin Configurations

1. TO-252-9S

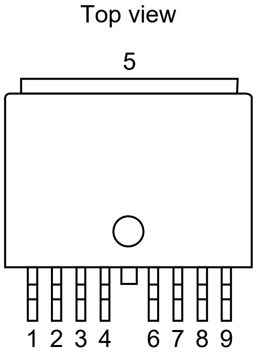


Figure 2

Table 5

Pin No.	Symbol	Description	
1	VOUT	Voltage output pin (Regulator block)	
2	WEN	Watchdog enable pin	
3	DLY	Connection pin for release delay time and monitoring time adjustment capacitor	
4	NC*1	No connection	
5	VSS	GND pin	
6	WO / RO*2	WO	Watchdog output pin
		RO	Reset output pin
7	WI	Watchdog input pin	
8	EN	Enable pin	
9	VIN	Voltage input pin (Regulator block)	

***1.** The NC pin is electrically open.
The NC pin can be connected to the VIN pin or the VSS pin.
***2.** The WO / RO pin combines the watchdog output pin and the reset output pin.

2. HSOP-8A

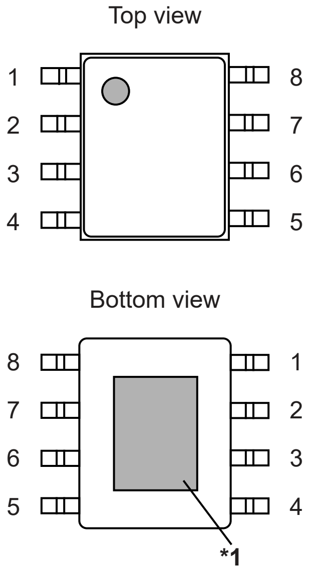


Figure 3

Table 6

Pin No.	Symbol	Description	
1	VOUT	Voltage output pin (Regulator block)	
2	WEN	Watchdog enable pin	
3	VSS	GND pin	
4	DLY	Connection pin for release delay time and monitoring time adjustment capacitor	
5	WO / RO*2	WO	Watchdog output pin
		RO	Reset output pin
6	WI	Watchdog input pin	
7	EN	Enable pin	
8	VIN	Voltage input pin (Regulator block)	

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.
***2.** The WO / RO pin combines the watchdog output pin and the reset output pin.

■ Absolute Maximum Ratings

Table 7

(T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
VIN pin voltage	V_{IN}	V_{SS} – 0.3 to V_{SS} + 45.0	V
EN pin voltage	V_{EN}	V_{SS} – 0.3 to V_{SS} + 45.0	V
VOUT pin voltage	V_{OUT}	V_{SS} – 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7.0	V
DLY pin voltage	V_{DLY}	V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
WEN pin voltage	V_{WEN}	V_{SS} – 0.3 to V_{SS} + 7.0	V
WI pin voltage	V_{WI}	V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
WO / RO pin voltage	$V_{WO / RO}$	V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
Output current	I_{OUT}	325	mA
	$I_{WO / RO}$	30	mA
Junction temperature	T_j	–40 to +150	°C
Operation ambient temperature	T_{opr}	–40 to +125	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

■ Thermal Resistance Value

Table 8

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1, *2	θ_{JA}	TO-252-9S	Board A	–	84	–	°C/W
			Board B	–	–	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	24	–	°C/W
		HSOP-8A	Board A	–	105	–	°C/W
			Board B	–	–	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	31	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A
***2.** Measurement values when this IC is mounted on each board

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Recommended Operation Conditions

Table 9

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VIN pin voltage	V_{IN}	–	3.0	–	36.0	V
		Autonomous watchdog operation function*1	$V_{OUT(S)}$ + 1.0	–	36.0	V
EN pin voltage	V_{EN}	–	0	–	V_{IN}	V
WEN pin voltage	V_{WEN}	–	0	–	V_{OUT}	V
WI pin voltage	V_{WI}	–	0	–	V_{OUT}	V
Watchdog input "H" time*2	t_{high}	–	5.0	–	–	μs
Watchdog input "L" time*2	t_{low}	–	5.0	–	–	μs
Watchdog input frequency*2	f_{WI}	Duty ratio 50%	–	–	0.2	MHz
Input capacitance	C_{IN}	–	1.0	–	–	μF
Output capacitance	C_L	–	1.0	–	–	μF
Equivalent series resistance	R_{ESR}	Output capacitor (C_L)	–	–	100	Ω
Release delay time and monitoring time adjustment capacitance*3	C_{DLY}	–	1	10	–	nF
External pull-up resistance for output pin	R_{extR}	Connected to WO / RO pin	3	–	–	kΩ

***1.** Refer to "**3. Watchdog timer block**" in "**■ Operation**" for the autonomous watchdog operation function.
***2.** When inputting a rising edge that satisfies the condition of **Figure 4** to the WI pin, the watchdog timer detects a trigger.
The signal input from the monitored object by the watchdog timer should satisfy the condition of **Figure 4**.
***3.** Refer to "**2. Release delay time and monitoring time adjustment capacitor (C_{DLY})**" in "**■ Selection of External Parts**" for the details.

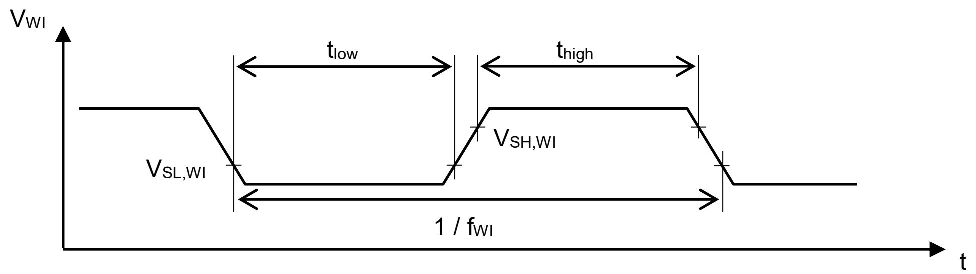


Figure 4

Caution **Generally a series regulator may cause oscillation, depending on the selection of external parts. Confirm that no oscillation occurs in the actual application using capacitors that meet the above C_{IN}, C_L, and R_{ESR}.**

■ Electrical Characteristics

1. Regulator block

Table 10

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Output voltage*1	$V_{OUT(E)}$	$V_{OUT(S)}$ + 1.0 V ≤ V_{IN} ≤ 18.0 V, 1 mA ≤ I_{OUT} ≤ 100 mA		$V_{OUT(S)}$ − 2.0%	$V_{OUT(S)}$	$V_{OUT(S)}$ + 2.0%	V	1
Output current*2	I_{OUT}	V_{IN} ≥ $V_{OUT(S)}$ + 1.0 V		250*7	−	−	mA	2
Dropout voltage*3	V_{drop}	I_{OUT} = 100 mA	$V_{OUT(S)}$ = 3.3 V	−	120	240	mV	1
			$V_{OUT(S)}$ = 5.0 V	−	100	200	mV	1
		I_{OUT} = 250 mA	$V_{OUT(S)}$ = 3.3 V	−	300	600	mV	1
			$V_{OUT(S)}$ = 5.0 V	−	250	500	mV	1
Line regulation*4	$\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}$	$V_{OUT(S)}$ + 1.0 V ≤ V_{IN} ≤ 36.0 V, I_{OUT} = 1 mA		−	0.01	0.02	%/V	1
Load regulation*5	ΔV_{OUT2}	V_{IN} = $V_{OUT(S)}$ + 1.0 V, 1 mA ≤ I_{OUT} ≤ 250 mA, Ta = +25°C		−	10	50	mV	1
Input voltage	V_{IN}	−		3.0	−	36.0	V	−
EN pin input voltage "H"	$V_{SH,EN}$	−		2	−	−	V	4
EN pin input voltage "L"	$V_{SL,EN}$	−		−	−	0.8	V	4
EN pin input current "H"	$I_{SH,EN}$	V_{EN} = V_{IN}		−	−	1	μA	4
EN pin input current "L"	$I_{SL,EN}$	V_{EN} = 0 V		−	−	0.1	μA	4
Ripple rejection	|RR|	V_{IN} = 13.5 V, I_{OUT} = 30 mA, f = 100 Hz, ΔV_{rip} = 1.0 V_{p-p}	$V_{OUT(S)}$ = 3.3 V	−	65	−	dB	3
			$V_{OUT(S)}$ = 5.0 V	−	60	−	dB	3
Limit current*6	I_{LIM}	V_{IN} = $V_{OUT(S)}$ + 1.0 V, Ta = +25°C		250	450	650	mA	2
Short-circuit current	I_{short}	V_{IN} = 13.5 V, V_{OUT} = 0 V, Ta = +25°C		40	80	120	mA	2
Thermal shutdown detection temperature	T_{SD}	Junction temperature		−	170	−	°C	−
Thermal shutdown release temperature	T_{SR}	Junction temperature		−	135	−	°C	−

***1.** The accuracy is guaranteed when the input voltage, output current, and temperature satisfy the conditions listed above.
$V_{OUT(S)}$: Set output voltage
$V_{OUT(E)}$: Actual output voltage

***2.** The output current when increasing the output current gradually until the output voltage has reached the value of 95% of $V_{OUT(E)}$.

***3.** The difference between input voltage (V_{IN1}) and the output voltage when decreasing input voltage (V_{IN}) gradually until the output voltage has dropped out to the value of 98% of output voltage (V_{OUT3}).
V_{drop}: V_{IN1} − (V_{OUT3} × 0.98)
V_{OUT3}: Output voltage when V_{IN} = $V_{OUT(S)}$ + 1.0 V

***4.** The dependency of the output voltage against the input voltage. The value shows how much the output voltage changes due to a change in the input voltage while keeping output current constant.

***5.** The dependency of the output voltage against the output current. The value shows how much the output voltage changes due to a change in the output current while keeping input voltage constant.

***6.** The current limited by overcurrent protection circuit.

***7.** Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large.
This specification is guaranteed by design.

2. Detector block

Table 11

(T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	–	$-V_{DET(S)}$ − 2.0%	$-V_{DET(S)}$	$-V_{DET(S)}$ + 2.0%	V	5
Hysteresis width*2	V_{HYS}	–	120	150	180	mV	5
Reset output voltage "H"	V_{ROH}	–	$V_{OUT(S)}$ × 0.9	–	–	V	5
Reset output voltage "L"	V_{ROL}	V_{OUT} ≥ 1.0 V, R_{extR} ≥ 3 kΩ, Connected to VOUT pin	–	0.2	0.4	V	5
Reset pull-up resistance	R_{RO}	VOUT pin internal resistance, V_{OUT} ≥ $+V_{DET}$	20	30	45	kΩ	–
Reset output current	I_{RO}	V_{RO} = 0.4 V, V_{OUT} = $-V_{DET(S)}$ × 0.95	3.0	–	–	mA	6
Release delay time*3	t_{rd}	C_{DLY} = 10 nF	16	20	24	ms	5
Reset reaction time*4	t_{rr}	–	–	–	200	μs	5

***1.** The VOUT pin voltage at which the output of the RO pin switches from "H" to "L".
$-V_{DET(S)}$: Set detection voltage
$-V_{DET}$: Actual detection voltage

***2.** The voltage difference between the detection voltage ($-V_{DET}$) and the release voltage ($+V_{DET}$). The relation between the actual output voltage ($V_{OUT(E)}$) of the regulator block and the actual release voltage ($+V_{DET} = -V_{DET} + V_{HYS}$) of the detector block is as follows.
$V_{OUT(E)} > +V_{DET}$

***3.** The time from when V_{OUT} exceeds $+V_{DET}$ to when the RO pin output inverts (Refer to **Figure 5**). This value changes according to the release delay time and monitoring time adjustment capacitor (C_{DLY}).
The time period from when V_{OUT} changes to $+V_{DET} \rightarrow V_{DET(S)}$ to when V_{RO} reaches V_{OUT} / 2.

***4.** The time from when V_{OUT} falls below $-V_{DET}$ to when the RO pin output inverts (Refer to **Figure 6**). The time period from when V_{OUT} changes to $V_{OUT(S)} \rightarrow -V_{DET}$ to when V_{RO} reaches V_{OUT} / 2.

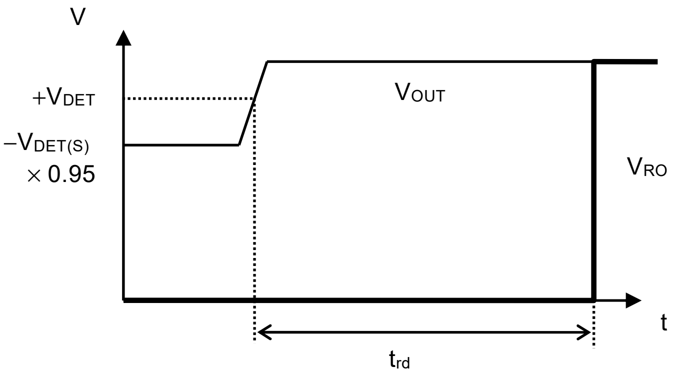


Figure 5 Release Delay Time

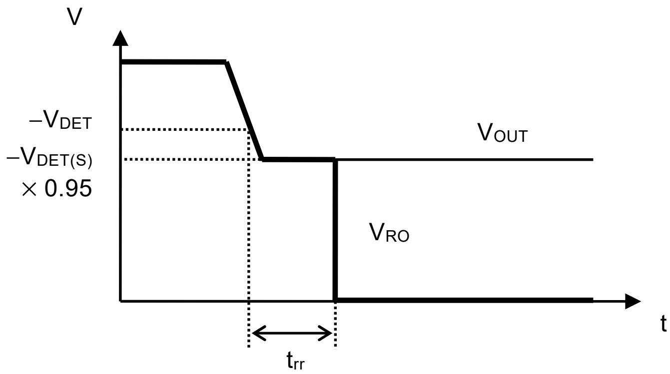


Figure 6 Reset Reaction Time

3. Watchdog timer block

Table 12

(V_{IN} = 13.5 V, T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Watchdog activation threshold current	$I_{O,WDact}$	–	–	1.5	1.9	mA	9
Watchdog deactivation threshold current	$I_{O,WDdeact}$	–	0.85	1.25	–	mA	9
WI pin input voltage "H"	$V_{SH,WI}$	–	$V_{OUT(S)}$ × 0.7	–	–	V	7
WI pin input voltage "L"	$V_{SL,WI}$	–	–	–	$V_{OUT(S)}$ × 0.3	V	7
WI pin input current "H"	$I_{SH,WI}$	$V_{WI} = V_{OUT(S)}$	–	–	1	μA	7
WI pin input current "L"	$I_{SL,WI}$	V_{WI} = 0 V	–	–	0.1	μA	7
WEN pin input voltage "H"	$V_{SH,WEN}$	–	2	–	–	V	8
WEN pin input voltage "L"	$V_{SL,WEN}$	–	–	–	0.8	V	8
WEN pin input curernt "H"	$I_{SH,WEN}$	$V_{WEN} = V_{OUT(S)}$	–	–	1	μA	8
WEN pin input current "L"	$I_{SL,WEN}$	V_{WEN} = 0 V	–	–	0.1	μA	8
Watchdog output "L" time*1	$t_{WD,L}$	C_{DLY} = 10 nF	9.2	11.5	13.8	ms	9
Watchdog trigger time*2	$t_{WI,tr}$	C_{DLY} = 10 nF	39.1	46	52.9	ms	9
Watchdog double-pulse detection time*3	$t_{WI,dp}$	C_{DLY} = 10 nF	9.2	11.5	13.8	ms	9

***1.** The time when the WO / RO pin continues "L" after the watchdog timer detects a time-out or double-pulse (Refer to **Figure 7**). This value changes according to C_{DLY}.

***2.** The time from when the watchdog timer initiates the detection of a trigger signal to when a time-out is detected and the WO / RO pin output changes to "L" (Refer to **Figure 7**). This value changes according to C_{DLY}.

***3.** The time from when the watchdog timer initiates the detection of a trigger signal to when a trigger is detected again before $t_{WI,dp}$ elapses and the WO / RO pin output changes to "L" (Refer to **Figure 8**). This value changes according to C_{DLY}.

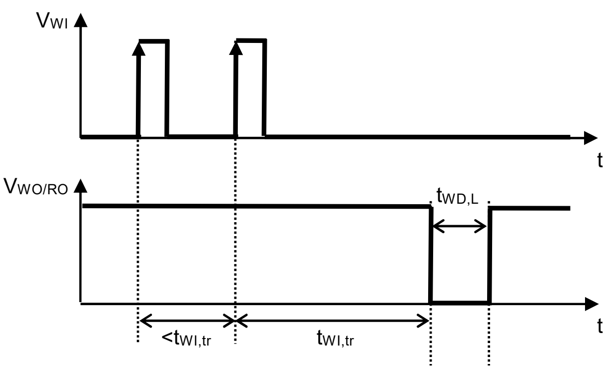


Figure 7 Watchdog Trigger Time

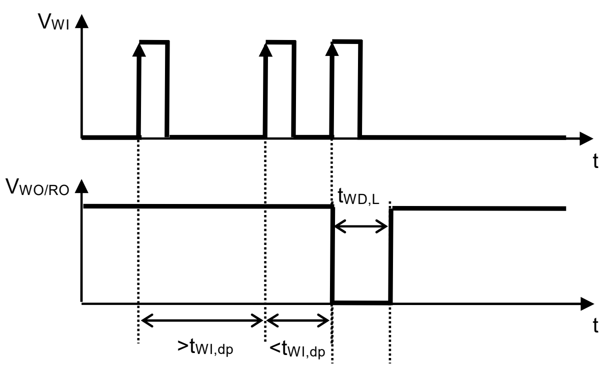


Figure 8 Watchdog Double-pulse Detection Time

4. Overall

Table 13

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption during operation	I_{SS1}	V_{EN} = V_{IN}, I_{OUT} ≤ 10 μA, during watchdog timer deactivation	−	3.2	9.8	μA	9
		V_{EN} = V_{IN}, I_{OUT} ≤ 2.5 mA, during watchdog timer activation, WO / RO pin = "H"	−	8.4	18	μA	9
Current consumption during power-off	I_{SS2}	V_{EN} = 0 V, I_{OUT} = 0 mA	−	0.1	4.0	μA	10

■ Test Circuits

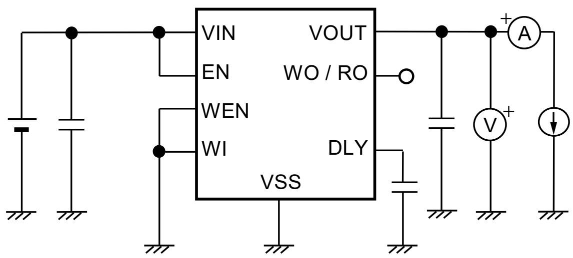


Figure 9 Test Circuit 1

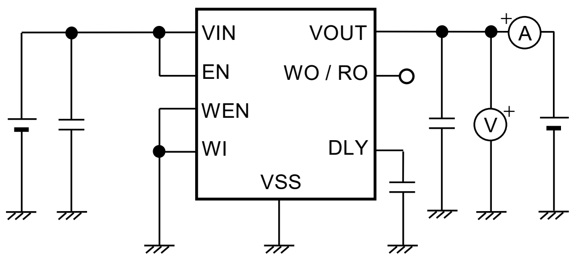


Figure 10 Test Circuit 2

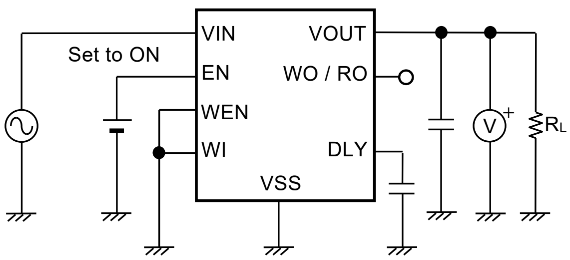


Figure 11 Test Circuit 3

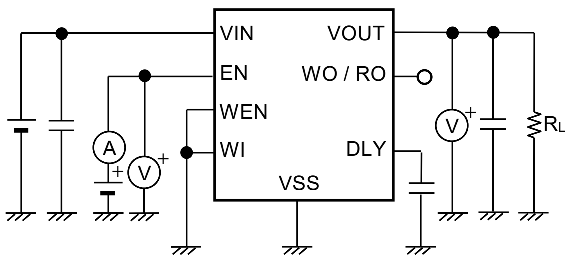


Figure 12 Test Circuit 4

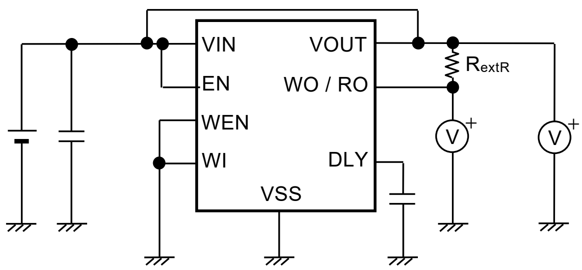


Figure 13 Test Circuit 5

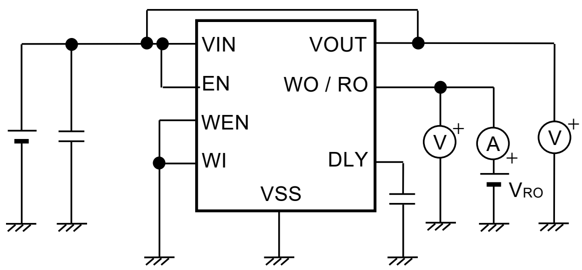


Figure 14 Test Circuit 6

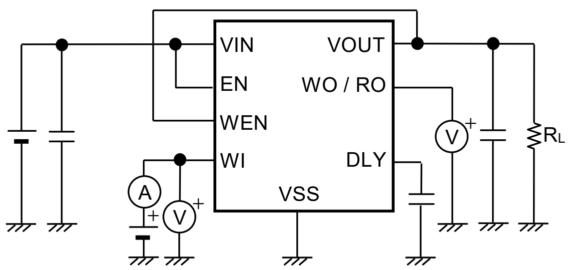


Figure 15 Test Circuit 7

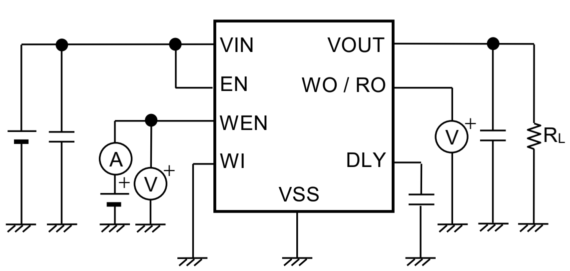


Figure 16 Test Circuit 8

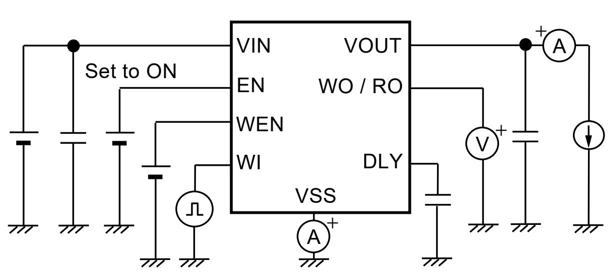


Figure 17 Test Circuit 9

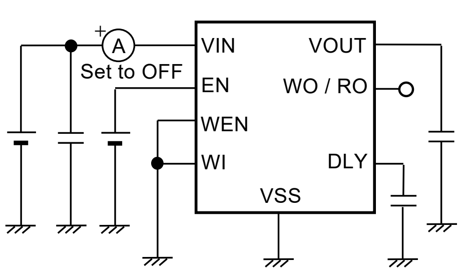


Figure 18 Test Circuit 10

■ Standard Circuit

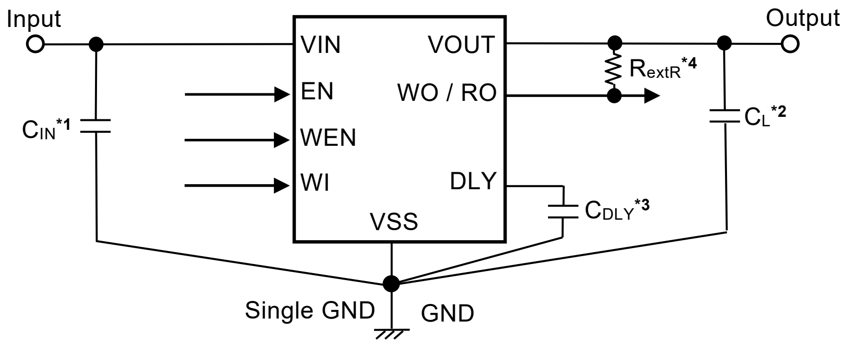


Figure 19

***1.** C_{IN} is a capacitor for stabilizing the input.
***2.** C_L is a capacitor for stabilizing the output.
***3.** C_{DLY} is the release delay time and monitoring time adjustment capacitor.
***4.** Connection of the external pull-up resistor is not absolutely essential since the S-19518 Series has a built-in pull-up resistor.

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

■ Selection of External Parts

1. Input and output capacitors (C_{IN}, C_L)

The S-19518 Series requires C_L between the VOUT pin and the VSS pin for phase compensation. Operation is stabilized by a ceramic capacitor with an output capacitance of 1.0 μF or more over the entire temperature range. When using an OS capacitor, a tantalum capacitor, or an aluminum electrolytic capacitor, the capacitance must be 1.0 μF or more, and the ESR must be 100 Ω or less.
The values of output overshoot and undershoot, which are transient response characteristics, vary depending on the value of the output capacitor.
The required value of capacitance for the input capacitor differs depending on the application.

Caution Define the capacitance of C_{IN} and C_L by sufficient evaluation including the temperature characteristics under the actual usage conditions.

2. Release delay time and monitoring time adjustment capacitor (C_{DLY})

In the S-19518 Series, the release delay time and monitoring time adjustment capacitor (C_{DLY}) is necessary between the DLY pin and the VSS pin to adjust the release delay time (t_{rd}) of the detector and the monitoring time of the watchdog timer.
The set release delay time ($t_{rd(S)}$), the set watchdog trigger time ($t_{WI,tr(S)}$), the set watchdog output "L" time ($t_{WD,L(S)}$) and the set watchdog double-pulse detection time ($t_{WI,dp(S)}$) are calculated by using following equations, respectively.
The release delay time (t_{rd}), the watchdog trigger time ($t_{WI,tr}$), the watchdog output "L" time ($t_{WD,L}$) and the watchdog double-pulse detection time ($t_{WI,dp}$) at the time of the condition of C_{DLY} = 10 nF are shown in "**■ Electrical Characteristics**".

$$t_{rd(S)}\ [\text{ms}] = t_{rd}\ [\text{ms}] \times \frac{C_{DLY}\ [\text{nF}]}{10\ [\text{nF}]}$$

$$t_{WI,tr(S)}\ [\text{ms}] = t_{WI,tr}\ [\text{ms}] \times \frac{C_{DLY}\ [\text{nF}]}{10\ [\text{nF}]}$$

$$t_{WD,L(S)}\ [\text{ms}] = t_{WD,L}\ [\text{ms}] \times \frac{C_{DLY}\ [\text{nF}]}{10\ [\text{nF}]}$$

$$t_{WI,dp(S)}\ [\text{ms}] = t_{WI,dp}\ [\text{ms}] \times \frac{C_{DLY}\ [\text{nF}]}{10\ [\text{nF}]}$$

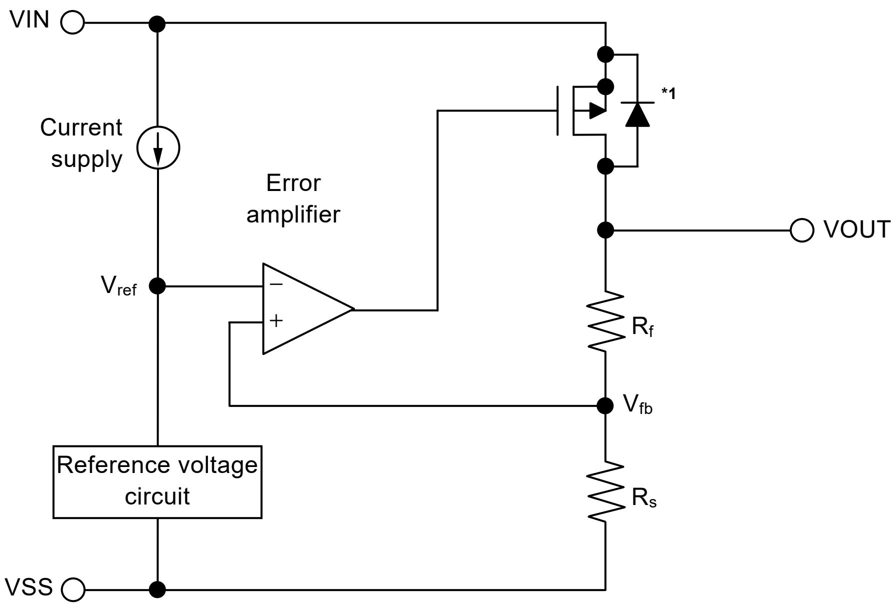
Caution 1. The above equations will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics using an actual application to set the constants.
2. Mounted board layout should be made in such a way that no current flows into or flows from the DLY pin since the impedance of the DLY pin is high, otherwise correct delay time and monitoring time may not be provided.
3. Select C_{DLY} whose leakage current can be ignored against the built-in constant current (0.6 μA typ.). The leakage current may cause deviation in delay time and monitoring time. When the leakage current is larger than the built-in constant current, no release takes place.
4. Deviations of C_{DLY} are not included in the equations mentioned above. Be sure to determine the constants considering the deviation of C_{DLY} to be used.

■ Operation

1. Regulator block

1. 1 Basic operation

Figure 20 shows the block diagram of the regulator in the S-19518 Series.
The error amplifier compares the reference voltage (V_{ref}) with feedback voltage (V_{fb}), which is the output voltage resistance-divided by feedback resistors (R_s and R_f). It supplies the gate voltage necessary to maintain the constant output voltage which is not influenced by the input voltage and temperature change, to the output transistor.



***1.** Parasitic diode

Figure 20

1. 2 Output transistor

In the S-19518 Series, a low on-resistance P-channel MOS FET is used as the output transistor.
Be sure that V_{OUT} does not exceed $V_{IN} + 0.3$ V to prevent the voltage regulator from being damaged due to reverse current flowing from the VOUT pin through a parasitic diode to the VIN pin, when the potential of V_{OUT} became higher than V_{IN}.

1. 3 Overcurrent protection circuit

The S-19518 Series includes an overcurrent protection circuit which having the characteristics shown in "**1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)**" of "**1. Regulator block**" in "**■ Characteristics (Typical Data)**", in order to limit an excessive output current and overcurrent of the output transistor due to short-circuiting between the VOUT pin and the VSS pin. The current when the output pin is short-circuited (I_{short}) is internally set at 80 mA typ., and the load current when short-circuiting is limited based on this value. The output voltage restarts regulating if the output transistor is released from overcurrent status.

Caution This overcurrent protection circuit does not work as for thermal protection. If this IC long keeps short circuiting, pay attention to the conditions of input voltage and load current so that, under the usage conditions including short circuit, the loss of the IC will not exceed power dissipation.

1. 4 Thermal shutdown circuit

The S-19518 Series has a thermal shutdown circuit to limit self-heating. When the junction temperature rises to 170°C typ., the thermal shutdown circuit operates to stop regulating. After that, when the junction temperature drops to 135°C typ., the thermal shutdown circuit is released to restart regulating.
Due to self-heating of the S-19518 Series, if the thermal shutdown circuit starts operating, it stops regulating so that the output voltage drops. For this reason, self-heating is limited and the IC's temperature drops.
When the temperature drops, the thermal shutdown circuit is released to restart regulating, thus self-heating is generated again due to rising of the output voltage. Repeating this procedure makes the waveform of the VOUT pin output into a pulse-like form. This phenomenon continues unless decreasing either or both of the input voltage and the output current in order to reduce the internal power consumption, or decreasing the ambient temperature. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously.

Table 14

Thermal Shutdown Circuit	VOUT Pin Voltage
Detect: 170°C typ.*1	V_{SS} level
Release: 135°C typ.*1	Set value

***1.** Junction temperature

1. 5 ON / OFF circuit

The ON / OFF circuit controls the internal circuit and the output transistor in order to start and stop the regulator. When the EN pin is set to "L" (OFF), the internal circuit stops operating and the output transistor between the VIN pin and the VOUT pin is turned off, reducing current consumption significantly.
The internal equivalent circuit related to the EN pin is configured as shown in **Figure 21**. Since the EN pin is internally pulled down by the constant current source, the EN pin is set to "L" if it is used in the floating status, and the output transistor is turned off. However, in order that the EN pin becomes OFF certainly, connect the EN pin to GND so that "L" is certainly input to the EN pin, since the impedance of the EN pin becomes high when using the EN pin in the floating status.
When not using the EN pin, connect it to the VIN pin. Note that the current consumption increases when an intermediate voltage is applied to the EN pin.

Table 15

EN Pin	Internal Circuit	VOUT Pin Voltage	Current Consumption
"H": ON	Operate	Constant value*1	I_{SS1}
"L": OFF	Stop	Pulled down to V_{SS}*2	I_{SS2}

***1.** The constant value is output due to the regulating based on the set output voltage value.
***2.** The VOUT pin voltage is pulled down to V_{SS} due to combined resistance (R_{LOW} = 1.2 kΩ typ.) of the discharge shunt circuit and the feedback resistors, and a load.

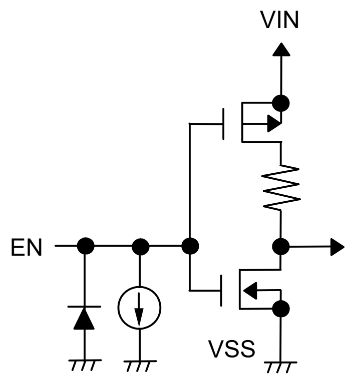


Figure 21

2. Detector block

2. 1 Basic operation

(1) When the output voltage (V_{OUT}) of the regulator is release voltage ($+V_{DET}$) of the detector or higher, the Nch transistor (N1 and N2) are turned off and "H" is output to the RO pin. Since the Pch transistor (P1) is turned on, the input voltage to the comparator (C1) is $\frac{R_B \bullet V_{OUT}}{R_A + R_B}$.

(2) Even if V_{OUT} decreases to $+V_{DET}$ or lower, "H" is output to the RO pin when V_{OUT} is the detection voltage ($-V_{DET}$) or higher. When V_{OUT} decreases to $-V_{DET}$ (point A in **Figure 23**) or lower, N1 which is controlled by C1 is turned on, and C_{DLY} is discharged. At the same time, N2, which is controlled by the delay circuit, is turned on, and "L" is output to the RO pin. At this time, P1 is turned off, and the input voltage to C1 is $\frac{R_B \bullet V_{OUT}}{R_A + R_B + R_C}$.

(3) If V_{OUT} further decreases to the IC's minimum operation voltage or lower, the RO pin output becomes uncertain. If the RO pin is pulled up, "H" is output.

(4) When V_{OUT} increases to the IC's minimum operation voltage or higher, "L" is output to the RO pin. Moreover, even if V_{OUT} exceeds $-V_{DET}$, the output is "L" when V_{OUT} is lower than $+V_{DET}$.

(5) When V_{OUT} increases to $+V_{DET}$ (point B in **Figure 23**) or higher, N1 is turned off and C_{DLY} is charged. When V_{DLY} increases to the threshold voltage (1.25 V typ.), N2, which is controlled by a delay circuit, is turned off and "H" is output to the RO pin.

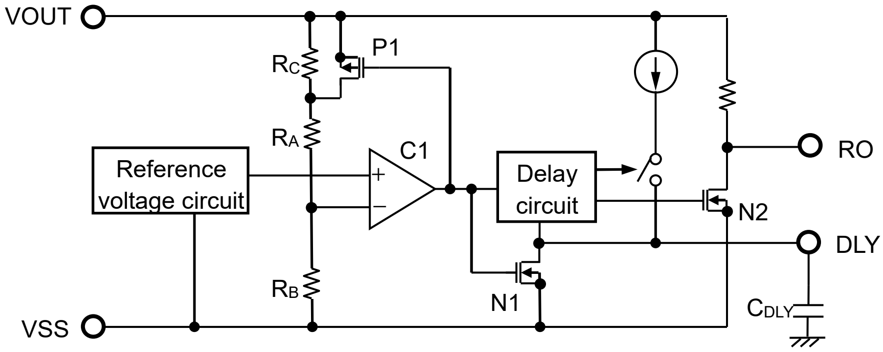


Figure 22 Operation of Detector Block

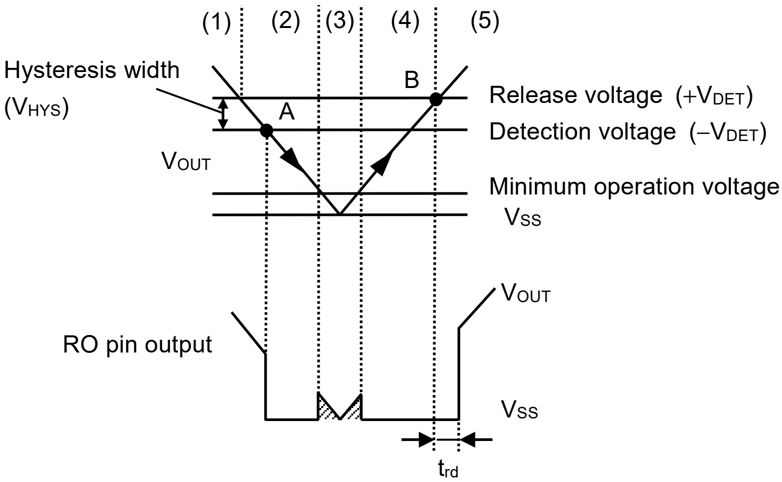


Figure 23 Timing Chart of Detector Block

2. 2 Delay circuit

When the output voltage (V_{OUT}) of the regulator rises under the status that "L" is output to the RO pin, the reset release signal is output to the RO pin later than when V_{OUT} becomes $+V_{DET}$. The release delay time (t_{rd}) changes according to C_{DLY}. Refer to "**2. Release delay time and monitoring time adjustment capacitor (C_{DLY})**" in "**■ Selection of External Parts**" for details.
In addition, if the time from when V_{OUT} decreases to $-V_{DET}$ or lower to when V_{OUT} increases to $+V_{DET}$ or higher is significantly shorter compared to the length of the reset reaction time (t_{rr}), "H" output may remain in the RO pin.

Caution Since t_{rd} depends on the charge time of C_{DLY}, t_{rd} may be shorter than the set value if the charge operation is initiated under the condition that a residual electric charge is left in C_{DLY}.

2. 3 Output circuit

Since the RO pin has a built-in resistor to pull up to the VOUT pin internally, the RO pin can output a signal without an external pull-up resistor
Do not connect to the pin other than VOUT pin when connecting an external pull-up resistor.
In the S-19518 Series, the reset output pin and the watchdog output pin are prepared as the WO / RO pin.
The output level of the WO / RO pin is applied by the AND logic of the reset output pin and the watchdog output pin.

Example: When the WO pin is "L" and the RO pin is "H", the WO / RO pin is "L".

Caution Define the external pull-up resistance by sufficient evaluation including the temperature characteristics under the actual usage conditions.

3. Watchdog timer block

3. 1 Basic operation

The watchdog timer operates as follows during monitoring operation.

(1) When the watchdog timer starts monitoring operation, it enters the Open window status, and C_{DLY} charge-discharge operation is carried out by an internal constant current source. If a rising edge is input to the WI pin in the Open window status, the watchdog timer detects a trigger, and switches to the Closed window status. If a trigger is not detected in the Closed window status, the C_{DLY} charge-discharge operation is carried out and if the watchdog double-pulse detection time ($t_{WI,dp}$) is exceeded, the watchdog timer switches to the Open window status. If the watchdog timer again detects a trigger in the Open window status, it switches to the Closed window status. During this time, the WO pin outputs "H". In order to verify the normal operation of the object being monitored, input a rising edge to the WI pin in the Open window status, and do not input a rising edge in the Closed window status.

(2) While no triggers are detected in the Open window status, the C_{DLY} charge-discharge operation is repeated, and once the watchdog trigger time ($t_{WI,tr}$) elapses after monitoring has started or after the last trigger was detected, the watchdog timer switches to the Watchdog fault status, and the WO pin outputs "L". This operation is called a "time-out detection". If the watchdog timer is deactivated while the WO pin is outputting "H", the number of charges and discharges and $t_{WI,tr}$ elapsed time are reset.

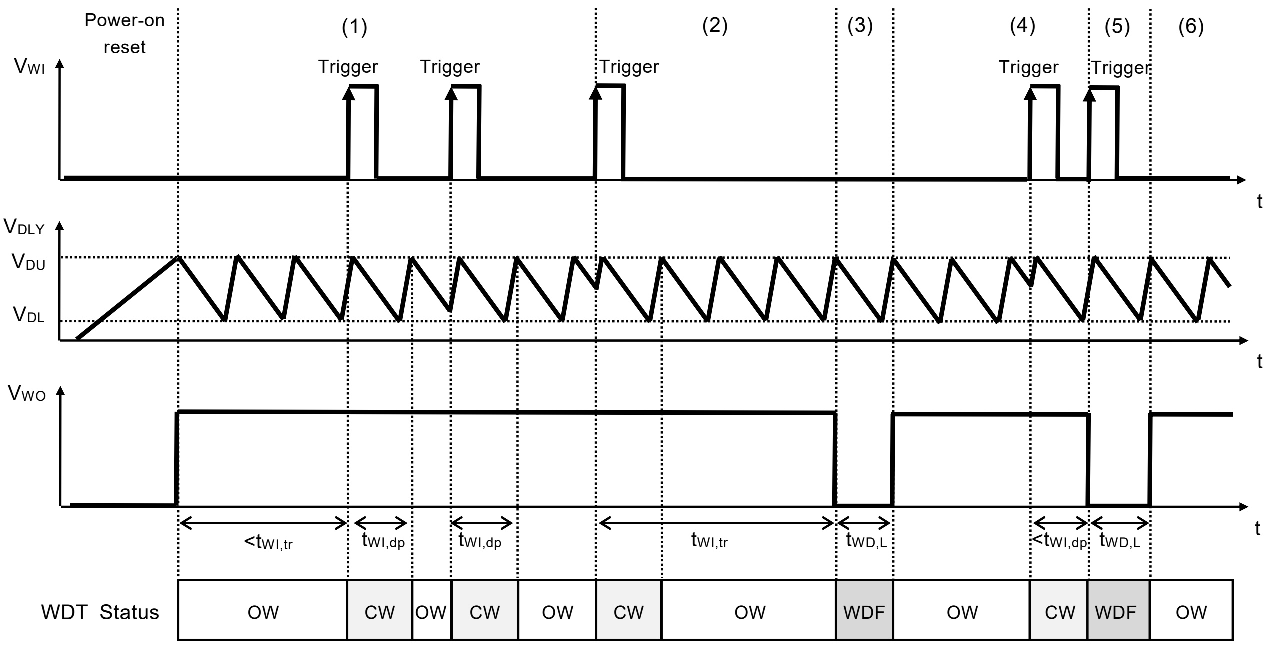
(3) After a time-out detection, C_{DLY} charge-discharge operation is carried out while the WO pin outputs "L" in the Watchdog fault status. After the watchdog output "L" time ($t_{WD,L}$) has elapsed, the watchdog timer switches to the Open window status and the WO pin outputs "H". Even if the watchdog timer is deactivated while the WO pin is outputting "L", the WO pin continues to output "L" until the $t_{WD,L}$ has elapsed.

(4) If the watchdog timer detects a trigger in the Open window status, switching to the Closed window status, a trigger is detected again before the $t_{WI,dp}$ elapses, the watchdog timer switches to the Watchdog fault status, and the WO pin outputs "L". This operation is called a "double-pulse detection".

(5) After a double-pulse detection, C_{DLY} charge-discharge operation is carried out while the WO pin outputs "L" in the Watchdog fault status. As with the case of (3), when $t_{WD,L}$ elapses, the watchdog timer switches to the Open window status and the WO pin outputs "H".

(6) After the watchdog timer reverts back to the Open window status from the Watchdog fault status, operation (1), (2), or (4) is continually carried out depending on input.

Refer to **Figure 25** for the status transition of watchdog timer block.



OW: Open window CW: Closed window WDF: Watchdog fault

Figure 24 Timing Chart of Watchdog Timer Block

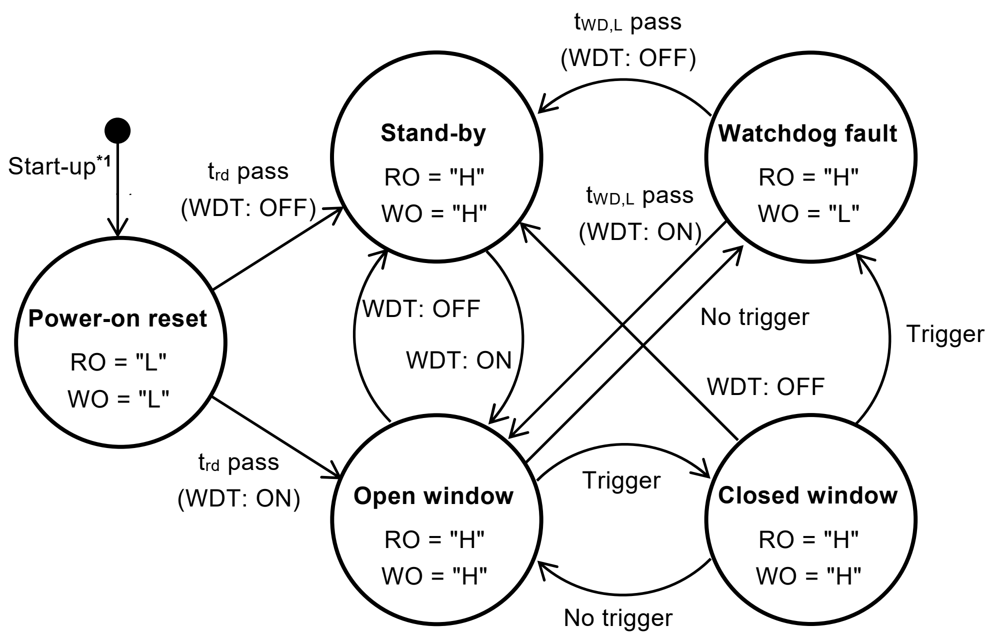


Figure 25 Status Transition of Watchdog Timer Block

***1.** If the detector block detects low voltage as a result of V_{OUT} dropping below the detection voltage ($-V_{DET}$), the watchdog timer resets to the initial status. If V_{OUT} is restored and exceeds the release voltage ($+V_{DET}$), the watchdog timer is activated and switches to the Power-on reset status.

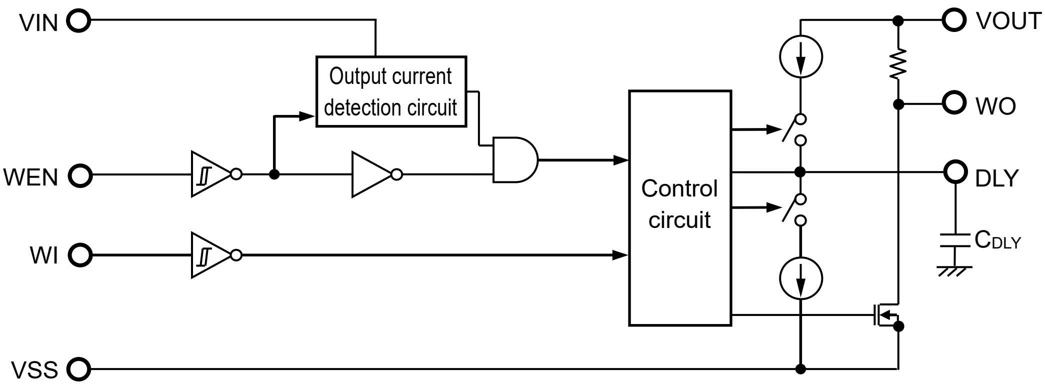


Figure 26 Operation of Watchdog Timer Block

3. 2 Autonomous watchdog operation function (Output current detection circuit)

Since the S-19518 Series has a built-in output current detection circuit, the watchdog timer operates autonomously. The current flows in the load is detected by the output current of the regulator, the watchdog timer initiates the activation when the output current is the watchdog activation threshold current ($I_{O,WDact}$) or more, the watchdog timer is deactivated when the output current is the watchdog deactivation threshold current ($I_{O,WDdeact}$) or less.

Figure 27 shows a block diagram which includes an output current detection circuit. If the regulator is connected to a microcontroller, the microcontroller operation current can be detected using the regulator output current. For example, if the microcontroller sleep operation current is lower than the watchdog deactivation threshold current ($I_{O,WDdeact}$), the watchdog timer autonomously deactivates monitoring operation when the microcontroller sleeps.
If the VIN pin voltage drops below the output current detection circuit minimum operation voltage, the output current detection circuit stops the operation. Refer to "**■ Recommended Operation Conditions**" for VIN pin voltage range.
In addition, in the S-19518 Series, if the watchdog timer is disabled using the WEN pin, the watchdog timer is deactivated regardless of the output current.

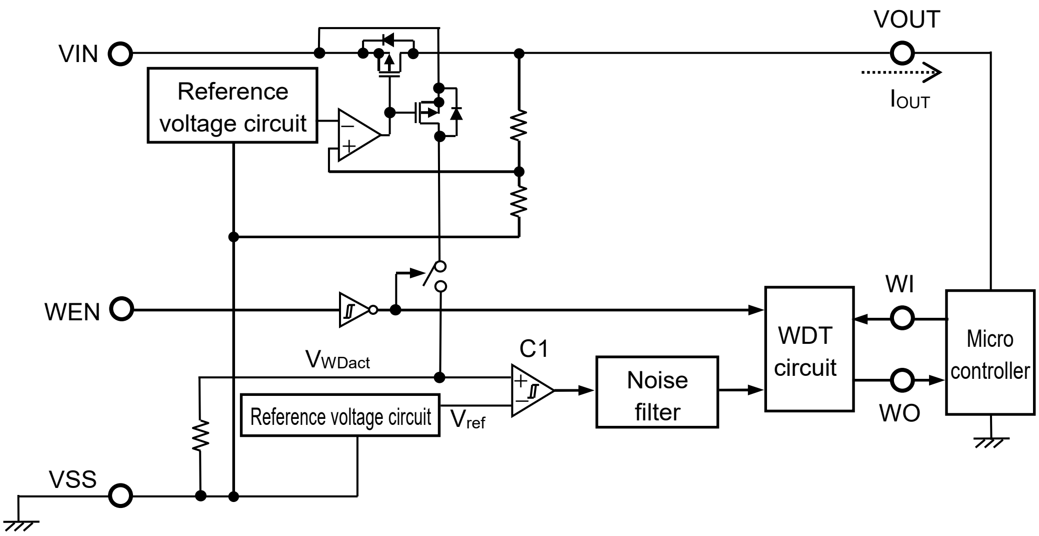


Figure 27 Operation of Output Current Detection Circuit

Caution Microcontroller is not built-in in the S-19518 Series. In addition, the above connection diagram will not guarantee successful operation. Perform thorough evaluation using the actual application to determine connections.

Since the S-19518 Series has the autonomous watchdog operation function, the watchdog timer monitoring activation is as follows.

(1) When I_{OUT} of the regulator is the watchdog activation threshold current ($I_{O,WDact}$) or more, the input voltage (V_{WDact}) of comparator (C1) is higher than the reference voltage (V_{ref}), and the output of C1 is "H". At this time, the watchdog timer activated.
(2) When I_{OUT} decreases to the watchdog deactivation threshold current ($I_{O,WDdeact}$) (point A in **Figure 28**) or less, V_{WDact} decreases to V_{ref} or less and the output of C1 is "L". At this time, the watchdog timer deactivates the monitoring. Even if I_{OUT} increases, the watchdog timer continues the monitoring deactivation when I_{OUT} is within less than $I_{O,WDact}$
(3) If I_{OUT} further increases to $I_{O,WDact}$ (point B in **Figure 28**) or more, V_{WDact} increases to V_{ref} or higher and the output of C1 is "H". And then, the watchdog timer initiates the monitoring activation.

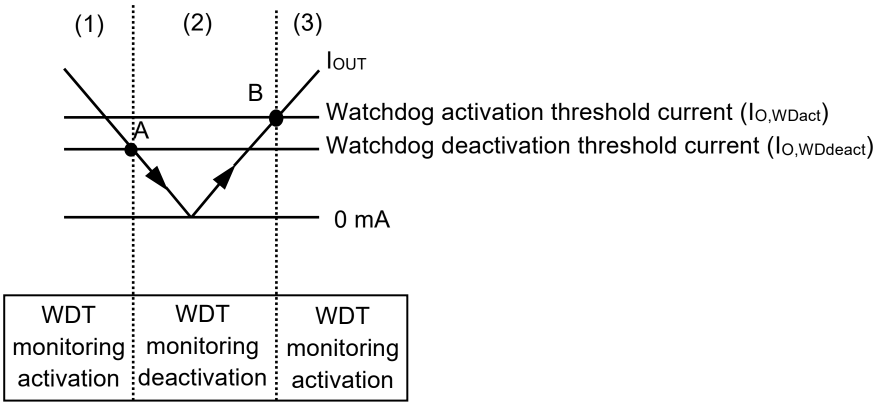


Figure 28 Autonomous Watchdog Operation Function

Caution If the output current of regulator transiently changes, the monitoring activation of watchdog timer may become unstable, resulting in switching between activation and deactivation. Regarding the activation at that time, perform thorough evaluation using an actual application.

3. 3 Watchdog enable circuit

When inputting "L" to the WEN pin, the watchdog timer becomes Disable and stops the output current detection operation and monitoring activation. When inputting "H" to the WEN pin, the watchdog timer becomes Enable.
The WEN pin is pulled down internally by the constant current source. For this reason, the WEN pin is set to "L" when using the WEN pin in the floating status, and the watchdog timer becomes Disable. However, in order that the watchdog timer becomes Disable certainly, connect the WEN pin to GND so that "L" is input to the WEN pin certainly, since the impedance of the WEN pin becomes high when using the WEN pin in the floating status.
In order to fix the watchdog timer to Enable, connect the WEN pin to the VOUT pin so that "H" is input to the WEN pin.
Table 16 shows the relation between each pin status and the watchdog timer monitoring operation.

Table 16

WEN Pin	Output Current*1	VOUT Pin Voltage	WDT Monitoring Operation
"H"	"H"	$\geq +V_{DET}$	ON
"H"	"L"	$\geq +V_{DET}$	OFF
"L"	Don't care	$\geq +V_{DET}$	OFF
Don't care	Don't care	$\leq -V_{DET}$	OFF

***1.** "H": $I_{OUT} > I_{O,WDact}$, "L": $I_{OUT} < I_{O,WDdeact}$

3. 4 Watchdog input circuit

By inputting a rising edge to the WI pin, the watchdog timer detects a trigger. Refer to "**■ Recommended Operation Conditions"** for the input conditions of the signal to be input from the watchdog timer monitored object to the WI pin.
The WI pin is pulled down internally by a constant current source. For this reason, if the WI pin is used in a floating status, the WI pin sets to "L".
Note that if any voltage other than "L" or "H" is input to the WI pin, the current consumption increases.
Triggers are detected only when the WO pin is outputting "H" and C_{DLY} charge-discharge operation is being carried out while the watchdog timer is carrying out monitoring operation.

Caution Under a noisy environment, the watchdog input circuit may detect the noise as a trigger signal. Sufficiently evaluate with the actual application to confirm that a trigger is detected only in the intended signal.

3. 5 Watchdog output circuit

Since the WO pin has a built-in resistor to pull up to the VOUT pin internally, the WO pin can output a signal without an external pull-up resistor
Do not connect to the pin other than VOUT pin when connecting an external pull-up resistor.
In the S-19518 Series, the reset output pin and the watchdog output pin are prepared as the WO / RO pin.
The output level of the WO / RO pin is applied by the AND logic of the reset output pin and the watchdog output pin.

Example: When the WO pin is "L" and the RO pin is "H", the WO / RO pin is "L".

Caution Define the external pull-up resistance by sufficient evaluation including the temperature characteristics under the actual usage conditions.

■ Timing Chart

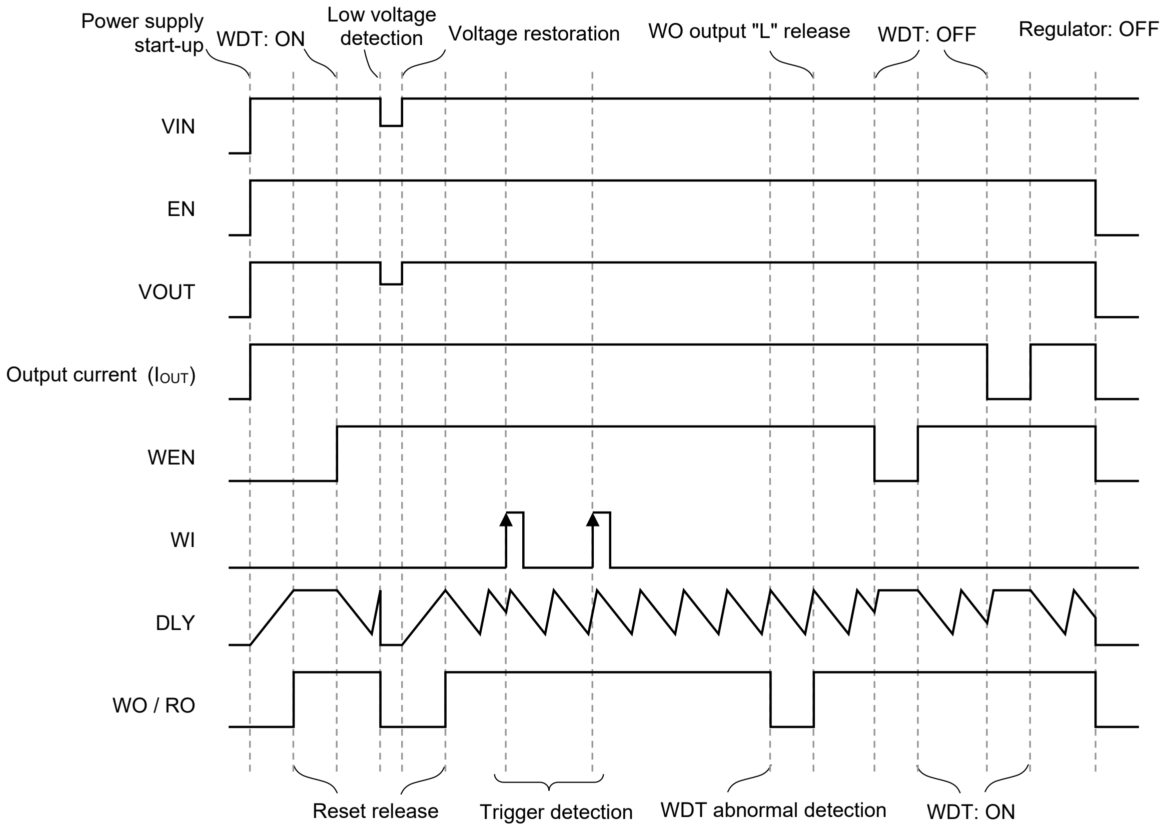


Figure 29

■ Precautions

- Wiring patterns for the VIN pin, the VOUT pin and GND should be designed so that the impedance is low. When mounting an output capacitor between the VOUT pin and the VSS pin (C_L) and an input capacitor between the VIN pin and the VSS pin (C_{IN}), the distance from the capacitors to these pins should be as short as possible.
- Note that generally the output voltage may increase when a series regulator is used at low load current (0.1 mA or less).
- Note that generally the output voltage may increase due to the leakage current from an output transistor when a series regulator is used at high temperature.
- Generally a series regulator may cause oscillation, depending on the selection of external parts. The following conditions are recommended for the S-19518 Series. However, be sure to perform sufficient evaluation under the actual usage conditions for selection, including evaluation of temperature characteristics. Refer to "**5. Example of equivalent series resistance vs. Output current characteristics (Ta = −40°C to +125°C)**" in "**■ Reference Data**" for the equivalent series resistance (R_{ESR}) of the output capacitor.

  Input capacitor (C_{IN}): 1.0 μF or more
  Output capacitor (C_L): 1.0 μF or more

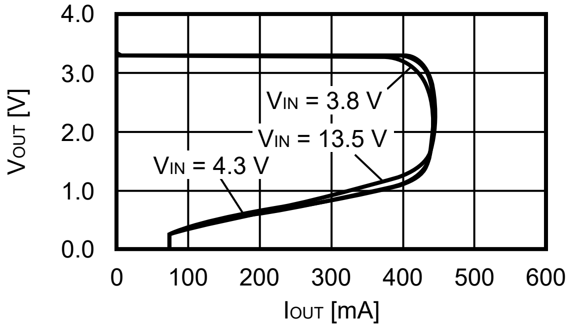
- In a series regulator, generally the values of overshoot and undershoot in the output voltage vary depending on the variation factors of power-on, power supply fluctuation and load fluctuation, or output capacitance.
  Determine the conditions of the output capacitor after sufficiently evaluating the temperature characteristics of overshoot or undershoot in the output voltage with the actual device.
- The voltage regulator may oscillate when the impedance of the power supply is high and the input capacitance is small or an input capacitor is not connected.
- Overshoot may occur in the output voltage momentarily if the voltage is rapidly raised at power-on or when the power supply fluctuates. Sufficiently evaluate the output voltage at that time with the actual device.
- If the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur to the VOUT pin due to resonance of the wiring inductance and the output capacitance in the application. The negative voltage can be limited by inserting a protection diode between the VOUT pin and the VSS pin or inserting a series resistor to the output capacitor.
- The application conditions for the input voltage, the output voltage, and the load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In determining the output current, attention should be paid to the output current value specified in **Table 10** in "**■ Electrical Characteristics**" and footnote ***7** of the table.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

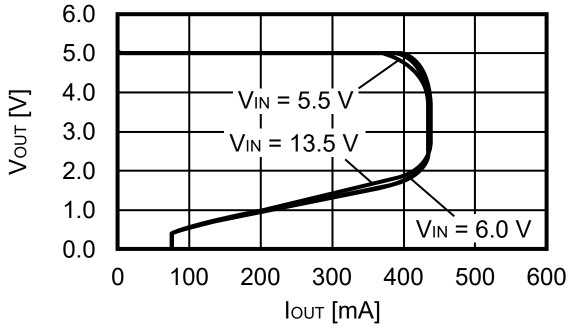
1. Regulator block

1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)

1. 1. 1 V_{OUT} = 3.3 V

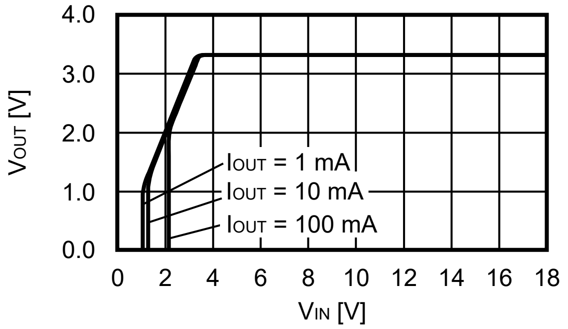


1. 1. 2 V_{OUT} = 5.0 V

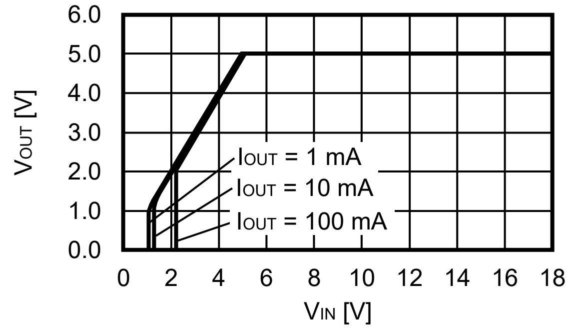


1. 2 Output voltage vs. Input voltage (Ta = +25°C)

1. 2. 1 V_{OUT} = 3.3 V

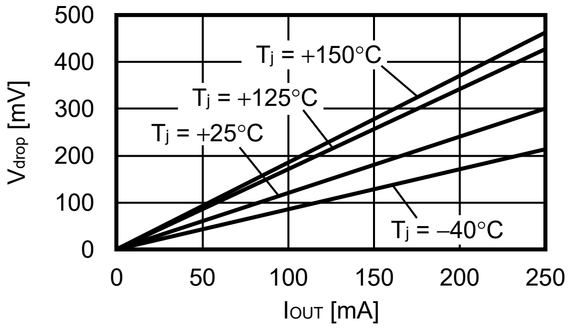


1. 2. 2 V_{OUT} = 5.0 V

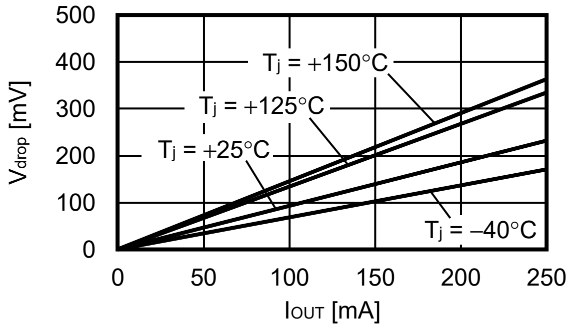


1. 3 Dropout voltage vs. Output current

1. 3. 1 V_{OUT} = 3.3 V

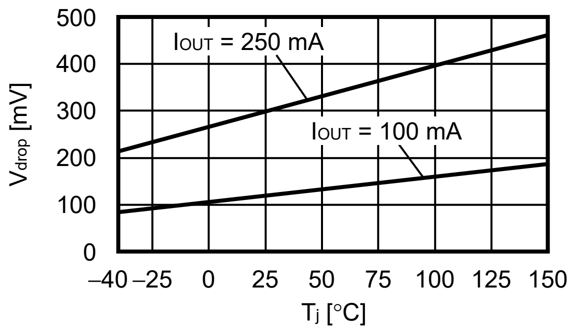


1. 3. 2 V_{OUT} = 5.0 V

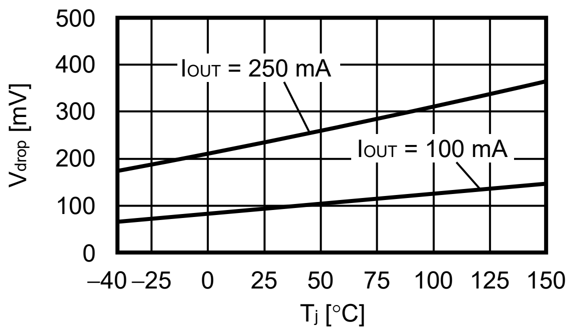


1. 4 Dropout voltage vs. Junction temperature

1. 4. 1 V_{OUT} = 3.3 V

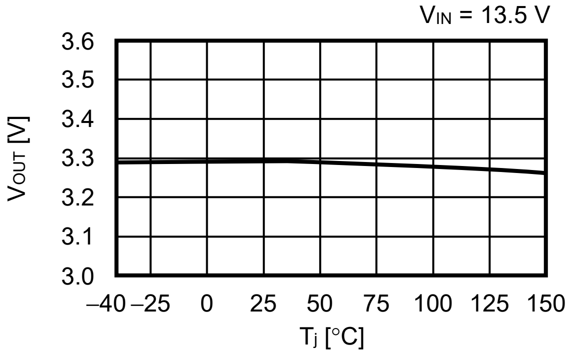


1. 4. 2 V_{OUT} = 5.0 V

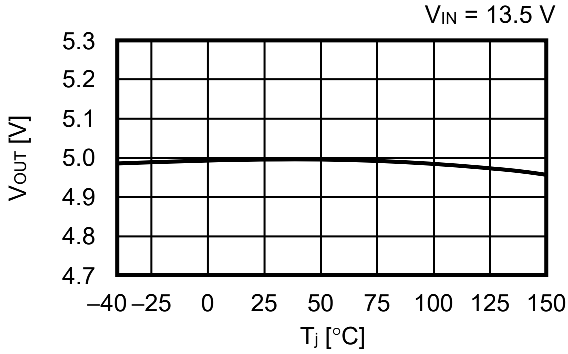


1. 5 Output voltage vs. Junction temperature

1. 5. 1 V_{OUT} = 3.3 V

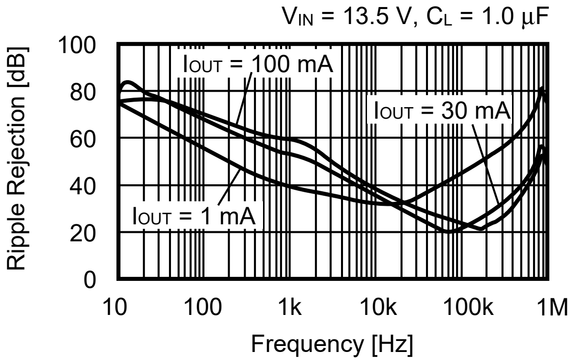


1. 5. 2 V_{OUT} = 5.0 V

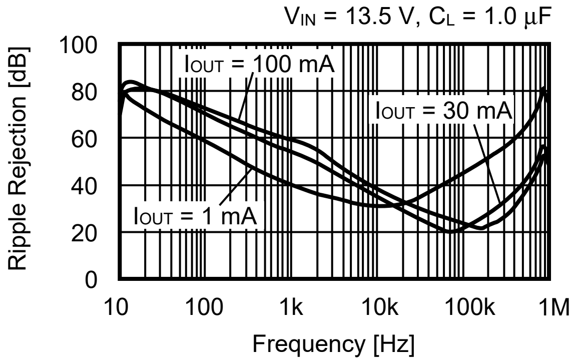


1. 6 Ripple rejection (Ta = +25°C)

1. 6. 1 V_{OUT} = 3.3 V



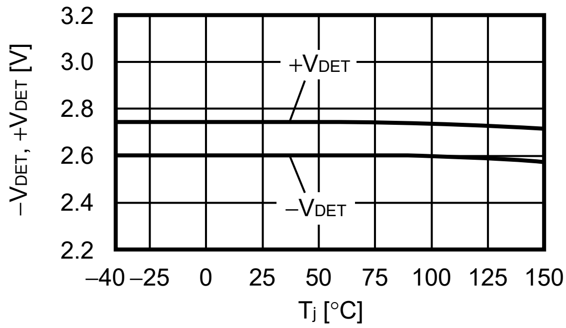
1. 6. 2 V_{OUT} = 5.0 V



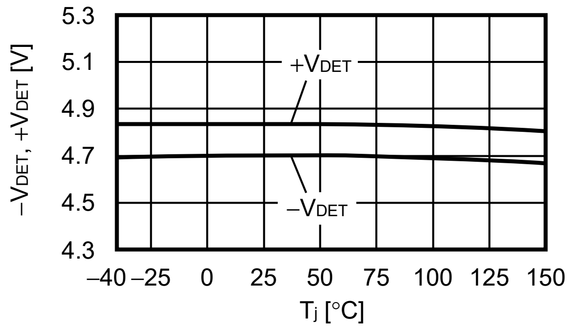
2. Detector block

2. 1 Detection voltage, Release voltage vs. Junction temperature

2. 1. 1 $-V_{DET}$ = 2.6 V

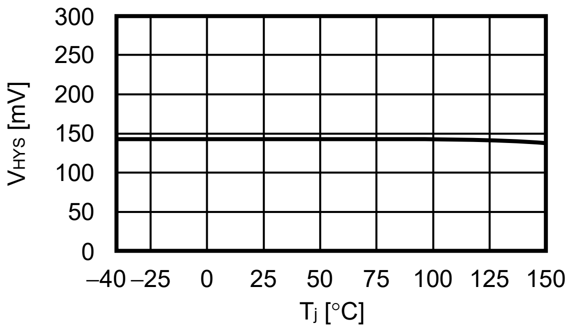


2. 1. 2 $-V_{DET}$ = 4.7 V

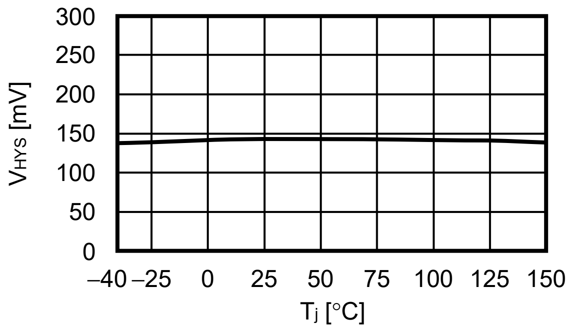


2. 2 Hysteresis width vs. Junction temperature

2. 2. 1 $-V_{DET}$ = 2.6 V

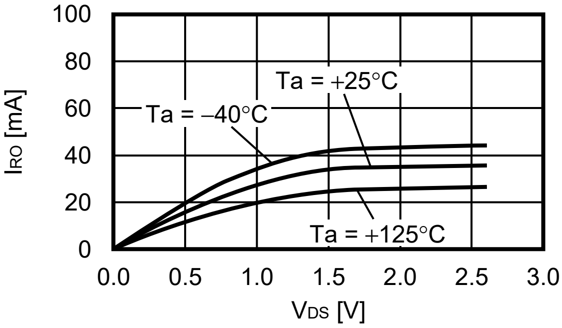


2. 2. 2 $-V_{DET}$ = 4.7 V

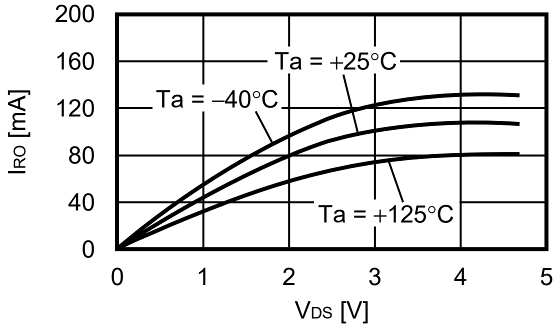


2. 3 Reset output current vs. V_{DS}

2. 3. 1 $-V_{DET}$ = 2.6 V



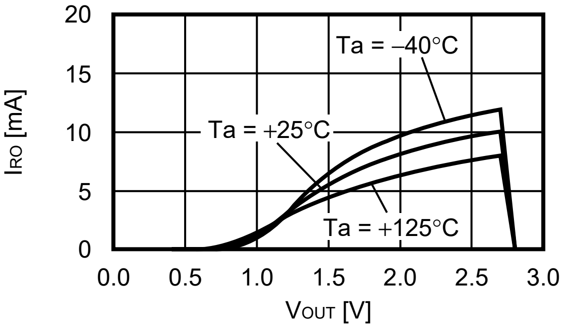
2. 3. 2 $-V_{DET}$ = 4.7 V



2. 4 Reset output current vs. Output voltage

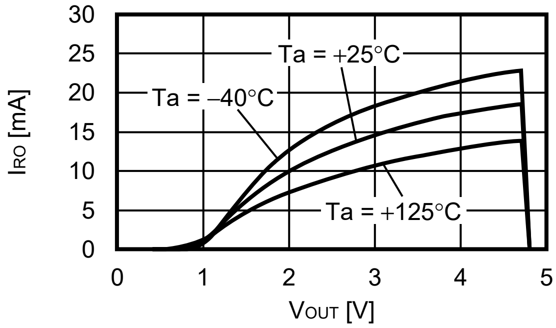
2. 4. 1 $-V_{DET}$ = 2.6 V

V_{DS} = 0.4 V



2. 4. 2 $-V_{DET}$ = 4.7 V

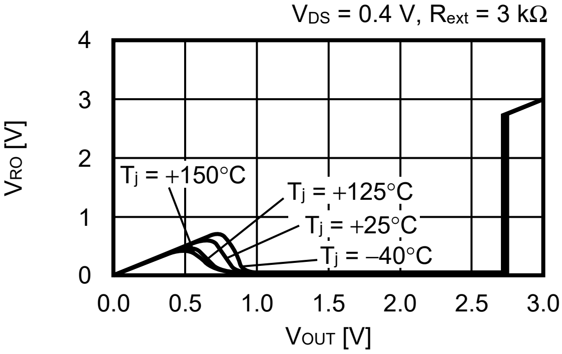
V_{DS} = 0.4 V



2. 5 RO pin voltage vs. Output voltage

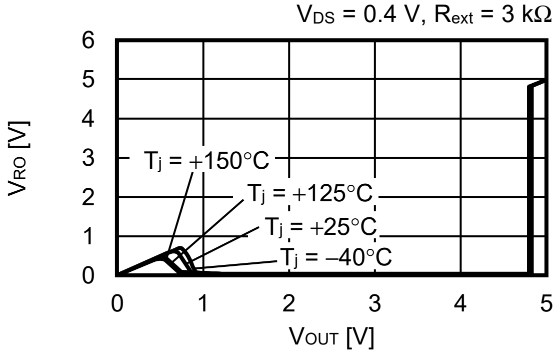
2. 5. 1 $-V_{DET}$ = 2.6 V

V_{DS} = 0.4 V, R_{ext} = 3 kΩ



2. 5. 2 $-V_{DET}$ = 4.7 V

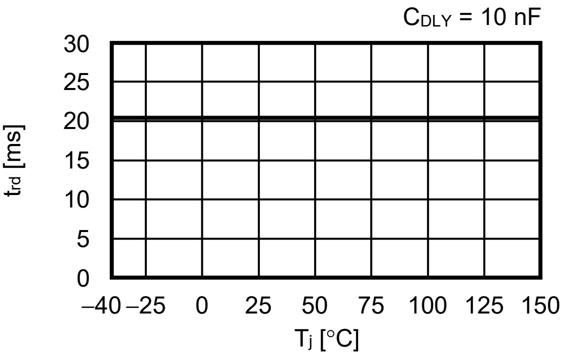
V_{DS} = 0.4 V, R_{ext} = 3 kΩ



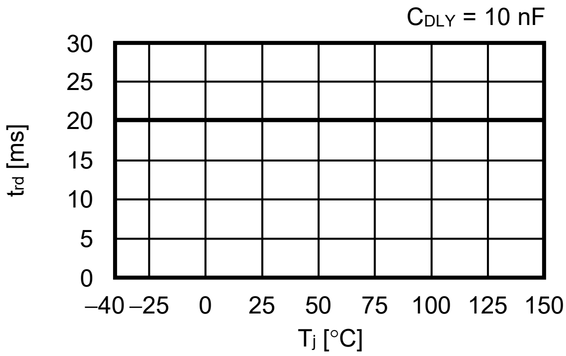
Remark I_{RO}: Nch transistor output current
V_{RO}: Nch transistor output voltage
V_{DS}: Drain-to-source voltage of Nch transistor

2. 6 Release delay time vs. Junction temperature

2. 6. 1 $-V_{DET}$ = 2.6 V

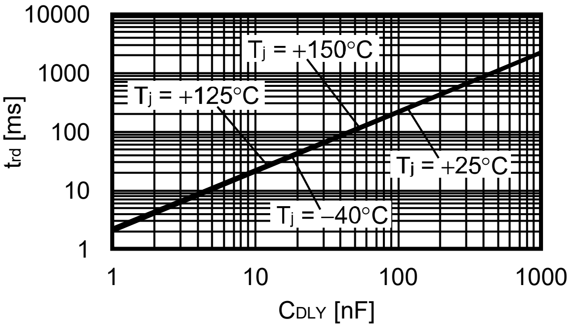


2. 6. 2 $-V_{DET}$ = 4.7 V

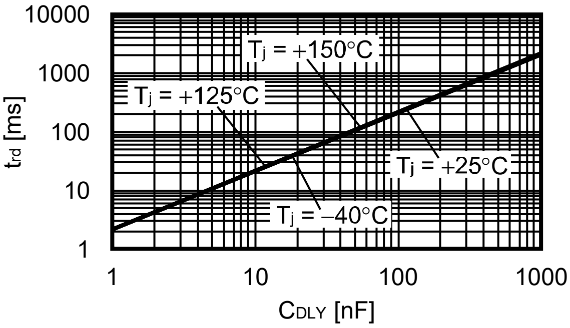


2. 7 Release delay time vs. Release delay time and monitoring time adjustment capacitance

2. 7. 1 $-V_{DET}$ = 2.6 V

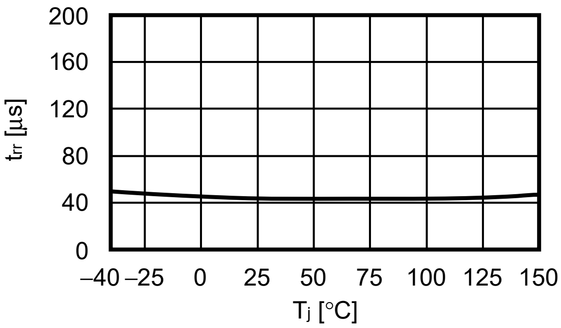


2. 7. 2 $-V_{DET}$ = 4.7 V

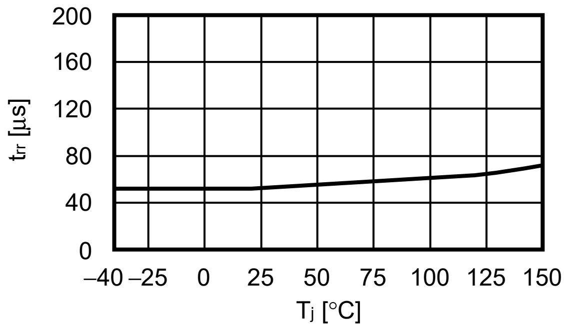


2. 8 Reset reaction time vs. Junction temperature

2. 8. 1 $-V_{DET}$ = 2.6 V



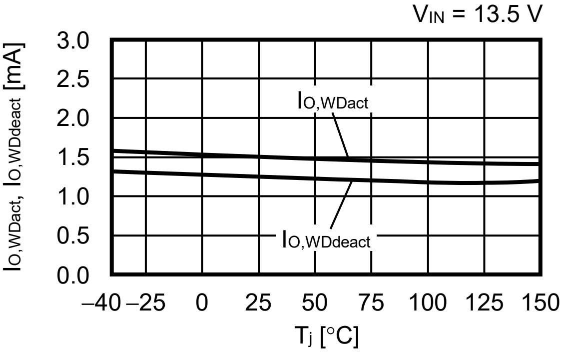
2. 8. 2 $-V_{DET}$ = 4.7 V



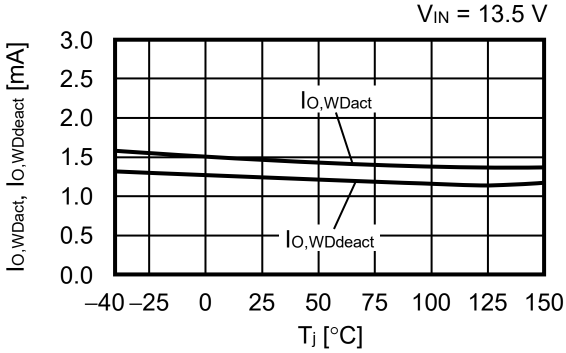
3. Watchdog timer block

3. 1 Watchdog activation threshold current, watchdog deactivation threshold current vs. Junction temperature

3. 1. 1 V_{OUT} = 3.3 V

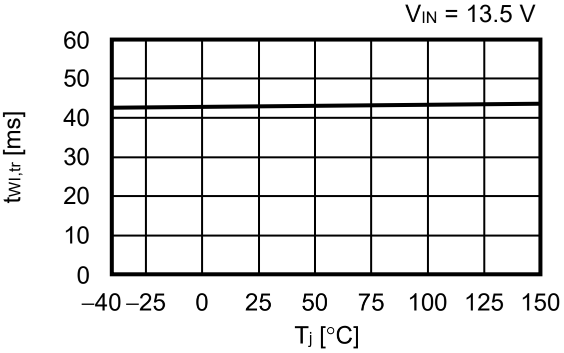


3. 1. 2 V_{OUT} = 5.0 V

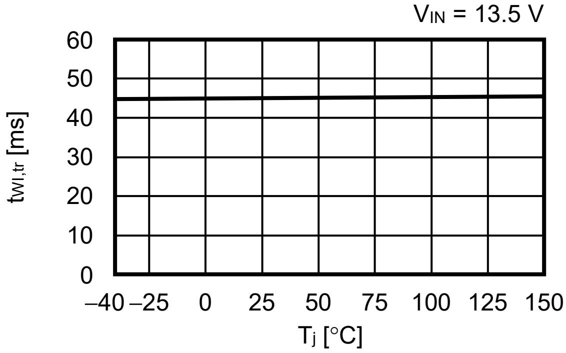


3. 2 Watchdog trigger time vs. Junction temperature

3. 2. 1 V_{OUT} = 3.3 V

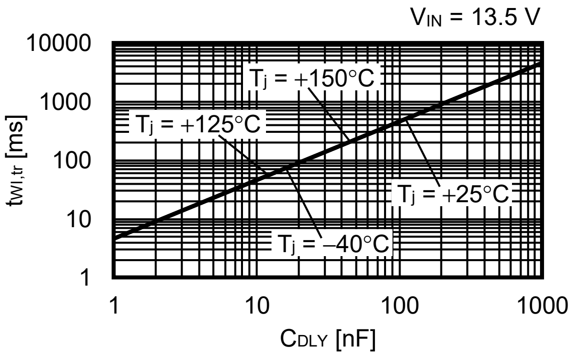


3. 2. 2 V_{OUT} = 5.0 V

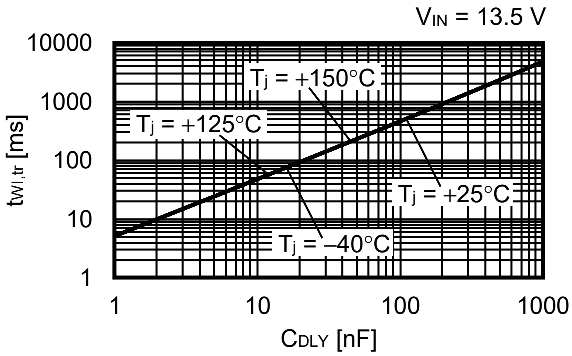


3. 3 Watchdog trigger time vs. Release delay time and monitoring time adjustment capacitance

3. 3. 1 V_{OUT} = 3.3 V



3. 3. 2 V_{OUT} = 5.0 V

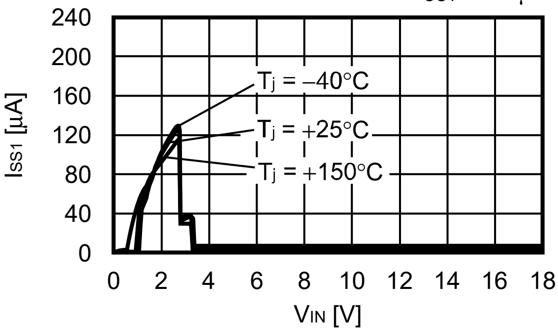


4. Overall

4. 1 Current consumption during operation vs. Input voltage

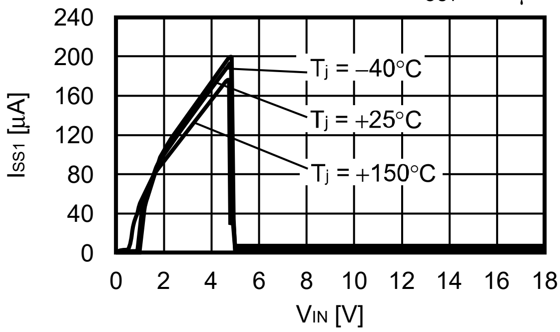
4. 1. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

I_{OUT} = 10 μA



4. 1. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

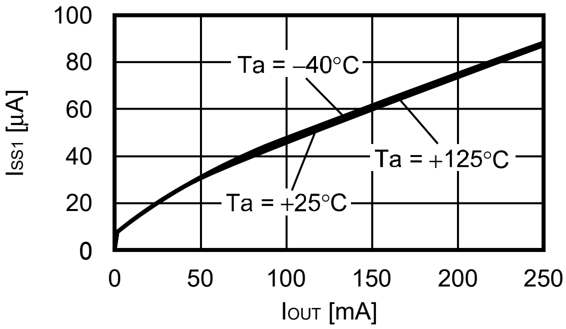
I_{OUT} = 10 μA



4. 2 Current consumption during operation vs. Output current

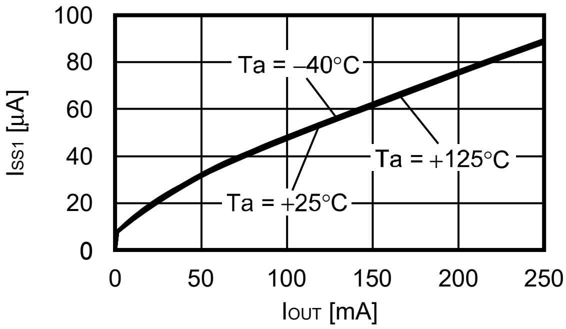
4. 2. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

V_{IN} = 4.3 V



4. 2. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

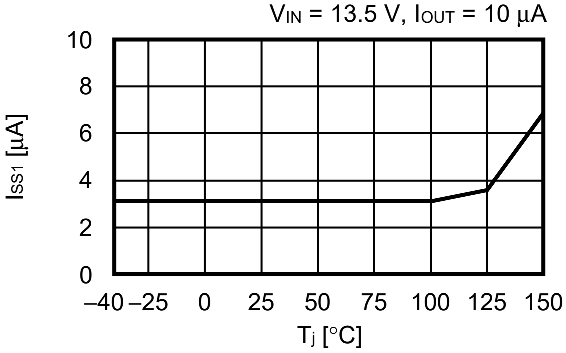
V_{IN} = 6.0 V



4. 3 Current consumption during operation vs. Junction temperature

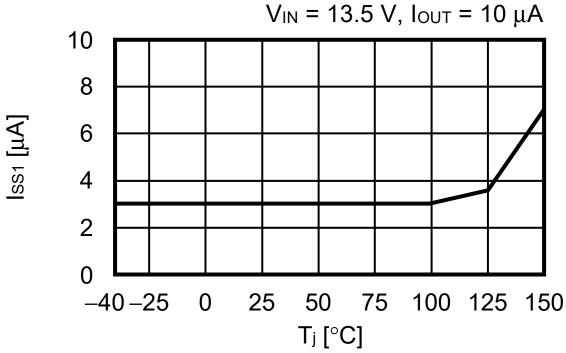
4. 3. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

V_{IN} = 13.5 V, I_{OUT} = 10 μA



4. 3. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

V_{IN} = 13.5 V, I_{OUT} = 10 μA

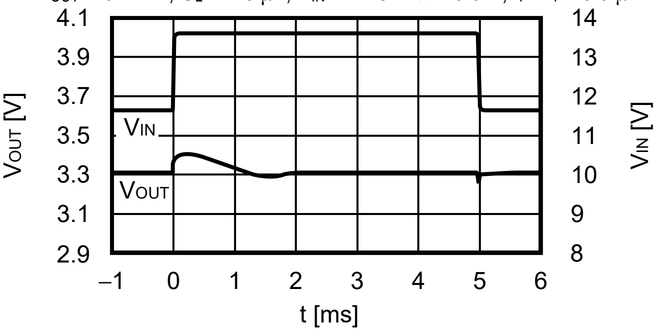


■ Reference Data

1. Characteristics of input transient response (Ta = +25°C)

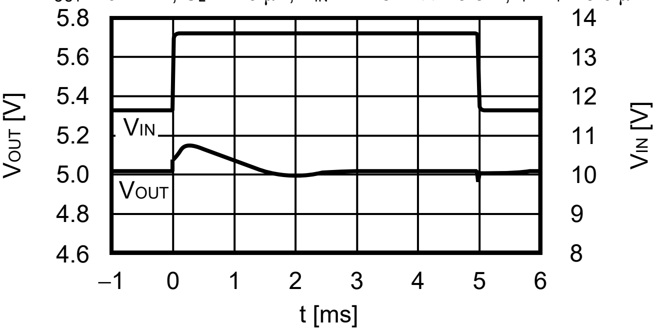
1. 1 V_{OUT} = 3.3 V

I_{OUT} = 0.1 mA, C_L = 1.0 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



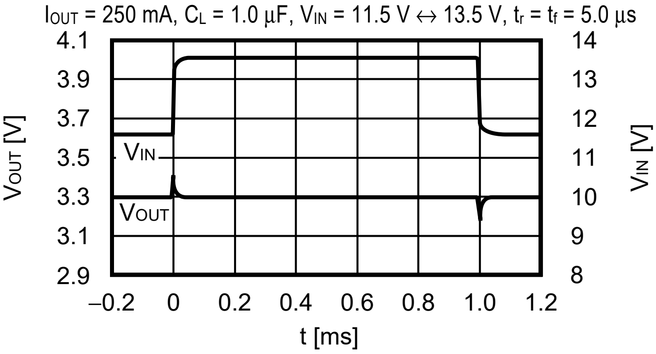
1. 2 V_{OUT} = 5.0 V

I_{OUT} = 0.1 mA, C_L = 1.0 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



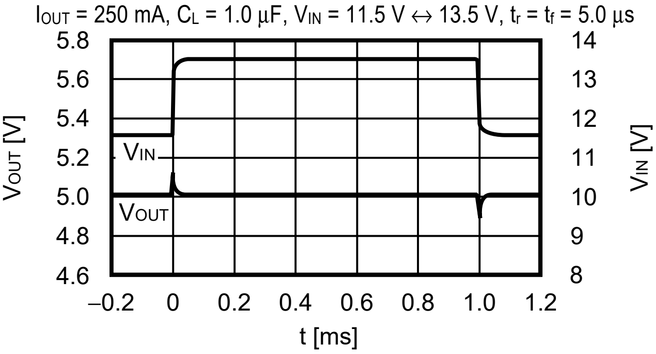
1. 3 V_{OUT} = 3.3 V

I_{OUT} = 250 mA, C_L = 1.0 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



1. 4 V_{OUT} = 5.0 V

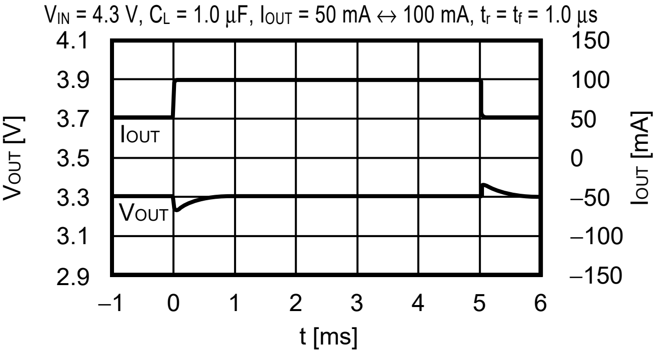
I_{OUT} = 250 mA, C_L = 1.0 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



2. Characteristics of load transient response (Ta = +25°C)

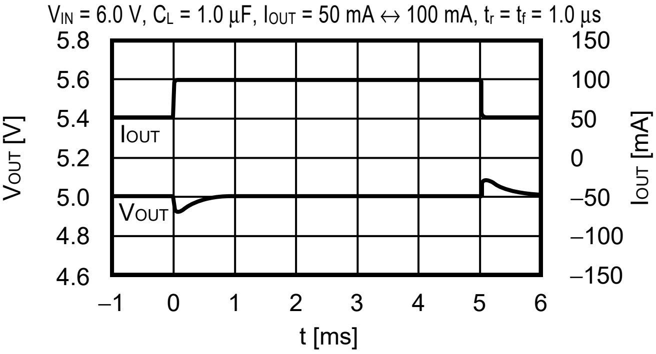
2. 1 V_{OUT} = 3.3 V

V_{IN} = 4.3 V, C_L = 1.0 µF, I_{OUT} = 50 mA ↔ 100 mA, t_r = t_f = 1.0 µs



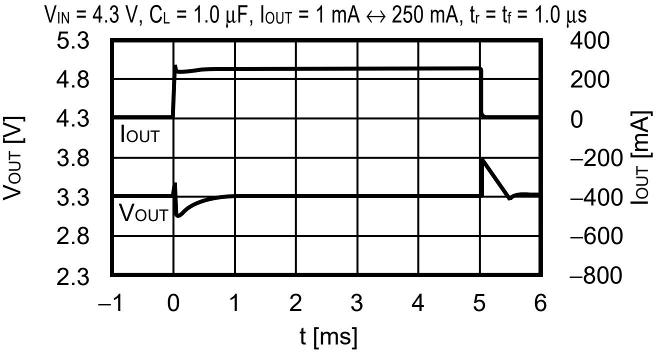
2. 2 V_{OUT} = 5.0 V

V_{IN} = 6.0 V, C_L = 1.0 µF, I_{OUT} = 50 mA ↔ 100 mA, t_r = t_f = 1.0 µs



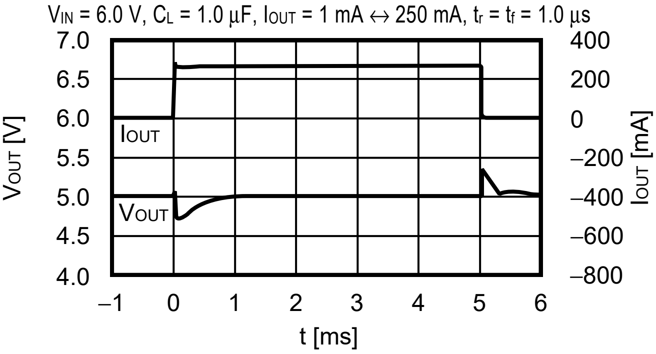
2. 3 V_{OUT} = 3.3 V

V_{IN} = 4.3 V, C_L = 1.0 µF, I_{OUT} = 1 mA ↔ 250 mA, t_r = t_f = 1.0 µs



2. 4 V_{OUT} = 5.0 V

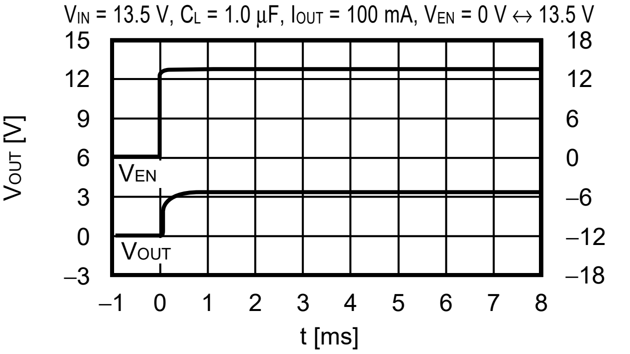
V_{IN} = 6.0 V, C_L = 1.0 µF, I_{OUT} = 1 mA ↔ 250 mA, t_r = t_f = 1.0 µs



3. Characteristics of EN pin transient response (Ta = +25°C)

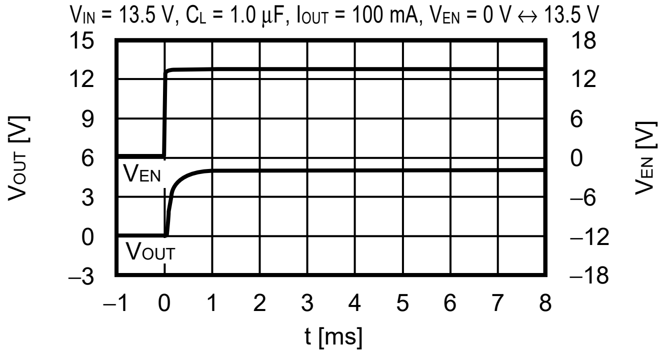
3. 1 V_{OUT} = 3.3 V

V_{IN} = 13.5 V, C_L = 1.0 µF, I_{OUT} = 100 mA, V_{EN} = 0 V ↔ 13.5 V



3. 2 V_{OUT} = 5.0 V

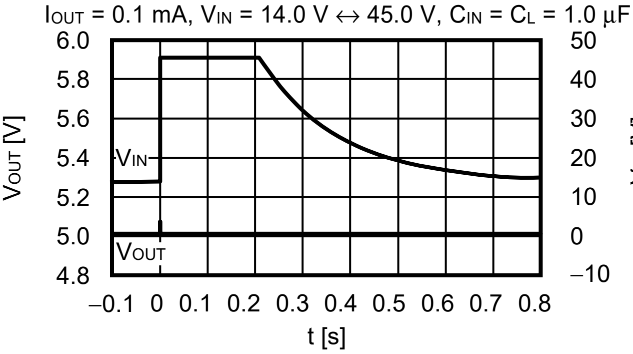
V_{IN} = 13.5 V, C_L = 1.0 µF, I_{OUT} = 100 mA, V_{EN} = 0 V ↔ 13.5 V



4. Load dump characteristics (Ta = +25°C)

4. 1 V_{OUT} = 5.0 V

I_{OUT} = 0.1 mA, V_{IN} = 14.0 V ↔ 45.0 V, C_{IN} = C_L = 1.0 µF



5. Example of equivalent series resistance vs. Output current characteristics (Ta = −40°C to +125°C)

C_{IN} = C_L = 1.0 µF, C_{DLY} = 10 nF

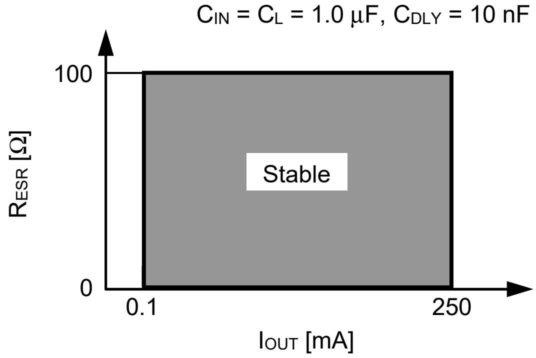
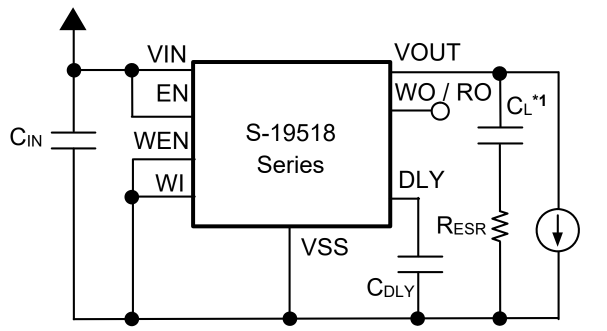


Figure 30

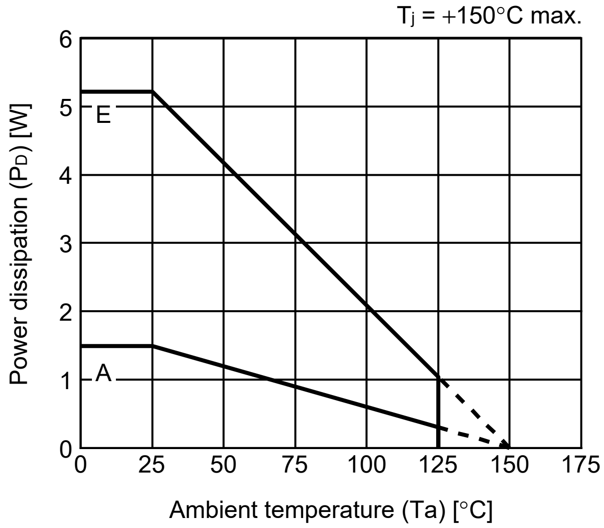


***1.** C_L: TDK Corporation CGA5L3X8R1H105K (1.0 µF)

Figure 31

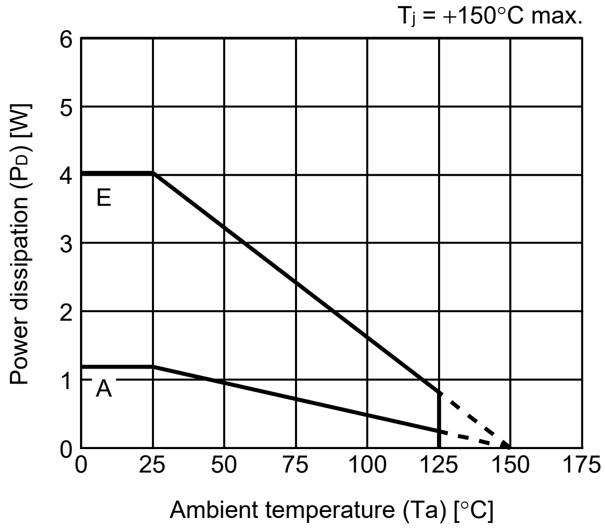
■ Power Dissipation

TO-252-9S



Board	Power Dissipation (P_D)*1
A	1.49 W
B	–
C	–
D	–
E	5.21 W

HSOP-8A



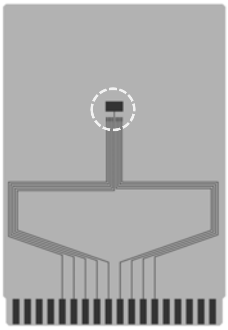
Board	Power Dissipation (P_D)*1
A	1.19 W
B	–
C	–
D	–
E	4.03 W

***1.** Measurement values when this IC is mounted on each board

TO-252-9S Test Board

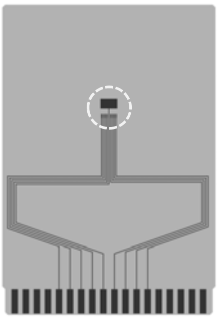
IC Mount Area

(1) Board A



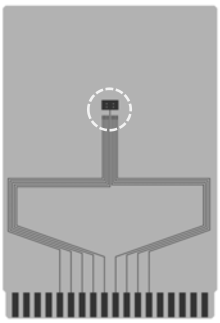
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

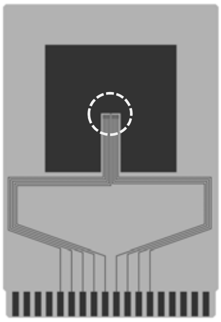
enlarged view

No. TO252-9S-A-Board-SD-1.0

TO-252-9S Test Board

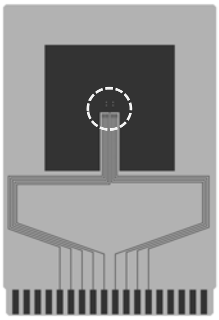
(4) **Board D**

IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) **Board E**



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

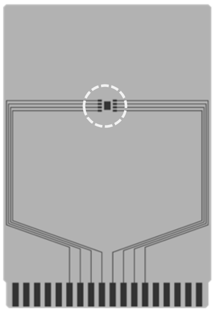
enlarged view

No. TO252-9S-A-Board-SD-1.0

HSOP-8A Test Board

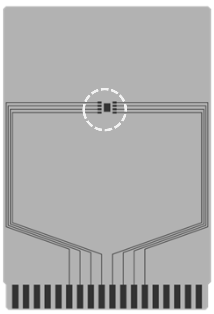
IC Mount Area

(1) Board A



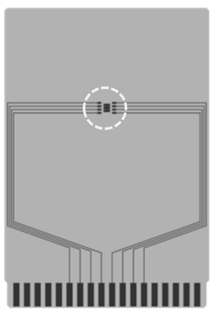
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B

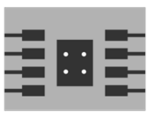


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



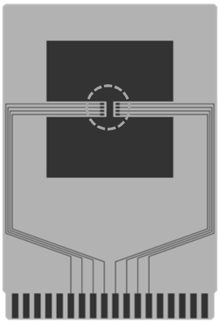
enlarged view

No. HSOP8A-A-Board-SD-1.0

HSOP-8A Test Board

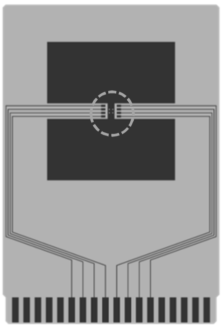
IC Mount Area

(4) Board D

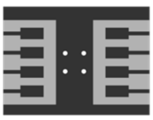


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E

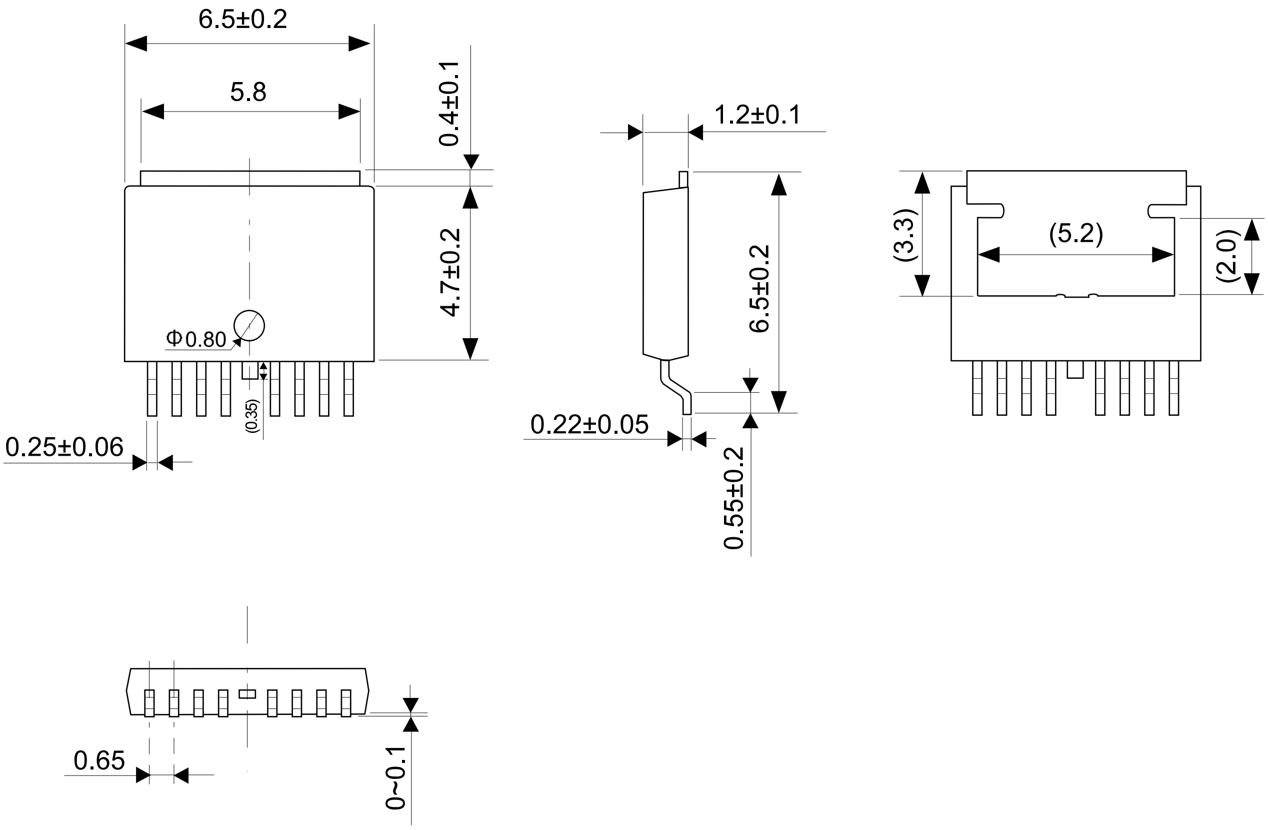


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



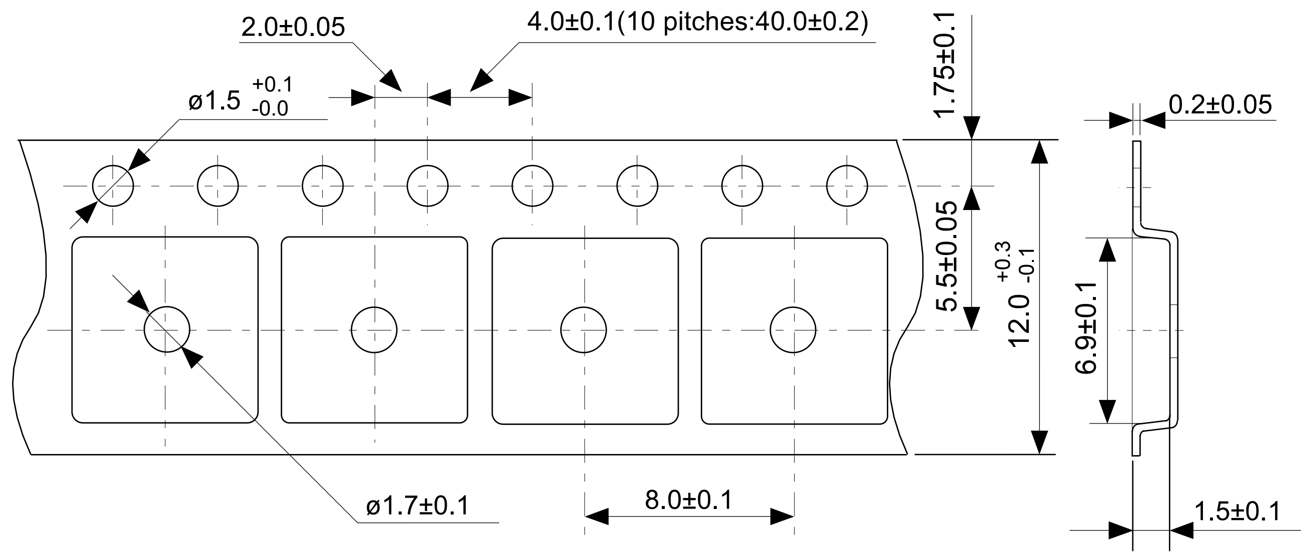
enlarged view

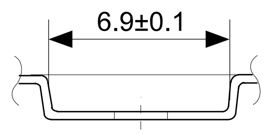
No. HSOP8A-A-Board-SD-1.0

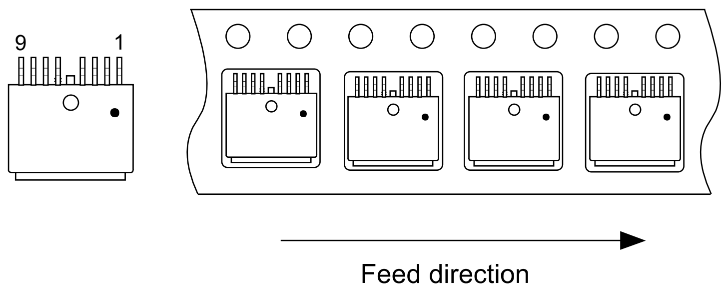


No. VA009-A-P-SD-2.0

TITLE	TO252-9S-A-PKG Dimensions
No.	VA009-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

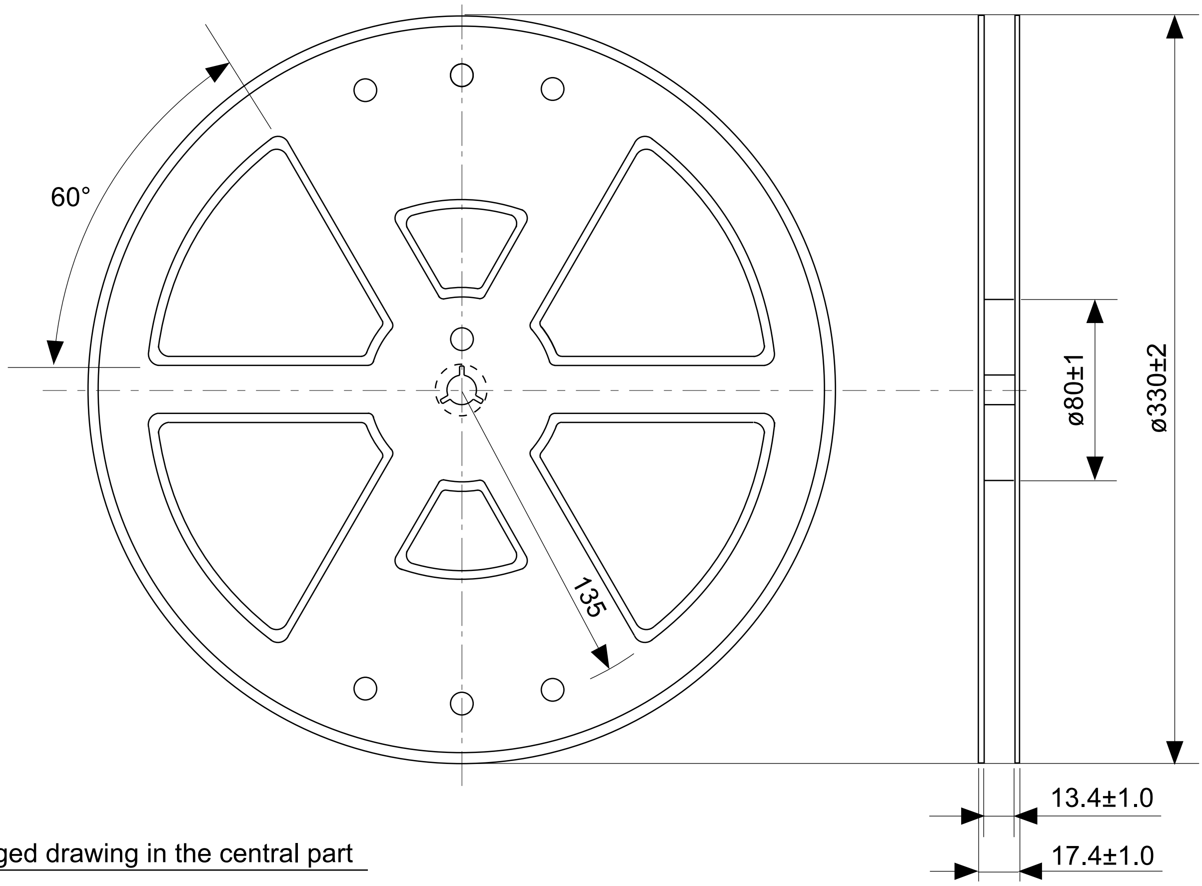




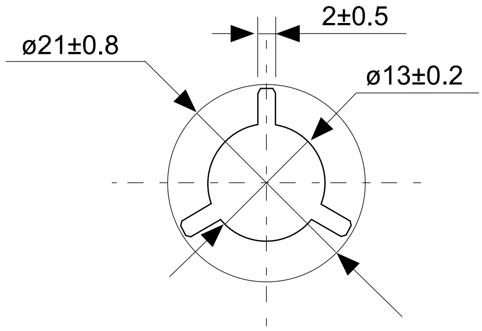


No. VA009-A-C-SD-1.0

TITLE	TO252-9S-A-Carrier Tape
No.	VA009-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



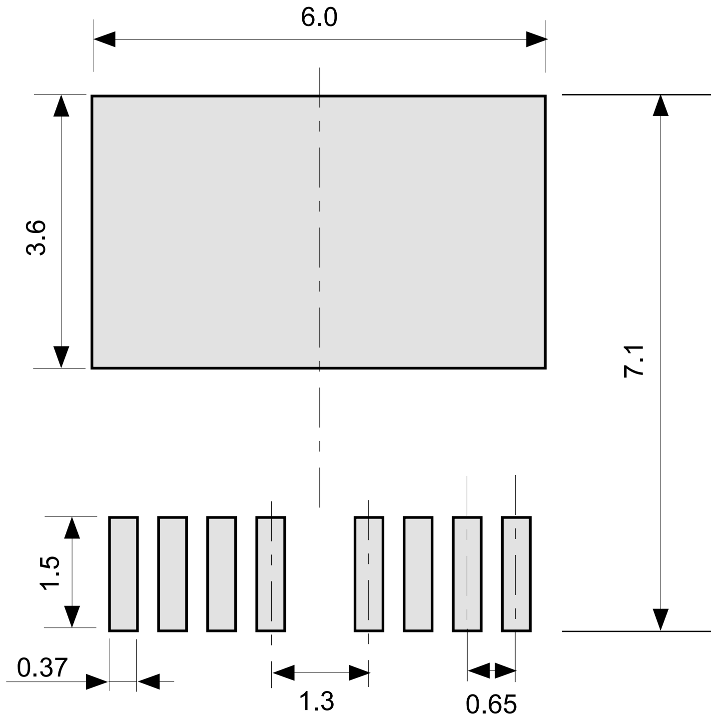
Enlarged drawing in the central part



No. VA009-A-R-SD-1.0

TITLE	TO252-9S-A-Reel		
No.	VA009-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		

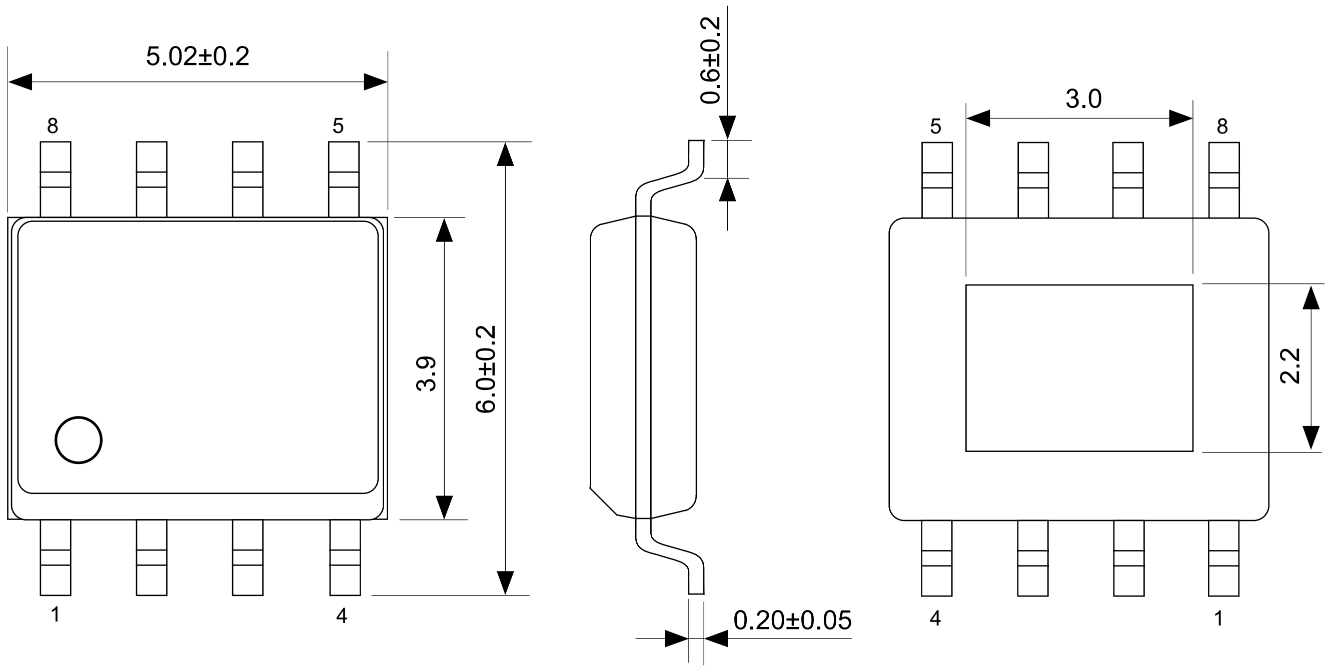
ABLIC Inc.

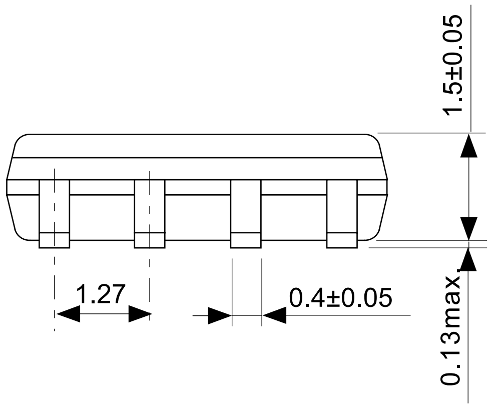


No. VA009-A-L-SD-1.0

TITLE	TO252-9S-A -Land Recommendation
No.	VA009-A-L-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.

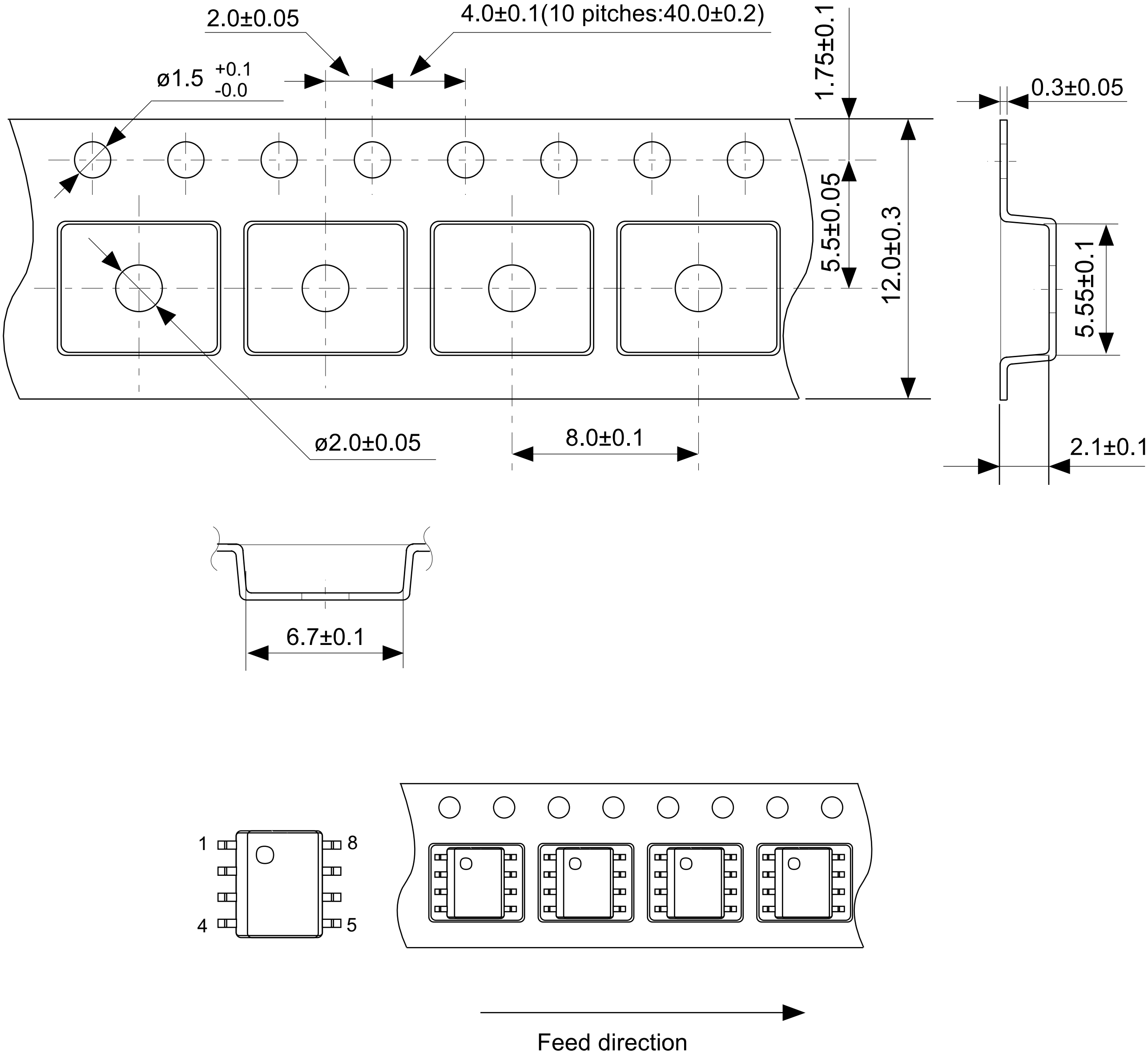




No. FH008-A-P-SD-2.0

TITLE	HSOP8A-A-PKG Dimensions
No.	FH008-A-P-SD-2.0
ANGLE	
UNIT	mm

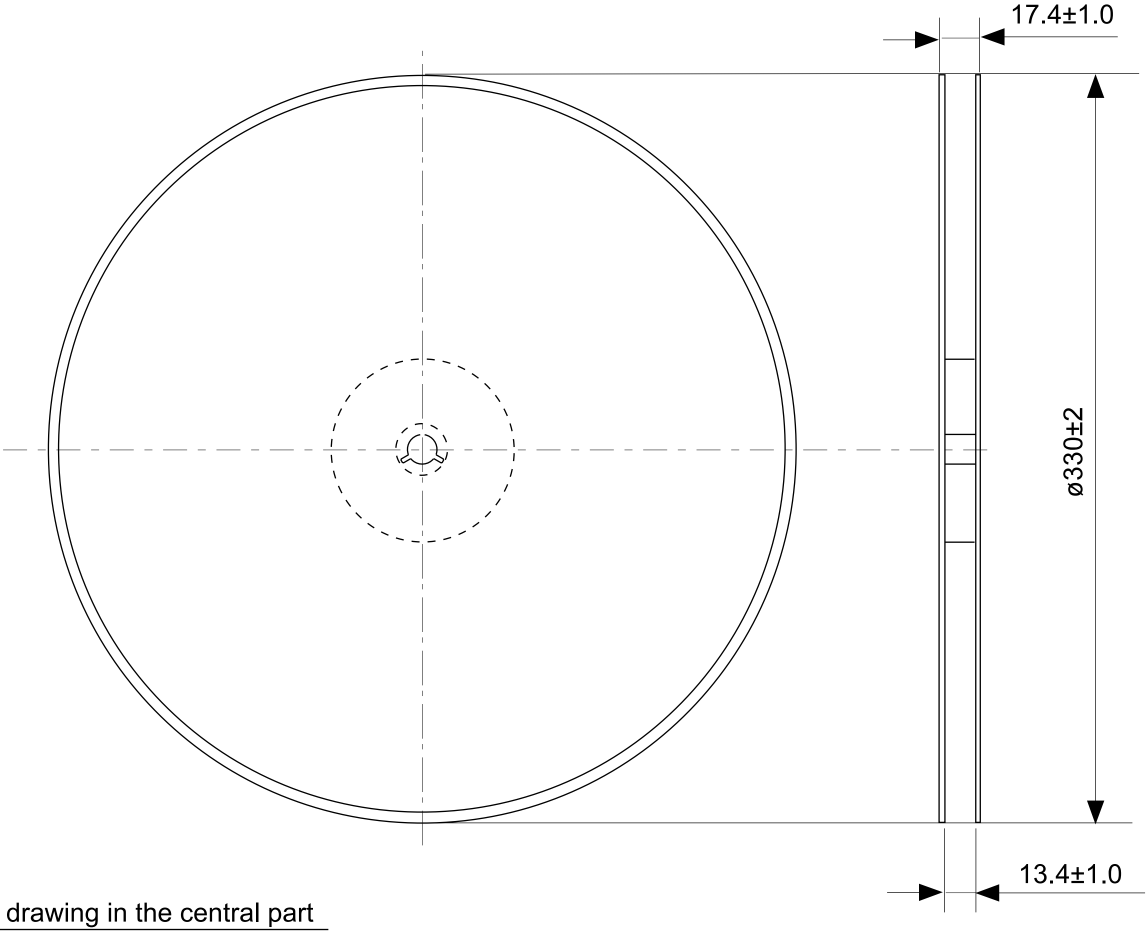
ABLIC Inc.



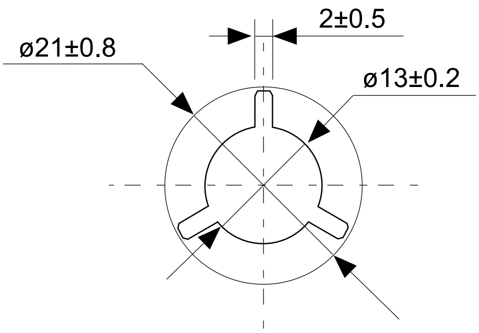
No. FH008-A-C-SD-1.0

TITLE	HSOP8A-A-Carrier Tape
No.	FH008-A-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



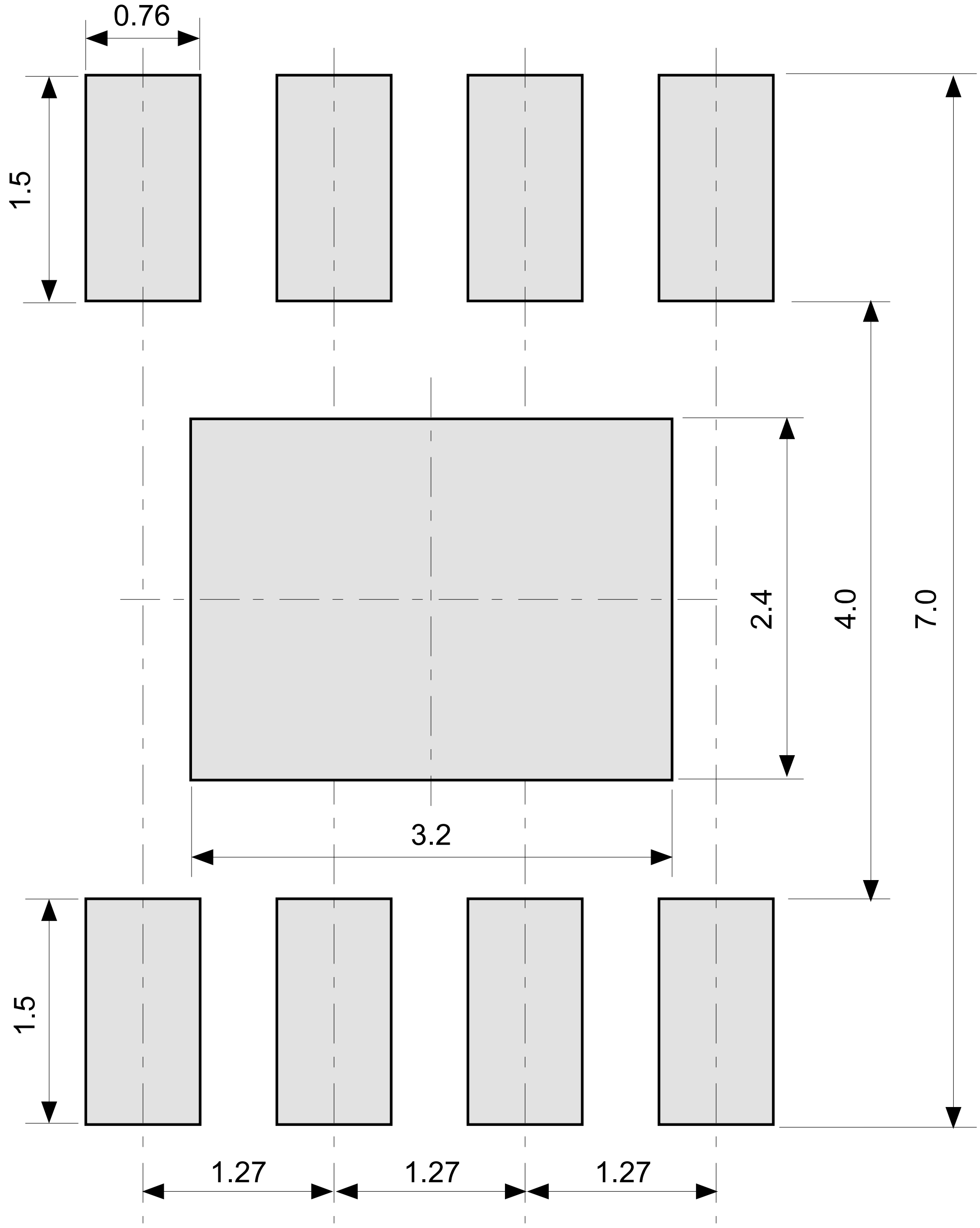
Enlarged drawing in the central part



No. FH008-A-R-SD-1.0

TITLE	HSOP8A-A-Reel		
No.	FH008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		

ABLIC Inc.



No. FH008-A-L-SD-1.0

TITLE	HSOP8A-A -Land Recommendation
No.	FH008-A-L-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.

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2.4-2019.07