



Intel® Wireless Flash Memory (W18/W30 SCSP)

32WQ and 64WQ Family with Asynchronous RAM

Datasheet

Product Features

- Device Architecture
 - Flash Density: 32-Mbit, 64-Mbit
 - Async PSRAM Density: 8-, 16-, 32-Mbit; Async SRAM Density: 4-, 8-, 16-Mbit
 - Top, Bottom or Dual flash parameter configuration
- Device Voltage
 - Flash $V_{CC} = 1.8\text{ V}$; Flash $V_{CCQ} = 1.8\text{ V}$ or 3.0 V
 - RAM $V_{CC} = 3.0\text{ V}$; RAM $V_{CCQ} = 1.8\text{ V}$ or 3.0 V
- Device Packaging
 - 88 balls (8 x 10 active ball matrix); Area: 8x10 mm; Height: 1.2 mm to 1.4 mm
- PSRAM Performance
 - 70 ns initial access, 25 ns async page reads at 1.8 V I/O
 - 70 ns initial access async PSRAM at 1.8V I/O
 - 88 ns initial access, 30 ns async page reads at 1.8 V I/O
 - 85 ns initial access, 35 ns async page reads at 3.0 V I/O
 - 70 ns initial access, 25 ns async page reads at 3.0 V I/O
- SRAM Performance
 - 70 ns initial access at 1.8 V or 3.0 V I/O
- Flash Performance
 - 65 ns initial access at 1.8 V I/O
 - 70 ns initial access at 3.0 V I/O
 - 25 ns async page at 1.8 V or 3.0 V I/O
 - 14 ns sync reads (t_{CHQV}) at 1.8 V I/O
 - 20 ns sync reads (t_{CHQV}) at 3.0 V I/O
 - Enhanced Factory Programming: 3.10 $\mu\text{s}/\text{Word}$ (Typ)
- Flash Architecture
 - Read-While-Write/Erase
 - Asymmetrical blocking structure
 - 4-KWord parameter blocks (Top or Bottom); 32-KWord main blocks
 - 4-Mbit partition size
 - 128-bit One-Time Programmable (OTP) Protection Register
 - Zero-latency block locking
 - Absolute write protection with block lock using F-VPP and F-WP#
- Flash Software
 - Intel® Flash Data Integrator (FDI) and Common Flash Interface (CFI)
- Quality and Reliability
 - Extended Temperature: $-25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
 - Minimum 100K flash block erase cycle
 - 90 nm ETOX™ IX flash technology
 - 130 nm ETOX™ VIII flash technology

The Intel® Wireless Flash Memory (W18/W30 SCSP) family offers various flash plus static RAM combinations in a common package footprint. The flash memory features 1.8 V low-power operations with flexible, multi-partition, dual-operation Read-While-Write / Read-While-Erase, asynchronous, and synchronous reads. This SCSP device integrates up to two flash die, one PSRAM die, and one SRAM die in a low-profile package compatible with other SCSP families with QUAD+ ballout.



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Intel Corporation may have patents or pending patent applications, trademarks, copyrights, or other intellectual property rights that relate to the presented subject matter. The furnishing of documents and other materials and information does not provide any license, express or implied, by estoppel or otherwise, to any such patents, trademarks, copyrights, or other intellectual property rights.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

*Other names and brands may be claimed as the property of others.

Copyright © 2005, Intel Corporation. All Rights Reserved.



- 1.0 Introduction**..... 6
 - 1.1 Nomenclature 6
 - 1.2 Conventions..... 6
- 2.0 Functional Overview** 8
 - 2.1 Block Diagram 8
 - 2.2 Flash Memory Map and Partitioning 9
- 3.0 Package Information** 11
- 4.0 Ballout and Signal Description** 13
 - 4.1 Signal Ballout..... 13
 - 4.2 Signal Descriptions 14
- 5.0 Maximum Ratings and Operating Conditions**..... 16
 - 5.1 Absolute Maximum Ratings 16
 - 5.2 Operating Conditions 17
 - 5.3 Capacitance..... 17
- 6.0 Electrical Specifications** 18
 - 6.1 DC Characteristics..... 18
- 7.0 AC Characteristics** 21
 - 7.1 Flash AC Characteristics 21
 - 7.2 SRAM AC Characteristics..... 21
 - 7.3 PSRAM AC Characteristics 24
 - 7.4 Device AC Test Conditions..... 29
- 8.0 Flash Power Consumption** 30
- 9.0 Device Operation** 31
 - 9.1 Bus Operations 31
 - 9.2 Flash Command Definitions..... 34
- 10.0 Flash Read Operations** 35
- 11.0 Flash Program Operations** 36
- 12.0 Flash Erase Operations** 37
- 13.0 Flash Security Modes**..... 38
- 14.0 Flash Read Configuration Register** 39
- 15.0 SRAM Operations** 40
 - 15.1 Power-up Sequence and Initialization 40
 - 15.2 Data Retention Mode..... 40
- 16.0 PSRAM Operations**..... 42
 - 16.1 Power-Up Sequence and Initialization..... 42
 - 16.1.1 16Mbit PSRAM Power-Up Sequence (Non-Page Mode)..... 42
 - 16.2 Standby Mode/ Deep Power-Down Mode 43
 - 16.3 PSRAM Special Read and Write Constraints 43



| | |
|--|-----------|
| Appendix A Write State Machine | 45 |
| Appendix B Common Flash Interface..... | 46 |
| Appendix C Flash Flowcharts | 47 |
| Appendix D Additional Information | 48 |
| Appendix E Ordering Information | 49 |



Revision History

| Date | Revision | Description |
|----------------|----------|---|
| June 2003 | -001 | Initial release. |
| September 2003 | -002 | Changed PSRAM Read values. Added new Transient Equivalent Testing Load Circuit figure. General text edits. |
| May 2004 | -006 | Reformatted the datasheet and moved sections around according to the new layout. |
| August 2004 | -007 | Added 90 nm product information. Added line items to Table 21 “32WQ and 64WQ W18/W30 SCSP Ordering Information (Flash Only)” on page 50 . Added DC and AC specs for the new line items and edits to related sections. |
| January 2005 | -008 | Added line items to Table 21 “32WQ and 64WQ W18/W30 SCSP Ordering Information (Flash Only)” on page 50 Added 32WQ product information. |
| June 2005 | -009 | Added line items to Table 21 “32WQ and 64WQ W18/W30 SCSP Ordering Information (Flash Only)” on page 50 |
| October 2005 | -010 | Removed Power-up sequence from Section 16; Added 70ns PSRAM (non-page mode) specification Updated Ordering Information |

1.0 Introduction

This document contains information pertaining to the products in the Intel® Wireless Flash Memory (W18/W30 SCSP) family with asynchronous RAM. The W18/W30 SCSP 32WQ and 64WQ families offer a wide variety of stacked combinations that include single flash die, two flash die, flash + PSRAM, and flash + SRAM options. This document provides information where this SCSP family differs from the Intel® Wireless Flash Memory (W18/W30) discrete device.

Refer to the discrete datasheets *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for flash product details not included in this SCSP datasheet.

1.1 Nomenclature

| | |
|----------|--|
| 0x | Hexadecimal prefix |
| 0b | Binary prefix |
| Byte | 8 bits |
| CFI | Common Flash Interface |
| CUI | Command User Interface |
| DU | Don't Use |
| ETOX | EPROM Tunnel Oxide |
| FDI | Flash Data Integrator (Intel® software solution) |
| k (noun) | 1 thousand |
| Kb | 1024 bits |
| KB | 1024 bytes |
| Kword | 1024 words |
| M (noun) | 1 million |
| Mb | 1,048,576 bits |
| MB | 1,048,576 bytes |
| OTP | One-Time Programmable |
| PLR | Protection Lock Register |
| PR | Protection Register |
| PRD | Protection Register Data |
| RCR | Read Configuration Register |
| RFU | Reserved for Future Use |
| SCSP | Stacked Chip Scale Package |
| SR | Status Register |
| SRD | Status Register Data |
| Word | 16 bits |
| WSM | Write State Machine |

1.2 Conventions

Group Membership Brackets: Square brackets are used to designate group membership or to define a group of signals with a similar function, such as A[21:1] and SR[4,1].

VCC vs. V_{CC}: When referring to a signal or package-connection name, the notation used is VCC, etc. When referring to a timing or electrical level, the notation used is subscripted such as V_{CC}, etc.



Device: This term is used interchangeably throughout this document to denote either a particular die, or the combination of multiple die within a single package.

F[3:1]-CE#, F[2:1]-OE#: This is the method used to refer to more than one chip-enable or output enable at the same time. When each is referred to individually, the reference will be F1-CE# and F1-OE# (for die #1), and F2-CE# and F2-OE# (for die #2).

F-VCC, P-VCC or S-VCC: When referencing flash memory signals or timings, the notation used is F-VCC or F-V_{CC}, respectively. When the reference is to PSRAM signals or timings, the notation is prefixed with “P-” (e.g., P-VCC, P-V_{CC}). When referencing SRAM signals or timings, the notation is prefixed with “S-” (e.g., S-VCC or S-V_{CC}). P-VCC and S-VCC are RFU for stacked combinations that do not include PSRAM or SRAM.

R-OE#, R-LB#, R-UB#, R-WE#: These are used to identify RAM OE#, LB#, UB#, WE# signals, and are usually shared between 2 or more RAM die. R-OE#, R-LB#, R-UB# and R-WE are RFU for stacked combinations that do not include PSRAM or SRAM.

2.0 Functional Overview

This section provides an overview of the features and capabilities of the Intel® Wireless Flash Memory (W18/W30 SCSP) family with asynchronous RAM device.

The W18/W30 SCSP device provides flash + RAM die combinations. Products range from single flash die, two flash die, flash + PSRAM, or flash + SRAM. You can choose a W18 SCSP device or a W30 SCSP device with SRAM or PSRAM offered with the same package footprint and signal ballout.

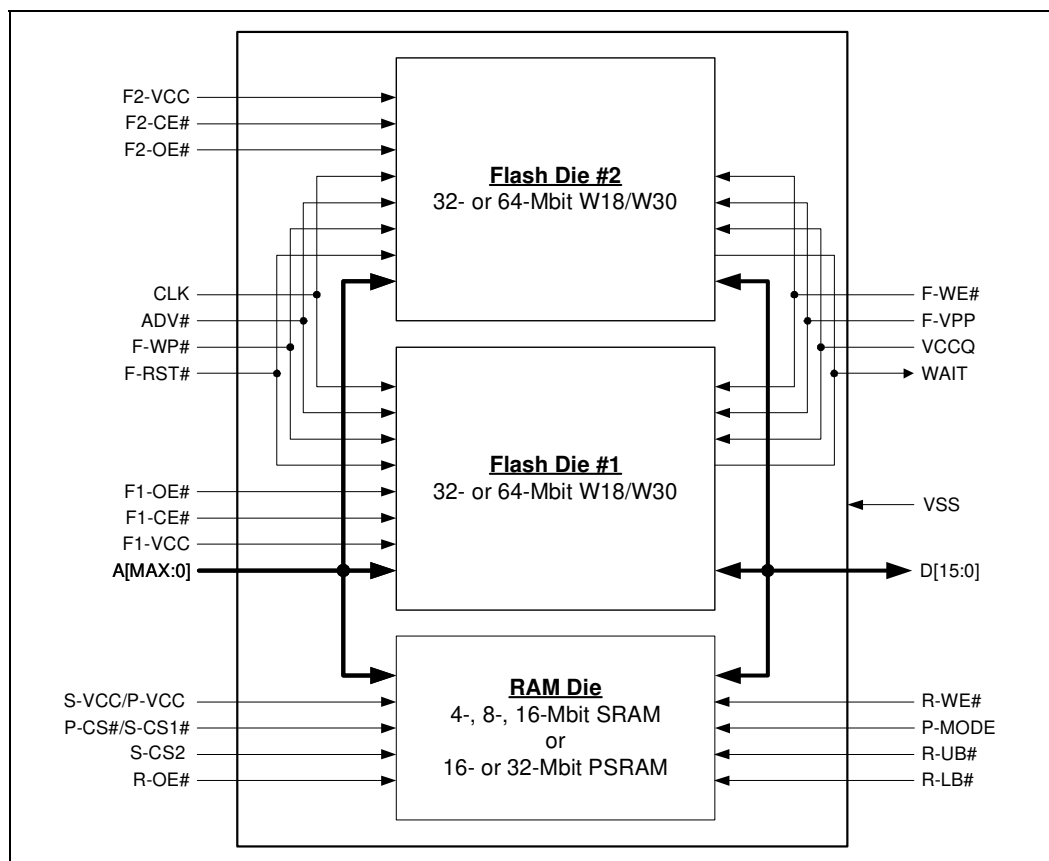
Table 21 on page 50 lists possible product combinations for the 32-Mbit and 64-Mbit W18/W30 SCSP family.

2.1 Block Diagram

Figure 1 shows all internal package connections for the SCSP family with multiple die. See Table 21 for valid combinations of flash and RAM die. Unused connections on combinations with less than three die are reserved and should not be used.

Please contact your local Intel representative for details regarding any reserved or RFU pins.

Figure 1. Block Diagram



2.2 Flash Memory Map and Partitioning

Consult the latest *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and the *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702), for individual flash die memory map and partitioning information.

Table 1 and Table 2 show memory map and partitioning information for dual-flash memory die configurations. Flash Die #1 (with F1-CE# as its Chip Select) is configured as a bottom boot while Flash Die #2 (with F2-CE# as its Chip Select) is configured as top boot.

Table 1. 64-Mbit Flash + 32-Mbit Flash Die W18/W30 SCSP Memory Map and Partitioning

| Partitioning | | | Block Size (KW) | Block # | Address Range |
|---------------------------|---------------------|-----------------|-----------------|---------|----------------|
| Flash Die #2 (32-Mbit) | Parameter Partition | Partition 0 | 4 | 63-70 | 1F8000-1FFFFFF |
| | | | 32 | 56-62 | 1C0000-1F7FFF |
| | Main Partitions | Partition 1 | 32 | 48-55 | 180000-1BFFFF |
| | | Partition 2 | 32 | 40-47 | 140000-17FFFF |
| | | Partition 3 | 32 | 32-39 | 100000-13FFFF |
| | | Partitions 4-7 | 32 | 0-31 | 000000-0FFFFFF |
| Flash Die #1 (64-Mbit) | Main Partitions | Partitions 8-15 | 32 | 71-134 | 200000-3FFFFFF |
| | | Partitions 4-7 | 32 | 39-70 | 100000-1FFFFFF |
| | | Partition 3 | 32 | 31-38 | 0C0000-0FFFFFF |
| | | Partition 2 | 32 | 23-30 | 080000-0BFFFF |
| | | Partition 1 | 32 | 15-22 | 040000-07FFFF |
| | Parameter Partition | Partition 0 | 32 | 8-14 | 008000-03FFFF |
| | | | 4 | 0-7 | 000000-007FFF |

Table 2. 64-Mbit Dual-Flash Die W18/W30 SCSP Memory Map and Partitioning

| Partitioning | | | Block Size (KW) | Block # | Address Range |
|-------------------------|---------------------|-----------------|-----------------|---------|----------------|
| Top Parameter | Parameter Partition | Partition 0 | 4 | 127-134 | 3F8000-3FFFFFF |
| | | | 32 | 120-126 | 3C0000-3F7FFF |
| | Main Partitions | Partition 1 | 32 | 112-119 | 380000-3BFFFF |
| | | Partition 2 | 32 | 104-111 | 340000-37FFFF |
| | | Partition 3 | 32 | 96-103 | 300000-33FFFF |
| | | Partitions 4-7 | 32 | 64-95 | 200000-2FFFFFF |
| | | Partitions 8-15 | 32 | 0-63 | 000000-1FFFFFF |
| Bottom Parameter | Main Partitions | Partitions 8-15 | 32 | 71-134 | 200000-3FFFFFF |
| | | Partitions 4-7 | 32 | 39-70 | 100000-1FFFFFF |
| | | Partition 3 | 32 | 31-38 | 0C0000-0FFFFFF |
| | | Partition 2 | 32 | 23-30 | 080000-0BFFFF |
| | | Partition 1 | 32 | 15-22 | 040000-07FFFF |
| | Parameter Partition | Partition 0 | 32 | 8-14 | 008000-03FFFF |
| | | | 4 | 0-7 | 000000-007FFF |

3.0 Package Information

The following packages are offered with the 32WQ and 64WQ Family:

- Figure 2, “Mechanical Specifications for 1- or 2-Die SCSP Device (8x10x1.2 mm)”
- Figure 3, “Mechanical Specifications for Triple-Die SCSP Device (8x10x1.4 mm)”

Figure 2. Mechanical Specifications for 1- or 2-Die SCSP Device (8x10x1.2 mm)

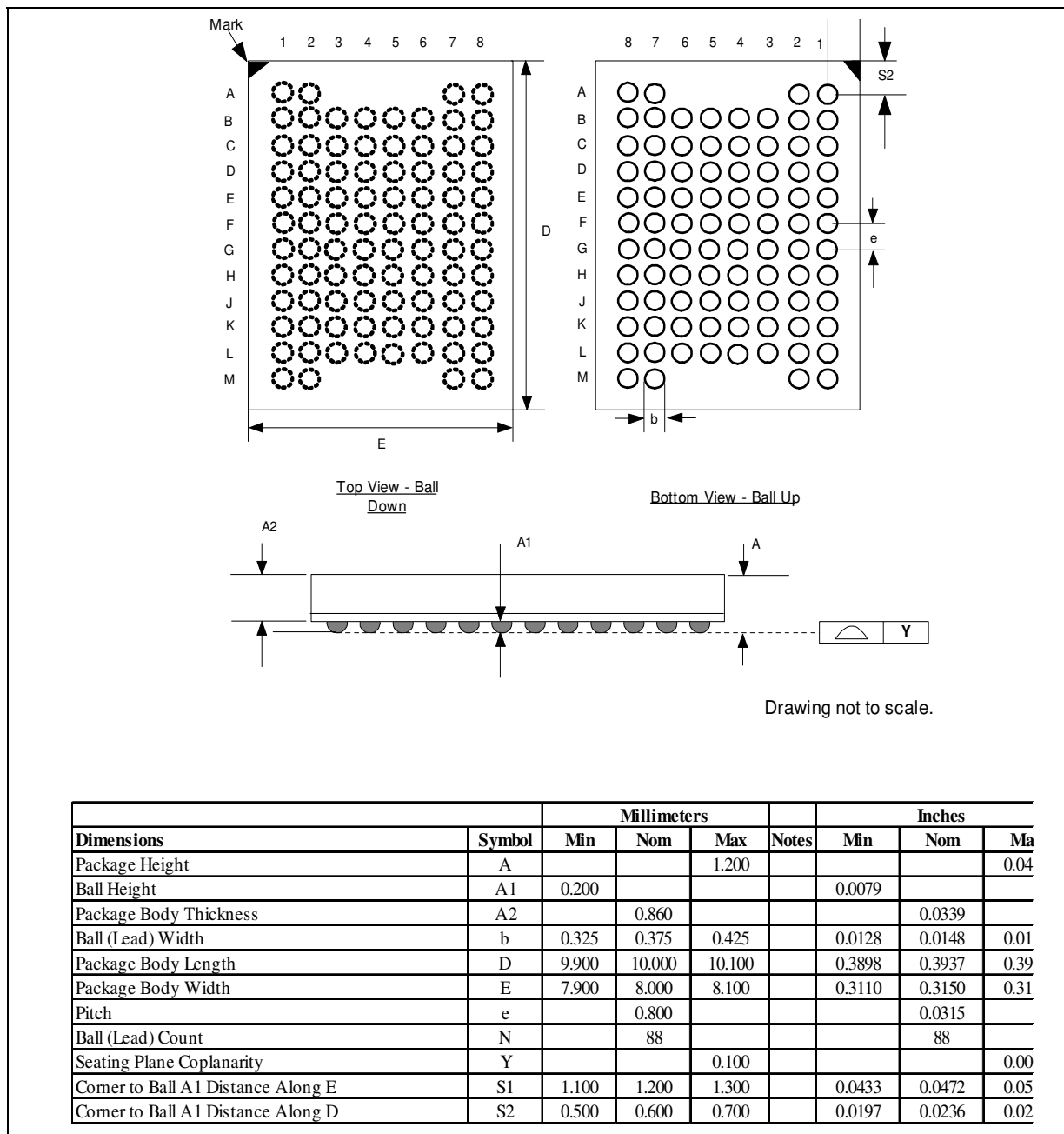
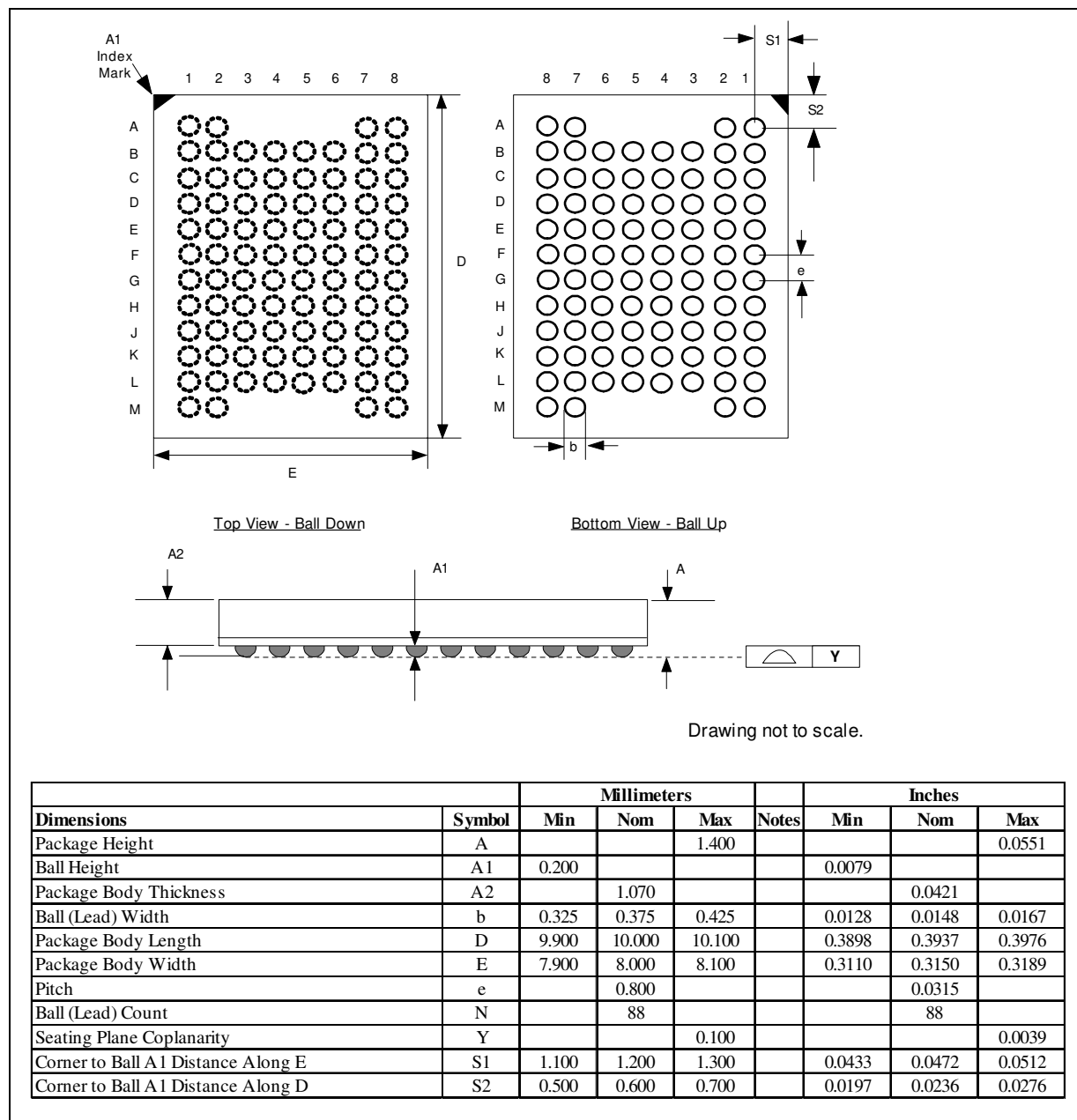


Figure 3. Mechanical Specifications for Triple-Die SCSP Device (8x10x1.4 mm)

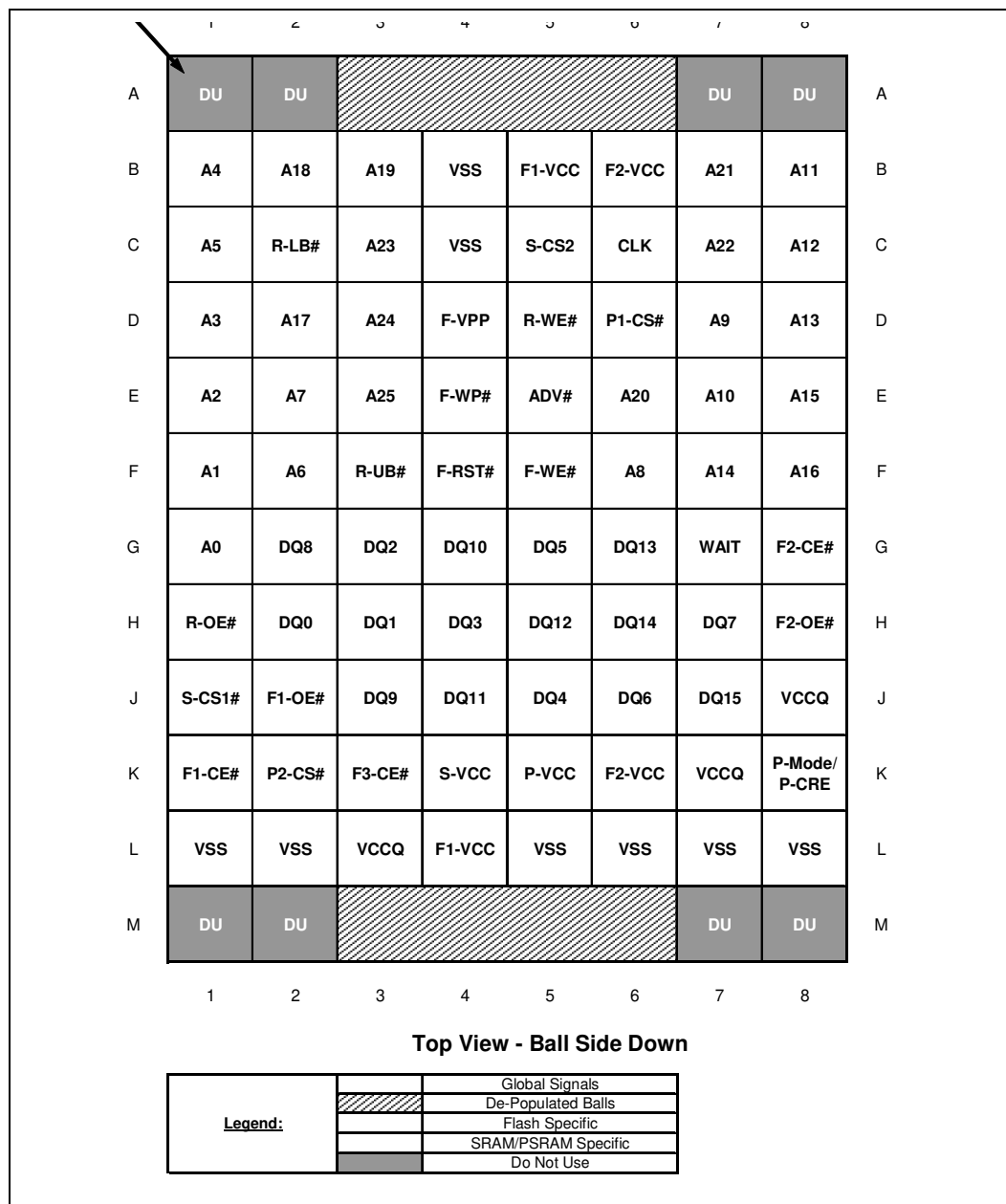


4.0 Ballout and Signal Description

4.1 Signal Ballout

Figure 4 shows the 32WQ and 64WQ W18/W30 SCSP family 88-ball (8x10 active ball matrix) device.

Figure 4. 88-Ball (8x10 Active Ball Matrix) QUAD+ Ballout



4.2 Signal Descriptions

Table 3 describes active signals used on the 32WQ and 64WQ W18/W30 SCSP family.

Table 3. Signal Descriptions (Sheet 1 of 2)

| Symbol | Type | Name and Function |
|-----------------|--------------|---|
| A[21:0] | Input | <p>ADDRESS INPUTS: Inputs for all die addresses during read and write operations. Addresses are internally latched during write operations.</p> <ul style="list-style-type: none"> • 4-Mbit: A[17:0] • 8-Mbit: A[18:0] • 16-Mbit: A[19:0] • 32-Mbit: A[20:0] • 64-Mbit: A[21:0] <p>A0 is the lowest-order word address. A[25:22] denote high-order addresses reserved for future device densities</p> |
| D[15:0] | Input/Output | <p>DATA INPUTS/OUTPUTS: Inputs data and commands during write cycles; outputs data during read cycles. Data signals float when the device or its outputs are deselected. Data are internally latched during writes.</p> |
| CLK | Input | <p>FLASH CLOCK: CLK synchronizes the selected flash die to the memory bus frequency in synchronous-read mode. During synchronous read operations, the initial address is latched on the rising edge of ADV#, or the rising/ falling edge of CLK when ADV# is low, whichever occurs first. CLK is only used in synchronous-read mode. Refer to the flash discrete product datasheet for information on how to use this signal in asynchronous-read mode.</p> |
| ADV# | Input | <p>FLASH ADDRESS VALID: Low-true; During synchronous read operations, the initial address is latched on the rising edge of ADV#, or the rising/ falling edge of CLK when ADV# is low, whichever occurs first. Refer to the flash discrete product datasheet for information on how to use this signal in asynchronous-read mode.</p> |
| WAIT | Output | <p>FLASH WAIT: When asserted, WAIT indicates invalid data from the selected flash die on D[15:0]. WAIT is High-Z whenever the flash die is deselected ($CE\# = V_{IL}$). WAIT is not gated by OE#.</p> <p>WAIT is only used in synchronous array-read mode. Refer to the flash discrete product datasheet for information on how to use this signal in asynchronous-read mode.</p> |
| F[3:1]-CE# | Input | <p>FLASH CHIP ENABLE: Low-true; CE#-low selects the associated flash memory die. When asserted, flash internal control logic, input buffers, decoders, and sense amplifiers are active. When deasserted, the associated flash die is deselected; power is reduced to standby levels, data and WAIT outputs are placed in High-Z.</p> <p>F1-CE# selects flash die #1; F2-CE# selects flash die #2 and is RFU on combinations with only one flash die. F3-CE# selects flash die #3 and is RFU on SCSP combinations with only one or two flash die.</p> |
| S-CS1# S-CS2 | Input | <p>SRAM CHIP SELECTS: When both SRAM chip selects are asserted, SRAM internal control logic, input buffers, decoders, and sense amplifiers are active. When either/both SRAM chip selects are deasserted ($S-CS1\# = V_{IH}$ and/or $S-CS2 = V_{IL}$), the SRAM is deselected and its power is reduced to standby levels.</p> <p>S-CS1# and S-CS2 are only available on SCSP combinations with SRAM die.</p> |
| P[2:1]-CS# | Input | <p>PSRAM CHIP SELECTS: Low-true; When asserted, PSRAM internal control logic, input buffers, decoders, and sense amplifiers are active. When deasserted, the PSRAM is deselected and its power is reduced to standby levels.</p> <p>P1-CS# selects PSRAM die #1 and is available only on SCSP combinations with PSRAM die. This ball is RFU on SCSP combinations without PSRAM. P2-CS# selects PSRAM die #2 and is available only on SCSP combinations with two PSRAM die. This ball is RFU on SCSP combinations without PSRAM or with a single PSRAM.</p> |

Table 3. Signal Descriptions (Sheet 2 of 2)

| Symbol | Type | Name and Function |
|-----------------|-------|--|
| F[2:1]-OE# | Input | FLASH OUTPUT ENABLE: Low-true; OE#-low enables the flash output buffers. OE#-high disables the flash output buffers, and places the flash outputs in High-Z. F1-OE# controls the outputs of flash die #1; F2-OE# controls the outputs of flash die #2 and #3, and is available only on SCSP combinations with two or three flash die and is RFU on SCSP combinations with only one flash die. |
| R-OE# | Input | RAM OUTPUT ENABLE: Low-true; R-OE#-low enables the RAM output buffers. R-OE#-high disables the RAM output buffers, and places the RAM outputs in High-Z. R-OE# is only available on SCSP combinations with RAM die. |
| R-UB# R-LB# | Input | RAM UPPER/ LOWER BYTE ENABLES: Low-true; During RAM reads, R-UB#-low enables the RAM high-order bytes on D[15:8], and R-LB#-low enables the RAM low-order bytes on D[7:0]. R-UB# and R-LB# are only available on SCSP combinations with either SRAM die or PSRAM die. |
| F-WE# | Input | FLASH WRITE ENABLE: Low-true; WE# controls writes to the selected flash die. Address and data are latched on the rising edge of WE#. |
| R-WE# | Input | RAM WRITE ENABLE: Low-true; R-WE# controls writes to the RAM die. R-WE# is only available on SCSP combinations with RAM die. |
| F-WP# | Input | FLASH WRITE PROTECT: Low-true; WP# enables/disables the lock-down protection mechanism of the flash die. WP#-low enables the lock-down mechanism- locked down blocks cannot be unlocked with software commands. WP#-high disables the lock-down mechanism, allowing locked down blocks to be unlocked with software commands. |
| F-RST# | Input | FLASH RESET: Low-true; RST#-low initializes flash internal circuitry and disables flash operations. RST#-high enables flash operation. Exit from reset places the flash in asynchronous read array mode. |
| F-VPP F-VPEN | Power | FLASH PROGRAM/ ERASE POWER: A valid F-V _{PP} voltage on this ball enables flash program/erase operations. Flash memory array contents cannot be altered when F-V _{PP} (V _{PEN}) < V _{PPLK} (V _{PENLK}). Erase/ program operations at invalid F-V _{PP} (V _{PEN}) voltages should not be attempted. Refer to the flash discrete product datasheet for additional details. F-V _{PEN} (Erase/Program/Block Lock Enables) is not available for W18/W30 products. |
| P-MODE | Input | PSRAM MODE: Low-true; P-MODE is used to enter/exit low power mode. Low power mode is not applicable to 38F2020W0ZTQ1, 38F2020W0ZBQ1, 38F2030W0YTQ1, 38F2030W0YBQ1, 38F2030W0ZTQ2, 38F2030W0ZBQ2, 38F1030W0ZTQ0, 38F1030W0ZBQ0, 38F1030W0YTQE, 38F1030W0YBQE. P-Mode is only available on SCSP combinations with PSRAM die. |
| F[2:1]-VCC | Power | FLASH LOGIC Power: F1-VCC supplies power to the core logic of flash die #1; F2-VCC supplies power to the core logic of flash die #2 and #3. Write operations are inhibited when F-V _{CC} < V _{LKO} . Device operations at invalid F-V _{CC} voltages should not be attempted. F2-VCC is only available on SCSP combinations with two or three flash die, and is RFU on SCSP combinations with only one flash die. |
| S-VCC | Power | SRAM Power Supply: Supplies power to the SRAM die. S-VCC is only available on SCSP combinations with SRAM die. |
| P-VCC | Power | PSRAM Power Supply: Supplies power to the PSRAM die. P-VCC is only available on SCSP combinations with PSRAM die. |
| VCCQ | Power | FLASH OUTPUT-BUFFER Power: Supplies power for the I/O output buffers. |
| VSS | Power | Ground: Connect to ground. Do not float any VSS connection. |
| RFU | — | Reserved for Future Use: Reserve for future device functionality/ enhancements. |
| DU | — | Do Not Use: Do not connect to any other signal, or power supply; must be left floating. |

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 4. Absolute Maximum Ratings

| Parameter | | Min | Max | Unit | Notes |
|---|-----------|------|-------|------|---------|
| Temperature under Bias Expanded | | -25 | +85 | °C | 7 |
| Storage Temperature | | -55 | +125 | °C | |
| Voltage On Any Signal (except F[2:1]-V _{CC} , V _{CCQ} , F-V _{PP} , S-V _{CC} and P-V _{CC}) | 1.8 V I/O | -0.2 | +2.45 | V | 1,2,3 |
| | 3.0 V I/O | -0.2 | +3.6 | V | 2,3 |
| F[2:1]-V _{CC} Voltage | | -0.5 | +2.45 | V | 2,3 |
| V _{CCQ} , S-V _{CC} and P-V _{CC} Voltage | 1.8 V I/O | -0.2 | +2.45 | V | 1,2,3 |
| | 3.0 V I/O | -0.2 | +3.6 | V | 2,3 |
| F-V _{PP} Voltage | | -0.2 | +14.0 | V | 2,3,4,5 |
| I _{SH} Output Short Circuit Current | | - | 100 | mA | 6 |

Notes:

- 90 nm is only avail with the 1.8 V I/O.
- All Specified voltages are relative to V_{SS}. Minimum DC voltage is -0.2 V on input/output signals, -0.2 V on F[2:1]-V_{CC} and F-V_{PP} signals. For 90 nm devices, during transitions, this level may overshoot to -1.5 V for periods < 20 ns, during transitions, may overshoot to F-V_{CC} + 1.5 V for periods < 20 ns.
- All Specified voltages are relative to V_{SS}. Minimum DC voltage is -0.2 V on input/output signals, -0.2 V on F[2:1]-V_{CC} and F-V_{PP} signals. For 130 nm devices, during transitions, this level may overshoot to -2 V for periods < 20 ns, during transitions, may overshoot to F-V_{CC} + 2 V for periods < 20 ns.
- Maximum DC voltage on F-V_{PP} may overshoot to +14.0 V for periods < 20 ns.
- F-V_{PP} program voltage is normally V_{PPL}. The maximum DC voltage on F-V_{PP} may overshoot to +14 V for periods < 20 ns. F-V_{PP} can be V_{PPH} for 1000 erase cycles on main blocks, 2500 cycles on parameter blocks.
- Output shorted for no more than one second. No more than one output shorted at a time.
- Devices available with -30° C temperature specifications are: 38F2020W0ZTQ1, 38F2020W0ZBQ1, 38F2030W0YTQ1, 38F2030W0YBQ1, 38F2030W0ZTQ2, 38F2030W0ZBQ2, 38F1030W0ZTQ0, 38F1030W0ZBQ0, 38F1030W0YTQE, 38F1030W0YBQE,

5.2 Operating Conditions

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 5. Operating Conditions

| Symbol | Parameter | Flash + Flash | | Flash + SRAM | | Flash + PSRAM | | Unit | Notes | |
|---|-------------------------------|---------------|------|--------------|------|---------------|------|------|-------|--|
| | | Min | Max | Min | Max | Min | Max | | | |
| T_C | Operating Temperature | -25 | +85 | -25 | +85 | -25 | +85 | °C | 2 | |
| $F-V_{CC}$ | Flash Supply Voltage | 1.7 | 1.95 | 1.7 | 1.95 | 1.7 | 1.95 | V | | |
| V_{CCQ} $S-V_{CC}$ $P-V_{CC}$ | Flash I/O Voltage | 3.0 V I/O | 2.2 | 3.3 | 2.2 | 3.3 | 2.7 | 3.1 | V | |
| | PSRAM and SRAM Supply Voltage | 1.8 V I/O | 1.7 | 1.95 | 1.7 | 1.95 | 1.8 | 1.95 | V | |
| V_{PPL} | Flash Program Logic Level | 0.9 | 1.95 | 0.9 | 1.95 | 0.9 | 1.95 | V | | |
| V_{PPH} | Flash Factory Program Voltage | 11.4 | 12.6 | 11.4 | 12.6 | 11.4 | 12.6 | V | 1 | |
| <p>Note:</p> <ol style="list-style-type: none"> 1. $F-V_{PP}$ is normally V_{PPL}. $F-V_{PP}$ can be connected to 11.4 V–12.6 V for 1000 cycles on main blocks for extended temperatures and 2500 cycles on parameter blocks at extended temperature. 2. Devices available with -30° C temperature specifications are: 38F2020W0ZTQ1, 38F2020W0ZBQ1, 38F2030W0YTQ1, 38F2030W0YBQ1, 38F2030W0ZTQ2, 38F2030W0ZBQ2, 38F1030W0ZTQ0, 38F1030W0ZBQ0, 38F1030W0YTQE, 38F1030W0YBQE,. | | | | | | | | | | |

5.3 Capacitance

NOTICE: Refer to the *1.8-Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) and *1.8-Volt Intel® Wireless Flash Memory with 3 Volt I/O Datasheet* (order number 290702) for flash capacitance details. For SCSP products with two flash die, flash capacitances for each of the flash die need to be considered accordingly.

Table 6. SRAM, PSRAM Capacitance

| Symbol | Parameter | Typ | Unit | Condition |
|-----------|--------------------|-----|------|--|
| C_{IN} | Input Capacitance | 10 | pF | $V_{IN} = 0.0\text{ V}$, $T_C = 25\text{ °C}$, $f = 1\text{ MHz}$ |
| C_{OUT} | Output Capacitance | 10 | pF | $V_{OUT} = 0.0\text{ V}$, $T_C = 25\text{ °C}$, $f = 1\text{ MHz}$ |

6.0 Electrical Specifications

6.1 DC Characteristics

SRAM and PSRAM DC characteristics are shown in [Table 7](#) and [Table 8](#). Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and the *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for flash DC characteristics.

Table 7. SRAM DC Characteristics

| Parameter | Description | Test Conditions | 1.8 V SRAM | | 3.0 V SRAM | | Unit | |
|-------------------|--|---|-------------------------|------------------------|------------------------|------------------------|------|----|
| | | | Min | Max | Min | Max | | |
| S-V _{CC} | Voltage Range | | 1.7 | 1.95 | 2.2 | 3.3 | V | |
| V _{DR} | V _{CC} for Data Retention | | 1.0 | – | 1.5 | – | V | |
| I _{CC} | Operating Current at min cycle time | I _{IO} = 0 mA | 4M | – | 25 | – | 45 | mA |
| | | | 8M | – | 35 | – | 50 | |
| | | | 16M | – | 40 | – | 55 | |
| I _{CC2} | Operating Current at max cycle time (1 μs) | I _{IO} = 0 mA | 4M | – | 4 | – | 10 | mA |
| | | | 8M | – | 6 | – | 10 | |
| | | | 16M | – | 10 | – | 15 | |
| I _{SB} | Standby Current | S-CS1# ≥ S-V _{CC} -0.2V or S-CS2 ≤ V _{SS} +0.2V Address/Data toggling at minimum cycle time | 4M | – | 12 | – | 15 | μA |
| | | | 8M | – | 20 | – | 25 | |
| | | | 16M | – | 30 | – | 45 | |
| I _{DR} | Current in Data Retention mode | 1.8 V SRAM: S-V _{CC} = 1.0 V 3.0 V SRAM: S-V _{CC} = 1.5 V | 4M | – | 6 | – | 5 | μA |
| | | | 8M | – | 10 | – | 12 | |
| | | | 16M | – | 18 | – | 15 | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -100 μA | S-V _{CC} -0.15 | – | S-V _{CC} -0.1 | – | V | |
| V _{OL} | Output LOW Voltage | I _{OL} = 100 μA, V _{CCMIN} | -0.1 | 0.2 | -0.1 | 0.1 | V | |
| V _{IH} | Input HIGH Voltage | | S-V _{CC} -0.4 | S-V _{CC} +0.2 | S-V _{CC} -0.4 | S-V _{CC} +0.2 | V | |
| V _{IL} | Input LOW Voltage | | -0.2 | 0.4 | -0.2 | 0.6 | V | |
| I _{OH} | Output HIGH Current | | – | – | – | – | mA | |
| I _{OL} | Output LOW Current | | – | – | – | – | mA | |
| *I _{IL} | Input Leakage Current | -0.2 < V _{IN} < S-V _{CC} + 0.2 V | -1 | +1 | -1 | +1 | μA | |
| *I _{LDR} | Input Leakage Current in Data Retention Mode | -0.2 < V _{IN} < S-V _{CC} + 0.2 V S-V _{CC} = V _{DR} | -1 | +1 | -1 | +1 | μA | |

* Input leakage currents include Hi-Z output leakage for bi-directional buffers with tri-state outputs.

Table 8. PSRAM DC Characteristics

| Parameter | Description | Test Conditions | 1.8 V PSRAM | | 3.0 V PSRAM | | Unit | Note | |
|-----------|---|---|-------------------|-------------------|-------------------|-------------------|------|---------|------|
| | | | Min | Max | Min | Max | | | |
| V_{CC} | Voltage Range | | 1.8 | 1.95 | 2.7 | 3.1 | V | | |
| I_{CC} | Operating Current at min cycle time | $I_{IO} = 0$ mA | 8M | – | – | – | 30 | mA | 2 |
| | | | 16M | – | 30 | – | 35 | | |
| | | | 16M | – | 20 | – | – | mA | 3 |
| | | | 32M | – | 35 | – | 45 | | |
| I_{CC2} | Operating Current at max cycle time (1 μ s) | $I_{IO} = 0$ mA | 8M | – | – | – | 5 | mA | 2 |
| | | | 16M | – | 5 | – | 7 | | |
| | | | 32M | – | – | – | 7 | | |
| I_{SB} | Standby Current | P-CS# \geq P- V_{CC} -0.2V. All inputs stable (either high or low) | 8M | – | – | – | 80 | μ A | 2, 4 |
| | | | 16M | – | 100 | – | 100 | | |
| | | P-CS# \geq P- V_{CC} -0.2V or P-Mode \geq P- V_{CC} -0.2V Address/Data toggling at minimum cycle time | 16M | – | – | – | 85 | μ A | 2, 5 |
| | | | 32M | – | 100 | – | 100 | | |
| I_{sbd} | Deep Power-Down | P-Mode \leq 0.2 V | 16M | – | – | – | 10 | μ A | 2, 4 |
| | | | 32M | – | 30 | – | 10 | | |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -0.5$ mA | 0.8P - V_{CC} | – | 2.4 | – | V | 4 | |
| | | $I_{OH} = -0.1$ mA | 1.4 | – | P- V_{CC} - 0.3 | – | V | 5 | |
| V_{OL} | Output LOW Voltage | $I_{OL} = 1$ mA, | – | 0.2P - V_{CC} | – | 0.4 | V | 4 | |
| | | $I_{OL} = 0.1$ mA, V_{CCMin} | -0.1 | 0.2 | -0.1 | 0.3 | V | 5 | |
| V_{IH} | Input HIGH Voltage | | 0.8P - V_{CC} | P- V_{CC} + 0.3 | P- V_{CC} - 0.3 | P- V_{CC} + 0.2 | V | 4 | |
| | | | P- V_{CC} - 0.3 | P- V_{CC} + 0.2 | P- V_{CC} - 0.4 | P- V_{CC} + 0.2 | V | 5 | |
| V_{IL} | Input LOW Voltage | | -0.3 | 0.2P - V_{CC} | -0.2 | 0.5 | V | 4 | |
| | | | -0.2 | 0.4 | -0.2 | 0.6 | V | 5 | |

Table 8. PSRAM DC Characteristics

| | | | | | | | | |
|----------|------------------------|---|----|----|----|----|---------------|------|
| I_{IL} | Input Leakage Current | $-0.2 < V_{IN} < P-V_{CC} + 0.2 \text{ V}$ | -1 | +1 | -1 | +1 | μA | 1, 2 |
| I_{OL} | Output Leakage Current | $-0.2 < V_{IN} < P-V_{CC} + 0.2 \text{ V}$ $P-V_{CC} = V_{DR}$ | -1 | +1 | -1 | +1 | μA | 1, 2 |

Notes:

1. Input Leakage currents include Hi-Z output leakage for bi-directional buffers with tri-state outputs.
2. All currents are in RMS unless noted otherwise.
3. Applicable only to parts 38F1030W0YxQF & 38F2030W0YxQF
4. Applicable to parts with P-Mode pin (38F2030W0ZxQ1, 38F2040W0YxQ0, 28F2240WWYxQ0).
5. Applicable to No-P-Mode (38F1030W0YxQE, 38F1030W0YxQ2, 38F1030W0ZxQ0, 38F2030W0YxQ1, 38F2030W0YxQE, 38F2030W0YxQ2, 38F2030W0YxQF, 38F2030W0ZxQ2, 38F2040W0ZxQ0)

7.0 AC Characteristics

7.1 Flash AC Characteristics

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702)

7.2 SRAM AC Characteristics

Table 9. SRAM AC Characteristics — Read Operations

| # | Symbol ¹ | Parameter | Min | Max | Unit | Notes |
|-----|---------------------|---|-----|-----|------|---------|
| R1 | t_{RC} | Read Cycle Time | 70 | – | ns | 1 |
| R2 | t_{AA} | Address to Output Delay | – | 70 | ns | 1 |
| R3 | t_{CO1} | S-CS1# to Output Delay | – | 70 | ns | 1 |
| R3 | t_{CO2} | S-CS2 to Output Delay | – | 70 | ns | 1 |
| R4 | t_{OE} | R-OE# to Output Delay | – | 35 | ns | 1 |
| R5 | t_{BA} | R-UB#, R-LB# to Output Delay | – | 70 | ns | 1 |
| R6 | t_{LZ} | S-CS1# or S-CS2 to Output in Low-Z | 5 | – | ns | 1,3,4 |
| R7 | t_{OLZ} | R-OE# to Output in Low-Z | 0 | – | ns | 1,4 |
| R8 | t_{HZ} | S-CS1# or S-CS2 to Output in High-Z | 0 | 25 | ns | 1,2,3,4 |
| R9 | t_{OHZ} | R-OE# to Output in High-Z | 0 | 25 | ns | 1,2,4 |
| R10 | t_{OH} | Output Hold (from Address, S-CS1#, S-CS2 or R-OE# Change, whichever occurs first) | 0 | – | ns | 1 |
| R11 | t_{BLZ} | R-UB#, R-LB# to Output in Low-Z | 0 | – | ns | 1,4 |
| R12 | t_{BHZ} | R-UB#, R-LB# to Output in High-Z | 0 | 25 | ns | 1,4 |

Note:

1. See Figure 5, “AC Waveform SRAM Read Operations” .
2. Timings of t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3. At any given temperature and voltage condition, t_{HZ} (Max) is less than t_{LZ} (Max) both for a given device and from device to device interconnection.
4. Sampled but not 100% tested.

Figure 5. AC Waveform SRAM Read Operations

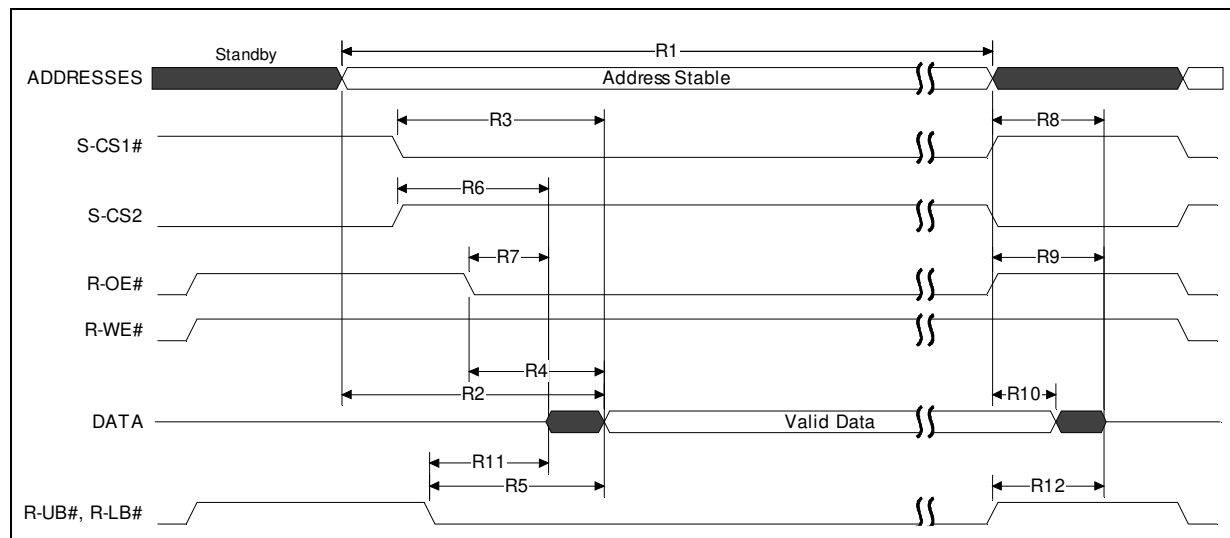


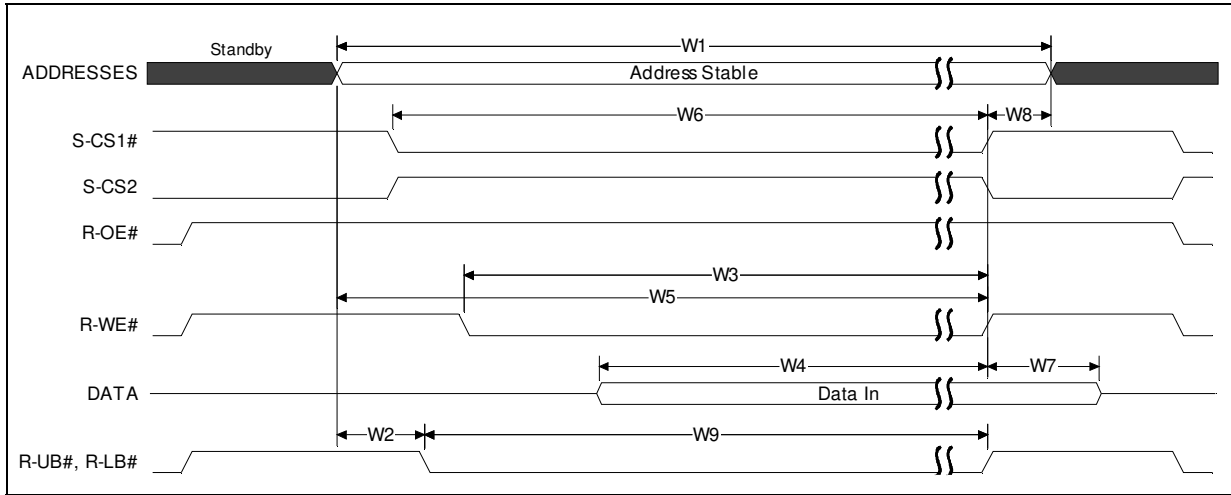
Table 10. SRAM AC Characteristics — Write Operations

| # | Symbol ¹ | Parameter | Min | Max | Unit | Notes |
|----|---------------------|---|-----|-----|------|-------|
| W1 | t_{WC} | Write Cycle Time | 70 | – | ns | 1 |
| W2 | t_{AS} | Address Setup to R-WE# (S-CS1#) and R-UB#/R-LB# Low | 0 | – | ns | 1,4 |
| W3 | t_{WP} | R-WE# (S-CS1#) Pulse Width | 55 | – | ns | 1,2,3 |
| W4 | t_{DW} | Data to Write Time Overlap | 30 | – | ns | 1 |
| W5 | t_{AW} | Address Setup to R-WE# (S-CS1#) High | 60 | – | ns | 1 |
| W6 | t_{CW} | S-CS1# (R-WE#) Setup to R-WE# (S-CS1#) High | 60 | – | ns | 1 |
| W7 | t_{DH} | Data Hold from R-WE# (S-CS1#) High | 0 | – | ns | 1 |
| W8 | t_{WR} | Write Recovery | 0 | – | ns | 1,5 |
| W9 | t_{BW} | R-UB#, R-LB# Setup to R-WE# (S-CS1#) High | 60 | – | ns | 1 |

Notes:

- See Figure 6, “AC Waveform SRAM Write Operations”.
- A write occurs during the overlap (t_{WP}) of low S-CS1# and low R-WE#. A write begins when S-CS1# goes low and R-WE# goes low with asserting R-UB# and R-LB# for single byte operation or simultaneously asserting R-UB#R-LB# and R-LB# for double byte operation. A write ends at the earliest high transition of S-CS1# and R-WE#.
- t_{WP} is measured from S-CS1# low to the end of a write.
- t_{AS} is measured from the address valid to the beginning of a write.
- t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as S-CS1# or R-WE# goes high.

Figure 6. AC Waveform SRAM Write Operations



7.3 PSRAM AC Characteristics

Table 11. PSRAM AC Characteristics (85ns or 88ns Initial Access) — Read Operations

| # | Symbol | Parameter ⁵ | 1.8 V | | 3.0 V | | Unit | Notes |
|-----|-----------|---|-------|-------|-------|-------|------|-------|
| | | | Min | Max | Min | Max | | |
| R1 | t_{RC} | Read Cycle Time | 88 | 4,000 | 85 | 4,000 | ns | |
| R2 | t_{AA} | Address to Output Delay | – | 88 | – | 85 | ns | |
| R3 | t_{CO} | P-CS# to Output Delay | – | 88 | – | 85 | ns | |
| R4 | t_{OE} | R-OE# to Output Delay | – | 65 | – | 40 | ns | |
| R5 | t_{BA} | R-UB#, R-LB# to Output Delay | – | 88 | – | 85 | ns | |
| R6 | t_{LZ} | P-CS# to Output in Low-Z | 10 | – | 10 | – | ns | 1,2 |
| R7 | t_{OLZ} | R-OE# to Output in Low-Z | 5 | – | 0 | – | ns | 2 |
| R8 | t_{HZ} | P-CS# to Output in High-Z | – | 25 | 0 | 25 | ns | 1,2,3 |
| R9 | t_{OHZ} | R-OE# to Output in High-Z | – | 25 | 0 | 25 | ns | 2,3 |
| R10 | t_{OH} | Output Hold (from Address, P-CS# or R-OE# change, whichever occurs first) | 5 | – | 0 | – | ns | |
| R11 | t_{BLZ} | R-UB#, R-LB# to Output in Low-Z | 5 | – | 0 | – | ns | 2 |
| R12 | t_{BHZ} | R-UB#, R-LB# to Output in High-Z | – | 25 | 0 | 25 | ns | 2 |
| PR1 | t_{PC} | Page Cycle Time | 30 | – | 40 | – | ns | 4 |
| PR2 | t_{PA} | Page Access Time | – | 30 | – | 35 | ns | 4 |

Note:

- At any given temperature and voltage condition, t_{HZ} (Max) is less than t_{LZ} (Max) both for a given device and from device to device interconnection.
- Sampled but not 100% tested.
- Timings of t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 4-Word Page read only available for 32-Mbit PSRAM. No page mode feature for 16-Mbit PSRAM.
- Applicable to parts with 85ns or 88ns initial access time: (38F2030W0ZxQ1, 38F2040W0YxQ0, 38F2040W0ZxQ0, 28F2240WWYxQ0).

Table 12. PSRAM AC Characteristics (70ns Initial Access)— Read Operations

| # | Symbol ¹ | Parameter ⁷ | 1.8 V | | 3.0 V | | Unit | Notes |
|-----|---------------------|---|-------|-------|-------|-------|------|-------|
| | | | Min | Max | Min | Max | | |
| R1 | t _{RC} | Read Cycle Time | 70 | 15000 | 70 | 15000 | ns | 2 |
| | | | 70 | 8000 | – | – | | |
| R2 | t _{AA} | Address to Output Delay | – | 70 | – | 70 | ns | |
| R3 | t _{CO} | P-CS# to Output Delay | – | 70 | – | 70 | ns | |
| R4 | t _{OE} | R-OE# to Output Delay | – | 45 | – | 45 | ns | |
| R5 | t _{BA} | R-UB#, R-LB# to Output Delay | – | 70 | – | 70 | ns | |
| R6 | t _{LZ} | P-CS# to Output in Low-Z | 5 | – | 5 | – | ns | 3 |
| R7 | t _{OLZ} | R-OE# to Output in Low-Z | 0 | – | 0 | – | ns | |
| R8 | t _{HZ} | P-CS# to Output in High-Z | 0 | 25 | 0 | 25 | ns | 3, 4 |
| R9 | t _{OHZ} | R-OE# to Output in High-Z | 0 | 25 | 0 | 25 | ns | 4 |
| R10 | t _{OH} | Output Hold (from Address, P-CS# or R-OE# change, whichever occurs first) | 0 | – | 0 | – | ns | |
| R11 | t _{BLZ} | R-UB#, R-LB# to Output in Low-Z | 0 | – | 0 | – | ns | |
| R12 | t _{BHZ} | R-UB#, R-LB# to Output in High-Z | 0 | 25 | 0 | 25 | ns | |
| PR1 | t _{PC} | Page Cycle Time | 25 | – | 25 | – | ns | 5 |
| PR2 | t _{PA} | Page Access Time | – | 25 | – | 25 | ns | 5 |
| | t _{CEL} | CE# low-time restriction | – | 8,000 | ns | 4 | ns | 6 |

Note:

- See Figure 7, “AC Waveform of PSRAM Read Operations” on page 27 and Figure 8, “AC Waveform of PSRAM 4-Word Page Read Operation” on page 27
- Spec’s only applicable to parts 38F1030W0YxQF & 38F2030W0YxQF
- At any given temperature and voltage condition, t_{HZ} (Max) is less than t_{LZ} (Max) both for a given device and from device to device interconnection.
- Timings of t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 4-Word Page read only available for 16-Mbit PSRAM. No page mode feature for 8-Mbit PSRAM. Parts 38F1030W0YxQF & 38F2030W0YxQF do not support page mode, so this spec will not apply to them
- CE# must go high and be maintained high for a minimum of 10ns at least once every 8,000ns
- Applicable to 70ns initial access P-SRAM’s (38F1030W0YxQE, 38F1030W0YxQ2, 38F1030W0ZxQ0, 38F2030W0YxQ1, 38F2030W0YxQE, 38F2030W0YxQ2, 38F2030W0YxQF, 38F2030W0ZxQ2)

Table 13. PSRAM AC Characteristics—Write Operations

| # | Symbol ¹ | Parameter ⁷ | 1.8 V | | 3.0 V | | Unit | Notes |
|-----|---------------------|---|-------|-------|-------|-----|------|-------|
| | | | Min | Max | Min | Max | | |
| W1 | t _{WC} | Write Cycle Time | 70 | 8000 | 70 | – | ns | |
| W2 | t _{AS} | Address Setup to R-WE# (P-CS#) and R-UB#, R-LB# going low | 0 | – | 0 | – | ns | 4 |
| W3 | t _{WP} | R-WE#(P-CS#) Pulse Width | 55 | – | 55 | – | ns | 2,3 |
| W4 | t _{DW} | Data to Write Time Overlap | 35 | – | 35 | – | ns | |
| W5 | t _{AW} | Address Setup to R-WE# (P-CS#) Going High | 60 | – | 60 | – | ns | |
| W6 | t _{CW} | P-CS# (R-WE#) Setup to R-WE# (P-CS#) Going High | 60 | – | 60 | – | ns | |
| W7 | t _{DH} | Data Hold from R-WE# (P-CS#) High | 0 | – | 0 | – | ns | |
| W8 | t _{WR} | Write Recovery | 0 | – | 0 | – | ns | 5 |
| W9 | t _{BW} | R-UB#, R-LB# Setup to R-WE# (P-CS#) Going High | 60 | – | 60 | – | ns | |
| | t _{CEL} | P-CE# low-time restriction | – | 8,000 | – | – | ns | 7,8 |
| W10 | t _{WPH} | Write High Pulse Width | 10 | – | – | – | ns | 8 |

Notes:

1. See Figure 9, “AC Waveform PSRAM Write Operation”.
2. A write occurs during the overlap (t_{WP}) of low P-CS# and low R-WE#. A write begins when P-CS# goes low and R-WE# goes low with asserting R-UB# or R-LB# for single byte operation or simultaneously asserting R-UB# and R-LB# for double byte operation. A write ends at the earliest transition when P-CS# goes high and R-WE# goes high.
3. t_{WP} is measured from P-CS# going low to end of a write.
4. t_{AS} is measured from the address valid to the beginning of a write.
5. t_{WR} is measured from the end of a write to the address change. t_{WR} applied in case a write ends as P-CS# or R-WE# going high.
6. W3 is 70 ns for continuous write operations over 50 times.
7. P-CE# must go high and be maintained high for a minimum of 10ns at least once every 8,000ns
8. Spec's only applicable to parts 38F1030W0YxQF & 38F2030W0YxQF
9. Applicable to 38F2020W0ZTQ1, 38F2020W0ZBQ1, 38F2030W0YTQ1, 38F2030W0YBQ1, 38F2030W0ZTQ2, 38F2030W0ZBQ2, 38F1030W0ZTQ0, 38F1030W0ZBQ0, 38F1030W0YTQE, 38F1030W0YBQE.

Figure 7. AC Waveform of PSRAM Read Operations

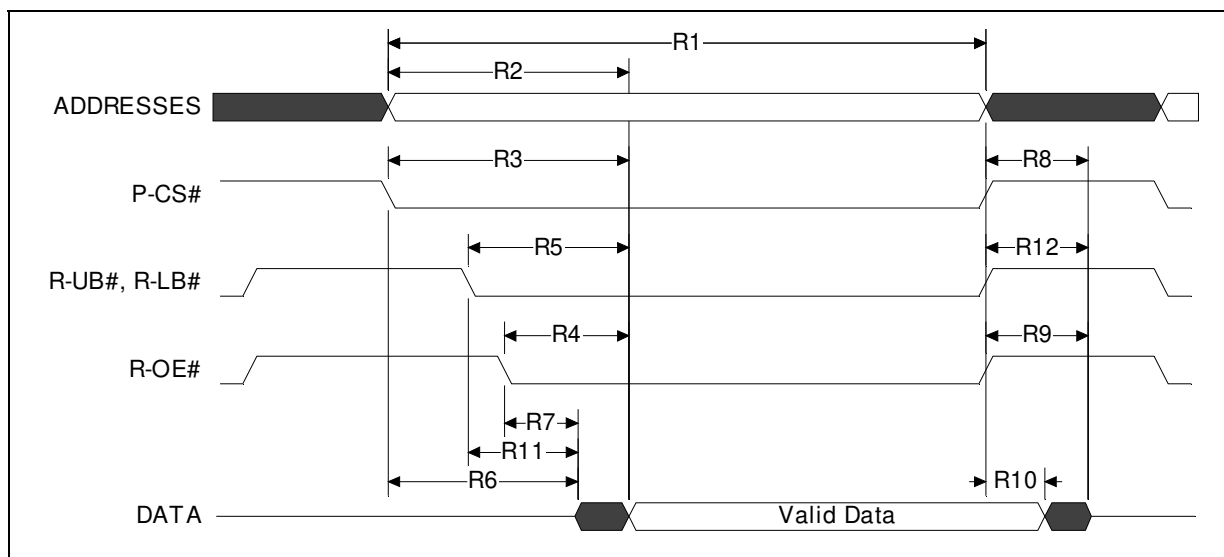
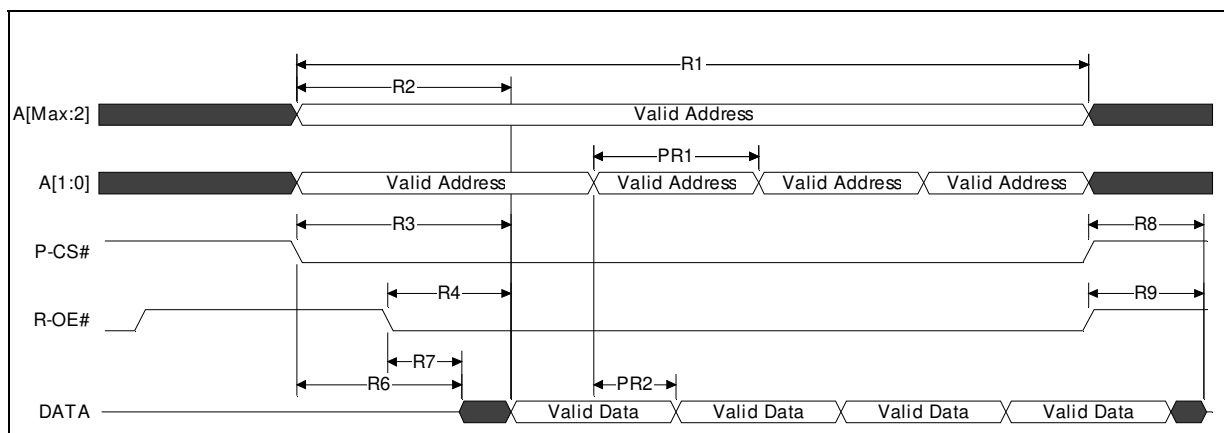
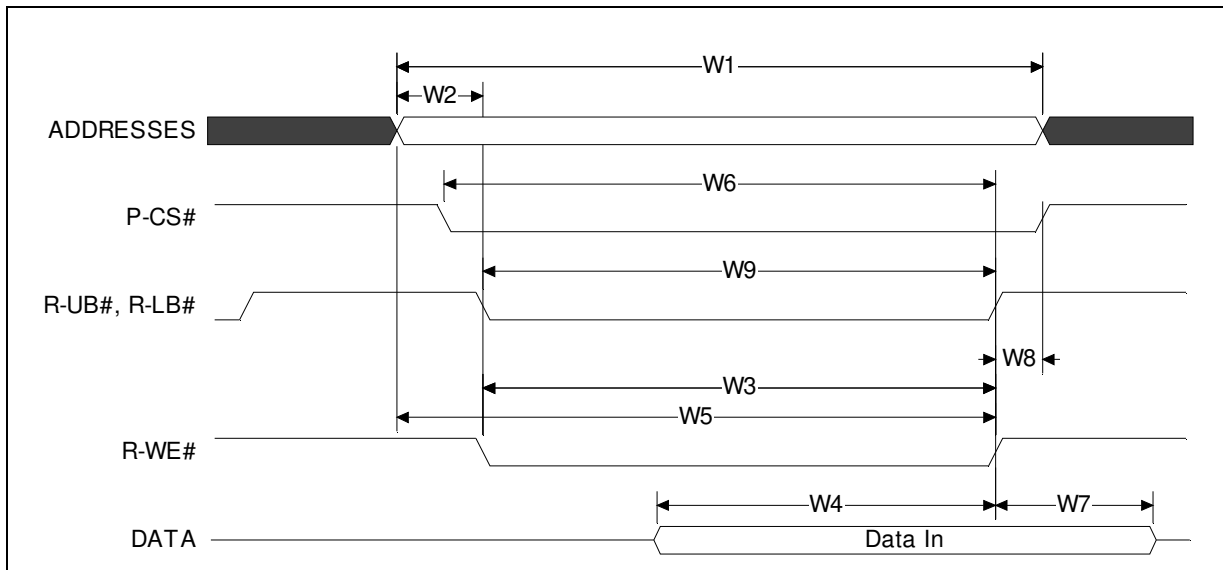


Figure 8. AC Waveform of PSRAM 4-Word Page Read Operation



Note: Available only for 32-Mbit PSRAM and line items with 16-Mbit PSRAM (70 ns) 38F2030W0YTQ1, 38F2030W0YBQ1, 38F2030W0ZTQ2, 38F2030W0ZBQ2, 38F1030W0ZTQ0, 38F1030W0ZBQ0, 38F1030W0YTQE, 38F1030W0YBQE. Not applicable to 8-Mbit PSRAM.

Figure 9. AC Waveform PSRAM Write Operation



7.4 Device AC Test Conditions

Figure 10. Transient Input/Output Reference Waveform

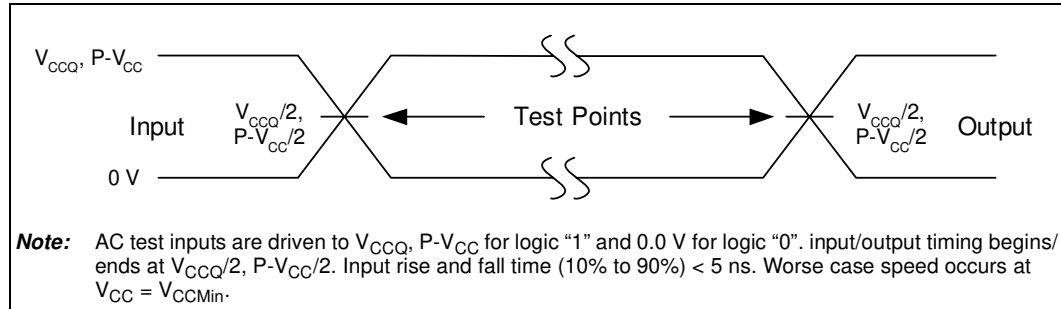
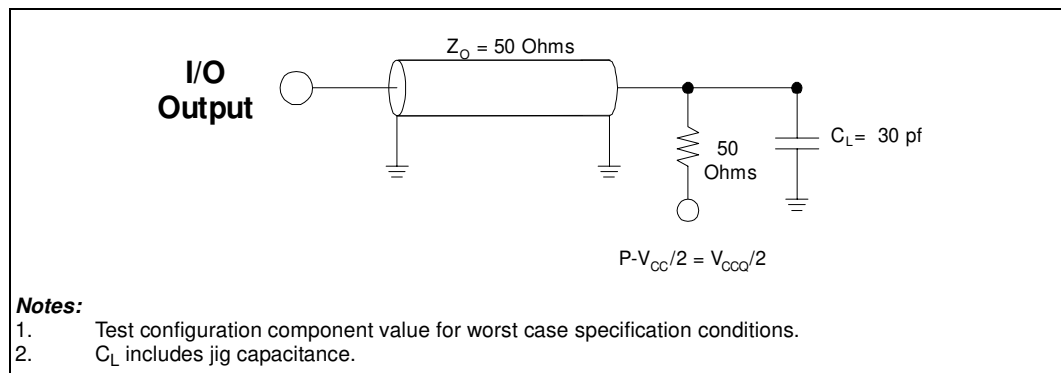


Figure 11. Transient Equivalent Testing Load Circuit



8.0 Flash Power Consumption

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for information regarding flash read modes and operations.

9.0 Device Operation

9.1 Bus Operations

Bus operations for the W18/W30 SCSP family involve the following chip enable and output enable signals, respectively:

- F1-CE# for Flash Die#1 and F2-CE# for Flash Die#2
- F1-OE# for Flash Die#1 and F2-OE# for Flash Die#2

All other control signals are shared between the two flash die. [Table 14](#) to [Table 16](#) explain the bus operations of products across this SCSP family. Refer to the W18/W30 discrete datasheets (order numbers 290701 and 290702) for single flash die SCSP bus operations.

Table 14. Flash-Only Bus Operations

| Device | Mode | F-RST# | F1-CE# | F1-OE# | F-WE# | ADV# | F-VPP | WAIT | F2-CE# | F2-OE# | D[15:0] | Notes |
|-------------|---------------------------------|--------|--------|--------|-------|------|--------------------------------------|----------|--------|--------|------------------------|------------|
| Flash Die#1 | Sync Array Read | H | L | L | H | L | X | Active | H | X | Flash D _{OUT} | 2, 3, 4 |
| | All Async / Sync Non-Array Read | H | L | L | H | X | X | Asserted | H | X | Flash D _{OUT} | 1, 3, 4, 5 |
| | Write | H | L | H | L | X | V _{PPH} or V _{PPL} | Asserted | H | X | Flash D _{IN} | 3, 4, 6 |
| | Output Disable | H | L | H | H | X | X | Active | X | X | Flash High-Z | 4 |
| | Standby | H | H | X | X | X | X | High-Z | X | X | Flash High-Z | 4 |
| | Reset | L | X | X | X | X | X | High-Z | X | X | Flash High-Z | 4 |

| Device | Mode | F-RST# | F1-CE# | F1-OE# | F-WE# | ADV# | F-VPP | WAIT | F2-CE# | F2-OE# | D[15:0] | Notes |
|-------------|---------------------------------|--------|--------|--------|-------|------|--------------------------------------|----------|--------|--------|------------------------|------------|
| Flash Die#2 | Sync Array Read | H | H | X | H | L | X | Active | L | L | Flash D _{OUT} | 2, 3, 4 |
| | All Async / Sync Non-Array Read | H | H | X | H | X | X | Asserted | L | L | Flash D _{OUT} | 1, 3, 4, 5 |
| | Write | H | H | X | L | X | V _{PPL} or V _{PPH} | Asserted | L | H | Flash D _{IN} | 3, 4, 6 |
| | Output Disable | H | X | X | H | X | X | Active | L | H | Flash High-Z | 4 |
| | Standby | H | X | X | X | X | X | High-Z | H | X | Flash High-Z | 4 |
| | Reset | L | X | X | X | X | X | High-Z | X | X | Flash High-Z | 4 |

Notes:

- For asynchronous read operation, both die may be simultaneously selected, but may not simultaneously drive the memory bus. See Section 9.2, "Flash Command Definitions" on page 34 for details regarding flash selection overlap.
- WAIT is only valid during synchronous flash reads. WAIT is driven if F-CE# is asserted. Refer to the W18 or W30 datasheet (order number 290701 and 29702) for further information regarding WAIT Signal.
- For either flash die, F[2:1]-OE# and F-WE# should never be asserted simultaneously. If done so on a particular flash die, F[2:1]-OE# will override F-WE#.
- L means V_{IL} while H means V_{IH}. X can be V_{IL} or V_{IH} for inputs, V_{PPL}, V_{PPH} or V_{PPLK} for F-VPP.
- Flash CFI query and status register accesses use D[7:0] only, all other reads use D[15:0].
- Refer to W18/W30 datasheet for valid D_{IN} during flash writes.

Table 15. Flash + SRAM Bus Operations

| Device | Mode | F-RST# | F[2:1]-CE# | F[2:1]-OE# | F-WE# | ADV# | F-VPP | WAIT | S-CS1# | S-CS2 | R-OE# | R-WE# | R-UB#, R-LB# | D[15:0] | Notes |
|---------------------|--------------------------------|--------|------------|------------|-------|------|--------------------------------------|----------|------------------------|-------|-------|-------|--------------|------------------------|---------------|
| Flash Die(#1 or #2) | Sync Array Read | H | L | L | H | L | X | Active | SRAM must be in High-Z | | | | | Flash D _{OUT} | 1, 2, 3, 5 |
| | All Async/ Sync Non-array Read | H | L | L | H | X | X | Asserted | | | | | | Flash D _{OUT} | 1, 2, 3, 5, 6 |
| | Write | H | L | H | L | L | V _{PPL} or V _{PPH} | Asserted | | | | | | Flash D _{IN} | 3, 7 |
| | Output Disable | H | L | H | H | X | X | Active | Any SRAM mode allowed | | | | | Flash High-Z | 5 |
| | Standby | H | H | X | X | X | X | High-Z | | | | | | Flash High-Z | 5 |
| | Reset | L | X | X | X | X | X | High-Z | | | | | | Flash High-Z | 5 |

Table 15. Flash + SRAM Bus Operations

| Device | Mode | F-RST# | F[2:1]-CE# | F[2:1]-OE# | F-WE# | ADV# | F-VPP | WAIT | S-CS1# | S-CS2 | R-OE# | R-WE# | R-UB#, R-LB# | D[15:0] | Notes | |
|----------------|----------------|-------------------------|------------|------------|-------|------|-------|------|----------------------|-------|-------|-------|-----------------|----------------|--------------------------|------------|
| SRAM | Read | Flash must be in High-Z | | | | | | | | L | H | L | H | L | SRAM D _{OUT} | 1, 4, 8, 2 |
| | Write | Flash must be in High-Z | | | | | | | | L | H | X | L | L | SRAM D _{IN} | 4, 5, 8, 2 |
| | Output Disable | Any flash mode allowed | | | | | | | | L | H | H | H | X | SRAM High-Z | 5, 2 |
| | Standby | Any flash mode allowed | | | | | | | | H | X | X | X | X | SRAM High-Z | 5, 8, 2 |
| | | | | | | | | | | X | L | | | | SRAM High-Z | |
| Data Retention | | | | | | | | | Same as SRAM standby | | | | | SRAM High-Z | 9, 2 | |

Notes:

- For asynchronous read operation, all die may be simultaneously selected, but may not simultaneously drive the memory bus.
- WAIT is only valid during synchronous flash reads. WAIT is driven if F-CE# is asserted.
- For flash die, F[2:1]-OE# and F-WE# should never be asserted simultaneously. If done so, F[2:1]-OE# will override F-WE#.
- For SRAM, R-OE# and R-WE# should never be asserted simultaneously.
- X can be V_{IL} or V_{IH} for inputs, V_{PPL}, V_{PPH} or V_{PPLK} for F-VPP.
- Flash CFI query and status register accesses use D[7:0] only, all other reads use D[15:0].
- Refer to W18 and W30 datasheet for valid D_{IN} during flash writes.
- The SRAM is enabled and/or disabled with the logical function: S-CS1# OR S-CS2.
- The SRAM can be placed into data retention mode by lowering S-VCC to the V_{DR} limit when in standby mode.

Table 16. Flash + PSRAM Bus Operations

| Device | Mode | F-RST# | F[2:1]-CE# | F[2:1]-OE# | F-WE# | ADV# | F-VPP | WAIT | P-CS# | P-Mode | R-OE# | R-WE# | R-UB#, R-LB# | D[15:0] | Notes |
|---------------------|-----------------------------------|--------|------------|------------|-------|------|--|----------|-------------------------|--------|-------|-------|-----------------|---------------------------|------------------|
| Flash Die(#1 or #2) | Sync Array Read | H | L | L | H | L | X | Active | PSRAM must be in High-Z | | | | | Flash D _{OUT} | 1, 2, 3, 4, 6 |
| | All Async/ Sync Non-array Read | H | L | L | H | X | X | Asserted | PSRAM must be in High-Z | | | | | Flash D _{OUT} | 1, 2, 3, 4, 6, 7 |
| | Write | H | L | H | L | X | V _{PPL} or V _{PPH} | Asserted | PSRAM must be in High-Z | | | | | Flash D _{IN} | 3, 4, 6, 8 |
| | Output Disable | H | L | H | H | X | X | Active | Any PSRAM mode allowed | | | | | Flash High-Z | 6 |
| | Standby | H | H | X | X | X | X | High-Z | Any PSRAM mode allowed | | | | | Flash High-Z | 6 |
| | Reset | L | X | X | X | X | X | High-Z | Any PSRAM mode allowed | | | | | Flash High-Z | 6 |

Table 16. Flash + PSRAM Bus Operations

| Device | Mode | F-RST# | F[2:1]-CE# | F[2:1]-OE# | F-WE# | ADV# | F-VPP | WAIT | P-CS# | P-Mode | R-OE# | R-WE# | R-UB#, R-LB# | D[15:0] | Notes | |
|--------|-----------------|----------------------------------|------------|------------|-------|------|-------|------|-------|--------|-------|-------|-----------------|---------|---------------------------|---------|
| PSRAM | Read | Flash#1 and #2 must be in High-Z | | | | | | | | L | H | L | H | L | PSRAM D _{OUT} | 1, 5, 2 |
| | Write | Flash#1 and #2 must be in High-Z | | | | | | | | L | H | H | L | L | PSRAM D _{IN} | 5, 2 |
| | Output Disable | Any flash mode allowed | | | | | | | | L | H | H | H | X | PSRAM High-Z | 6, 2 |
| | Standby | Any flash mode allowed | | | | | | | | H | H | X | X | X | PSRAM High-Z | 6, 2 |
| | Deep Power-Down | Any flash mode allowed | | | | | | | | H | L | X | X | X | PSRAM High-Z | 6, 9, 2 |

Notes:

- For asynchronous read operation, all die may be simultaneously selected, but may not simultaneously drive the memory bus. For synchronous burst-mode reads, only two die (one flash and the PSRAM) may be simultaneously selected.
- WAIT is only valid during synchronous flash reads. WAIT is driven if F-CE# is asserted.
- F1-CE# for Flash Die#1, F2-CE# for Flash Die#2. F1-OE# is for Flash Die#1, F2-OE# for Flash Die#2.
- For either flash die, F[2:1]-OE# and F-WE# should never be asserted simultaneously. If done so on a particular flash die, F[2:1]-OE# will override F-WE#.
- For PSRAM, R-OE# and R-WE# should never be asserted simultaneously.
- X can be V_{IL} or V_{IH} for inputs, V_{PPL}, V_{PPH} or V_{PPLK} for F-VPP.
- Flash CF1 query and status register accesses use D[7:0] only, all other reads use D[15:0].
- Refer to W30/W18 datasheet for Valid D_{IN} during flash writes.
- Deep power-down is not applicable to 38F2020W0ZTQ1, 38F2020W0ZBQ1, 38F2030W0YTQ1, 38F2030W0YBQ1, 38F2030W0ZTQ2, 38F2030W0ZBQ2, 38F1030W0ZTQ0, 38F1030W0ZBQ0, 38F1030W0YTQE, 38F1030W0YBQE.

9.2 Flash Command Definitions

Refer to the discrete datasheets, *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for information regarding flash command definitions.

10.0 Flash Read Operations

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for information regarding flash read modes and operations.

11.0 Flash Program Operations

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for information regarding flash read modes and operations.

12.0 Flash Erase Operations

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for information regarding flash read modes and operations.

13.0 Flash Security Modes

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for information regarding flash read modes and operations.

14.0 Flash Read Configuration Register

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for information regarding flash read modes and operations.

15.0 SRAM Operations

15.1 Power-up Sequence and Initialization

The SRAM functionality and reliability are independent of the power-up sequence and power-up slew rate of the core $S-V_{CC}$. Any power-up sequence and power-up slew rate is possible under use conditions. SRAM reliability is also independent of the power-down sequence and power-down slew rate of the core $S-V_{CC}$.

15.2 Data Retention Mode

Table 17. SRAM Data Retention Operation

| Symbol | Parameter | Min | Max | Unit | Notes |
|-----------|------------------------------|----------|-----|------|-------|
| t_{SDR} | Data Retention Set-up Time | 0 | – | ns | |
| t_{RDR} | Data Retention Recovery Time | t_{RC} | – | ns | 1 |

Note:

- t_{RC} is defined in Table 7.2, “SRAM AC Characteristics” on page 21.

Figure 12. SRAM Data Retention Operation Waveform—S-CS1# Controlled

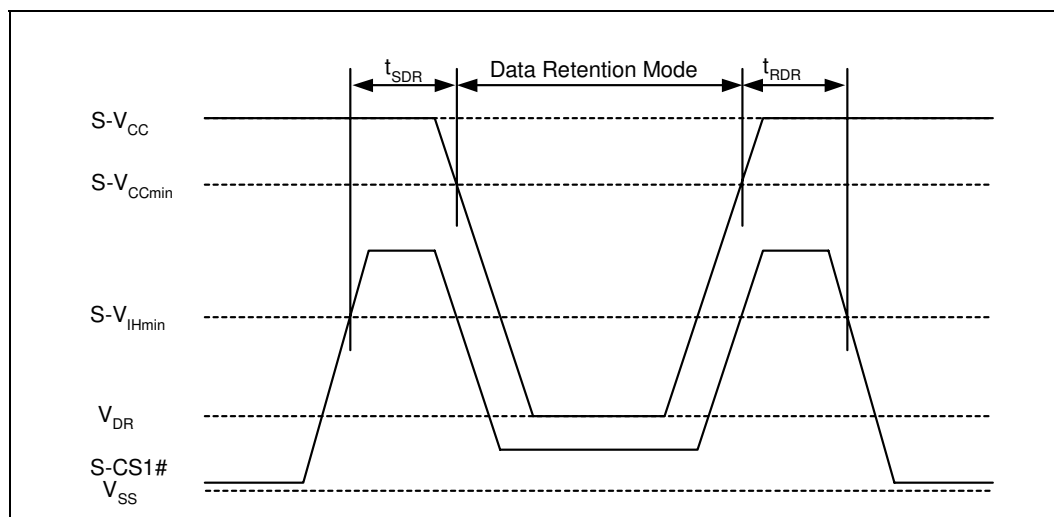
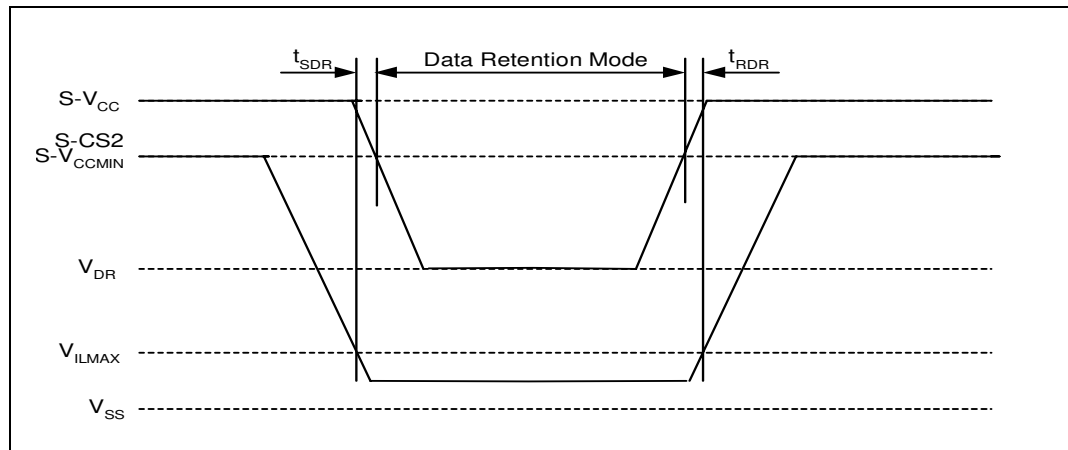


Figure 13. SRAM Data Retention Operation Waveform—S-CS2 Controlled



16.0 PSRAM Operations

16.1 Power-Up Sequence and Initialization

The PSRAM functionality and reliability are independent of the power-up sequence and slew rate of the core P-V_{CC}. Any power-up sequence and slew rate is possible under use conditions. PSRAM reliability are also independent of the power-down sequence and slew rate of the core P-V_{CC}.

The following power-up sequence and register setting should be used before starting normal operation. The PSRAM power-up sequence is represented in Figure 14. Following power application, make P-Mode high after fixing P-Mode to a low level for a period of t_{11} . Make P-CS# high before making P-Mode high. P-CS# and P-Mode are fixed to a high level for period of t_{13} .

Figure 14. Timing Waveform for Power-Up Sequence

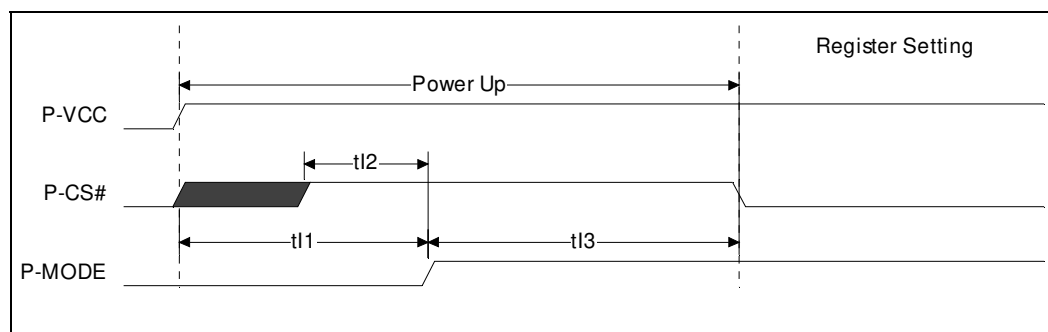


Table 18. Power-Up Sequence Specifications

| Parameter | Description | Min | Max | Unit | Notes |
|-----------|--|-----|-----|---------|-------|
| t_{11} | Power application with P-Mode held low | 50 | — | μ s | 1,2,3 |
| t_{12} | P-CS# high to P-Mode high | 10 | — | ns | |
| t_{13} | P-Mode high to P-CS# low | 500 | — | μ s | |

Notes:

1. Toggle P-Mode to low when starting the power-up sequence.
2. t_{11} is specified from when the power supply voltage reaches V_{CCMIN} .
3. Does not apply to 38F2020W0ZTQ1, 38F2020W0ZBQ1, 38F2030W0YTQ1, 38F2030W0YBQ1, 38F2030W0ZTQ2, and 38F2030W0ZBQ2, 38F1030W0ZTQ0, 38F1030W0ZBQ0, 38F1030W0YTQE, 38F1030W0YBQE line items. Valid PSRAM operations for these line items can begin 200 μ s after P-V_{cc} has reached P-V_{cc} min.

16.1.1 16Mbit PSRAM Power-Up Sequence (Non-Page Mode)

For the non-page mode PSRAM (part's RD38F1030W0YQF, PF38F1030W0YQF, RD38F2030W0YQF, PF38F2030W0YQF) the PSRAM functionality and reliability must be independent of the power-up sequence and power-up slew rate of the core V_{cc} and the I/O V_{cc}

(Vccq.) Any power-up sequence and power-up slew rate is possible under use conditions. PSRAM reliability must also be independent of the power-down sequence and power-down slew rate of the core Vcc and the I/O Vcc (Vccq.)

Once power supply voltages have reached the minimum spec value of 1.7V (or higher), CE# must be maintained high for minimum 200us prior to commencing valid PSRAM operation.

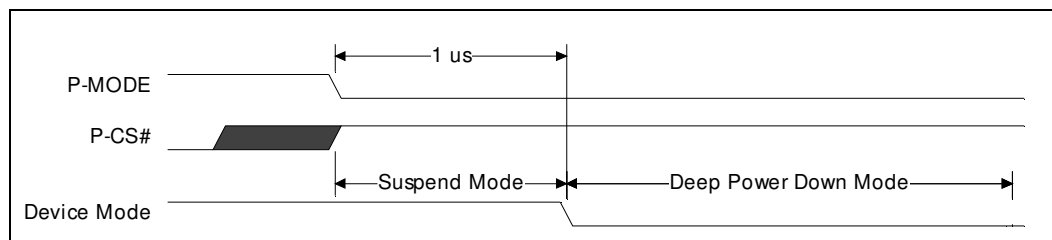
16.2 Standby Mode/ Deep Power-Down Mode

Caution: All line items that do not have the P-Mode pin will not have the deep power-down feature (38F1030W0YxQE, 38F1030W0YxQ2, 38F1030W0ZxQ0, 38F2030W0YxQ1, 38F2030W0YxQE, 38F2030W0YxQ2, 38F2030W0YxQF, 38F2030W0ZxQ2, 38F2040W0ZxQ0).

Data is lost during deep power-down mode as shown in the Table below. Wake-up from deep power-down mode involves the same initialization sequence as discussed in Section 16.1, “Power-Up Sequence and Initialization” on page 42.

| Mode | Memory Cell Data | Delay time to go Active |
|-----------------|------------------|-------------------------|
| Standby | Valid | 0 ns |
| Deep Power-Down | Invalid | Start-Up Sequence |

Figure 15. Timing Waveform for Entering Deep Power-Down Mode



16.3 PSRAM Special Read and Write Constraints

Caution: This section will not apply to line items that do not have the P-Mode pin will not have the deep power-down feature (38F1030W0YxQE, 38F1030W0YxQ2, 38F1030W0ZxQ0, 38F2030W0YxQ1, 38F2030W0YxQE, 38F2030W0YxQ2, 38F2030W0YxQF, 38F2030W0ZxQ2, 38F2040W0ZxQ0).

Table 19. PSRAM Special Read Constraints

| Description | Min | Max | Unit | Notes |
|--|-----|-----|------|-------|
| Cannot have sub t_{RC} address toggle for more than 4 μ s in active mode. Need either a read operation or P-CS# high for t_{RC} in that time frame | N/A | N/A | – | |
| P-CS# high level pulse width | 10 | – | ns | 1 |

Table 19. PSRAM Special Read Constraints

| | | | | |
|---|----|--------|----|---|
| R-UB#/R-LB# high level pulse width | 10 | – | ns | 1 |
| R-OE# high level pulse width in active mode (P-CS# low) | 10 | 10,000 | ns | |
| P-CS# low to R-OE# low | – | 10,000 | ns | |
| Address Skew time (unstable address with P-CS# low) | – | 10 | ns | 2 |

Notes:

1. Toggling of these control signals is not necessary during address controlled read operations.
2. Address skew time (t_{SKEW}) indicates the following three types of time depending on the condition.
 - a. When switching P-CS# from high to low, t_{SKEW} is the time from the P-CS# low input point until the next address is determined.
 - b. When switching P-CS# from low to high, t_{SKEW} is the time from the address change start point to the P-CS# high input point.
 - c. When P-CS# is fixed to low, t_{SKEW} is the time from the address start point until the next address is determined.

Since specs are defined for t_{SKEW} only when P-CS# is active, t_{SKEW} is not subject to limitations when P-CS# is switched from high to low following address determination, or when the address is changed after P-CS# is switched from low to high.

Table 20. PSRAM Special Write Constraints

| Description | Min | Max | Unit | Notes |
|---|-----|--------|------|-------|
| Need either R-WE# high or P-CS# high for at least t_{WC} time, for every 4us window during write operations. | N/A | N/A | – | |
| R-OE# high to R-WE# low in active mode (P-CS# low) | 0 | 10,000 | ns | |
| R-WE# high to R-OE# low in active mode (P-CS# low) | 10 | 10,000 | ns | |
| Address Skew time (unstable address with P-CS# low) | – | 10 | ns | 1 |

Note:

1. Address skew time (t_{SKEW}) indicates the following three types of time depending on the condition.
 - a. When switching P-CS# from high to low, t_{SKEW} is the time from the P-CS# low input point until the next address is determined.
 - b. When switching P-CS# from low to high, t_{SKEW} is the time from the address change start point to the P-CS# high input point.
 - c. When P-CS# is fixed to low, t_{SKEW} is the time from the address start point until the next address is determined.

Since specs are defined for t_{SKEW} only when P-CS# is active, t_{SKEW} is not subject to limitations when P-CS# is switched from high to low following address determination, or when the address is changed after P-CS# is switched from low to high.



Appendix A Write State Machine

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for the WSM details.



Appendix B Common Flash Interface

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for the CFI details.



Appendix C Flash Flowcharts

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) and *Intel® Wireless Flash Memory (W30) Datasheet* (order number 290702) for the flash flowchart details.

Appendix D Additional Information

| Order Number | Document |
|--------------|---|
| 290701 | <i>Intel® Wireless Flash Memory (W18) Datasheet</i> |
| 290702 | <i>Intel® Wireless Flash Memory with 3 Volt I/O (W30) Datasheet</i> |
| 251216 | <i>64-Mbit 1.8 Volt Intel® Wireless Flash Memory SCSP Family Application Note</i> |

Notes:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. For the most current information on Intel® Flash memory products, software and tools, visit our website at <http://developer.intel.com/design/flash>.

Appendix E Ordering Information

Figure 16 shows the decoder for products in this SCSP family with both flash and RAM. Figure 17 shows the decoder for products in this SCSP family with flash die only (no RAM). Table 23, “32WQ and 64WQ W18/W30 SCSP Ordering Information (Flash + PSRAM)” on page 52 lists available product combinations.

Figure 16. Decoder for Flash + RAM SCSP Family Devices

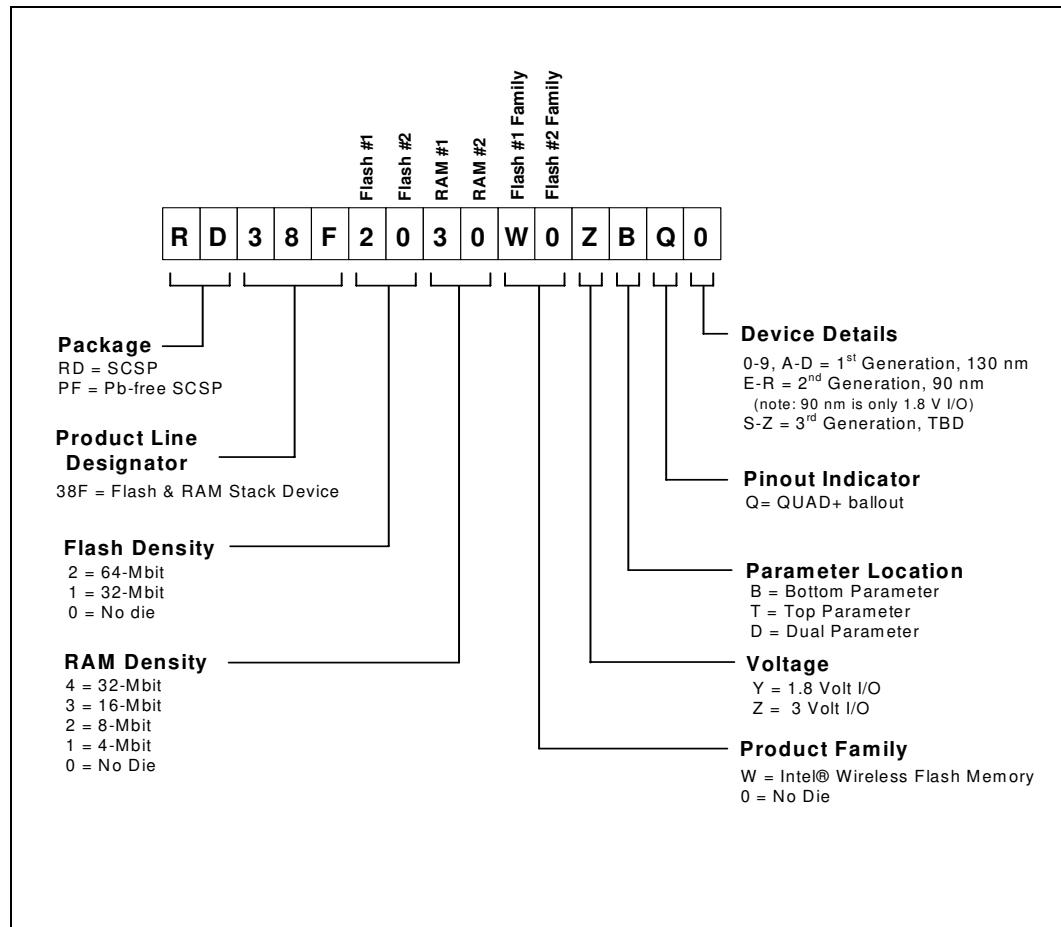


Figure 17. Decoder for Flash-Only SCSP Family Devices

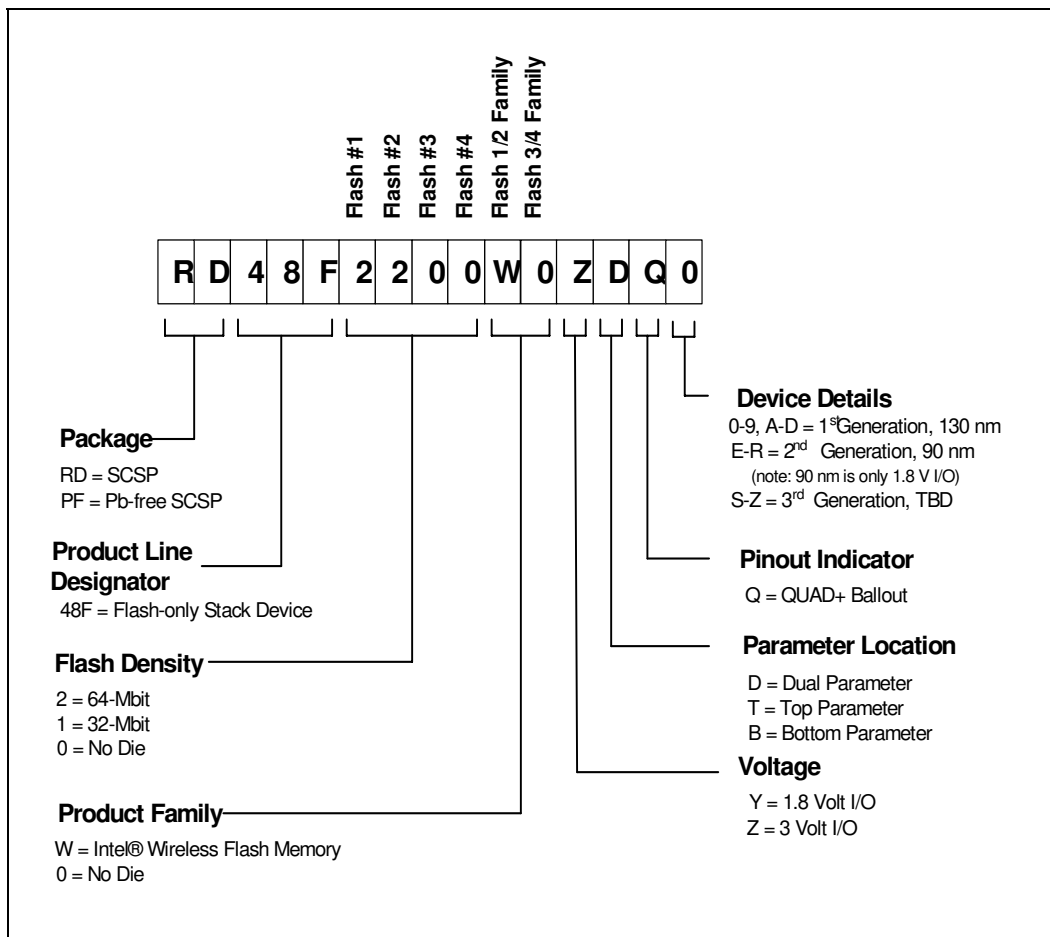


Table 21. 32WQ and 64WQ W18/W30 SCSP Ordering Information (Flash Only)

| Flash Component | Package | | | Product Number (1,2,3,4,5) |
|-----------------|--------------|-----------|---------|------------------------------------|
| | Size (mm) | Type | Ballout | |
| 32 W30 | 8 x 10 x 1.2 | Lead-free | Quad + | PF48F1000W0ZTQ0 PF48F1000W0ZBQ0 |
| 64 W30 | 8 x 10 x 1.2 | Lead-free | Quad + | PF48F2000W0ZTQ0 PF48F2000W0ZBQ0 |
| 64 W18 + 32 W18 | 8 x 10 x 1.2 | Leaded | Quad + | RD48F2100W0YDQE |
| 64 W18 + 64W18 | 8 x 10 x 1.2 | Leaded | Quad + | RD48F2200W0YDQ0 |

Notes:



1. W18 = Intel® Wireless Flash Memory (W18) with 1.8 V I/O; W30 = Intel® Wireless Flash Memory (W30) with 3.0 V I/O.
2. B = Bottom Parameter, where Flash Die #1, F1-CE# = Bottom Parameter and Flash Die #2, F2-CE# = Top Parameter.
3. T = Top Parameter where Flash Die #1, F1-CE# = Top Parameter and Flash Die #2, F2-CE# = Bottom Parameter.
4. D = Dual Parameter where Flash Die #1, F1-CE# = Bottom Parameter and Flash Die #2, F2-CE# = Top Parameter.
5. Parts ending with "QE" are 90 nm Flash devices.

Table 22. 32WQ and 64WQ W18/W30 SCSP Ordering Information (Flash + SRAM)

| Flash Component | RAM | Package | | | Product Number ^(1,2,3,4) |
|-------------------------|-----------------------|--------------|--------|---------|-------------------------------------|
| Size in Mbit and Family | Size in Mbit and Type | Size (mm) | Type | Ballout | |
| 64 W18 | 4 SRAM | 8 x 10 x 1.2 | Leaded | Quad+ | RD38F2010W0YTQ0 RD38F2010W0YBQ0 |
| | 8 SRAM | 8 x 10 x 1.2 | Leaded | Quad+ | RD38F2020W0YTQ0 RD38F2020W0YBQ0 |
| | 16 SRAM | 8 x 10 x 1.2 | Leaded | Quad+ | RD38F2030W0YTQ0 RD38F2030W0YBQ0 |
| 64 W30 | 8 SRAM | 8 x 10 x 1.2 | Leaded | Quad+ | RD38F2020W0ZTQ0 RD38F2020W0ZBQ0 |
| | 16 SRAM | 8 x 10 x 1.2 | Leaded | Quad+ | RD38F2030W0ZTQ0 RD38F2030W0ZBQ0 |
| 64 W18 + 64 W18 | 16 SRAM | 8 x 10 x 1.4 | Leaded | Quad+ | RD38F2230WWYDQ0 |
| 64 W30 + 64 W30 | 16 SRAM | 8 x 10 x 1.4 | Leaded | Quad+ | RD38F2230WWZDQ0 |

Notes:

1. W18 = Intel® Wireless Flash Memory (W18) with 1.8 V I/O; W30 = Intel® Wireless Flash Memory (W30) with 3.0 V I/O.
2. B = Bottom Parameter, where Flash Die #1, F1-CE# = Bottom Parameter and Flash Die #2, F2-CE# = Top Parameter.
3. T = Top Parameter where Flash Die #1, F1-CE# = Top Parameter and Flash Die #2, F2-CE# = Bottom Parameter.
4. D = Dual Parameter where Flash Die #1, F1-CE# = Bottom Parameter and Flash Die #2, F2-CE# = Top Parameter.

Table 23. 32WQ and 64WQ W18/W30 SCSP Ordering Information (Flash + PSRAM) (Sheet 1 of 2)

| Flash Component | RAM | Package | | | Product Number (1,2,3,4,5) | PSRAM used |
|-----------------|----------|--------------|---------|-----------|------------------------------------|--|
| | | Size (mm) | Ballout | Type | | |
| 32 W18 | 16 PSRAM | 8 x 10 x 1.2 | Quad+ | Lead-free | PF38F1030W0YTQE PF38F1030W0YBQE | 70 ns, No PMODE pin |
| 32 W18 | 16 PSRAM | 8 x 10 x 1.2 | Quad+ | Leaded | RD38F1030W0YTQ2 RD38F1030W0YBQ2 | 70 ns, No PMODE pin & Non-Page Mode Support |
| | | | | Lead-free | PF38F1030W0YTQ2 PF38F1030W0YBQ2 | |
| 32 W30 | 16 PSRAM | 8 x 10 x 1.2 | Quad+ | Leaded | RD38F1030W0ZTQ0 RD38F1030W0ZBQ0 | 70 ns, No PMODE pin |
| | | | | Lead-free | PF38F1030W0ZTQ0 PF38F1030W0ZBQ0 | |
| 64 W18 | 16 PSRAM | 8 x 10 x 1.2 | Quad+ | Leaded | RD38F2030W0YTQ1 RD38F2030W0YBQ1 | 70 ns, No PMODE pin |
| | | | | Lead-free | PF38F2030W0YTQ1 PF38F2030W0YBQ1 | |
| | | | | Leaded | RD38F2030W0YTQE RD38F2030W0YBQE | |
| | | | | Lead-free | PF38F2030W0YTQE PF38F2030W0YBQE | |
| 64 W18 | 16 PSRAM | 8 x 10 x 1.2 | Quad+ | Leaded | RD38F2030W0YTQ2 RD38F2030W0YBQ2 | 70 ns, No PMODE pin & Non-Page Mode Support |
| | | | | Lead-free | PF38F2030W0YTQ2 PF38F2030W0YBQ2 | |
| | | | | Leaded | RD38F2030W0YTQF RD38F2030W0YBQF | |
| | | | | Lead-free | PF38F2030W0YTQF PF38F2030W0YBQF | |
| 64 W30 | 16 PSRAM | 8 x 10 x 1.2 | Quad+ | Leaded | RD38F2030W0ZTQ1 RD38F2030W0ZBQ1 | 85 ns, with PMODE pin |
| | | | | Leaded | RD38F2030W0ZTQ2 RD38F2030W0ZBQ2 | 70 ns, No PMODE pin |
| | | | | Lead-free | PF38F2030W0ZTQ2 PF38F2030W0ZBQ2 | |
| 64 W18 | 32 PSRAM | 8 x 10 x 1.2 | QUAD+ | Leaded | RD38F2040W0YTQ0 RD38F2040W0YBQ0 | 88 ns, with PMODE pin |
| | | | | Lead-free | PF38F2040W0YTQ0 PF38F2040W0YBQ0 | |



Table 23. 32WQ and 64WQ W18/W30 SCSP Ordering Information (Flash + PSRAM) (Sheet 2 of 2)

| Flash Component | RAM | Package | | | Product Number (1,2,3,4,5) | PSRAM used |
|-----------------|----------|--------------|---------|--------|---|--------------------------|
| | | Size (mm) | Ballout | Type | | |
| 64 W30 | 32 PSRAM | 8 x 10 x 1.2 | QUAD+ | Leaded | RD38F2040W0ZTQ0 RD38F2040W0ZBQ0 | 85 ns, No PMODE pin |
| 64 W18 + 64 W18 | 32 PSRAM | 8 x 10 x 1.4 | QUAD+ | Leaded | RD38F2240WWYDQ0 ⁽⁶⁾ RD38F2240WWYDQ1 | 88 ns, with PMODE pin |
| 64 W30 + 64 W30 | 32 PSRAM | 8 x 10 x 1.4 | QUAD+ | Leaded | RD38F2240WWZDQ0 RD38F2240WWZDQ1 | 85 ns, No PMODE pin |

Notes:

1. W18 = Intel® Wireless Flash Memory (W18) with 1.8 V I/O; W30 = Intel® Wireless Flash Memory (W30) with 3.0 V I/O.
2. B = Bottom Parameter, where Flash Die #1, F1-CE# = Bottom Parameter and Flash Die #2, F2-CE# = Top Parameter.
3. T = Top Parameter where Flash Die #1, F1-CE# = Top Parameter and Flash Die #2, F2-CE# = Bottom Parameter.
4. D = Dual Parameter where Flash Die #1, F1-CE# = Bottom Parameter and Flash Die #2, F2-CE# = Top Parameter.
5. Parts ending with "QE" are 90 nm Flash devices.
6. RD38F2240WWYDQ0 = Engineering Samples; RD38F2240WWYDQ1 = Production

