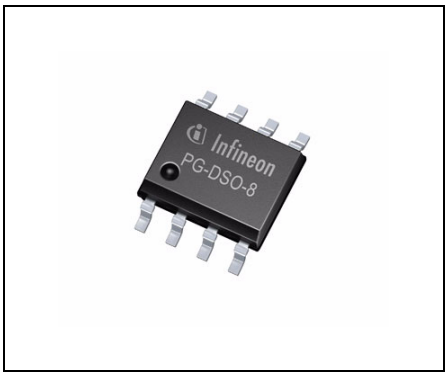
Voltage-Current Regulator

TLE 4305

RoHS

Features



- Wide supply voltage operation range
- Wide ambient temperature operation range
- Minimized external circuitry
- High voltage regulation accuracy
- High current limit regulation accuracy
- Low temperature drift
- Independent voltage- current-loop compensation
- Internal fixed amplification
- Fully temperature compensated current- and voltage OTA (operational transconductance amplifier)
- SMD package
- Industrial type
- Green Product (RoHS compliant)

Functional Description

The TLE 4305 G is specifically designed to control the output voltage and the output current of a switch mode power supply.

Independent compensation networks for the voltage- and for the current-loop can be realized by external circuitry.

The device contains a high accuracy bandgap reference voltage, two operational trans conductance amplifier (OTA), an opto-coupler driver output stage and an high-voltage bias circuit.

The device is based on Infineons double isolated power line technology DOPL which allows to produce high precision bipolar voltage regulators with breakdown voltages up to 45 V.

Type	Package
TLE 4305 G	PG-DSO-8

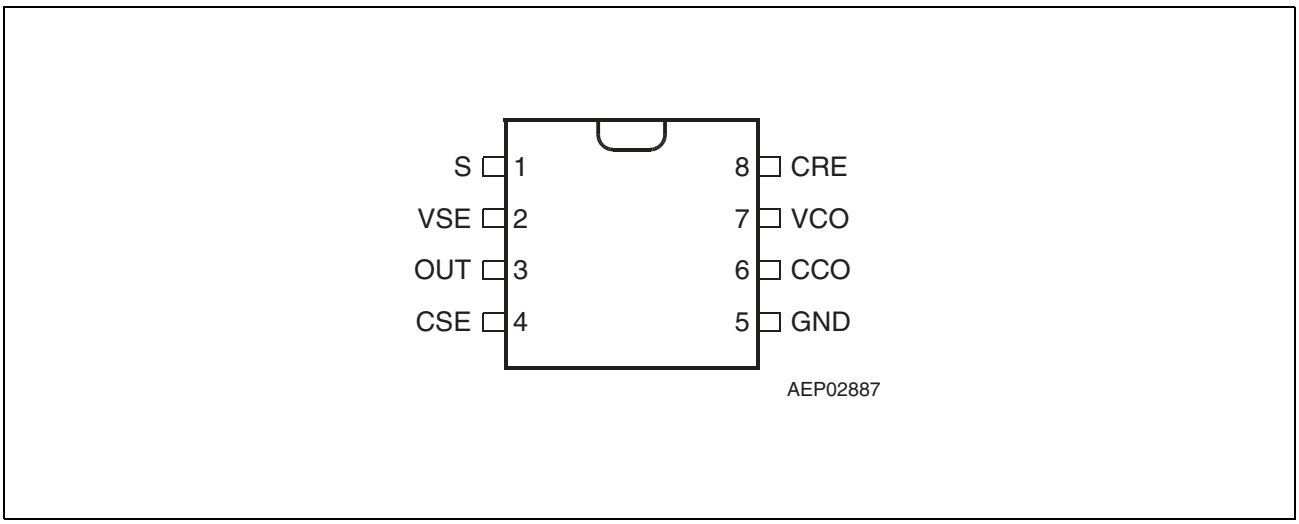


Figure 1 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin No.	Symbol	Function
1	S	**Supply voltage;** external blocking capacitor necessary (see Figure 4).
2	VSE	**Voltage Sense Input;** non inverting with respect to voltage compensation VCO; internal compared with the high accuracy bandgap-reference (typ. 2.5 V).
3	OUT	**Output;** NPN emitter follower output with an internal series resistor of 1 kΩ; controlled by the potential of VCO or CCO; output voltage is internally clamped therefore the output current is internally limited.
4	CSE	**Current Sense Input 1;** connected to an internal voltage divider (reference to the inverting input of the current OTA; see Figure 7).
5	GND	**Ground;** reference potential unless otherwise specified.
6	CCO	**Current Compensation Output;** internal series resistor to the current-OTA output (typ. 1 kΩ); amplification internal temperature compensated; current loop compensation can be done by an external capacitor to GND.
7	VCO	**Voltage Compensation Output;** internal series resistor to the voltage-OTA output (typ. 1 kΩ); amplification internal temperature compensated; voltage loop compensation can be done by an external capacitor to GND.
8	CRE	**Current-OTA Reference Input;** current sense reference input; non inverting input of the current-OTA.

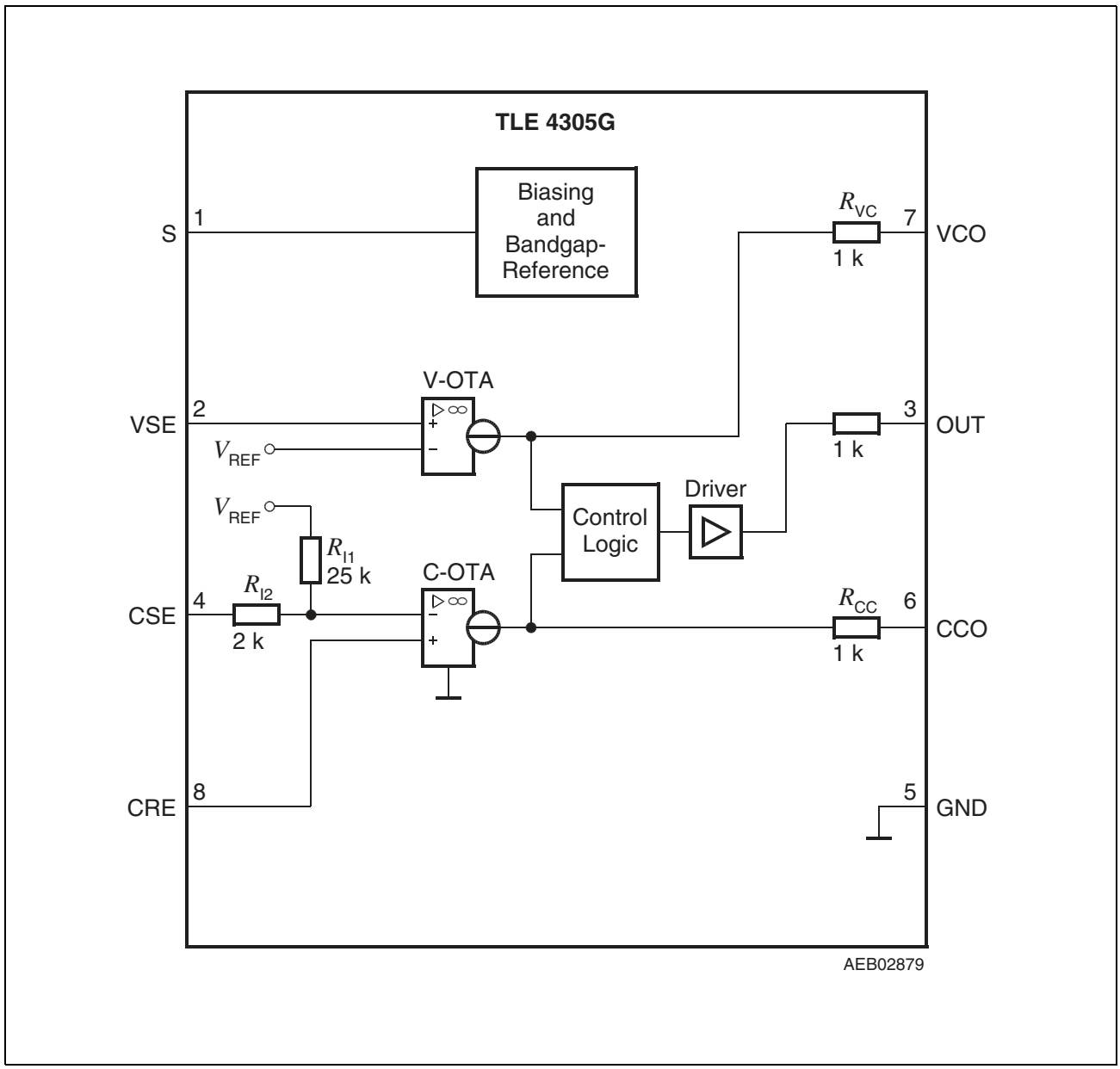


Figure 2 Block Diagram

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltages					
Supply voltage	V_S	-0.3	45	V	–
Input voltages	V_{VSE}; V_{CSE}; V_{CRE}	-0.3	7	V	–
Output voltages	V_{OUT}; V_{VCO}; V_{CCO}	-0.3	7	V	–
Currents					
Output current	I_{OUT}	-5	3	mA	–
Output current	I_{VCO}; I_{CCO}	-0.5	0.5	mA	–
ESD-Protection					
Human Body Model	V_{ESD}	-1.5	1.5	kV	according JEDEC JESD22-A114
Temperatures					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–
Thermal Resistances					
Junction ambient	$R_{thj\text{-}a}$	–	200	K/W	–

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Supply voltage	V_S	8	42	V	–
Junction temperature	T_j	-40	150	°C	–

Note: In the operating range, the functions given in the circuit description are fulfilled.

Table 4 Electrical Characteristics

8 V < V_S < 42 V; -40 °C < T_j < 150 °C; I_{OUT} = 0 mA; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Current Consumption						
Supply current	I_S	–	1	1.5	mA	V_S = 9 V; T_j = 25 °C
Supply current	I_S	–	–	2	mA	V_S = 9 V
Supply current	I_S	–	1.5	2.5	mA	V_S = 42 V; T_j = 25 °C
Supply current	I_S	–	–	4	mA	V_S = 42 V
Reference Voltage (measurable at pin CSE)						
Voltage at pin CSE	$V_{CSE,ref}$	2.45	2.50	2.55	V	T_j = 25 °C; I_{CSE} = 0 mA
Voltage at pin CSE	$V_{CSE,ref}$	2.425	–	2.575	V	I_{CSE} = 0 mA
Temperature Coefficient	$\Delta V_{CSE,ref}$	-50	–	50	ppm/K	–
Voltage-OTA; Pin VSE and VCO						
Input voltage threshold	V_{VSE}	–	V_{REF}	–	V	I_{VCO} = 0 mA; V_{VCO} = 2.5 V
Input offset voltage	$V_{VSE,io}$	-5	–	5	mV	I_{VCO} = 0 mA; V_{VCO} = 2.5 V
Transconductance	g_V	–	1	–	mS	$g_V = \Delta I_{VCO} / \Delta U_{VSE}$
Output series resistor	R_{VCO}	–	2	–	kΩ	–
Gain Bandwidth Product	B_V	–	500	–	kHz	–
Input current	I_{VSE}	-1.0	-0.2	-0	µA	V_{VSE} = 0 V
Output current; source	I_{VCO}	-150	-60	-25	µA	V_{VSE} = 5 V; V_{VCO} = 2.5 V
Output current; sink	I_{VCO}	25	60	150	µA	V_{VSE} = 0 V; V_{VCO} = 2.5 V

Table 4 Electrical Characteristics (cont'd)

8 V < V_S < 42 V; -40 °C < T_j < 150 °C; I_{OUT} = 0 mA; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Current-OTA; Pin CSE and CCO						
Input voltage threshold	V_{CSE}	-210	-200	-190	mV	I_{CCO} = 0 mA; V_{CCO} = 2.5 V
Transconductance	g_C	–	1	–	mS	$g_C = \Delta I_{CCO} / \Delta U_{CSE}$
Output series resistor	R_{CCO}	–	2	–	kΩ	–
Gain Bandwidth Product	B_C	–	500	–	kHz	–
Input current	I_{CSE}	-200	-100	-50	µA	V_{CSE} = 0 V
Output current; source	I_{CCO}	-150	-60	-25	µA	V_{CRE} = 2.5 V; V_{CSE} = 0 V; V_{CCO} = 2.5 V
Output current; sink	I_{CCO}	25	60	150	µA	V_{CRE} = 0 V; V_{CSE} = 0 V; V_{CCO} = 2.5 V
Current Reference Input Pin CRE						
Input Current	I_{CRE}	-1.0	-0.2	-0	µA	V_{CSE} = 0 V; V_{CRE} = 0 V
Output Pin OUT						
Output voltage limit	V_{OUT}	3	4	5.5	V	V_{VSE} = 5 V; $R_{OUT-GND}$ = 22 kΩ
Output current; voltage loop controlled	I_{OUT}	-8.5	-4	-2	mA	10 V < V_S < 42 V; V_{VSE} = 5 V; V_{OUT} = 0 V
Output current; voltage loop controlled	I_{OUT}	-4.5	-2.0	-0.5	mA	8 V < V_S < 10 V; V_{VSE} = 5 V; V_{OUT} = 0 V

Table 4 Electrical Characteristics (cont'd)

8 V < V_S < 42 V; -40 °C < T_j < 150 °C; I_{OUT} = 0 mA; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Output current; current loop controlled	I_{OUT}	-8.5	-4	-2	mA	10 V < V_S < 42 V; V_{CSE} = 0 V; V_{CRE} = 5 V; V_{OUT} = 0 V
Output current; current loop controlled	I_{OUT}	-4.5	-2.0	-0.5	mA	8 V < V_S < 10 V; V_{CSE} = 0 V; V_{CRE} = 5 V; V_{OUT} = 0 V

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Application Information

The TLE 4305 is a voltage and current regulator for Switch Mode Power Supply (SMPS) applications.

It controls the output voltage and the maximum output current of a power supply unit. It is located on the secondary side of the SMPS.

The TLE 4305 consists of a output voltage control loop and a current control loop. The driver is especially designed to drive the opto-isolator. The current controls the PWM duty cycle of the primary regulator.

Isolated SMPS

Switch mode power supply (SMPS) systems generate a regulated DC voltage V_Q that is isolated from the primary side. A maximum output current I_{Qmax} is defined to protect the system in any load failures.

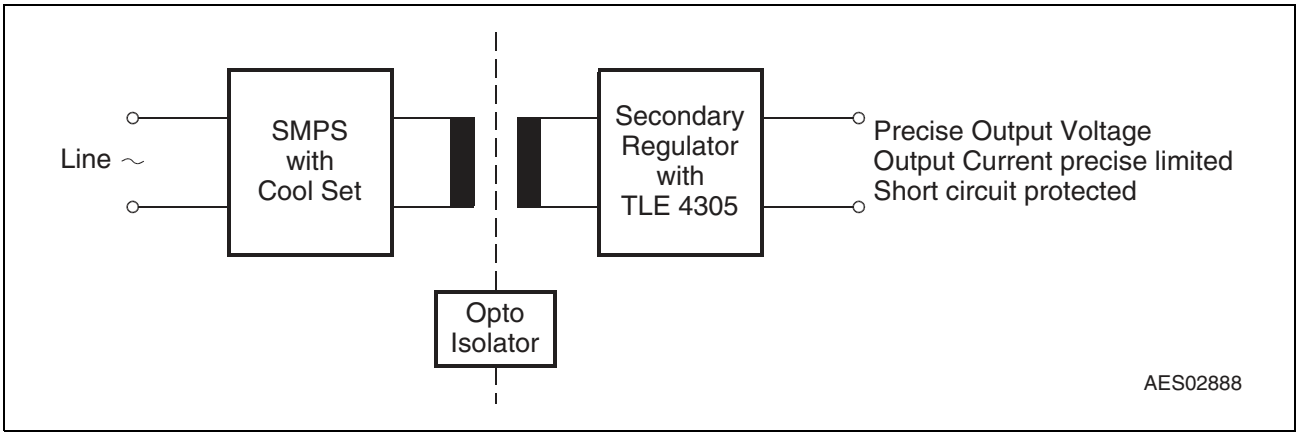


Figure 3 Isolated SMPS Principle

The principle of an isolated SMPS is shown in **Figure 3**. The primary side of the SMPS is supplied by the line. The secondary side supplies a regulated voltage to the load. Primary and secondary side are isolated from each other by the transformer and an opto isolator.

A SMPS controller such as the Infineon TDA1683x controls the PWM duty cycle of the output voltage signal. The signal is transmitted by a Transformer with n1:n2 (n: number of windings). On the secondary side a load capacitor is charged. The secondary regulator controls the output voltage V_Q and limits the output current. It generates an analog control signal to the primary side through an opto isolator to regulate the PWM duty cycle of the primary signal. The loop is closed through the primary SMPS regulator and the transformer.

Simple SMPS defines the output voltage by a voltage divider and a transistor. This requires very precise resistor values and due to the nature of the transistor the control signal is dependent on temperature and device variation. The current limitation has to be done on the primary side with elements suitable for high voltages.

SMPS with TLE 4305 Secondary Regulator

The TLE 4305 is located on the secondary side of the regulator and controls the output voltage as well as it limits the output current. Voltage and current can be chosen independent from each other by the designer according to the application's requirements.

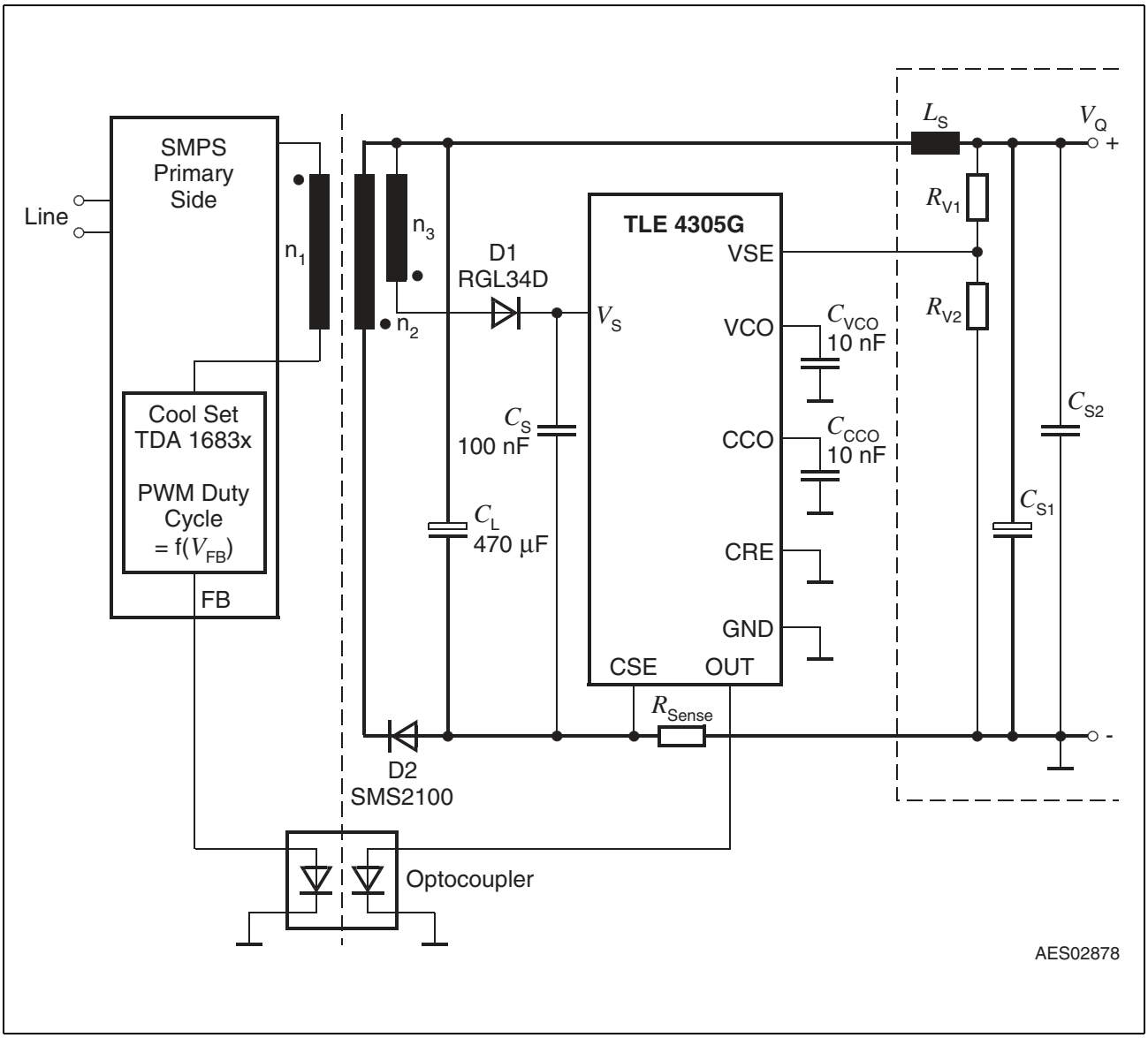


Figure 4 Application Circuit

$$V_Q = 2.5\ V \times (R_{V1} + R_{V2}) / R_{V2} \quad (1)$$

$$I_Q = 0.2\ V / R_{Sense} \quad (2)$$

Figure 3 shows the TLE 4305 as SMPS secondary regulator as application circuit. The load capacitor C_L is charged by the PWM-signal at the secondary side of the transformer. The diode D2 defines the current flow in the transformer.

The TLE 4305 includes an independent voltage control and current control loop. The internal schematic is shown in **Figure 2**. For $I_Q < I_{Qmax}$ the voltage control gets priority. If the supply operates in the overcurrent protection mode, the current loop is active and reduces the output voltage with constant output current I_{Qmax}. The output voltage/output current curve is shown in **Figure 5**.

Both the current control loop and the voltage control loop are temperature compensated.

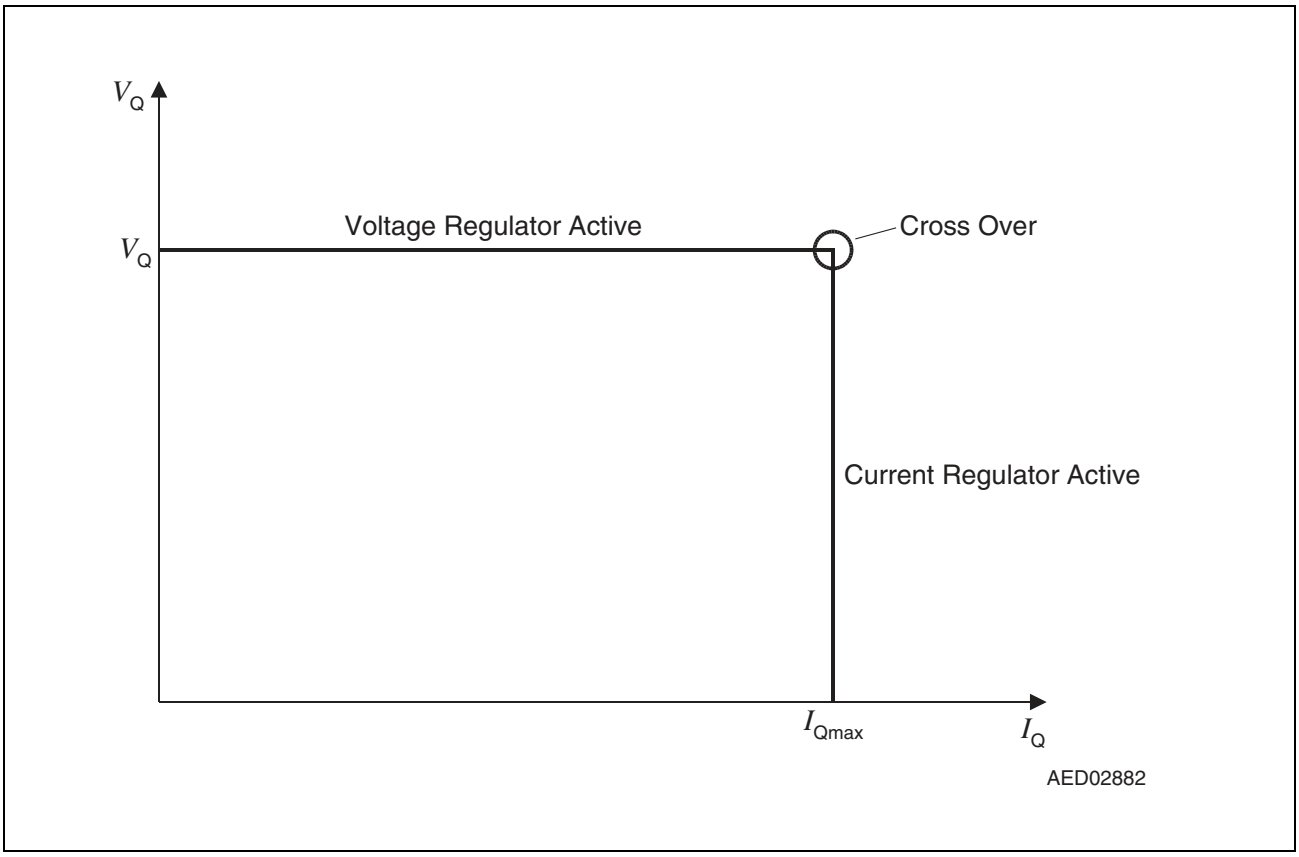


Figure 5 Current and Voltage Limit

The voltage or current loop regulator result defines the current into the opto isolator to control the PWM duty cycle. The LED driver is fully integrated, no external components are required.

Voltage Control Loop

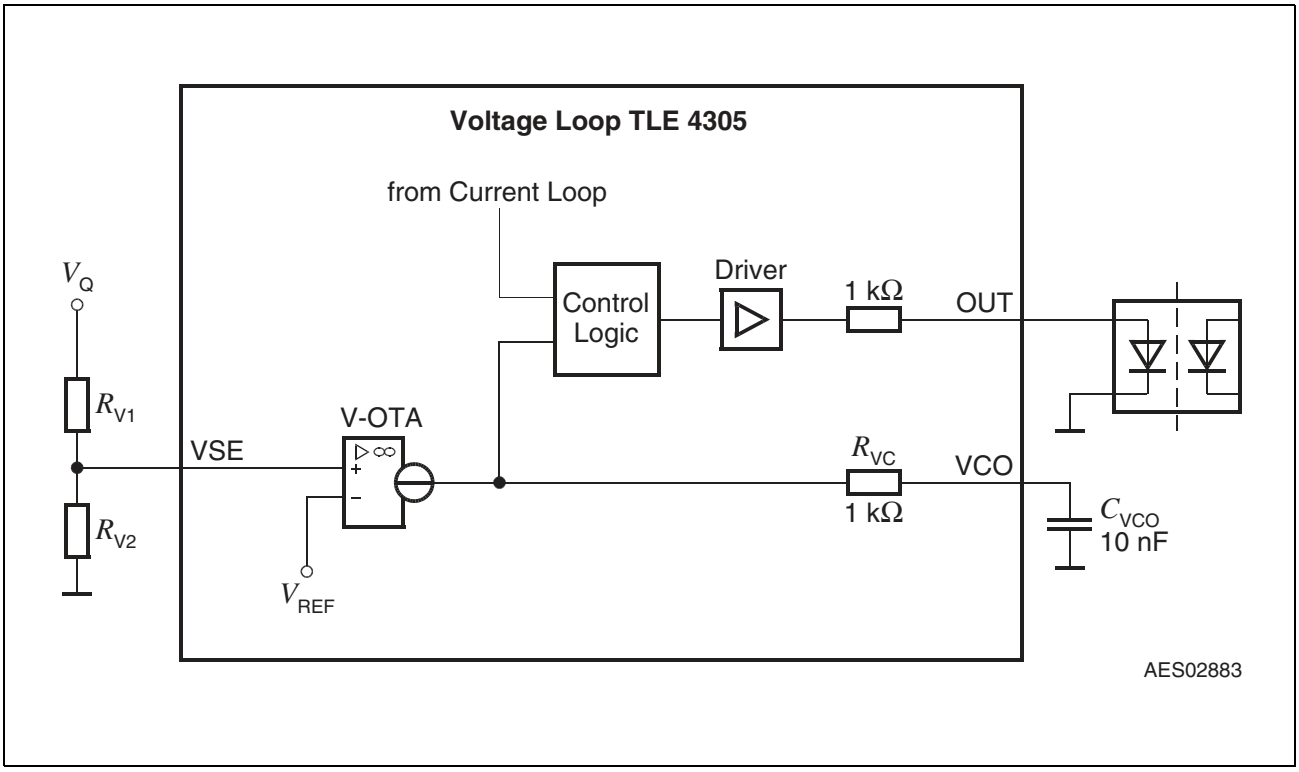


Figure 6 Voltage Loop

The voltage loop regulator compares the input voltage V_{SE} to a reference voltage V_{ref} of typical 2.5 V. The difference is attenuated and proportional current drives the opto isolator. The control loop output voltage V_Q, pin VSE, pin OUT, opto isolator, primary regulator and the transformer close the loop.

To program an output voltage a divider is used. The resistors are chosen according to **Equation (5)**.

$$V_{VSE} = V_{ref} \quad (3)$$

$$V_{VSE} = V_Q \times R_{V2} / (R_{V1} + R_{V2}) \quad (4)$$

with V_{ref} typical 2.5 V

$$V_Q = V_{VSE} \times (R_{V1} + R_{V2}) / R_{V2} \quad (5)$$

To compensate the voltage loop a 10 nF capacitor should be connected to pin VCO. With the internal 1 kΩ resistor it reduces the overall closed voltage loop's bandwidth.

If the gain of the overall loop has to be adapted to the application's needs, the output capacitor can be modified accordingly.

Current Control Loop

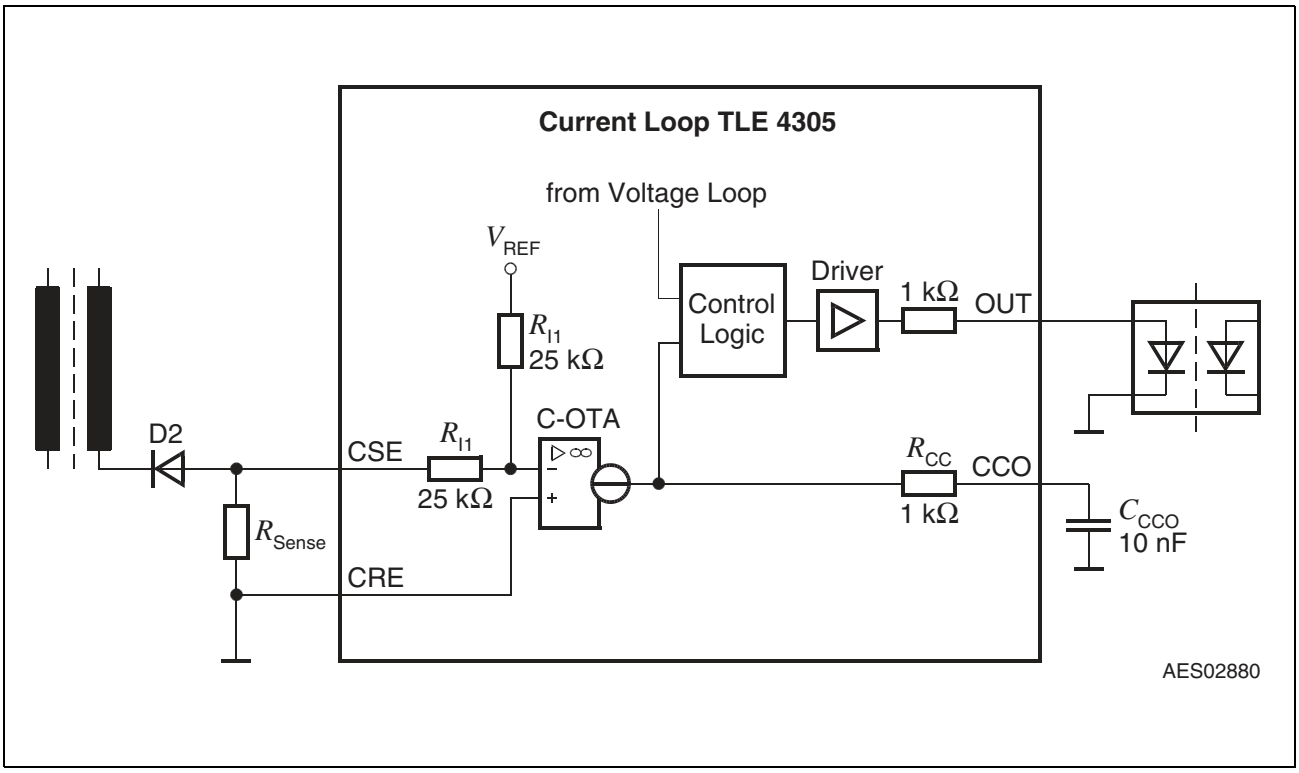


Figure 7 Current Control Loop

To detect the current a sense resistor R_{sense} is placed in the current back-path to the transformer (see **Figure 4** and **Figure 7**).

The control operational amplifier compares the voltage at pin CRE to the voltage at the inverting input of the OTA. In an overcurrent condition, the overall closed loop through current loop, opto isolator, primary regulator, transformer and the application reduces the PWM duty cycle to meet the closed loop condition.

V_{CSE} - V_{CRE} is typical 200 mV.

The current limit is defined by

$$I_{Qmax} = 200\ mV / R_{sense} \quad (6)$$

To compensate the overall closed current loop a 10 nF capacitor should be connected to pin VCO. With the internal 1 kΩ resistor it reduces the voltage loop's bandwidth.

As already explained for the voltage loop, the capacitor can be modified according to the overall loop's bandwidth.

To further improve the current control in addition a compensation can be added at pin CRE as shown in **Figure 8**.

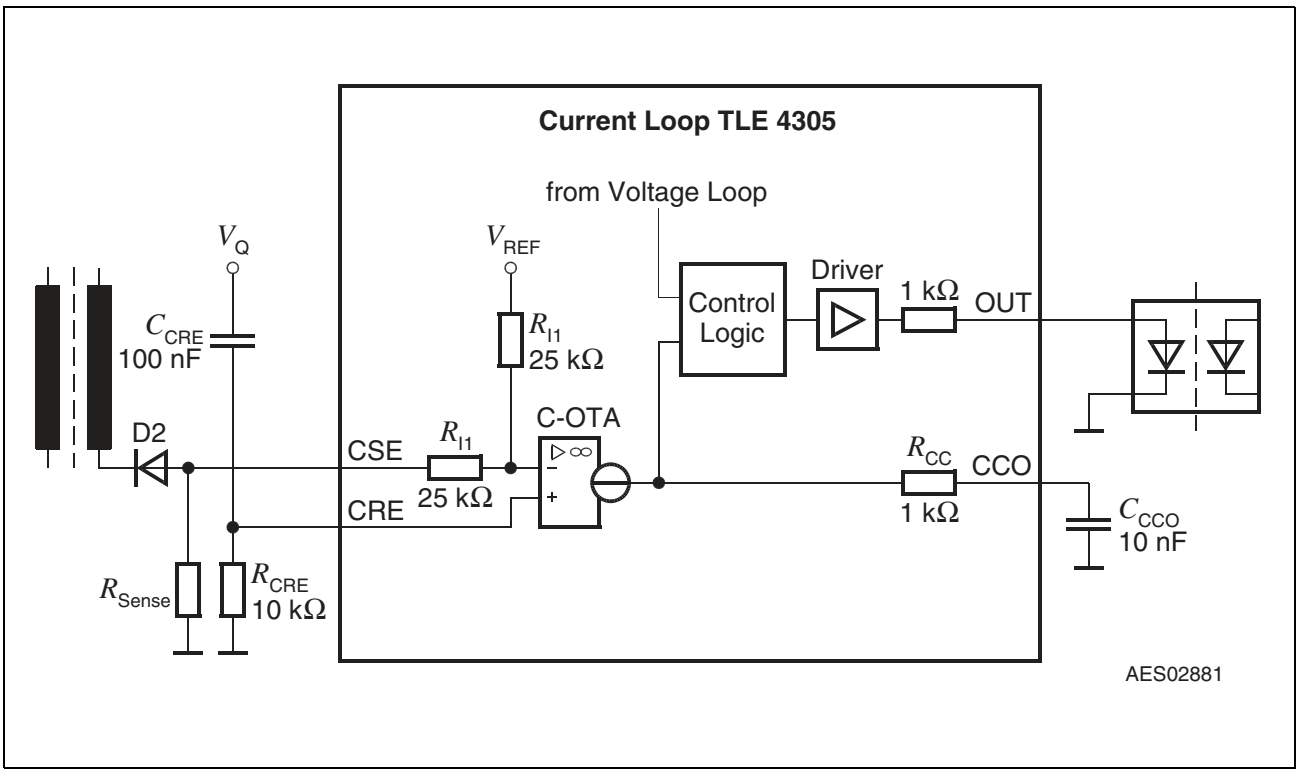


Figure 8 Improved Current Control Loop

The calculation of the current is identical to the above calculation (**Equation (6)**). The voltage at resistor R_{CRE} can be neglected (typical 2 mV for 10 kΩ resistor). The resistor R_{CRE} and the Capacitor C_{CRE} improve further the current control loop response.

Supply of the TLE 4305

The TLE 4305 is an active circuitry and requires a supply voltage at pin V_S. During start up of the supply, there is no energy stored in the load capacitor. Dependent on the required output voltage also during operation the output voltage might be too small. Therefore a second transformer-winding n3 is required. The voltage charges the input capacitor C_S though the diode D1. Internally the TLE 4305 generates for input voltages above 8 V a preregulated 6 V internal rail. The device generates biasing currents and reference voltages from this rail.

To avoid Ground and V_Q-shifts, all GND connections should be connected to one point as well as all V_Q-signals.

If the application requires more than one voltage linear post-regulators can be used. In the application a choke should be placed in series. An electrolyte or tantalum capacitor of 10 µF to 100 µF should be used in parallel to a 10 to 100 nF ceramic capacitor to filter high frequency noise. The size of the choke and the capacitors depend on the application requirements.

Package Outlines

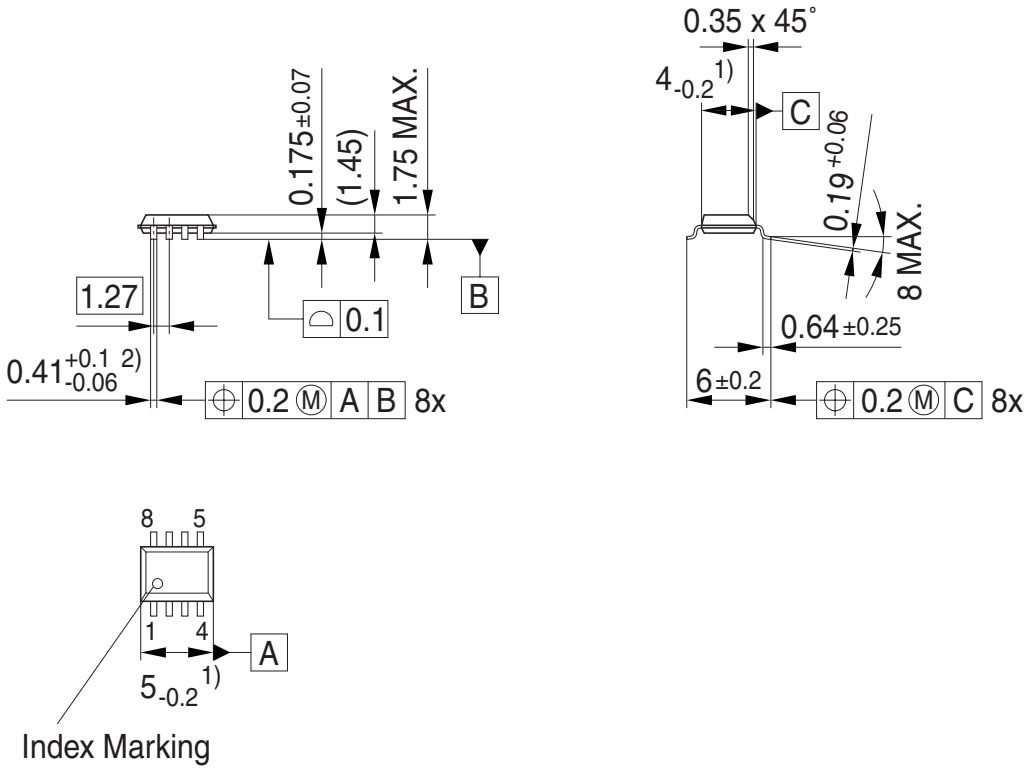


Figure 9 **PG-DSO-8** (Plastic Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

Revision History

Version	Date	Changes
Rev. 2.2	2008-11-17	Initial version of RoHS-compliant derivate of TLE 4305. **Page 4**: ESD rating changed to HBM 1.5kV with modified test condition (changed test standard to JEDEC JESD22-A114) **Page 1** and **Page 14**: RoHS compliance statement and Green product feature added **Page 1** and **Page 14**: Package changed to RoHS compliant version Legal Disclaimer updated

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