Fault Protection and Detection, 10 Ω R_{ON}, Dual SPDT Switch

Data Sheet **ADG5436F**

FEATURES

- Overvoltage protection up to −55 V and +55 V
  - Power-off protection up to −55 V and +55 V
  - Overvoltage detection on source pins
  - Interrupt flags indicate fault status
- Low on resistance: 10 Ω (typical)
  - On-resistance flatness of 0.5 Ω (maximum)
- 6 kV human body model (HBM) ESD rating
- Latch-up immune under any circumstance
- Known state without digital inputs present
- V_{SS} to V_{DD} analog signal range
  - ±5 V to ±22 V dual supply operation
  - 8 V to 44 V single-supply operation
  - Fully specified at ±15 V, ±20 V, +12 V, and +36 V

APPLICATIONS

- Analog input/output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation
- Avionics
- Automatic test equipment
- Communication systems
- Relay replacement

FUNCTIONAL BLOCK DIAGRAM

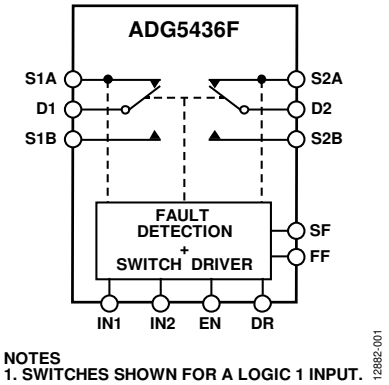

Figure 1.

GENERAL DESCRIPTION

The ADG5436F is an analog multiplexer, containing two independently selectable single-pole, double-throw (SPDT) switches. An EN input is used to disable all the switches. For use in multiplexer applications, both switches exhibit break-before-make switching action.

Each channel conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. The digital inputs are compatible with 3 V logic inputs over the full operating supply range.

When no power supplies are present, the switch remains in the off condition, and the channel inputs are high impedance. Under normal operating conditions, if the analog input signal level on any Sxx pin exceeds V_{DD} or V_{SS} by a threshold voltage, V_T, the channel turns off and that Sxx pin becomes high impedance. If the channel is on, the drain pin reacts according to the drain response (DR) input pin. If the DR pin is left floating or pulled high, the drain remains high impedance and floats. If the DR pin is pulled low, the drain pulls to the exceeded rail. Input signal levels of up to +55 V or −55 V relative to ground are blocked, in both the powered and unpowered conditions. The low on resistance of the ADG5436F, combined with the on-resistance flatness over a significant portion of the signal range, makes it an ideal solution for data acquisition and gain switching applications where excellent linearity and low distortion are critical.

Note that, throughout this data sheet, the dual function pin names are referenced only by the relevant function where applicable. See the Pin Configurations and Function Descriptions section for full pin names and function descriptions.

PRODUCT HIGHLIGHTS

1. Source pins are protected against voltages greater than the supply rails, up to −55 V and +55 V.
2. Source pins are protected against voltages between −55 V and +55 V in an unpowered state.
3. Overvoltage detection with digital output indicates the operating state of the switches.
4. Trench isolation guards against latch-up.
5. Optimized for low on resistance and on-resistance flatness.
6. The ADG5436F operates from a dual supply of ±5 V up to ±22 V, or a single power supply of 8 V up to 44 V.

Rev. C Document Feedback

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REVISION HISTORY

10/2017—Rev. B to Rev. C

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1/2015—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 13.5 V, V_{SS} = −13.5 V, see Figure 30
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	10			Ω typ	Voltage on the Sxx pins (V_S) = ±10 V, I_S = −10 mA
	11.2	14	16.5	Ω max	
	9.5			Ω typ	V_S = ±9 V, I_S = −10 mA
	10.7	13.5	16	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.15			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.65	0.8	0.95	Ω max	
	0.15			Ω typ	V_S = ±9 V, I_S = −10 mA
	0.6	0.7	0.8	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.6			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.9	1.1	1.1	Ω max	
	0.1			Ω typ	V_S = ±9 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 26
LEAKAGE CURRENTS					V_{DD} = 16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±10 V, voltage on the Dx pin (V_D) = ∓10 V, see Figure 31
	±1.5	±5.0	±21	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V, see Figure 31
	±1.5	±7.0	±25	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.5			nA typ	V_S = V_D = ±10 V, see Figure 32
	±1.5	±5.0	±21	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage			±72	µA typ	V_{DD} = 16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±55 V, see Figure 35
Power Supplies Grounded or Floating			±49	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, EN = 0 V or floating, INx = 0 V or floating, V_S = ±55 V, see Figure 36
Drain Leakage Current, I_D					DR = floating or >2 V
With Overvoltage	±2.0			nA typ	V_{DD} = 16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±55 V, see Figure 35
	±20	±30	±65	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, INx = 0 V or floating, V_S = ±55 V, EN = 0 V, see Figure 36
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, EN = 0 V, see Figure 36
DIGITAL INPUTS/OUTPUTS					
Input Voltage High, V_{INH}			2.0	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			±1.2	µA max	
Digital Input Capacitance, C_{IN}	6.0			pF typ	
Output Voltage High, V_{OH}	2.0			V min	
Output Voltage Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	400			ns typ	R_L = 300 Ω, C_L = 35 pF
	540	555	570	ns max	V_S = 10 V, see Figure 46
t_{ON} (EN)	435			ns typ	R_L = 300 Ω, C_L = 35 pF
	515	530	550	ns max	V_S = 10 V, see Figure 45
t_{OFF} (EN)	165			ns typ	R_L = 300 Ω, C_L = 35 pF
	210	215	220	ns max	V_S = 10 V, see Figure 45
Break-Before-Make Time Delay, t_D	320			ns typ	R_L = 300 Ω, C_L = 35 pF
			190	ns min	V_S = 10 V, see Figure 44
Overvoltage Response Time, $t_{RESPONSE}$	510			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 39
	680	725	750	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	820			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 40
	1100	1150	1200	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 12 pF, see Figure 41
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 12 pF, see Figure 42
	600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 43
Charge Injection, Q_{INJ}	−724			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 47
Off Isolation	−71			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
Channel-to-Channel Crosstalk	−73			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 15 V p-p, f = 20 Hz to 20 kHz, see Figure 38
−3 dB Bandwidth	169			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 37
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
Source Capacitance (C_S), Off	12			pF typ	V_S = 0 V, f = 1 MHz
Drain Capacitance (C_D), Off	24			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	37			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 16.5 V, V_{SS} = −16.5 V, GND = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	Digital inputs = 5 V
	1.0		1.8	mA max	V_S = ±55 V, V_D = 0 V
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design. Not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = 20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 18 V, V_{SS} = −18 V, see Figure 30
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	10			Ω typ	V_S = ±15 V, I_S = −10 mA
	11.5	14.5	16.5	Ω max	
	9.5			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	11	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.15			Ω typ	V_S = ±15 V, I_S = −10 mA
	0.65	0.8	0.95	Ω max	
	0.15			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	0.6	0.7	0.8	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.0			Ω typ	V_S = ±15 V, I_S = −10 mA
	1.4	1.5	1.5	Ω max	
	0.1			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 26
LEAKAGE CURRENTS					V_{DD} = 22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ±15 V, see Figure 31
	±1.5	±5.0	±21	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ±15 V, see Figure 31
	±1.5	±7.0	±25	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.5			nA typ	V_S = V_D = ±15 V, see Figure 32
	±1.5	±5.0	±21	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage			±84	µA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±55 V, see Figure 35
Power Supplies Grounded or Floating			±49	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, EN = 0 V or floating, INx = 0 V or floating, V_S = ±55 V, see Figure 36
Drain Leakage Current, I_D					DR = floating or >2 V
With Overvoltage	±5.0			nA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, INx = 0 V or floating, V_S = ±55 V, see Figure 35
	±1.0	±1.0	±1.0	µA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, EN = 0 V, see Figure 36
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, EN = 0 V, see Figure 36
DIGITAL INPUTS					
Input Voltage High, V_{INH}			2.0	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	6.0			pF typ	
Output Voltage High, V_{OH}	2.0			V min	
Output Voltage Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	405			ns typ	R_L = 300 Ω, C_L = 35 pF
	540	555	570	ns max	V_S = 10 V, see Figure 46
t_{ON} (EN)	430			ns typ	R_L = 300 Ω, C_L = 35 pF
	535	560	585	ns max	V_S = 10 V, see Figure 45
t_{OFF} (EN)	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	205	210	215	ns max	V_S = 10 V, see Figure 45
Break-Before-Make Time Delay, t_D	330			ns typ	R_L = 300 Ω, C_L = 35 pF
			205	ns min	V_S = 10 V, see Figure 44
Overvoltage Response Time, $t_{RESPONSE}$	430			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 39
	560	605	630	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	930			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 40
	1300	1500	1700	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 12 pF, see Figure 41
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 12 pF, see Figure 42
	600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 43
Charge Injection, Q_{INJ}	−737			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 47
Off Isolation	−72			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
Channel-to-Channel Crosstalk	−73			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 20 V p-p, f = 20 Hz to 20 kHz, see Figure 38
−3 dB Bandwidth	171			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 37
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
C_S (Off)	11			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	23			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	36			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 22 V, V_{SS} = −22 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	Digital inputs = 5 V
	1.0		1.8	mA max	V_S = ±55 V, V_D = 0 V
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design. Not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V, V_{SS} = 0 V, see Figure 30
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	22			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	24.5	31	37	Ω max	
	10			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −10 mA
	11.2	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.2			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.65	0.8	0.95	Ω max	
	0.2			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −10 mA
	0.65	0.8	0.95	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	14.5	19	23	Ω max	
	0.6			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −10 mA
	0.9	1.1	1.3	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 26
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 31
	±1.5	±5.0	±21	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 31
	±1.5	±7.0	±25	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.5			nA typ	V_S = V_D = 1 V/10 V, see Figure 32
	±1.5	±5.0	±21	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage			±65	µA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 35
Power Supplies Grounded or Floating			±49	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, EN = 0 V or floating, V_S = ±55 V, see Figure 36
Drain Leakage Current, I_D					DR = floating or >2 V
With Overvoltage	±2.0			nA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, INx = 0 V or floating, V_S = ±55 V, see Figure 35
	±20	±30	±65	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, EN = 0 V, see Figure 36
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, EN = 0 V, see Figure 36
DIGITAL INPUTS					
Input Voltage High, V_{INH}			2.0	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	6.0			pF typ	
Output Voltage High, V_{OH}	2.0			V min	
Output Voltage Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	400			ns typ	R_L = 300 Ω, C_L = 35 pF
	545	560	570	ns max	V_S = 10 V, see Figure 46
t_{ON} (EN)	435			ns typ	R_L = 300 Ω, C_L = 35 pF
	515	530	550	ns max	V_S = 8 V, see Figure 45
t_{OFF} (EN)	185			ns typ	R_L = 300 Ω, C_L = 35 pF
	230	240	250	ns max	V_S = 8 V, see Figure 45
Break-Before-Make Time Delay, t_D	300			ns typ	R_L = 300 Ω, C_L = 35 pF
			180	ns min	V_S = 8 V, see Figure 44
Overvoltage Response Time, $t_{RESPONSE}$	590			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 39
	770	830	870	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	680			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 40
	850	910	1000	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 12 pF, see Figure 41
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 12 pF, see Figure 42
	600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 43
Charge Injection, Q_{INJ}	−341			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 47
Off Isolation	−68			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Total Harmonic Distortion Plus Noise, THD + N	0.007			% typ	R_L = 10 kΩ, V_S = 6 V p-p, f = 20 Hz to 20 kHz, see Figure 38
−3 dB Bandwidth	152			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 37
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
C_S (Off)	14			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	30			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	41			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V, V_{SS} = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	Digital inputs = 5 V
	1.0		1.8	mA max	V_S = ±55 V, V_D = 0 V
V_{DD}			8	V min	GND = 0 V
			44	V max	GND = 0 V

[1] Guaranteed by design. Not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 32.4 V, V_{SS} = 0 V, see Figure 30
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	22			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	24.5	31	37	Ω max	
	10			Ω typ	V_S = 4.5 V to 28 V, I_S = −10 mA
	11	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.15			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	0.65	0.8	0.95	Ω max	
	0.15			Ω typ	V_S = 4.5 V to 28 V, I_S = −10 mA
	0.6	0.7	0.8	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	14.5	19	23	Ω max	
	0.1			Ω typ	V_S = 4.5 V to 28 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 26
LEAKAGE CURRENTS					V_{DD} =39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 31
	±1.5	±5.0	±21	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 31
	±1.5	±7.0	±25	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.5			nA typ	V_S = V_D = 1 V/30 V, see Figure 32
	±1.5	±5.0	±21	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage			±60	µA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, INx = 0 V or floating, V_S = +55 V, −40 V, see Figure 35
Power Supplies Grounded or Floating			±49	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = +55 V, −40 V, see Figure 36
Drain Leakage Current, I_D					DR = floating or >2 V
With Overvoltage	±2.0			nA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +55 V, −40 V, see Figure 35
	±20	±30	±65	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = +55 V, −40 V, EN = 0 V, see Figure 36
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = +55 V, −40 V, EN = 0 V, see Figure 36
DIGITAL INPUTS					
Input Voltage High, V_{INH}			2.0	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	6.0			pF typ	
Output Voltage High, V_{OH}	2.0			V min	
Output Voltage Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	400			ns typ	R_L = 300 Ω, C_L = 35 pF
	540	555	570	ns max	V_S = 10 V, see Figure 46
t_{ON} (EN)	440			ns typ	R_L = 300 Ω, C_L = 35 pF
	520	540	560	ns max	V_S = 18 V, see Figure 45
t_{OFF} (EN)	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	190	195	200	ns max	V_S = 18 V, see Figure 45
Break-Before-Make Time Delay, t_D	330			ns typ	R_L = 300 Ω, C_L = 35 pF
			210	ns min	V_S = 18 V, see Figure 44
Overvoltage Response Time, $t_{RESPONSE}$	260			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 39
	340	360	385	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	1500			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 40
	2100	2400	2700	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 12 pF, see Figure 41
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 12 pF, see Figure 42
	600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 43
Charge Injection, Q_{INJ}	−627			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF, see Figure 47
Off Isolation	−71			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
Channel-to-Channel Crosstalk	−73			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 18 V p-p, f = 20 Hz to 20 kHz, see Figure 38
−3 dB Bandwidth	173			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 37
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
C_S (Off)	11			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	23			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)	36			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V, V_{SS} = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					V_S = +55 V, −40 V
I_{DD}	1.2			mA typ	
	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	Digital inputs = 5 V
	1.0		1.8	mA max	V_S = ±55 V, V_D = 0 V
V_{DD}			8	V min	GND = 0 V
			44	V max	GND = 0 V

[1] Guaranteed by design. Not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sxx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
16-Lead TSSOP					
θ_{JA} = 112.6°C/W	113	77	50	mA max	$V_S = V_{SS} + 4.5$ V to $V_{DD} - 4.5$ V
	88	61	42	mA max	$V_S = V_{SS}$ to V_{DD}
16-Lead LFCSP					
θ_{JA} = 30.4°C/W	207	125	68	mA max	$V_S = V_{SS} + 4.5$ V to $V_{DD} - 4.5$ V
	161	103	61	mA max	$V_S = V_{SS}$ to V_{DD}

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	−48 V to +0.3 V
Sxx to GND	−55 V to +55 V
Sxx to V_{DD} or V_{SS}	80 V
V_S to V_D	80 V
Dx Pin[1] to GND	V_{SS} − 0.7 V to V_{DD} + 0.7 V or 30 mA, whichever occurs first
Digital Inputs to GND	GND − 0.7 V to 48 V or 30 mA, whichever occurs first
Peak Current, Sxx or Dx Pins	288 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sxx or Dx	Data[2] + 15%
Digital Output	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
Dx Pin, Overvoltage State, DR = GND, Load Current	1 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb-Free	As per JEDEC J-STD-020
ESD Rating, HBM: ESDA/JEDEC JS-001-2011	
Input/Output (I/O) Port to Supplies	6 kV
I/O Port to I/O Port	6 kV
All Other Pins	6 kV

[1] Overvoltages at the Dx pin are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5.

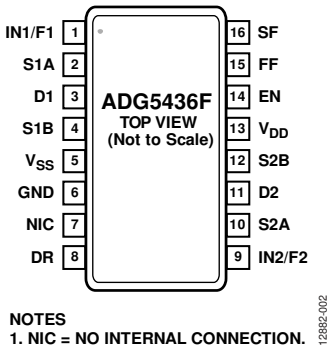
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

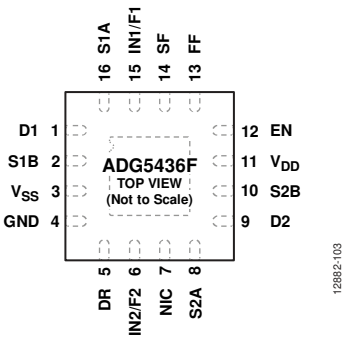
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION.

Figure 2. TSSOP Pin Configuration



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. THE EXPOSED PAD IS INTERNALLY CONNECTED. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE CONNECTED TO THE LOWEST SUPPLY VOLTAGE, V_{SS}.

Figure 3. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	IN1/F1	Logic Control Input 1 (IN1). See Table 8. Decoder Pin (F1). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 9.
2	16	S1A	Overvoltage Protected Source Terminal 1A. This pin can be an input or output.
3	1	D1	Drain Terminal 1. This pin can be an input or output.
4	2	S1B	Overvoltage Protected Source Terminal 1B. This pin can be an input or output.
5	3	V_{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7	7	NIC	No Internal Connection.
8	5	DR	Drain Response Digital Input. Tying this pin to GND enables the drain to pull to V_{DD} or V_{SS} during an overvoltage fault condition. The default condition of the drain is open-circuit when the pin is left floating or if it is tied to V_{DD}.
9	6	IN2/F2	Logic Control Input 2 (IN2). See Table 8. Decoder Pin (F2). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 9.
10	8	S2A	Overvoltage Protected Source Terminal 2A. This pin can be an input or output.
11	9	D2	Drain Terminal 2. This pin can be an input or output.
12	10	S2B	Overvoltage Protected Source Terminal 2B. This pin can be an input or output.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the INx logic inputs determine the on switches.
15	13	FF	Fault Flag Digital Output. This pin has a high output when the device is in normal operation or a low output when a fault condition occurs on any of the Sxx inputs. The FF pin has a weak internal pull-up that allows the signals to be combined into a single interrupt for larger modules that contain multiple devices.
16	14	SF	Specific Fault Digital Output. This pin has a high output when the device is in normal operation, or a low output when a fault condition is detected on a specific pin, depending on the state of F1 and F2 per Table 9.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the lowest supply voltage, V_{SS}.

TRUTH TABLES FOR SWITCHES

Table 8. Truth Table

INx	SxA	SxB
0	Off	On
1	On	Off

Table 9. Fault Diagnostic Output Truth Table

	State of Specific Fault Pin (SF) with Decoder Pins (F2, F1)				
Switch in Fault[1]	F2 = 0, F1 = 0	F2 = 0, F1 = 1	F2 = 1, F1 = 0	F2 = 1, F1 = 1	State of Fault Flag (FF)
None	1	1	1	1	1
S1A	0	1	1	1	0
S1B	1	0	1	1	0
S2A	1	1	1	0	0
S2B	1	1	0	1	0
S1A, S1B	0	0	1	1	0
S1A, S2A	0	1	1	0	0
S1A, S2B	0	1	0	1	0
S1B, S2A	1	0	1	0	0
S1B, S2B	1	0	0	1	0
S2A, S2B	1	1	0	0	0
S1A, S1B, S2A	0	0	1	0	0
S1A, S1B, S2B	0	0	0	1	0
S1A, S2A, S2B	0	1	0	0	0
S1B, S2A, S2B	1	0	0	0	0
S1A, S1B, S2A, S2B	0	0	0	0	0

[1] Note that more than one pin can be in fault at any one time. See the Applications Information section for more details.

TYPICAL PERFORMANCE CHARACTERISTICS

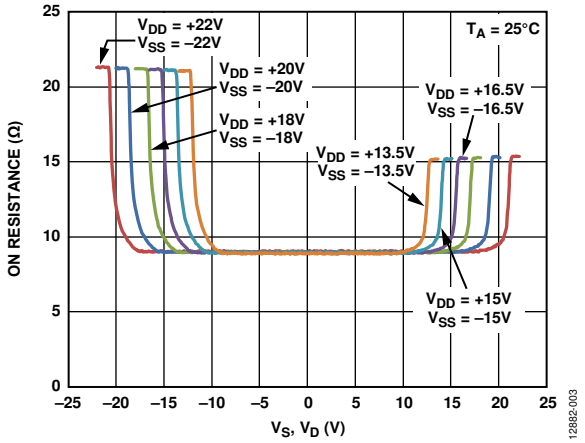


Figure 4. R_{ON} as a Function of V_S and V_D, Various Dual Supplies

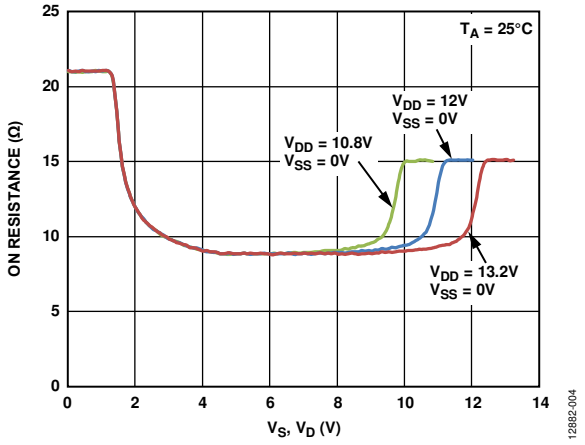


Figure 5. R_{ON} as a Function of V_S and V_D, 12 V Single Supply

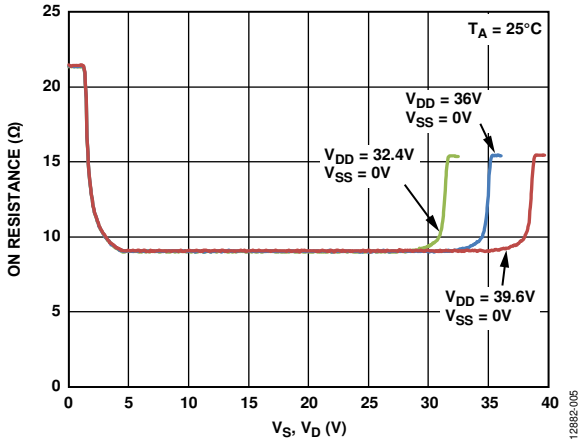


Figure 6. R_{ON} as a Function of V_S and V_D, 36 V Single Supply

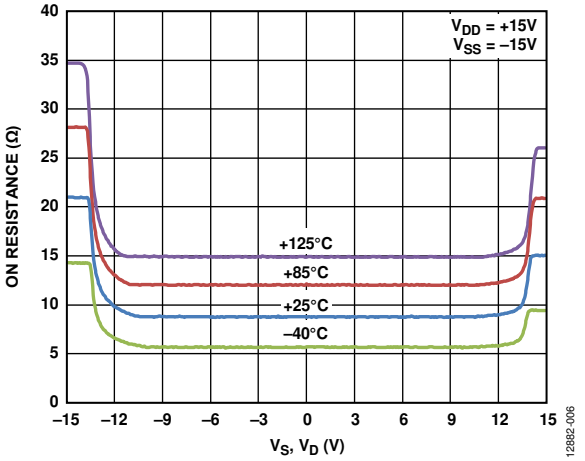


Figure 7. R_{ON} as a Function of V_S and V_D for Different Temperatures, ±15 V Dual Supply

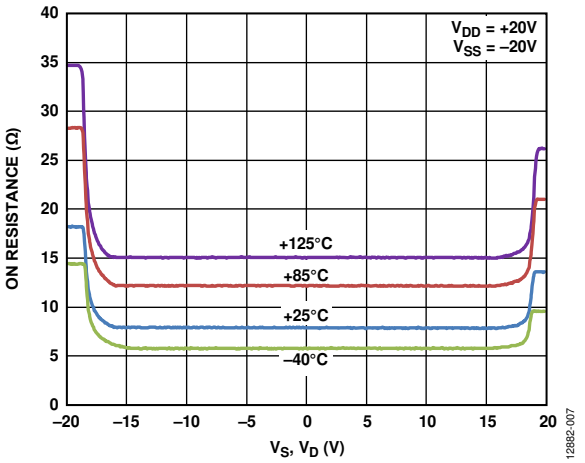


Figure 8. R_{ON} as a Function of V_S and V_D for Different Temperatures, ±20 V Dual Supply

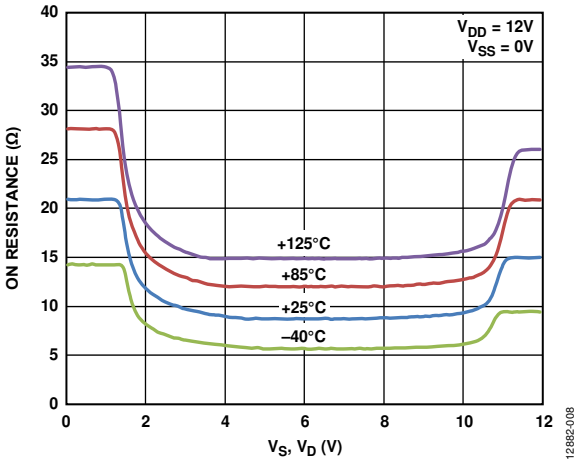


Figure 9. R_{ON} as a Function of V_S and V_D for Different Temperatures, 12 V Single Supply

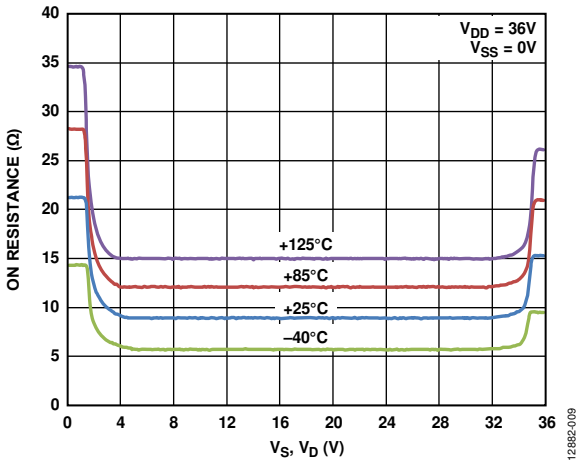


Figure 10. R_{ON} as a Function of V_S and V_D for Different Temperatures, 36 V Single Supply

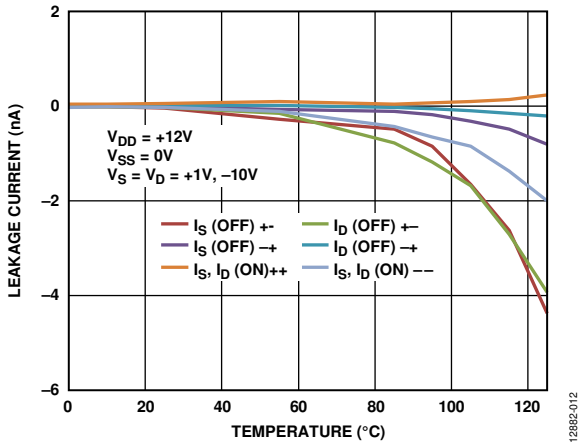


Figure 13. Leakage Current vs. Temperature, 12 V Single Supply

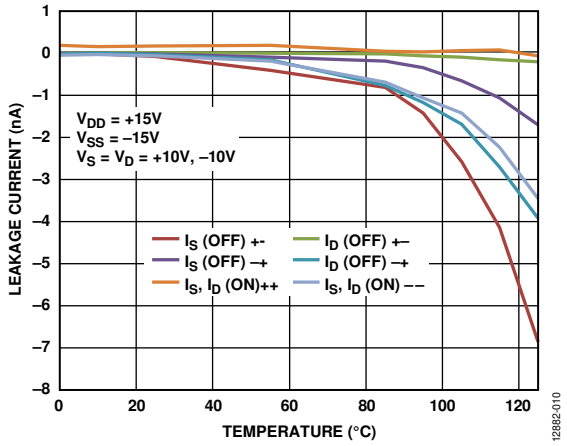


Figure 11. Leakage Current vs. Temperature, ±15 V Dual Supply

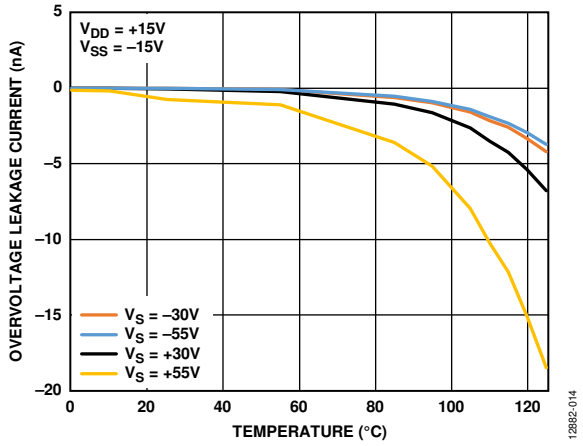


Figure 14. Overvoltage Leakage Current vs. Temperature, ±15 V Dual Supply

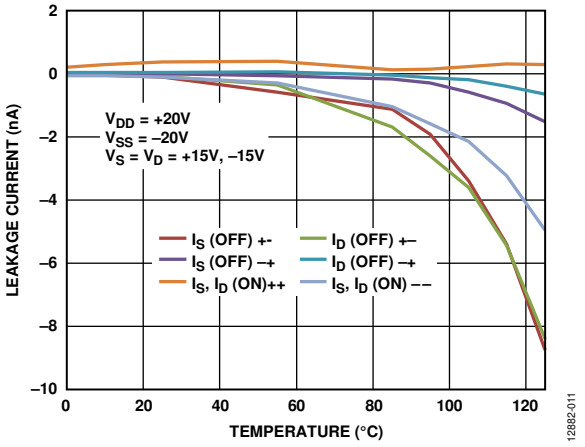


Figure 12. Leakage Current vs. Temperature, ±20 V Dual Supply

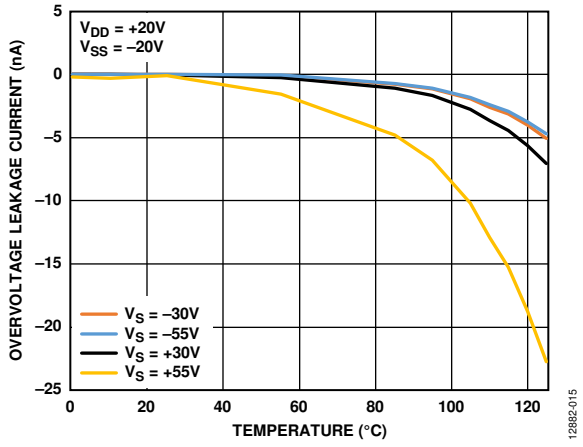


Figure 15. Overvoltage Leakage Current vs. Temperature, ±20 V Dual Supply

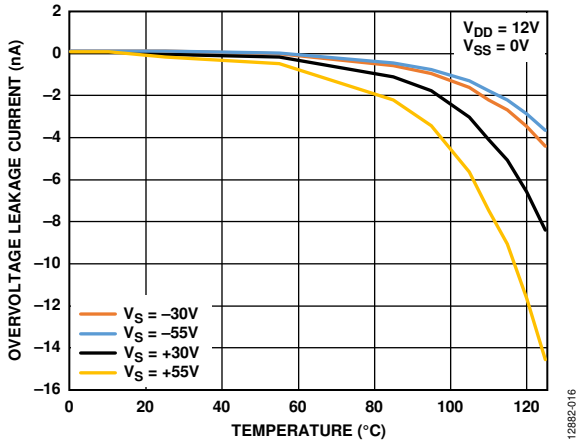


Figure 16. Overvoltage Leakage Current vs. Temperature, 12 V Single Supply

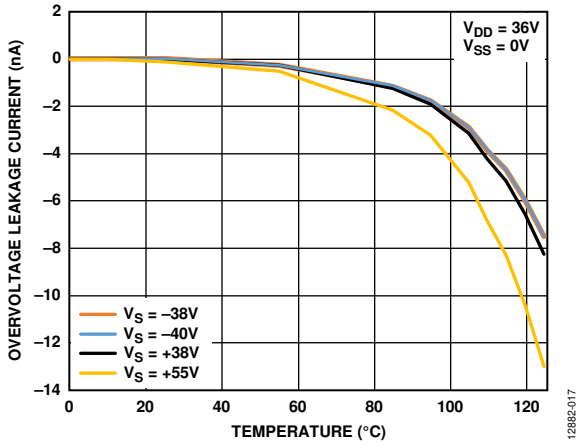


Figure 17. Overvoltage Leakage Current vs. Temperature, 36 V Single Supply

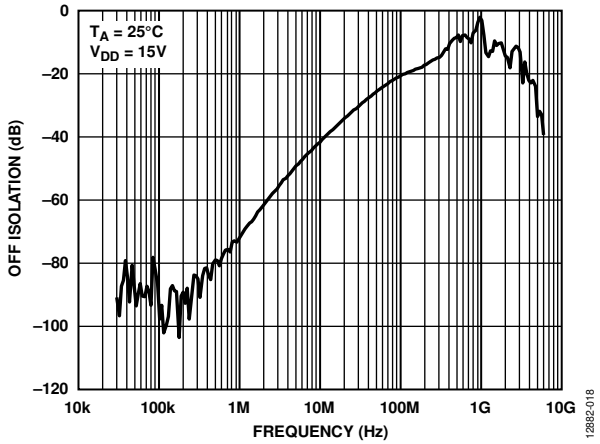


Figure 18. Off Isolation vs. Frequency

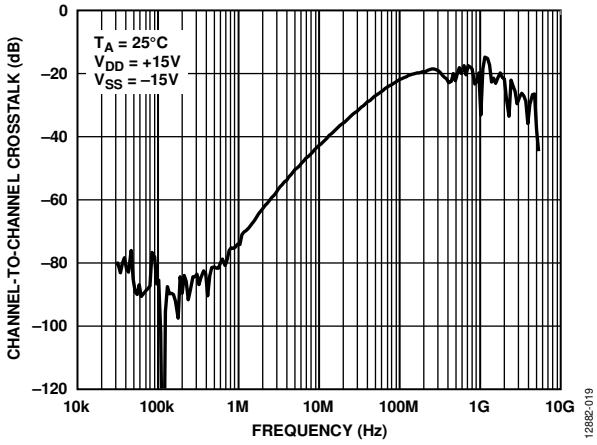


Figure 19. Channel-to-Channel Crosstalk vs. Frequency

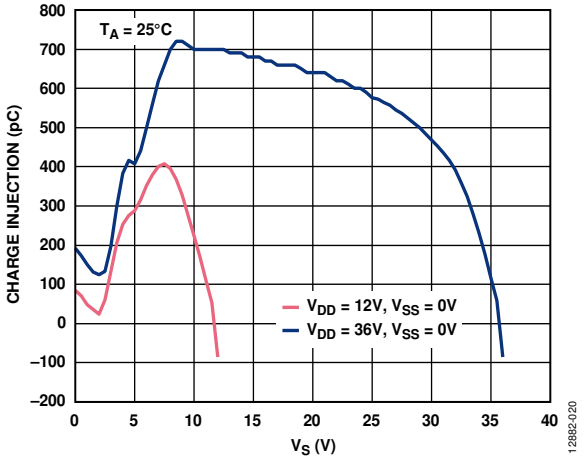


Figure 20. Charge Injection vs. Source Pin Voltage (V_S), Single Supply

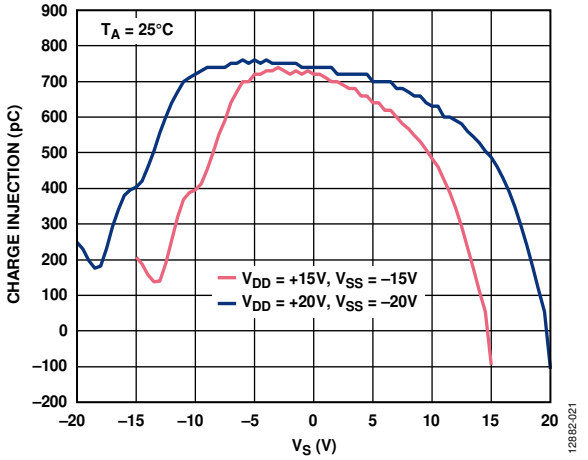


Figure 21. Charge Injection vs. Source Pin Voltage (V_S), Dual Supply

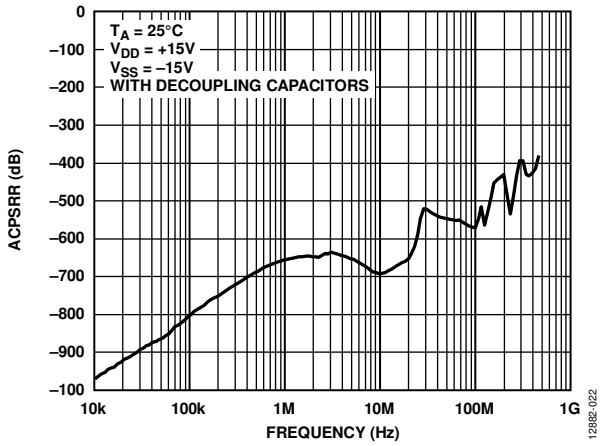


Figure 22. ACPSRR vs. Frequency

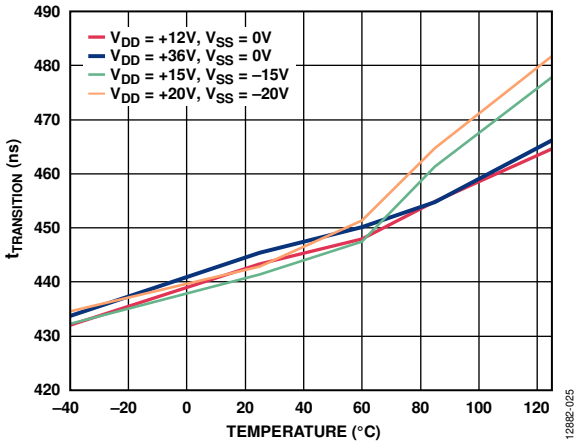


Figure 25. $t_{TRANSITION}$ vs. Temperature

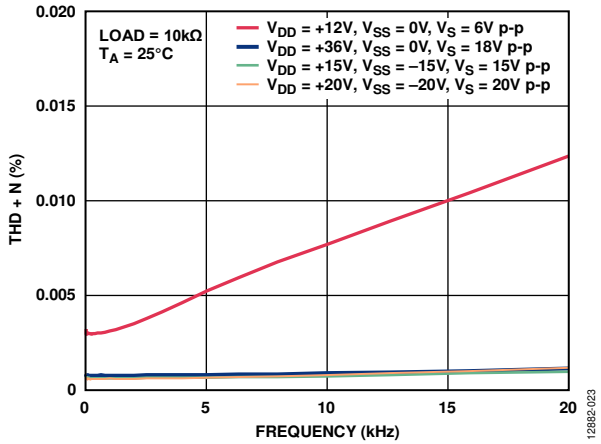


Figure 23. THD + N vs. Frequency

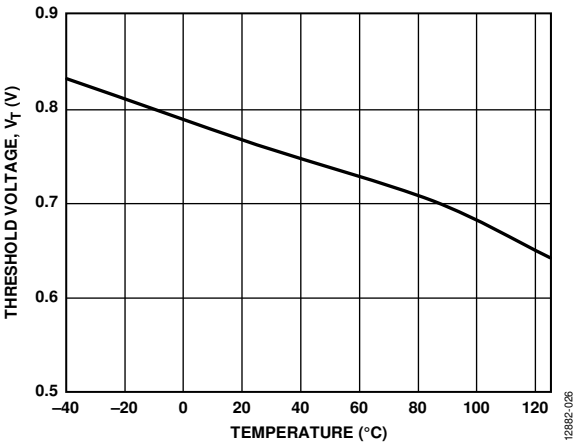


Figure 26. Threshold Voltage (V_T) vs. Temperature

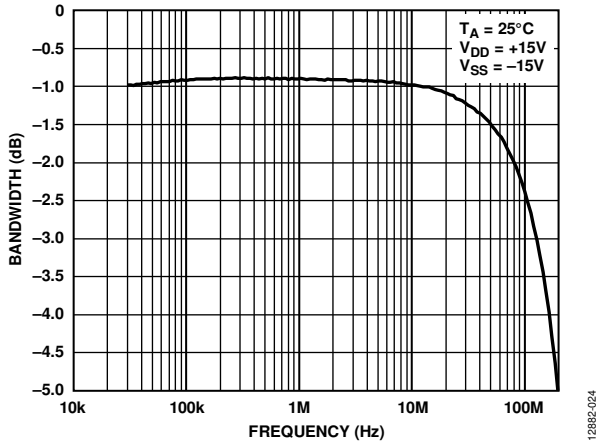


Figure 24. Bandwidth vs. Frequency

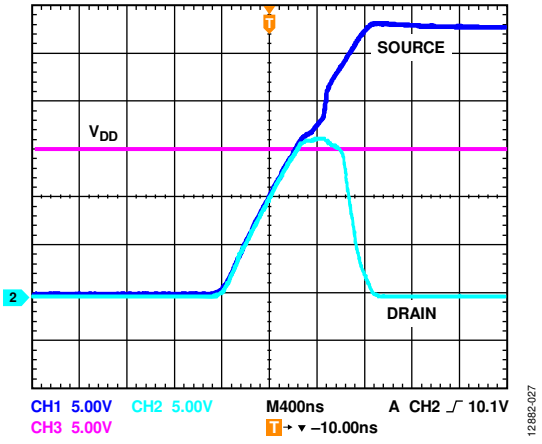


Figure 27. Drain Output Response to Positive Overvoltage (DR Pin = Floating or High)

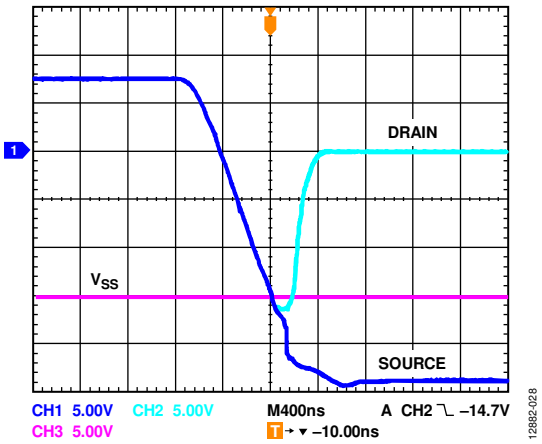


Figure 28. Drain Output Response to Negative Overvoltage (DR Pin = Floating or High)

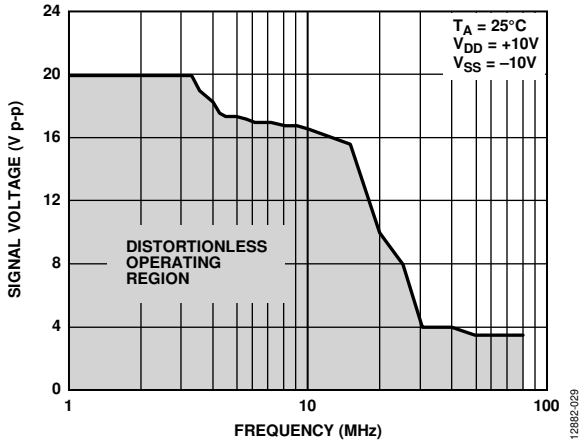


Figure 29. Large Signal Voltage Tracking vs. Frequency

TEST CIRCUITS

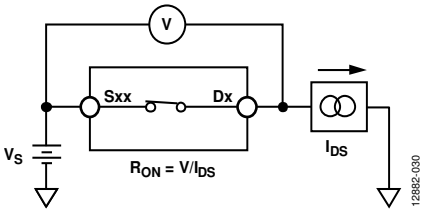


Figure 30. On Resistance

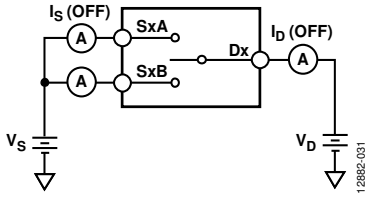


Figure 31. Off Leakage

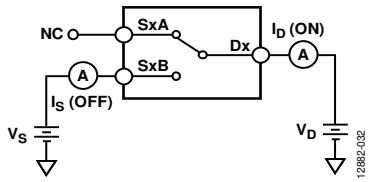


Figure 32. Channel On Leakage

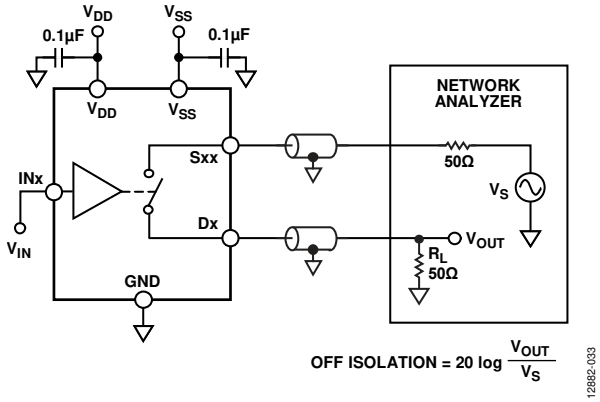


Figure 33. Off Isolation

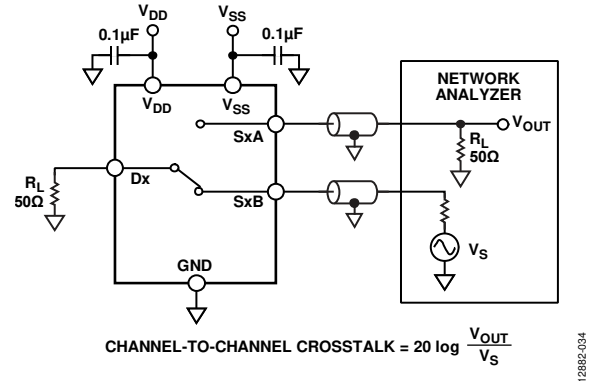


Figure 34. Channel-to-Channel Crosstalk

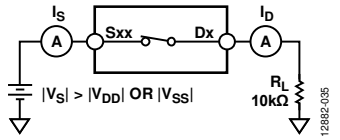


Figure 35. Switch Overvoltage Leakage

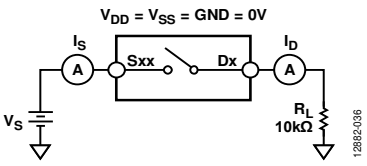


Figure 36. Switch Unpowered Leakage

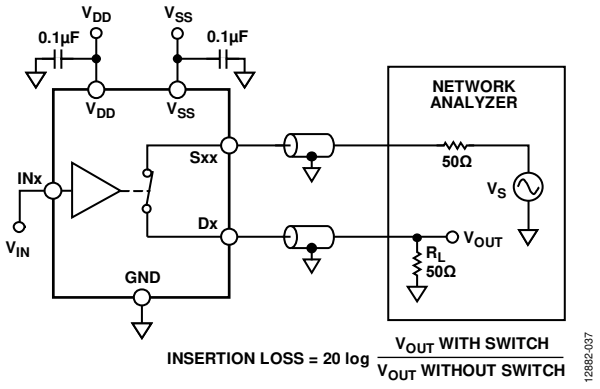


Figure 37. Bandwidth

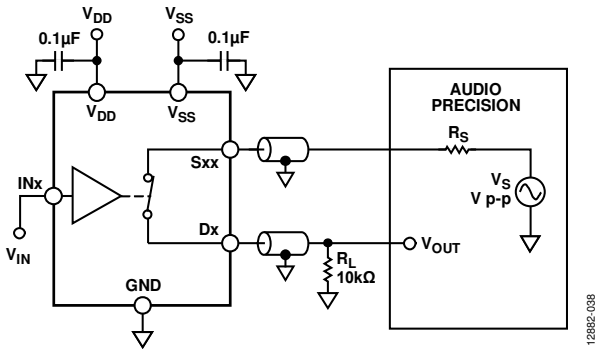


Figure 38. THD + N

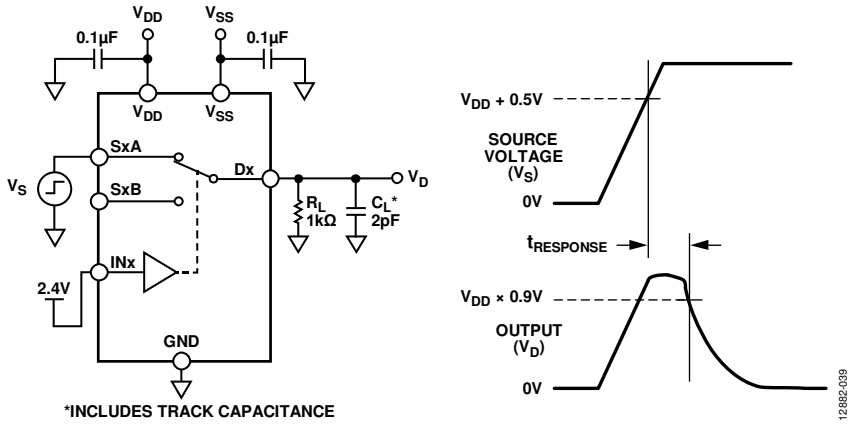


Figure 39. Overvoltage Response Time, $t_{RESPONSE}$

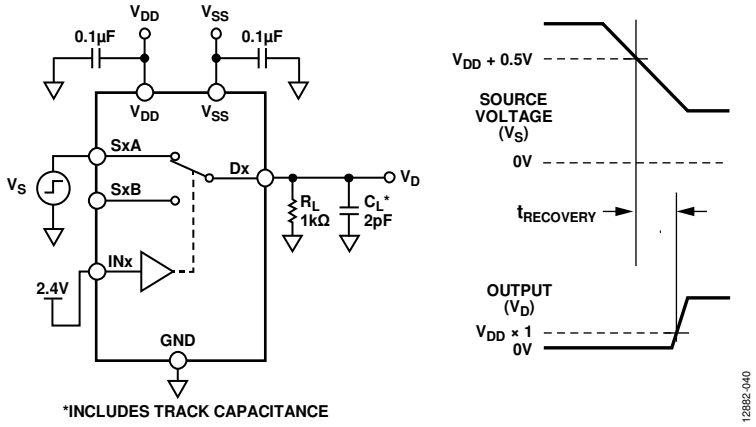


Figure 40. Overvoltage Recovery Time, $t_{RECOVERY}$

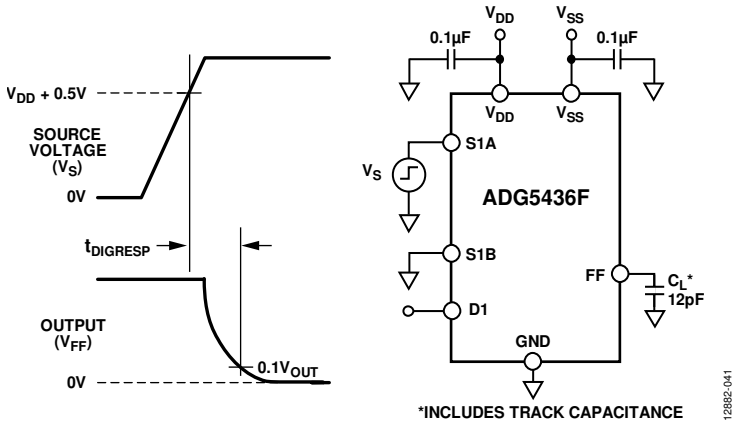


Figure 41. Interrupt Flag Response Time, $t_{DIGRESP}$

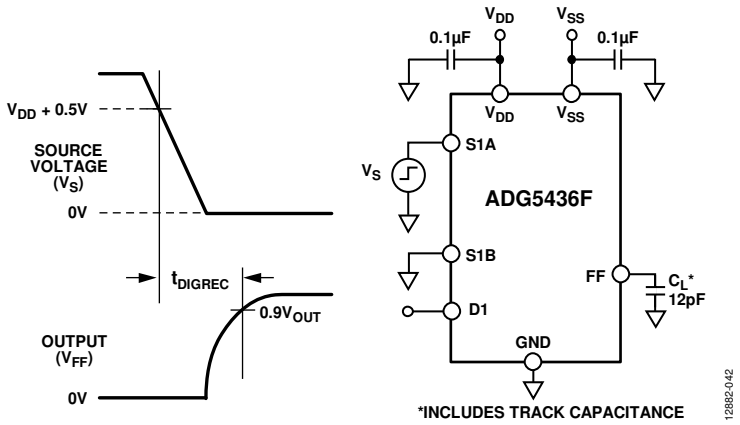


Figure 42. Interrupt Flag Recovery Time, t_{DIGREC}

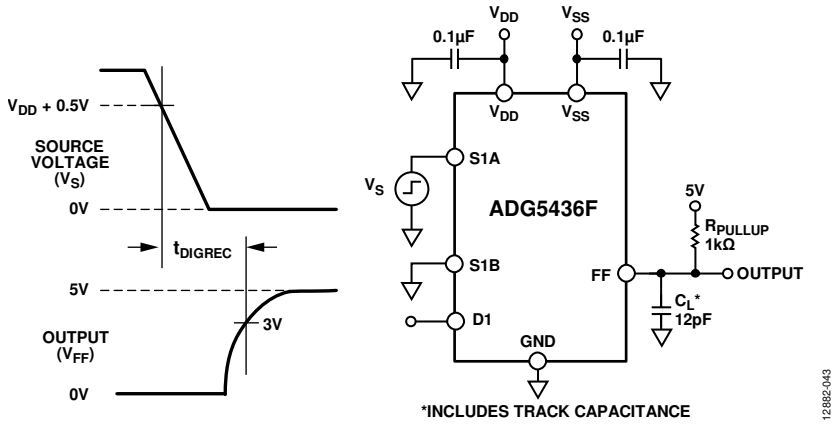


Figure 43. Interrupt Flag Recovery Time, t_{DIGREC}, with a 1 kΩ Pull-Up Resistor

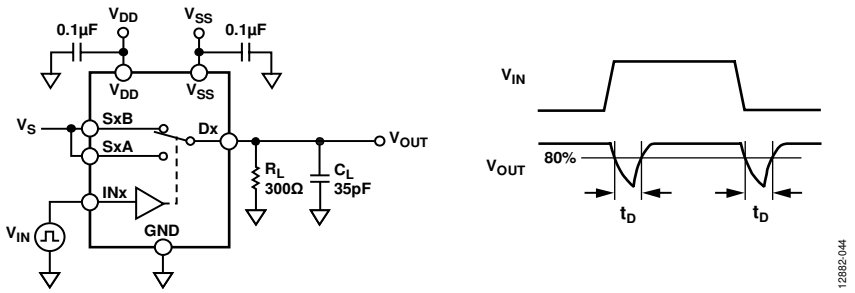


Figure 44. Break-Before-Make Time Delay, t_D

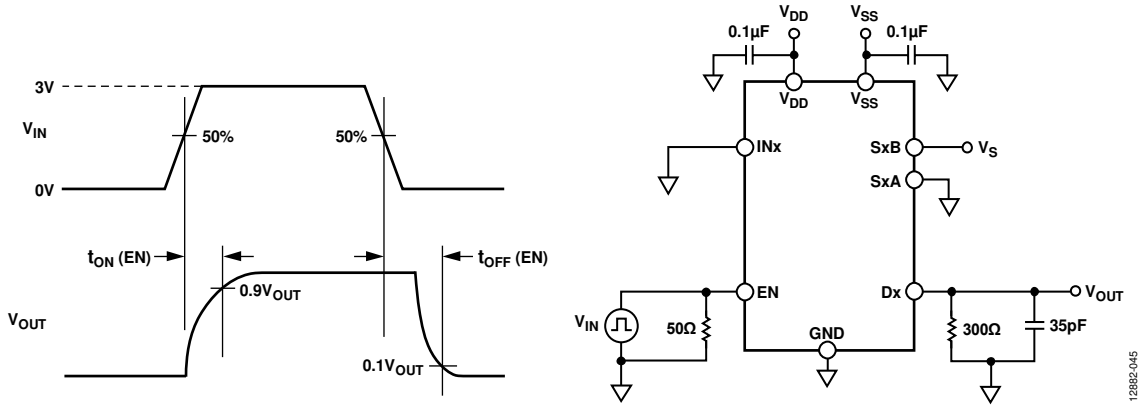


Figure 45. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

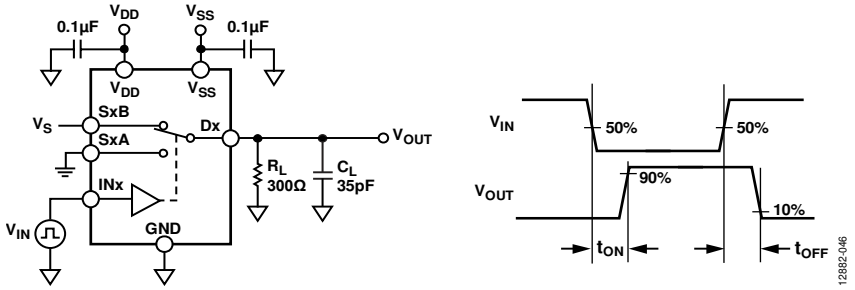


Figure 46. Address to Output Switching Times, $t_{TRANSITION}$

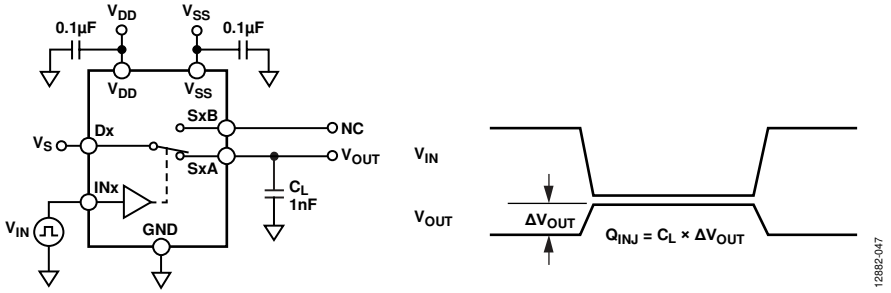


Figure 47. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on the Dx pins and the Sxx pins, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between the Dx pins and the Sxx pins.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
$R_{FLAT(ON)}$ is the flatness defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} represents the delay between applying the digital control input and the output switching on (see Figure 45).

t_{OFF}
t_{OFF} represents the delay between applying the digital control input and the output switching off (see Figure 45).

t_D
t_D represents the off time measured between the 90% point of both switches when switching from one address state to another.

$t_{DIGRESP}$
$t_{DIGRESP}$ is the time required for the FF pin to go low (0.3 V), measured with respect to the voltage on the source pin exceeding the supply voltage by 0.5 V.

t_{DIGREC}
t_{DIGREC} is the time required for the FF pin to return high, measured with respect to the voltage on the Sxx pin falling below the supply voltage plus 0.5 V.

$t_{RESPONSE}$
$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 90% of the supply voltage.

$t_{RECOVERY}$
$t_{RECOVERY}$ represents the delay between an overvoltage on the Sxx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 10% of the supply voltage.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Channel-to-Channel Crosstalk
Channel-to-channel crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
−3 dB bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion Plus Noise (THD + N)
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of the signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

V_T
V_T is the voltage threshold at which the overvoltage protection circuitry engages (see Figure 26).

THEORY OF OPERATION

SWITCH ARCHITECTURE

Each channel of the ADG5436F consists of a parallel pair of NDMOS and PDMOS transistors. This construction provides excellent performance across the signal range. The ADG5436F channels operate as standard switches when input signals with a voltage between V_{SS} and V_{DD} are applied. For example, the on resistance is 10 Ω typically and the appropriate control pin, INx, controls the opening or closing of the switch.

Additional internal circuitry enables the switch to detect overvoltage inputs by comparing the voltage on the source pin with V_{DD} and V_{SS}. A signal is considered overvoltage if it exceeds the supply voltages by the voltage threshold, V_T. The threshold voltage is typically 0.7 V, but can range from 0.8 V at −40°C down to 0.6 V at +125°C. See Figure 26 to see the change in V_T with operating temperature.

The maximum voltage that can be applied to any source input is −55 V or +55 V. When the device is powered using a single supply of greater than 25 V, the maximum undervoltage signal level reduces down from −55 V. For example, the undervoltage signal reduces to −40 V at V_{DD} = 40 V to remain within the 80 V maximum rating. The construction of the process allows the channel to withstand 80 V across the switch when it is opened. These overvoltage limits apply whether the power supplies are present or not.

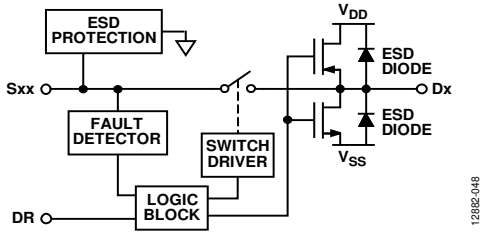


Figure 48. Switch Channel and Control Function

When an overvoltage condition is detected on a source pin (Sxx), the switch automatically opens and the source pin (Sxx) becomes high impedance and ensures that no current flows through the switch. If the DR pin is driven low, the drain pin, Dx, is pulled to the supply that was exceeded. For example, if the source voltage exceeds V_{DD}, the drain output pulls to V_{DD}. The same is true for V_{SS}. If the DR pin is allowed to float or is driven high, the Dx pin also becomes open circuit. The voltage on the Dx pin follows the voltage on the source pin, Sxx, until the switch turns off completely and the drain voltage discharges through the load. The maximum voltage on the drain is limited by the internal ESD diodes and the rate at which the output voltage discharges is dependent on the load at the pin.

During overvoltage conditions, the leakage current into and out of the source pins (Sxx) is limited to tens of microamperes. If the DR pin is allowed to float or is driven high, only nanoamperes of leakage are seen on the drain pin (Dx). If the DR pin is driven low, the drain pin (Dx) is pulled to the rail. The device that pulls the drain pin to the rail has an impedance of approximately 40 kΩ; therefore, the Dx pin current is limited to about 1 mA during a shorted load condition. This internal impedance also determines the minimum external load resistance required to ensure that the drain pin is pulled to the desired voltage level during a fault.

When an overvoltage event occurs, the channels undisturbed by the overvoltage input continue to operate normally without additional crosstalk.

ESD Performance

The ADG5436F has an ESD (HBM) rating of 6 kV.

The drain pins (Dx) have ESD protection diodes to the supply rails, and the voltage at these pins must not exceed the supply voltage.

The source pins (Sxx) have specialized ESD protection that allows the signal voltage to reach ±55 V with a ±22 V dual supply, and from −40 V to +55 V with a +40 V single supply. See Figure 48 for the switch channel overview. Exceeding ±55 V on any source input may damage the ESD protection circuitry on the device.

Trench Isolation

In the ADG5436F, an insulating oxide layer (trench) is placed between the NDMOS and the PDMOS transistors of each switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a switch that is latch-up immune under all circumstances. This device passes a JESD78D latch-up test of ±500 mA for 1 sec, the strictest test in the specification.

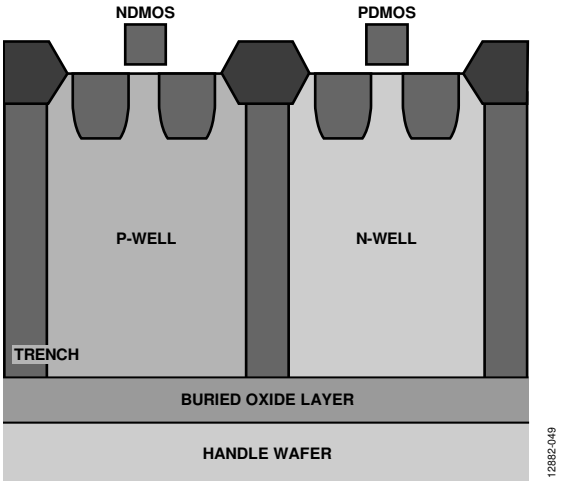


Figure 49. Trench Isolation

FAULT PROTECTION

When the voltages at the source inputs exceed V_{DD} or V_{SS} by V_T, the switch turns off, or, if the device is unpowered, the switch remains off. The switch input remains high impedance regardless of the digital input state or the load resistance, and the output acts as a virtual open circuit. Signal levels up to +55 V and −55 V are blocked in both the powered and unpowered conditions as long as the 80 V limitation between the source and supply pins is met.

Power-On Protection

The following three conditions must be satisfied for the switch to be in the on condition:

- V_{DD} to $V_{SS} \geq 8$ V.
- The input signal is between $V_{SS} - V_T$ and $V_{DD} + V_T$.
- The digital logic control input, INx, is turned on.

When the switch is turned on, the signal levels up to the supply rails are passed.

The switch responds to an analog input that exceeds V_{DD} or V_{SS} by a threshold voltage, V_T, by turning off. The absolute input voltage limits are −55 V and +55 V, while maintaining an 80 V limit between the source pin and the supply rails. The switch remains off until the voltage at the source pin returns to between V_{DD} and V_{SS}.

The fault response time ($t_{RESPONSE}$) when powered by a ±15 V dual supply is typically 510 ns, and the fault recovery time ($t_{RECOVERY}$) is 820 ns. These vary with supply voltages and output load conditions.

Exceeding ±55 V on any source input may damage the ESD protection circuitry on the device.

The maximum stress across the switch channel is 80 V. Therefore, the user must pay close attention to this limit when using the device with a 40 V single supply. In this case, the maximum undervoltage condition is −40 V to maintain the 80 V across the switch channel.

For undervoltage and overvoltage conditions, consider the case where the device is set up as shown in Figure 50.

- V_{DD}/V_{SS} = ±22 V.
- S1A and S2A = 22 V, and are both on. Therefore, D1 and D2 = 22 V.
- S1B has a −55 V fault and S2B has a +55 V fault.
- The voltage between S1B and D1 = 22 V − (−55 V) = +77 V.
- The voltage between S2B and D2= 22 V− 55 V = -33 V.

These calculations are all within device specifications: a 55 V maximum fault on source inputs and a maximum of 80 V across the off switch channel.

FF is low due to the fault conditions. The specific switches in fault can be deduced by cycling through F2 and F1 and noting the state of SF. In this example, SF is low (asserted) when F2 = 0 and F1 = 1; it is also low when F2 = 1 and F1 = 0. This signifies a fault on S1B and S2B. See Table 9 for details on how to decode SF by F2 and F1.

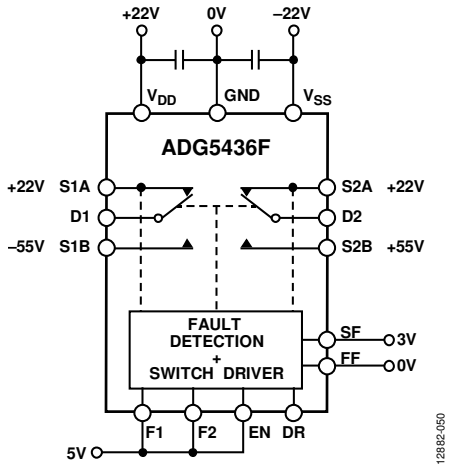


Figure 50. ADG5436F Under Example Overvoltage Conditions

Power-Off Protection

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switch or downstream circuitry. The switch output is a virtual open circuit.

The switch remains off regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to ±55 V are blocked in the unpowered condition.

Digital Input Protection

The ADG5436F can tolerate unpowered digital input signals present on the device. When the device is unpowered, the switch is guaranteed to be in the off state, regardless of the state of the digital logic signals.

The digital inputs are protected against positive faults up to 44 V. The digital inputs do not offer protection against negative overvoltages. ESD protection diodes connected to GND are present on the digital inputs.

Overvoltage Interrupt Flag

The voltages on the source inputs of the ADG5436F are continuously monitored, and the state of the switches is indicated by an active low digital output pin, FF.

The voltage on the FF pin indicates if any of the source input pins are experiencing a fault condition. The output of the FF pin is a nominal 3 V when all source pins are within normal operating range. If any source pin voltage exceeds the supply voltage by V_T, the FF output reduces to below 0.8 V.

Use the specific fault digital output pin, SF, to decode which inputs are experiencing a fault condition. The SF pin reduces to below 0.8 V when a fault condition is detected on a specific pin, depending on the state of F1 and F2 (see Table 9). The specific fault feature also works with the switches disabled (EN pin low), which allows the user to cycle through and check the fault conditions without connecting the fault to the drain output.

APPLICATIONS INFORMATION

The overvoltage protected family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments where overvoltage signals can be present and the system must remain operational both during and after the overvoltage has occurred.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 µF decoupling capacitors are required.

The ADG5436F can operate with bipolar supplies between ±5 V and ±22 V. The supplies on V_{DD} and V_{SS} do not need to be symmetrical, but the V_{DD} to V_{SS} range must not exceed 44 V. The ADG5436F can also operate with single supplies between 8 V and 44 V, with V_{SS} connected to GND.

The ADG5436F is fully specified at the ±15 V, ±20 V, 12 V, and +36 V supply ranges.

POWER SUPPLY SEQUENCING PROTECTION

The switch channel remains open when the device is unpowered and signals from −55 V to +55 V can be applied without damaging the device. The switch channel closes only when the supplies are connected, a suitable digital control signal is placed on the INx pins, and the signal is within the normal operating range. Placing the ADG5436F between external connectors and sensitive components offers protection in systems where a signal is presented to the source pins before the supply voltages are available.

SIGNAL RANGE

The ADG5436F has overvoltage detection circuitry on the inputs that compares the voltage levels at the source terminals with V_{DD} and V_{SS}. To protect downstream circuitry from overvoltage conditions, supply the ADG5436F with voltages that match the intended signal range. The low on-resistance switch allows signals to the supply rails to be passed with very little distortion. A signal that exceeds the supply rail by the threshold voltage is then blocked. This signal block offers protection to both the device and any downstream circuitry.

LOW IMPEDANCE CHANNEL PROTECTION

The ADG5436F can be used as a protective element in signal chains that are sensitive to both channel impedance and overvoltage signals. Traditionally, series resistors limit the current during an overvoltage condition to protect susceptible components.

These series resistors affect the performance of the signal chain and reduce the signal chain precision. A compromise must be reached on the value of the series resistance that is high enough to sufficiently protect sensitive components, but low enough that the precision performance of the signal chain is not sacrificed.

The ADG5436F enables the designer to remove these resistors and retain precision performance without compromising the protection of the circuit.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 51. The ADP7118 and ADP7182 can be used to generate clean positive and negative rails from the dual switching regulator output. These rails can be used to power the ADG5436F, amplifier, and/or precision converter in a typical signal chain.

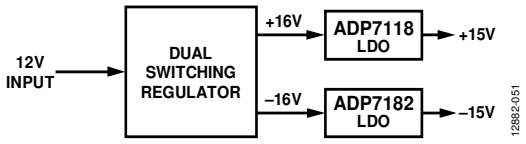


Figure 51. Bipolar Power Solution

Table 10. Recommended Power Management Devices

Product	Description
ADP7118	20 V, 200 mA, low noise, CMOS LDO
ADP7142	40 V, 200 mA, low noise, CMOS LDO
ADP7182	−28 V, −200 mA, low noise, linear regulator

HIGH VOLTAGE SURGE SUPPRESSION

The ADG5436F is not intended for use in very high voltage applications. The maximum operating voltage of the transistor is 80 V. In applications where the inputs are likely to be subject to overvoltage conditions exceeding the breakdown voltage, use transient voltage suppressors (TVSs) or similar devices.

INTELLIGENT FAULT DETECTION

The ADG5436F digital output pin, FF, can interface with a microprocessor or control system and can be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which it connects.

The control system can use the digital interrupt, FF, to start a variety of actions, as follows:

- Initiating an investigation into the source of an overvoltage fault.
- Shutting down critical systems in response to the overvoltage condition.
- Using data recorders to mark data during these events as unreliable or out of specification.

For systems sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the ADG5436F is powered on and that all input voltages are within the normal operating range before initiating operation.

The FF pin is a weak pull-up, which allows the signals to combine into a single interrupt for larger modules that contain multiple devices.

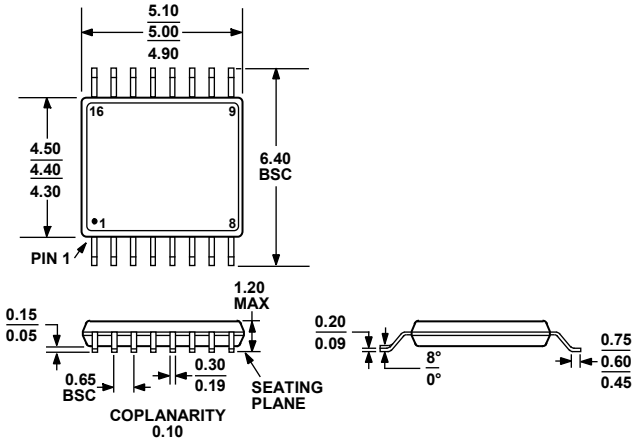
The recovery time, t_{DIGREC}, can be decreased from a typical 60 µs to 600 ns by using a 1 kΩ pull-up resistor.

The specific fault digital output, SF decodes which inputs are experiencing a fault condition. The SF pin reduces to below 0.8 V when a fault condition is detected on a specific pin, depending on the state of F1 and F2 (see Table 9). The specific fault feature also works with the switches disabled (EN pin low), which allows the user to cycle through and check the fault conditions without connecting the fault to the drain output.

LARGE VOLTAGE, HIGH FREQUENCY SIGNALS

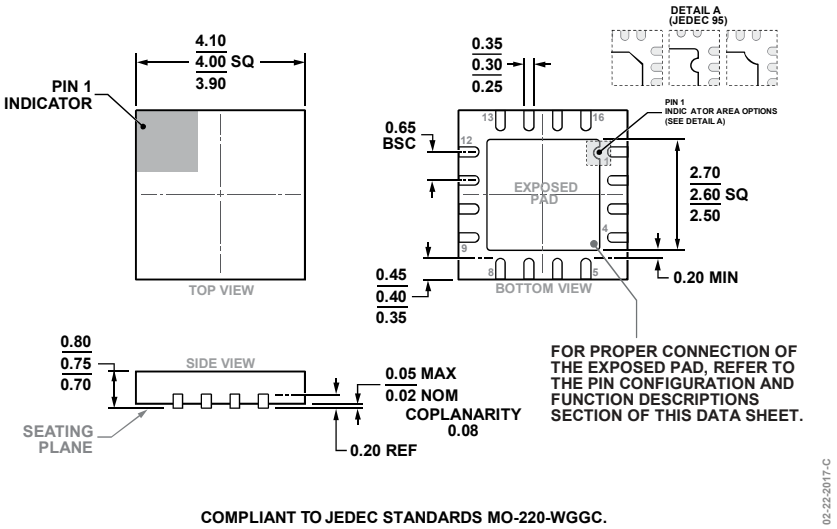
Figure 29 shows the voltage range and frequencies that the ADG5436F can reliably convey. For signals extending across the full signal range from V_{SS} to V_{DD}, keep the frequency below 3 MHz. If the required frequency is greater than 3 MHz, decrease the signal range appropriately to ensure signal integrity.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 52. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 53. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5436FBRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5436FBRUZ-RL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5436FBCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17

[1] Z = RoHS Compliant Part.

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