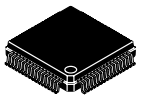


MC33772C

Battery cell controller IC

Rev. 3 — 4 June 2021 Product brief

1 General description

The MC33772C is a SMARTMOS lithium-ion battery cell controller IC designed for automotive applications, such as hybrid electric (HEV) and electric vehicles (EV) along with industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems.

The device performs ADC conversions of the differential cell voltages and current, as well as battery coulomb counting and battery temperature measurements. The information is transmitted to MCU using one of the microcontroller interfaces: serial peripheral interface (SPI) or isolated daisy chain communication interface [also referred as transformer physical layer (TPL)] which supports both capacitive and inductive isolation between nodes of the IC. The product is AEC-Q100 qualified and operates up to 125 °C ambient temperature.

2 Features

- 5.0 V ≤ V_{PWR} ≤ 30 V operation, 40 V transient
- 3 to 6 cells management
- Isolated 2.0 Mbit/s differential communication or 4.0 Mbit/s SPI
- Addressable on initialization
- Bi-directional transceiver to support up to 63 nodes in daisy chain
- 0.8 mV total voltage measurement error
- Synchronized cell voltage/current measurement with coulomb count
- Averaging of cell voltage measurements
- Total stack voltage measurement
- Seven GPIO/temperature sensor inputs
- 5.0 V at 5.0 mA reference supply output
- Automatic over/undervoltage and temperature detection routable to fault pin
- Integrated sleep mode over/undervoltage and temperature monitoring
- Onboard 300 mA passive cell balancing with diagnostics
- Hot plug capable
- Detection of internal and external faults, as open lines, shorts, and leakage
- Designed to support ISO 26262, up to ASIL D safety system
- Fully compatible with the MC33771C and the MC33664
- Qualified in compliance with AEC-Q100

3 Simplified application diagram

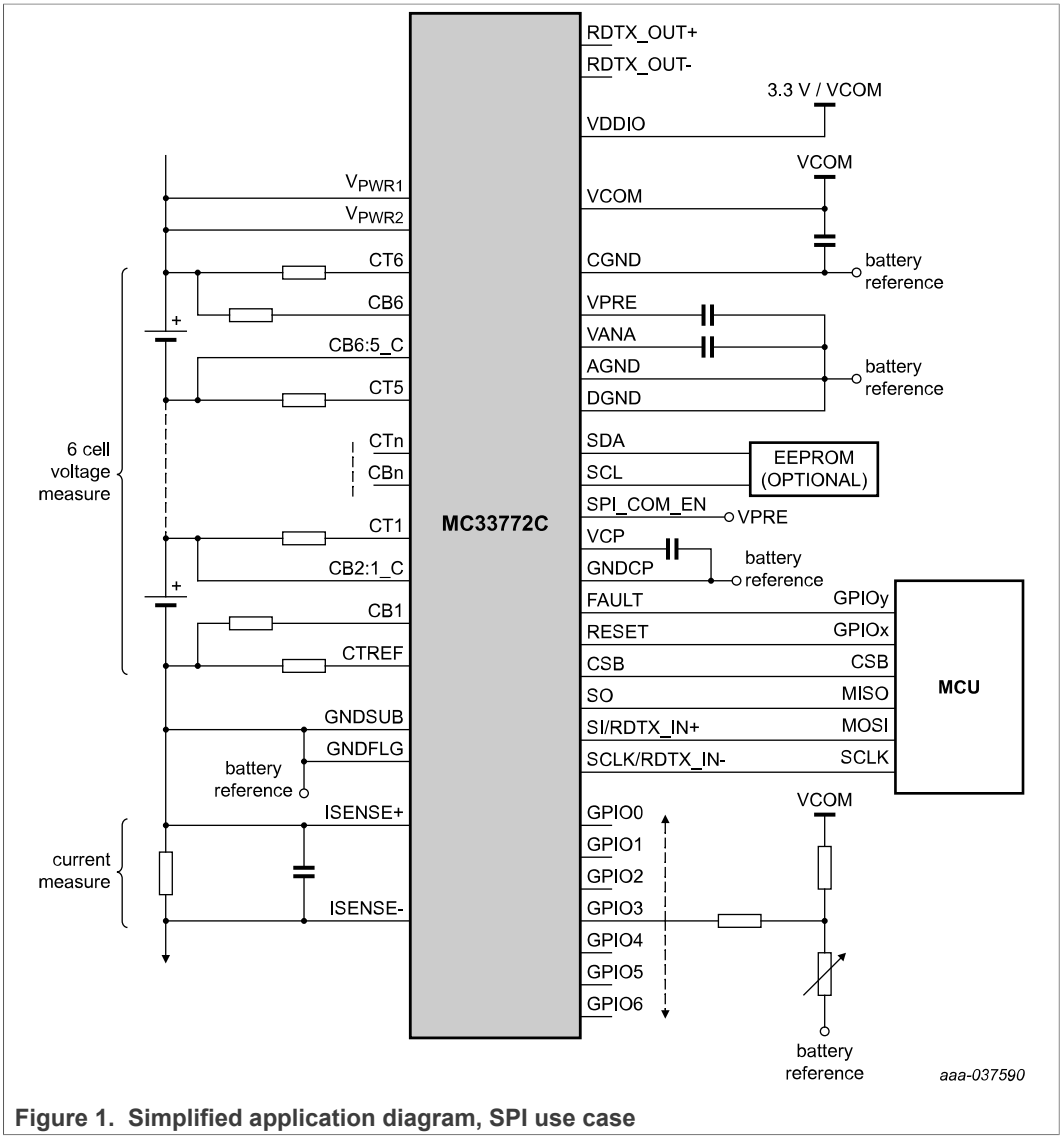


Figure 1. Simplified application diagram, SPI use case

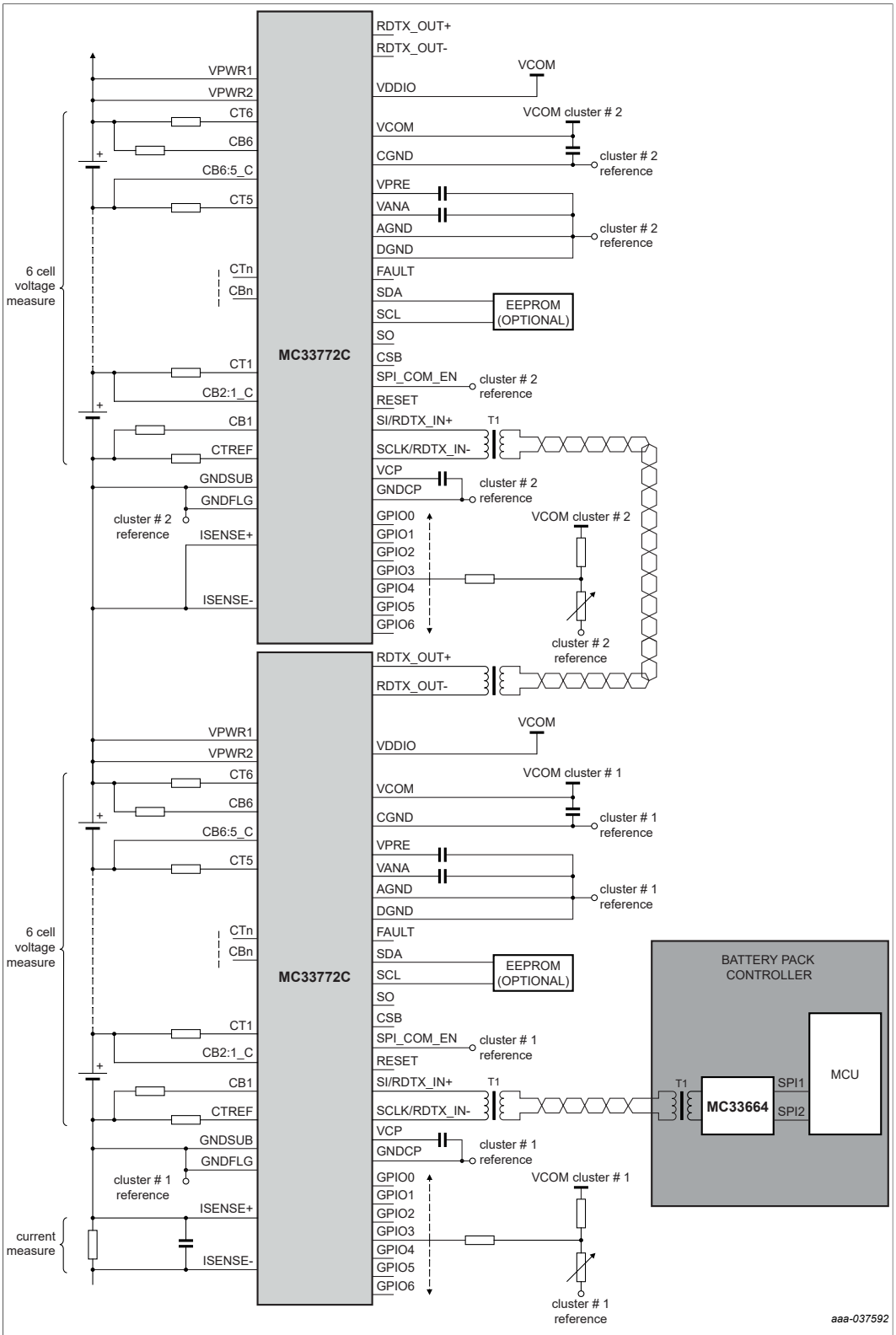


Figure 2. Simplified application diagram, TPL use case

4 Applications

- Automotive: 12 V and high-voltage battery packs
- E-bikes, e-scooters, drones
- Energy storage systems
- Uninterruptible power supply (UPS)
- Battery junction box

5 Ordering information

5.1 Part numbers definition

MC33772C x y z AE/R2

Table 1. Part number breakdown

Code	Option	Description
x	T	x = T (TPL communication type)
y	A	y = A (Advanced)
	C	y = C (Current)
	P	y = P (Premium)
z	0	z = 0 (0 channels)
	1	z = 1 (3 to 6 channels)
	2	z = 2 (3 to 4 channels)
	AE	Package suffix
	R2	Tape and reel indicator

5.2 Part numbers list

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com.

Table 2. Advanced orderable part table

Package type is 48-pin LQFP-EP

Orderable part	Number of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
TPL differential communication protocol				
MC33772CTA1AE	3 to 6	Yes	Yes	No
MC33772CTA2AE	3 to 4	Yes	Yes	No

Table 3. Premium orderable part table

Package type is 48-pin LQFP-EP

Orderable part	Number of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
TPL differential communication protocol with current measurement option				
MC33772CTP1AE	3 to 6	Yes	Yes	Yes
MC33772CTP2AE	3 to 4	Yes	Yes	Yes

Table 4. Current orderable part table

Package type is 48-pin LQFP-EP

Orderable part	Number of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
TPL differential communication protocol				
MC33772CTC0AE	0	No	Yes	Yes
MC33772CTC1AE	1	No	Yes	Yes

Note: *To order parts in tape and reel, add an R2 suffix to the part number.*

6 Pinning information

6.1 Pinout diagram

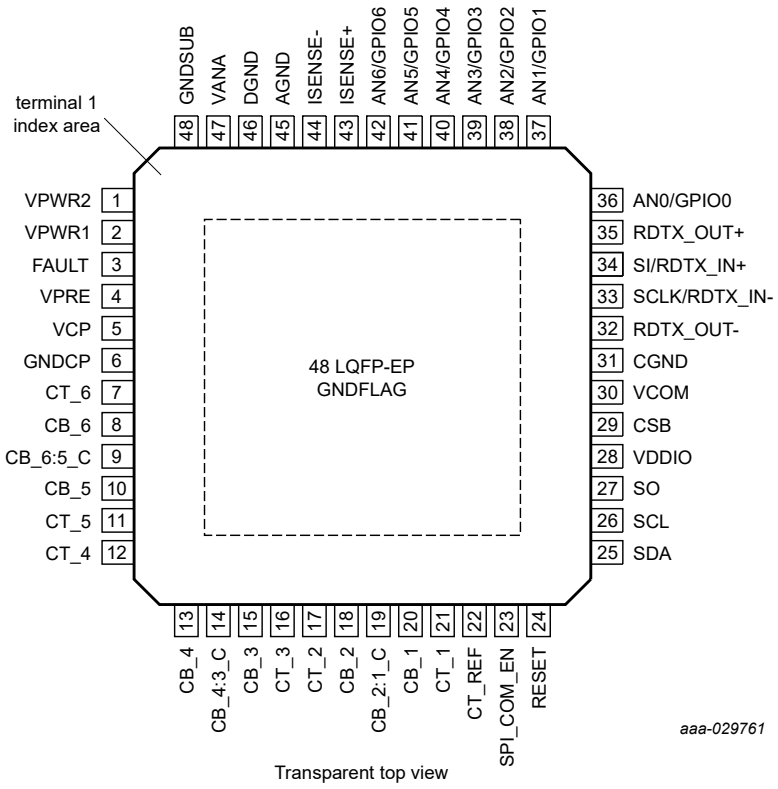


Figure 3. Pinout diagram

6.2 Pin definitions

Table 5. Pin definitions

Pin number	Pin name	Pin function	Definition
1	VPWR2	Input	Power supply input to the MC33772C
2	VPWR1	Input	Power supply input to the MC33772C
3	FAULT	Output	Fault output dependent on user defined internal or external faults. If not used, it must be left open
4	VPRE	Output	Pre-regulator voltage. Connect to a 470 nF capacitor
5	VCP	Output	Charge pump. Decouple with a 10 nF capacitor
6	GNDCP	Ground	Charge pump capacitor ground
7	CT_6	Input	Cell terminal pin 6 input. Terminate to LPF resistor
8	CB_6	Output	Cell balance driver. Terminate to cell 6 cell balance load resistor
9	CB_6:5_C	Output	Cell balance 6:5 common. Terminate to cell 6 and 5 common pin
10	CB_5	Output	Cell balance driver. Terminate to cell 5 cell balance load resistor
11	CT_5	Input	Cell terminal pin 5 input. Terminate to LPF resistor
12	CT_4	Input	Cell terminal pin 4 input. Terminate to LPF resistor
13	CB_4	Output	Cell balance driver. Terminate to cell 4 cell balance load resistor

Table 5. Pin definitions*...continued*

Pin number	Pin name	Pin function	Definition
14	CB_4:3_C	Output	Cell balance 4:3 common. Terminate to cell 4 and 3 common pin
15	CB_3	Output	Cell balance driver. Terminate to cell 3 cell balance load resistor
16	CT_3	Input	Cell terminal pin 3 input. Terminate to LPF resistor
17	CT_2	Input	Cell pin 2 input. Terminate to LPF resistor
18	CB_2	Output	Cell balance driver. Terminate to cell 2 cell balance load resistor
19	CB_2:1_C	Output	Cell balance 2:1 common. Terminate to cell 2 and 1 common pin
20	CB_1	Output	Cell balance driver. Terminate to cell 1 cell balance load resistor
21	CT_1	Input	Cell pin 1 input. Terminate to LPF resistor
22	CT_REF	Input	Cell terminal REF input. Terminate to LPF resistor
23	SPI_COM_EN	Input	SPI communication enable input. Wire to VPRE to use SPI communication, else wire to ground to use TPL communication
24	RESET	Input	RESET is an active high input. RESET has an internal pull down. If not used, it can be shorted to GND
25	SDA	I/O	I^2C data
26	SCL	I/O	I^2C clock
27	SO	Output	SPI serial output
28	VDDIO	Input	IO voltage for I^2C and SPI interfaces. Voltage level corresponding to logic 1 will be the same as VDDIO
29	CSB	Input	SPI active low chip select. If not used, it must be shorted to ground
30	VCOM	Output	Communication regulator output. Decouple with 2.2 µF to CGND
31	CGND	Ground	Communication decoupling ground, terminate to GNDSUB
32	RDTX_OUT−	I/O	TPL receive/transmit output negative
33	SCLK/RDTX_IN-	I/O	SPI clock or TPL receive/transmit input negative
34	SI/RDTX_IN+	I/O	SPI serial input or TPL receive/transmit input positive
35	RDTX_OUT+	I/O	TPL receive/transmit output positive
36	AN0 GPIO0	I/O	General purpose input/output
37	AN1 GPIO1	I/O	General purpose input/output
38	AN2 GPIO2	I/O	General purpose input/output
39	AN3 GPIO3	I/O	General purpose input/output
40	AN4 GPIO4	I/O	General purpose input/output
41	AN5 GPIO5	I/O	General purpose input/output
42	AN6 GPIO6	I/O	General purpose input/output
43	ISENSE+	Input	Current measurement input +
44	ISENSE−	Input	Current measurement input −
45	AGND	I/O	Analog ground, terminate to GNDSUB
46	DGND	I/O	Digital ground, terminate to GNDSUB
47	VANA	Output	Precision ADC analog supply. Decouple with 47 nF capacitor to AGND
48	GNDSUB	Ground	Ground reference for device, terminate to reference of battery cluster
49	GNDFLAG	Ground	Exposed pad, terminate to lowest potential of the battery cluster and to heat dissipation area of PCB

7 General product characteristics

7.1 Ratings and operating requirements relationship

The operating voltage range pertains to the VPWR pins referenced to the AGND pins.

Table 6. Ratings vs. operating requirements

Fatal range Permanent failure may occur	Lower limited operating range No permanent failure, but IC functionality is not guaranteed	Normal operating range 100 % functional	Upper limited operating range	Fatal range Permanent failure may occur
V_{PWR} < −0.3 V	5.0 V ≤ V_{PWR} ≤ 6.0 V (SPI) 6.4 V ≤ V_{PWR} ≤ 7.0 V (TPL) **Reset range:** –0.3 V ≤ V_{PWR} ≤ 5.0 V (SPI) –0.3 V ≤ V_{PWR} ≤ 6.4 V (TPL) **POR with V_{PWR} falling:** 4.8 V ≤ V_{PWR} < 5.0 V (SPI) 6.1 V ≤ V_{PWR} < 6.4 V (TPL) **POR with V_{PWR} rising:** 5.6 V ≤ V_{PWR} < 6.0 V (SPI) 6.6 V ≤ V_{PWR} < 7.0 V (TPL)	6.0 V ≤ V_{PWR} ≤ 30 V (SPI) 7.0 V ≤ V_{PWR} ≤ 30 V (TPL)	30 V < V_{PWR} ≤ 40 V **IC parameters might be out of specification. Detection of V_{PWR} overvoltage is functional**	40 V < V_{PWR}
	Handling range - No permanent failure			

In both upper and lower limited operating range, no information can be provided about IC performance. Only the detection of V_{PWR} overvoltage is guaranteed in the upper limited operating range.

Performance in normal operating range is guaranteed only if there is a minimum of three battery cells in the stack.

7.2 Maximum ratings

Table 7. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings might cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
Electrical ratings				
VPWR1, VPWR2	Supply input voltage	–0.3	40	V
CT6	Cell terminal voltage	−0.3	40	V
VPWR to CT6	Voltage across VPWR1,2 pins pair and CT6 pin	−10	10	V
CT_N to CT_{N-1}	Cell terminal differential voltage [1]	−0.3	6.7	V
$CT_{N(CURRENT)}$	Cell terminal input current	—	±500	µA
CB_N to $CB_{N:N-1\_C}$ $CB_{N:N-1\_C}$ to CB_{N-1}	Cell balance differential voltage	—	10	V
CB_{N-1} to CT_{N-1}	Cell balance input to cell terminal input	−10	+10	V
VISENSE	ISENSE+ and ISENSE– pin voltage	−0.5	2.5	V
VCOM	Maximum voltage may be applied to VCOM pin from external source	—	5.8	V

Table 7. Maximum ratings...*continued*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings might cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
VANA	Maximum voltage may be applied to VANA pin	—	3.1	V
VPRE	Maximum voltage which may be applied to VPRE pin from external source	—	7.0	V
VCP	Maximum voltage which may be applied to VCP pin from external source	—	14	V
VDDIO	Maximum voltage which may be applied to VDDIO pin from external source	—	5.8	V
V_{GPIO0}	GPIO0 pin voltage	–0.3	6.5	V
V_{GPIOx}	GPIOx pins (x = 1 to 6) voltage	–0.3	VCOM + 0.5	V
V_{DIG}	Voltage I^2C pins (SDA, SCL)	–0.3	VDDIO + 0.5	V
V_{RESET}	RESET pin	–0.3	6.5	V
V_{CSB}	CSB pin	–0.3	6.5	V
$V_{SPI\_COMM\_EN}$	SPI_COMM_EN	–0.3	7.0	V
V_{SO}	SO pin	–0.3	VDDIO + 0.5	V
$V_{GPIO5,6}$	Maximum voltage for GPIO5 and GPIO6 pins used as current input	−0.3	2.5	V
FAULT	Maximum applied voltage to pin	−0.3	7.0	V
$I_{pin\_unpowered}$	Input current in a pin when the device is unpowered	−2	2	mA
V_{COMM}	Maximum voltage to pins RDTX_OUT+, RDTX_OUT–, SI/RDTX_IN+, CLK/RDTX_IN–	−10	10	V
V_{ESD1}	ESD voltage			V
	Human body model (HBM)	—	±2000	
	Charge device model (CDM)	—	±500	
	Charge device model corner pins (CDM)	—	±750	
V_{ESD2}	ESD voltage (VPWR1, VPWR2, CTx, CBx, GPIOx, ISENSE+, ISENSE–, RDTX_OUT+, RDTX_OUT–, SI/RDTX_IN+, SCLK/ RDTX_IN–) [2]			V
	Human body model (HBM)	—	±4000	
V_{ESD3}	ESD voltage (CTREF, CTx, CBx, GPIOx, ISENSE+, ISENSE−, RDTX_OUT+, RDTX_OUT−, SI/RDTX_IN+, SCLK/ RDTX_IN−) [3]			V
	IEC 61000-4-2, Unpowered (Gun configuration: 330 Ω / 150 pF)	—	±8000	
	HMM, Unpowered (Gun configuration: 330 Ω / 150 pF)	—	±8000	
	ISO 10605:2009, Unpowered (Gun configuration: 2 kΩ / 150 pF)	—	±8000	
	ISO 10605:2009, Powered (Gun configuration: 2 kΩ / 330 pF)	—	±8000	

[1] Adjacent CT pins may experience an overvoltage that exceeds their maximum rating during OV/UV functional verification test or during open line diagnostic test. Nevertheless, the IC is completely tolerant to this special situation.

[2] ESD testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).

[3] These voltage values can be sustained only if ESD caps are used as described in MC33772C External Components.

7.3 Thermal characteristics

Table 8. Thermal ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings might cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
Thermal ratings				
	Operating temperature			°C
T_A	Ambient (SPI application)	–40	+125	
T_A	Ambient (TPL application)	–40	+105	
T_J	Junction[1]	–40	+150	
T_{STG}	Storage temperature	−55	+150	°C
T_{PPRT}	Peak package reflow temperature [2] [3]	—	260	°C
Thermal resistance and package dissipation ratings				
$R_{\Theta JB}$	Junction-to-board (bottom exposed pad soldered to board) 48 LQFP EP [4]	—	11	°C/W
$R_{\Theta JA}$	Junction-to-ambient, natural convection, single-layer board (1s) 48 LQFP EP [5] [6]	—	72	°C/W
$R_{\Theta JA}$	Junction-to-ambient, natural convection, four-layer board (2s2p) 48 LQFP EP [5] [6]	—	30	°C/W
$R_{\Theta JCTOP}$	Junction-to-case top (exposed pad) 48 LQFP EP [7]	—	24	°C/W
$R_{\Theta JCBOTTOM}$	Junction-to-case bottom (exposed pad) 48 LQFP EP [8]	—	0.98	°C/W
ΨJT	Junction to package top, natural convection [9]	—	4	°C/W

[1] The user must ensure that the average maximum operating junction temperature (Tj) is not exceeded.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
[3] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[6] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
[7] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1), with the cold plate temperature used for the case temperature.
[8] Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
[9] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

7.4 Electrical characteristics

Table 9. Static and dynamic electrical characteristics

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Power management					
$V_{PWR(FO)}$	Supply voltage				V
	Full parameter specification (SPI application)	6.0	—	30	
	Full parameter specification (TPL application)	7.0	—	30	
I_{VPWR}	Supply current (base value)				mA
	Normal mode, cell balance OFF, ADC inactive, SPI communication inactive, IVCOM = 0 mA	—	6.0	—	
	Normal mode, cell balance OFF, ADC inactive, TPL communication inactive, IVCOM = 0 mA	—	8.0	—	
$I_{VPWR(TPL\_TX1)}$	Supply current adder when TPL communication active with only one device in daisy chain	—	—	8.3	mA
$I_{VPWR(TPL\_TX1/TX2)}$	Supply current adder when TPL communication active with multiple devices in daisy chain	—	—	10	mA
$I_{VPWR(CBON)}$	Supply current adder to set all 6 cell balance switches ON	—	2.0	—	mA
$I_{VPWR(ADC)}$	Delta supply current to perform ADC conversions (addend)				mA
	ADC1-A,B continuously converting	—	4.7	—	
	ADC2 continuously converting	—	1.0	—	
$I_{VPWR(SS)}$	Supply current in sleep and idle modes, communication inactive, cell balance off, oscillator monitor on, cyclic measurement off				
	SPI mode (T_A = 25 °C)	—	32	—	µA
	SPI mode (−40 °C ≤ T_A ≤ 85 °C)	—	—	60	
	SPI mode (T_A = 125 °C)	—	42	—	
	TPL mode (T_A = 25 °C)	—	75	—	
	TPL mode (−40 °C ≤ T_A ≤ 85 °C)	—	—	100	
	TPL mode (T_A = 125 °C)	—	—	138	
$I_{VPWR(CKMON)}$	Clock monitor current consumption	—	5	—	µA
$V_{PWR(OV\_FLAG)}$	V_{PWR} overvoltage fault threshold (flag)	—	33.5	—	V
$V_{PWR(LV\_FLAG)}$	V_{PWR} low-voltage warning threshold (flag)	—	7.8	—	V
$V_{PWR(UV\_POR)}$	V_{PWR} undervoltage shutdown threshold (POR), falling VPWR				V
	SPI mode	—	4.9	—	
	TPL mode	—	6.25	—	
$V_{PWR(UV\_RIS)}$	V_{PWR} undervoltage shutdown threshold (POR), rising VPWR				V
	SPI mode	—	5.8	—	
	TPL mode	—	6.8	—	
$t_{VPWR(FILTER)}$	V_{PWR} OV, LV filter	—	50	—	µs

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
VPRE power supply					
VPRE	Pre-regulator voltage range - decouple with 470 nF SPI mode, ILoad = 15 mA SPI mode, ILoad = 15 mA, 5.0 V ≤ VPWR < 6.0 V TPL mode, ILoad = 70 mA	 — 4.9 —	 5.75 — 6.5	 — — —	V
$V_{PRE(UV\_TH)}$	PRE undervoltage threshold leading to a reset	—	4.25	—	V
VCP power supply					
VCP	Charge pump voltage range	2 × V_{PRE} – 2	—	2 × V_{PRE}	V
$V_{CP(UV\_TH)}$	Undervoltage threshold for VCP minus VPRE	—	1.5	—	V
VDDIO power supply					
V_{DDIO}	IO supply for I^2C and SPI interfaces - voltage range	—	4.15	—	V
VCOM power supply					
V_{COM}	VCOM output voltage	—	5.0	—	V
I_{VCOM}	VCOM output current allocated for external use	—	—	5.0	mA
$V_{COM(UV)}$	VCOM undervoltage fault threshold	—	4.4	—	V
V_{COM_HYS}	VCOM undervoltage hysteresis	—	100	—	mV
$t_{VCOM(FLT\_TIMER)}$	VCOM undervoltage fault timer	—	10	—	µs
$t_{VCOM(RETRY)}$	VCOM fault retry timer	—	10	—	ms
$V_{COM(OV)}$	VCOM overvoltage fault threshold	5.4	—	5.9	V
$I_{LIM(OC)}$	VCOM current limit in TPL mode VCOM current limit SPI mode	65 35	— —	140 140	mA
$R_{VCOM(SS)}$	VCOM sleep mode pulldown resistor	—	2.0	—	kΩ
t_{VCOM}	VCOM rise time (CL = 2.2 µF ceramic X7R only)	—	—	400	µs
VANA power supply					
V_{ANA}	VANA output voltage (not used by external circuits) Decouple with 47 nF X7R 0603 or 0402	 —	 2.65	 —	V
$V_{ANA(UV)}$	VANA undervoltage fault threshold	—	2.4	—	V
V_{ANA_HYS}	VANA undervoltage hysteresis	—	50	—	mV
$V_{ANA(FLT\_TIMER)}$	VANA undervoltage fault timer	—	11	—	µs
$V_{ANA(OV)}$	VANA overvoltage fault threshold	—	2.8	—	V
$t_{VANA(RETRY)}$	VANA fault retry timer	—	10	—	ms
$I_{LIM(OC)}$	VANA current limit	5	—	10	mA
R_{VANA_RPD}	VANA sleep mode pull-down resistor	—	1.0	—	kΩ
t_{VANA}	VANA rise time (CL = 47 nF ceramic X7R only)	—	—	100	µs
ADC1-A, ADC1-B					
$CTn_{(LEAKAGE)}$	Cell terminal input leakage current	—	10	—	nA
CT_N	Cell terminal input current during conversion	—	50	—	nA
R_{PD}	Cell terminal open load detection pulldown resistor	—	950	—	Ω
V_{VPWR_RES}	VPWR terminal measurement resolution	—	2.44148	—	mV/LSB

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
V_{VPWR_RNG}	VPWR terminal measurement range				V
	SPI application	6.0	—	36	
	TPL application	7.0	—	36	
$VPWR_{TERM\_ERR}$	VPWR terminal measurement accuracy	−0.5	—	0.5	%
V_{CT_RNG}	ADC differential input voltage range for CTn to CTn-1	0.0	—	4.85	V
$V_{CT\_ANx\_RES}$	Cell voltage and ANx resolution in 15-bit MEAS_xxxx registers	—	152.58789	—	µV/LSB
$V_{ANx\_RATIO\_RES}$	ANx resolution in 15-bit MEAS_xxxx registers in ratiometric mode	—	VCOM × 30.51758	—	
V_{ERR}	Cell voltage measurement error 0.1 V ≤ V_{CELL} ≤ 4.85 V, –40 °C ≤ T_A ≤ 105 °C (or –40 °C ≤ T_J ≤ 125 °C)	—	±0.7	—	mV
V_{ERR_1}	Cell voltage measurement error 0 V ≤ V_{CELL} ≤ 1.5 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	—	±0.4	—	mV
V_{ERR_2}	Cell voltage measurement error 1.5 V ≤ V_{CELL} ≤ 2.7 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	—	±0.4	—	mV
V_{ERR_3}	Cell voltage measurement error 2.7 V ≤ V_{CELL} ≤ 3.7 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	—	±0.5	—	mV
V_{ERR_4}	Cell voltage measurement error 3.7 V ≤ V_{CELL} ≤ 4.3 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	—	±0.7	—	mV
V_{ERR_5}	Cell voltage measurement error 1.5 V ≤ V_{CELL} ≤ 4.5 V, –40 °C ≤ T_A ≤ 105 °C (or –40 °C ≤ T_J ≤ 125 °C)	—	±0.7	—	mV
V_{ANx_ERR}	Magnitude of ANx error in the entire measurement range:				mV
	Ratiometric measurement	−16	—	16	
	Absolute measurement, input in the range [1.0, 4.5] V	−10	—	10	
	Absolute measurement, input in the range [0, 4.85] V for −40 °C < T_A < 60 °C	−8.0	—	8.0	
	Absolute measurement after soldering and aging, input in the range [0, 4.85] V for −40 °C < T_A < 105 °C	−11	—	11	
t_{VCONV}	Single channel net conversion time				µs
	13-bit resolution	—	6.77	—	
	14-bit resolution	—	9.43	—	
	15-bit resolution	—	14.75	—	
	16-bit resolution	—	25.36	—	
V_{V_NOISE}	Conversion noise				µVrms
	13-bit resolution	—	1800	—	
	14-bit resolution	—	1000	—	
	15-bit resolution	—	600	—	
	16-bit resolution	—	400	—	

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
ADC2/current sense module					
V_{INC}	ISENSE+/ISENSE− input voltage (reference to AGND)	−300	—	300	mV
V_{IND}	ISENSE+/ISENSE− differential input voltage range	−150	—	150	mV
$V_{ISENSEX(OFFSET)}$	ISENSE+/ISENSE− input voltage offset error	—	—	0.5	µV
$I_{SENSEX(BIAS)}$	ISENSE+/ISENSE− input bias current	−100	—	100	nA
$I_{SENSE(DIF)}$	ISENSE+/ISENSE− differential input bias current	−5.0	—	5.0	nA
$I_{GAINERR}$	ISENSE error including nonlinearities	−0.5	—	0.5	%
I_{ISENSE_OL}	ISENSE open load injected current	—	130	—	µA
V_{ISENSE_OL}	ISENSE open load detection threshold	—	460	—	mV
V_{2RES}	Current sense user register resolution	—	0.6	—	µV/LSB
V_{PGA_SAT}	PGA saturation half-range				mV
	Gain = 256	—	4.9	—	
	Gain = 64	—	19.5	—	
	Gain = 16	—	78.1	—	
	Gain = 4	—	150	—	
V_{PGA_ITH}	Voltage threshold for PGA gain increase				mV
	Gain = 256	—	—	—	
	Gain = 64	—	2.344	—	
	Gain = 16	—	9.375	—	
	Gain = 4	—	37.50	—	
V_{PGA_DTH}	Voltage threshold for PGA gain decrease				mV
	Gain = 256	—	4.298	—	
	Gain = 64	—	17.188	—	
	Gain = 16	—	68.750	—	
	Gain = 4	—	—	—	
t_{AZC_SETTLE}	Time to perform auto-zero procedure after enabling the current channel	—	200	—	µs
t_{ICONV}	ADC conversion time including PGA settling time				µs
	13-bit resolution	—	19.00	—	
	14-bit resolution	—	21.67	—	
	15-bit resolution	—	27.00	—	
	16-bit resolution	—	37.67	—	
V_{I_NOISE}	Noise at 16-bit conversion	—	3.01	—	µVrms
V_{I_NOISE}	Noise error at 13-bit conversion	—	8.33	—	µVrms
ADC_{CLK}	ADC2 and ADC1-A,B clocking frequency	—	6.0	—	MHz
Cell balance drivers					
$V_{DS(CLAMP)}$	Cell balance driver VDS active clamp voltage	—	11	—	V
$V_{OUT(FLT\_TH)}$	Output fault detection voltage threshold				V
	Balance off (open load) Balance on (shorted load)	—	0.55	—	
R_{PD_CB}	Output OFF open load detection pull-down resistor				kΩ
	Balance off, open load detect disabled	—	2.0	—	

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
$I_{OUT(LKG)}$	Output leakage current Balance off, open load detect disabled at V_{DS} = 4.0 V	—	—	1.0	µA
$R_{DS(on)}$	Drain-to-source on resistance I_{OUT} = 300 mA, T_J = 125 °C I_{OUT} = 300 mA, T_J = 25 °C I_{OUT} = 300 mA, T_J = −40 °C	 — — —	 — 0.5 0.4	 0.80 — —	Ω
I_{LIM_CB}	Driver current limitation (shorted resistor)	310	—	950	mA
t_{ON}	Cell balance driver turn on R_L = 15 Ω	—	350	—	µs
t_{OFF}	Cell balance driver turn off R_L = 15 Ω	—	200	—	µs
$t_{BAL\_DEGLICTH}$	Short/open detect filter time	—	20	—	µs
Internal temperature measurement					
IC_TEMP1_ERR	IC temperature measurement error	−3.0	—	3.0	K
IC_TEMP1_RES	IC temperature resolution	—	0.032	—	K/LSB
TSD_TH	Thermal shutdown	—	170	—	°C
TSD_HYS	Thermal shutdown hysteresis	—	10	—	°C
Default operational parameters					
$V_{CTOV(TH)}$	Cell overvoltage threshold (8 bits)	0.0	4.2	5.0	V
$V_{CTOV(RES)}$	Cell overvoltage threshold resolution	—	19.53125	—	mV/LSB
$V_{CTUV(TH)}$	Cell undervoltage threshold (8 bits)	0.0	2.5	5.0	V
$V_{CTUV(RES)}$	Cell undervoltage threshold resolution	—	19.53125	—	mV/LSB
$V_{GPIO\_OT(TH)}$	GPIOx configured as ANx input overtemperature threshold from POR	—	1.16	—	V
$V_{GPIO\_OT(RES)}$	Overtemperature voltage threshold resolution	—	4.8828125	—	mV/LSB
$V_{GPIO\_UT(TH)}$	GPIOx configured as ANx input undertemperature threshold from POR	—	3.82	—	V
$V_{GPIO\_UT(RES)}$	Undertemperature voltage threshold resolution	—	4.8828125	—	mV/LSB
General purpose input/output GPIOx					
V_{IH}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	100	—	mV
I_{IL}	Input leakage current Pins 3-state, V_{IN} = V_{COM} or AGND	−100	—	100	nA
I_{IDL}	Differential input leakage current GPIO 5,6 GPIO 5,6 configured as digital inputs for current measurement	−30	—	30	nA
V_{OH}	Output high-voltage I_{OH} = −0.5 mA	V_{COM} − 0.8	—	—	V
V_{OL}	Output low-voltage I_{OL} = +0.5 mA	—	—	0.8	V
V_{ADC}	Analog ADC input voltage range for ratiometric measurements	AGND	—	V_{COM}	V

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
$V_{OL(TH)}$	Analog input open pin detect threshold	—	0.15	—	V
R_{OPENPD}	Internal open detection pull-down resistor	—	5.0	—	kΩ
t_{GPIO0_WU}	GPIO0 WU de-glitch filter	—	50	—	µs
t_{GPIO0_FLT}	GPIO0 daisy chain de-glitch filter both edges	—	20	—	µs
t_{GPIO2_SOC}	GPIO2 convert trigger de-glitch filter	—	2.0	—	µs
t_{GPIOx_DIN}	GPIOx configured as digital input de-glitch filter	2.5	—	5.6	µs
Reset input					
V_{IH_RST}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL_RST}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	0.6	—	V
$t_{RESETFLT}$	RESET de-glitch filter	—	100	—	µs
R_{RESET_PD}	Input logic pull down (RESET)	—	100	—	kΩ
SPI_COM_EN input					
V_{IH}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	450	—	mV
Digital interface					
V_{FAULT_HA}	FAULT output (high active, I_{OH} = 1.0 mA)	—	4.9	—	V
I_{FAULT_CL}	FAULT output current limit	3.0	—	25	mA
R_{FAULT_PD}	FAULT output pulldown resistance	—	100	—	kΩ
V_{IH_COMM}	Voltage threshold to detect the input as high SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL (NOTE: needs to be 3.3 V compatible)	—	—	2.0	V
V_{IL_COMM}	Voltage threshold to detect the input as low SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL	0.8	—	—	V
V_{HYS}	Input hysteresis SI/RDTX_IN+, SCLK/RDTX_IN−, CSB, SDA, SCL	—	100	—	mV
I_{LOGIC_SS}	Sleep state input logic current CSB	−100	—	100	nA
R_{SCLK_PD}	Input logic pulldown resistance (SCLK/RDTX_IN–, SI/RDTX+)	—	20	—	kΩ
R_{I_PU}	Input logic pullup resistance to V_{COM} (CSB, SDA, SCL)	—	100	—	kΩ
I_{SO_TRI}	3-state SO input current 0 V to V_{COM}	−2.0	—	2.0	µA
V_{SO_HIGH}	SO high-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA	V_{DDIO} − 0.4	—	—	V
V_{SO_LOW}	SO, SDA, SLK low-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA	—	—	0.4	V
CSB_{WU_FLT}	CSB wake-up de-glitch filter, low to high transition	—	50	—	µs

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
System timing					
t_{CELL_CONV}	Time needed to acquire all 6 cell voltages and the current after an on demand conversion				µs
	13-bit resolution	—	41	—	
	14-bit resolution	—	57	—	
	15-bit resolution	—	89	—	
	16-bit resolution	—	152	—	
t_{SYNC}	V/I synchronization time				µs
	ADC1-A,B at 13 bit, ADC2 at 13 bit	—	41.39	—	
	ADC1-A,B at 14 bit, ADC2 at 13 bit	—	42.71	—	
	ADC1-A,B at 15 bit, ADC2 at 13 bit	—	47.37	—	
	ADC1-A,B at 16 bit, ADC2 at 13 bit	—	95.14	—	
t_{SYNC}	V/I synchronization time				µs
	ADC1-A,B at 13 bit, ADC2 at 14 bit	—	46.73	—	
	ADC1-A,B at 14 bit, ADC2 at 14 bit	—	48.05	—	
	ADC1-A,B at 15 bit, ADC2 at 14 bit	—	50.71	—	
	ADC1-A,B at 16 bit, ADC2 at 14 bit	—	92.47	—	
t_{SYNC}	V/I synchronization time				µs
	ADC1-A,B at 13 bit, ADC2 at 15 bit	—	57.39	—	
	ADC1-A,B at 14 bit, ADC2 at 15 bit	—	58.71	—	
	ADC1-A,B at 15 bit, ADC2 at 15 bit	—	61.37	—	
	ADC1-A,B at 16 bit, ADC2 at 15 bit	—	87.14	—	
t_{SYNC}	V/I synchronization time				µs
	ADC1-A,B at 13 bit, ADC2 at 16 bit	—	78.73	—	
	ADC1-A,B at 14 bit, ADC2 at 16 bit	—	80.05	—	
	ADC1-A,B at 15 bit, ADC2 at 16 bit	—	82.71	—	
	ADC1-A,B at 16 bit, ADC2 at 16 bit	—	88.02	—	
$t_{VPWR(READY)}$	Time after VPWR connection for the IC to be ready for initialization	—	—	5.0	ms
$t_{WAKE-UP}$	Power up duration	—	—	440	µs
t_{WAKE_DELAY}	Time between wake pulses	—	600	—	µs
t_{NOWUP}	Time, starting from the first SOM received, to go back to Sleep/Idle mode time after receiving incomplete TPL bus wake-up sequence	—	—	1.3	ms
t_{IDLE}	Idle timeout after POR	—	60	—	s
$t_{BALANCE}$	Cell balance timer range	0.5	—	511	min
t_{CYCLE}	Cyclic acquisition timer range	0.0	—	8.5	s
t_{FAULT}	Fault detection to activation of fault pin				µs
	Normal mode	—	—	56	
t_{DIAG}	Diagnostic mode timeout	0.047	1.0	8.5	s
t_{EOC}	SOC to data ready (includes post processing of data)				µs
	13-bit resolution	—	148	—	
	14-bit resolution	—	201	—	
	15-bit resolution	—	307	—	
	16-bit resolution	—	520	—	
t_{SETTLE}	Time after SOC to begin converting with ADC1-A,B	—	12.28	—	µs

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLST_TPL}	Time needed to send an SOC command and read back 6 cell voltages, 7 temperatures, 1 current, and 1 coulomb counter with TPL communication working at 2.0 Mbit/s and ADC1-A,B configured as follows (with ADC_CFG[AVG] = 0): 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 — — — —	 0.79 0.85 0.95 1.16	 — — — —	ms
t_{CLST_SPI}	Time needed to send an SOC command and read back 6 cell voltages, 7 temperatures, 1 current, and 1 coulomb counter with SPI communication working at 4.0 Mbit/s and ADC1-A,B configured as follows (with ADC_CFG[AVG] = 0): 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 — — — —	 0.48 0.54 0.64 0.86	 — — — —	ms
$t_{I2C\_DOWNLOAD}$	Time to download EEPROM calibration after POR	—	—	1.0	ms
t_{I2C_ACCESS}	EEPROM access time, EEPROM write (depends on device selection)	—	5.0	—	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx}$ = 00	 —	 500	 —	µs
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx}$ = 01	 —	 1.0	 —	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx}$ = 10	 —	 10	 —	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx}$ = 11	 —	 100	 —	ms
$t_{WAVE\_DC\_ON}$	Daisy chain duty cycle on time	—	500	—	µs
t_{COM_LOSS}	Time out to reset the IC in the absence of communication	—	1024	—	ms
SPI interface					
t_{TD}	Sequential data transfer delay in SPI mode (N)	1.0	—	—	µs
F_{SCK}	SCLK frequency	—	—	4.0	MHz
t_{SCK_H}	SCLK high time (A)	125	—	—	ns
t_{SCK_L}	SCLK high time (B)	125	—	—	ns
t_{SCK}	SCLK period (A+B)	250	—	—	ns
t_{FALL}	SCLK falling time	—	—	15	ns
t_{RISE}	SCLK rising time	—	—	15	ns
t_{SET}	SCLK setup time (O)	20	—	—	ns
t_{HOLD}	SCLK hold time (P)	20	—	—	ns
t_{SI_SETUP}	SI setup time (F)	40	—	—	ns
t_{SI_HOLD}	SI hold time (G)	40	—	—	ns
t_{SO_VALID}	SO data valid, rising edge of SCLK to SO data valid (I)	—	—	40	ns

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
t_{SO_EN}	SO enable time (H)	—	—	40	ns
$t_{SO\_DISABLE}$	SO disable time (K)	—	—	40	ns
t_{CSB_LEAD}	CSB lead time (L)	100	—	—	ns
t_{CSB_LAG}	CSB lag time (M)	100	—	—	ns
TPL interface (MCU)					
t_{MCU_RES}	Time between two consecutive message request transmitted by MCU	4.0	—	—	µs
t_{WU_Wait}	Time the MCU shall wait after sending first wake-up message per MC33772C IC	0.75	—	—	ms
TPL interface (MC33772C)					
t_{TPL_TD}	Sequential data transfer delay in TPL mode	—	4.0	—	µs
t_{TPL}	Transmit pulse duration	—	208	—	ns
t_{port_delay}	Port delay introduced by each repeater in MC33772C	—	—	0.95	µs
t_{RES}	Slave response after read command	—	5.0	—	µs
$V_{RDTX\ INTH}$	Differential receiver threshold	—	580	—	mV
t_{EOM}	Message timeout duration	—	250	—	µs

7.5 Timing diagrams

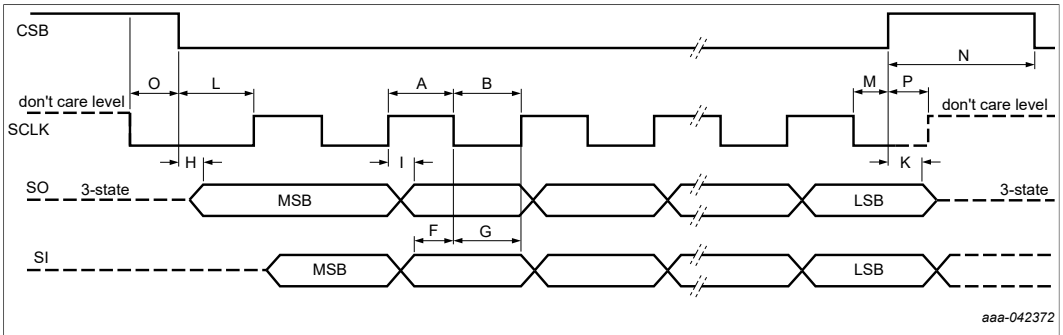


Figure 4. Low-voltage SPI interface timing

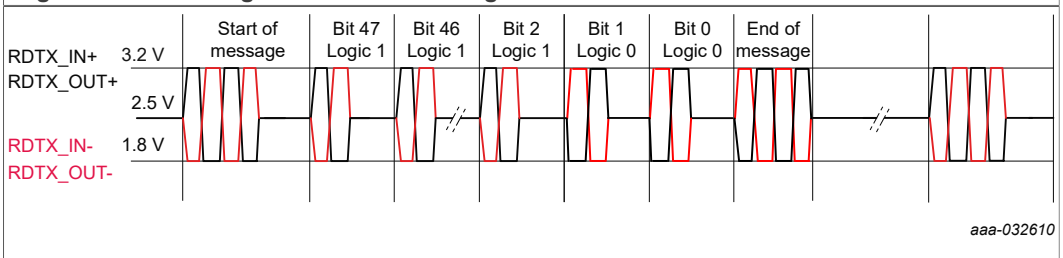


Figure 5. Transformer communication signaling

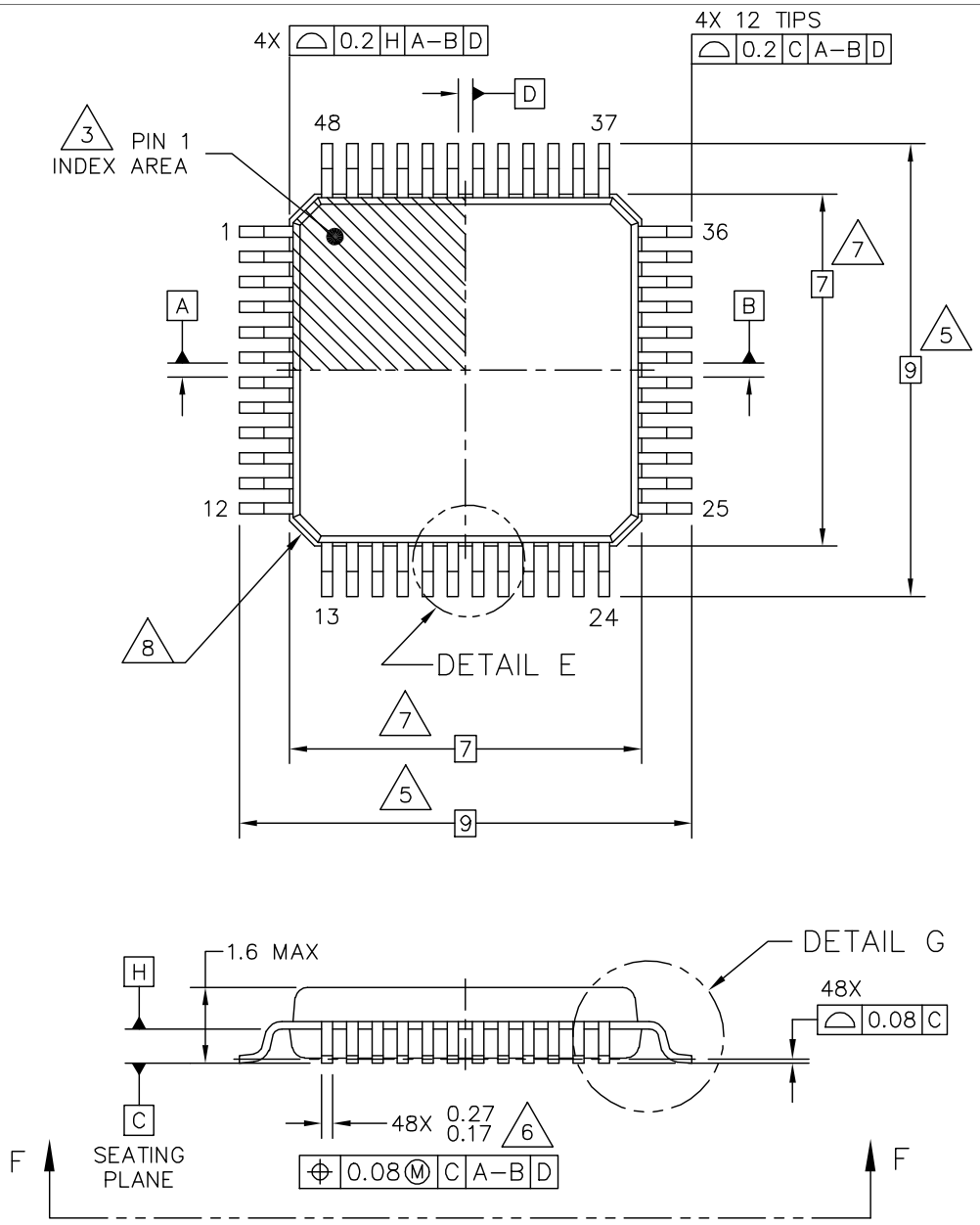
8 Packaging

8.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the document number of the drawings.

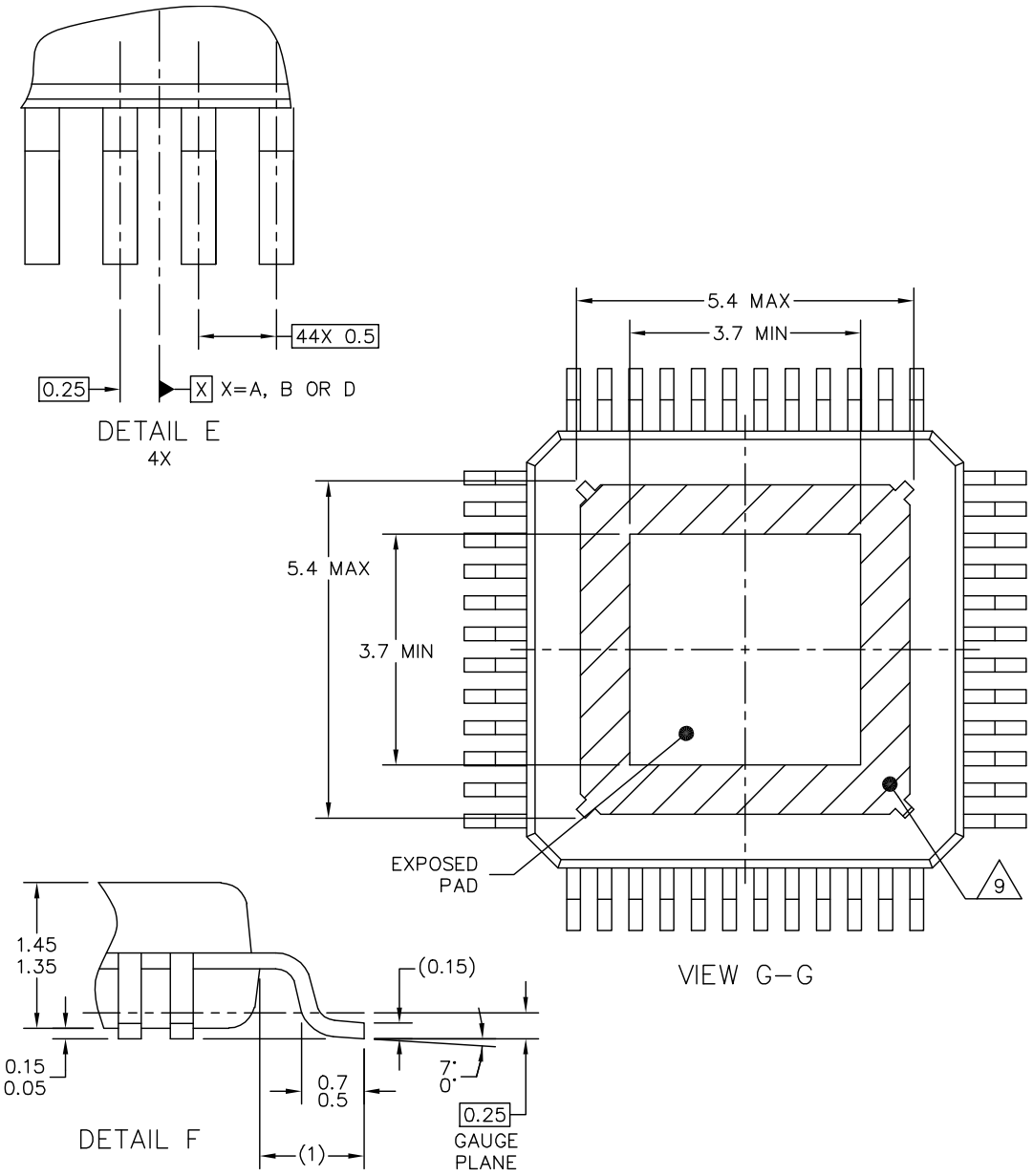
Table 10. Package Outline

Package	Suffix	Package outline drawing number
48-pin LQFP-EP	AE	SOT1571-1



DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	



 DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
7. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 6. Package outline

9 Revision history

Revision history

Revision	Date	Description
v.3	20210604	update to align with data sheet MC33772C v.3
v.2	20210310	update to align with preliminary data sheet
v.1	20200324	initial version

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Tables

Figures

Contents

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