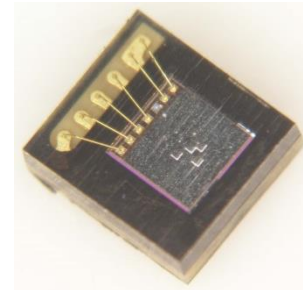


## Brief Description

The ZOPT2201 Sensor integrates an ambient light sensor (ALS) and ultraviolet energy sensor (UVBS). The device can be connected via an I<sup>2</sup>C interface to an external microcontroller. Other I<sup>2</sup>C or SMBus devices can be connected to the same interface. The device has a programmable interrupt with hysteresis to respond to events and reduce the microcontroller tasks.

A major application of the device is in smart phones or other mobile devices to enable brightness control of display panels (ALS) and diverse health care applications or contextual awareness algorithms (UVBS).



## Features

- High ambient light and UVB energy sensitivity
- Superior infrared energy suppression
- Very stable spectral response over angle of light incidence
- Wide dynamic range
- Excellent temperature compensation
- Lowest conversion repeat noise
- I<sup>2</sup>C interface capable of standard mode (100kHz) or fast mode (400kHz) communication; 1.8V logic compatible
- Programmable interrupt function for ALS and UVBS with upper and lower thresholds

## ALS Features

- Integrated ALS closely matches human eye response for high lux accuracy over different light sources
- Absolute sensitivity: 0.008 lux to 157000 lux
- Configurable output resolution: 13 to 20 bits
- Configurable analog gain: x1 to x18
- Linear output code
- 50Hz/60Hz light flicker immunity
- Fluorescent light flicker immunity

## UVBS Features

- Linear UV index measurement (1 to >11)
- Tailored temperature compensation

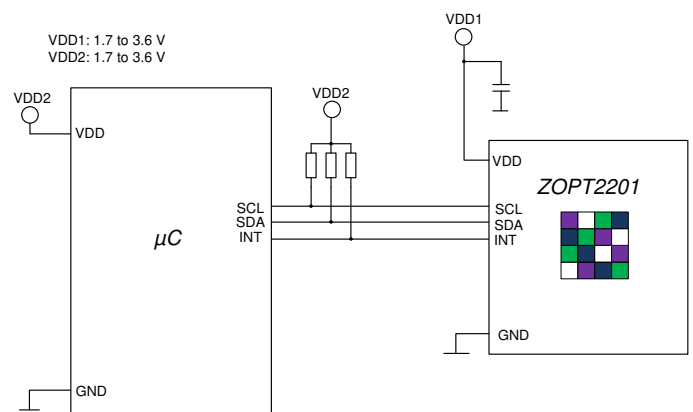
## Physical Characteristics

- Wide operation temperature: -40°C to +90°C
- Wide supply voltage: 1.7V to 3.6V
- Minimum active current at maximum duty cycle:
  - ALS: 110µA typical
  - UVBS: 100µA typical

Note: Average current is proportionally lower with lower measurement rates.

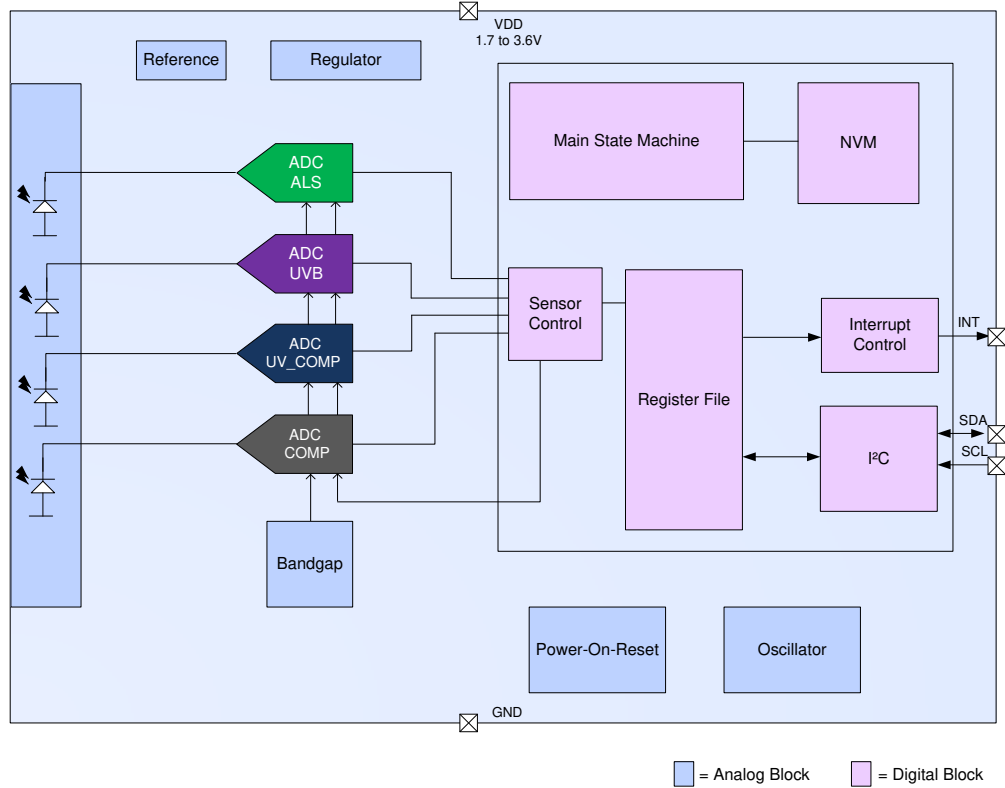
- Low standby current: 1µA typical
- Packages:
  - LGA6 (2.0 × 2.2 × 0.7 mm)
  - TSV (1.1 × 1.2 × 0.26 mm)

## ZOPT2201 Application Circuit



# ZOPT2201 Block Diagram

- Applications**
- Cellular phones
  - Notebooks
  - Consumer devices



## Ordering Information

Product Sales Code	Description	Delivery Package
ZOPT2201AC5R	ZOPT2201 LGA6 – Temperature range: -40 to +90°C	Reel
ZOPT2201AC9R	ZOPT2201 TSV – Temperature range: -40 to +90°C	Reel
ZOPT2201KIT V1.0	ZOPT2201 Evaluation Kit, including ZOPT Control Board, mini-USB cable, and 1 ZOPT2201 sample mounted on the LGA6 Sensor Board; kit software is available for free download – see the <i>ZOPT Evaluation Kit Quick Start Guide</i> included in the kit for instructions.	

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## 1. Characteristics

### 1.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The device might not function or be operable above the recommended operating conditions given in section 1.2. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the "Absolute Maximum Ratings."

Parameter	Symbol	Conditions	Min.	Max.	Units
Maximum input supply voltage (VDD pin)	$V_{DD-GND}$			4.0	V
Maximum voltage on SCL, SDA and INT pins	$V_{I2C}$		-0.5	4.0	V
Maximum operating temperature range	$T_{AMB\_MAX}$		-40	90	°C
Storage temperature	$T_{STOR}$		-45	95	°C
Maximum input current into any pin except supply pins (latch-up)	$I_{IN}$		-100	100	mA
Electrostatic discharge protection [a]	$V_{HBM}$	Human Body Model, JESD22-A114	2000		V

[a] HBM: C = 100pF charged to  $V_{HBM}$  with resistor R = 1.5k $\Omega$  in series; valid for all pins.

### 1.2 Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Voltage supply on VDD pin	$V_{DD}$		1.7		3.6	V
Ambient operating temperature range	$T_{AMB}$		-40		90	°C

### 1.3 Electrical and Optical Parameters

$V_{DD} = 2.8V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+90^{\circ}C$ , unless otherwise noted.

Note: See important table notes at the end of the table.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>Power On Reset</b>						
DC power-on reset level	POR <sub>LH</sub>	Slow variation of VDD	1.00	1.34	1.60	V
	POR <sub>HL</sub>					
<b>Current Consumption</b>						
ALS Mode [a]	I <sub>ALS</sub>	Maximum duty cycle, VDD = 2.8V, Gain Mode 3		110		μA
UVBS Mode [b]	I <sub>UVBS</sub>	Maximum duty cycle, VDD = 2.8V		100		μA
ALS/UVBS_Raw Mode [a]	I <sub>ALS+UVBS</sub>	Maximum duty cycle, VDD = 2.8V		130		μA
Standby Mode	I <sub>SBY</sub>	ZOPT2201 in Standby Mode, no active I <sup>2</sup> C communication		1	2	μA
<b>I<sup>2</sup>C Interface</b>						
I <sup>2</sup> C signal input high	V <sub>I2Chigh</sub>		1.5		VDD	V
I <sup>2</sup> C signal input low	V <sub>I2Clow</sub>		0		0.4	V
<b>ALS Characteristics</b>						
Spectral response			See Figure 2.1.			
Detection range at gain 1	G <sub>1</sub>	Minimum specification applies to default setting of 18-bit resolution. Specification changes with the resolution setting as shown in Table 3.5.	0.6		157286	lux
Detection range at gain 3	G <sub>3</sub>		0.2		52429	lux
Detection range at gain 6 [c]	G <sub>6</sub>		0.1		26214	lux
Detection range at gain 9 [c]	G <sub>9</sub>		0.0667		17476	lux
Detection range at gain 18 [c]	G <sub>18</sub>		0.0333		8738	lux
Calibrated lux error at gain 3		White LED, 5000K, T <sub>AMB</sub> = +25°C			10	%
Light source matching		Fluorescent versus incandescent light			10	%
ALS output resolution	ALS <sub>RES</sub>	Programmable to 13, 16, 17, 18, 19, or 20 bit	13	18	20	Bit

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
50/60 Hz flicker noise error					±5	%
Dark level count	ALS <sub>DARK</sub>	0 lux, 18-bit range, T <sub>AMB</sub> = -40 to +60°C		0		Count
<b>UVBS Characteristics</b>						
Spectral Response			See Figure 2.7 and Figure 2.8.			
Sensitivity at gain 1	G <sub>1</sub>	Specifications apply to 20-bit resolution setting. Specification changes with resolution setting as shown in Table 3.6.		0.36		$\frac{\mu W/cm^2}{count}$
Sensitivity at gain 3	G <sub>3</sub>			0.12		$\frac{\mu W/cm^2}{count}$
Sensitivity at gain 6 [c]	G <sub>6</sub>			0.06		$\frac{\mu W/cm^2}{count}$
Sensitivity at gain 9 [c]	G <sub>9</sub>			0.04		$\frac{\mu W/cm^2}{count}$
Sensitivity at gain 18 [c]	G <sub>18</sub>			0.02		$\frac{\mu W/cm^2}{count}$
Calibrated error at gain 18		Calibration done with UVB LED, 310nm, T <sub>AMB</sub> = +25°C			10	%
UVBS output resolution	UVBS <sub>RES</sub>	Programmable to 13, 16, 17, 18, 19, or 20 bit	13	18	20	Bit
<b>Conversion Timing</b>						
Minimum integration time [d]	t <sub>INTmin1</sub>			3.125		ms
	t <sub>INTmin2</sub>	With 50/60 Hz rejection		50		ms
Maximum integration time [d]	t <sub>INTmax</sub>	With 50/60 Hz rejection		400		ms
Wake-up time from Standby Mode	t <sub>WAKE-STB</sub>	From Standby to Active Mode (measurement can start)		500		μs
Measurement repeat rate [d]		Programmable	25		2000	ms
Timing accuracy [e]			-25		+25	%

[a] For ALS, the maximum duty cycle is selected with a 100ms measurement time (default) and 100ms repeat rate at an illumination of 1000 lux.

[b] For UVBS, the maximum duty cycle is selected with 100ms measurement time (default), 100ms repeat rate.

[c] Values valid up to 60°C.

[d] Typical timing accuracy applied.

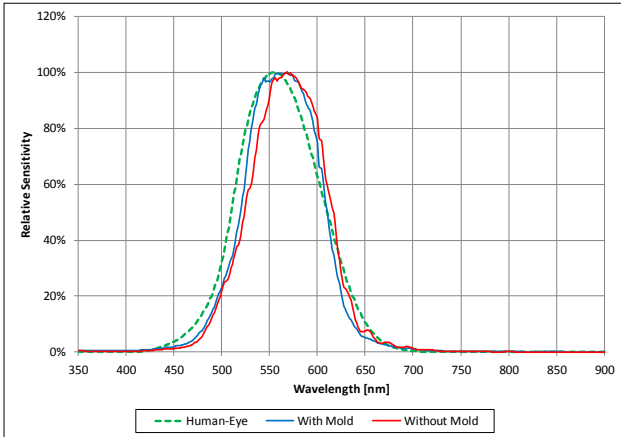
[e] All specifications related to timing can vary by this value; for example, a repeat rate of 50ms could vary up to 62.5ms.



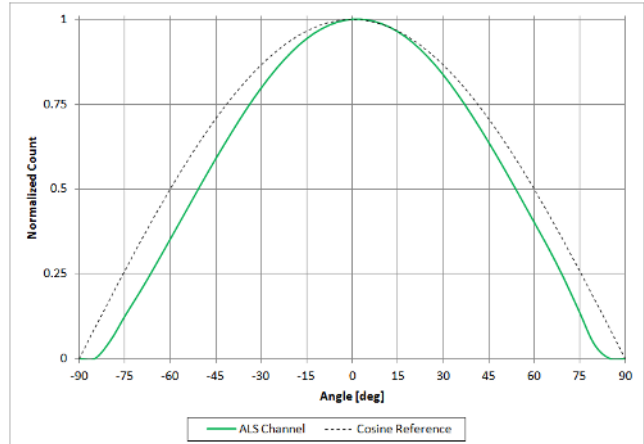
## 2. Typical Device Parameters

$V_{DD} = 2.8V$ , default power-up setting, unless otherwise noted.

**Figure 2.1 Spectral Response ALS**

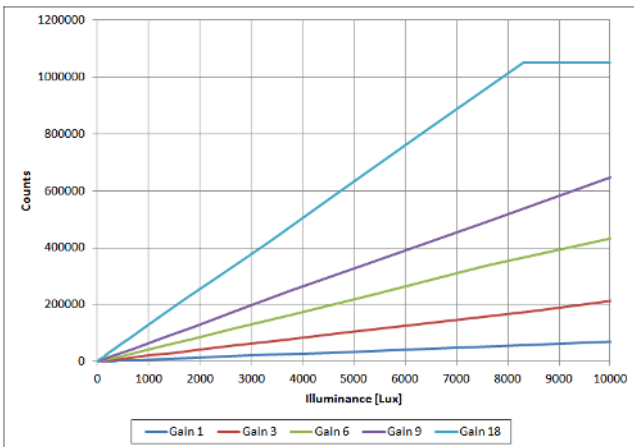


**Figure 2.2 ALS Sensitivity vs. Angle of Incidence**



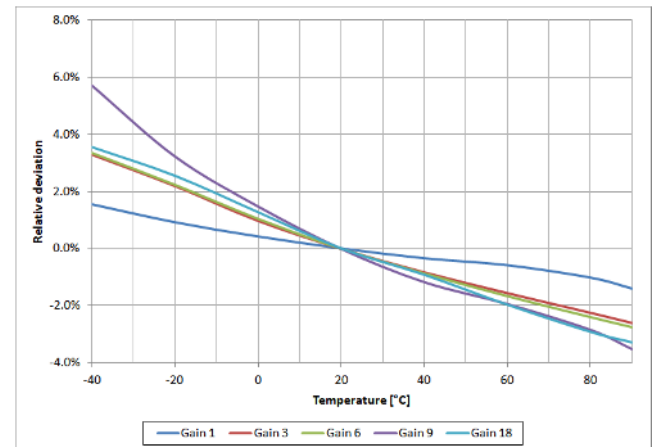
**Figure 2.3 ALS Linearity of all Gain Ranges**

Default 18-Bit Mode

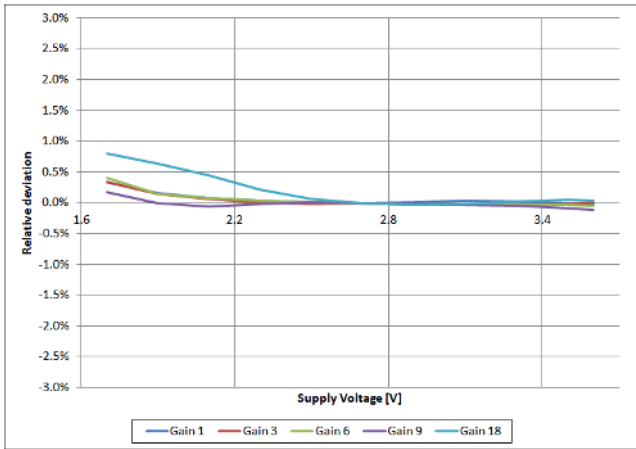


**Figure 2.4 ALS vs. Temperature at 1000 lux**

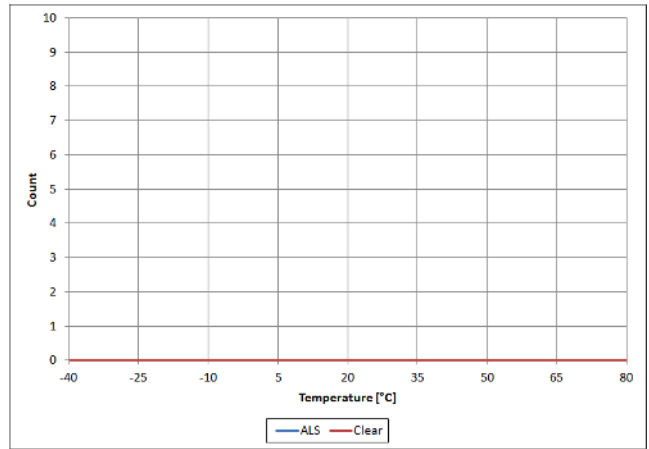
White LED



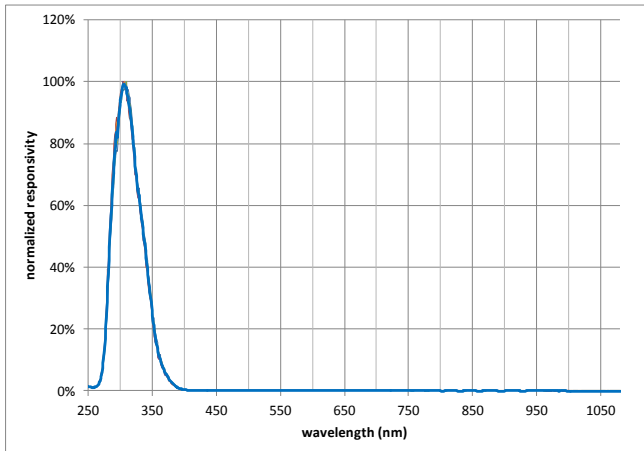
**Figure 2.5 ALS vs. Voltage at 1000 lux**



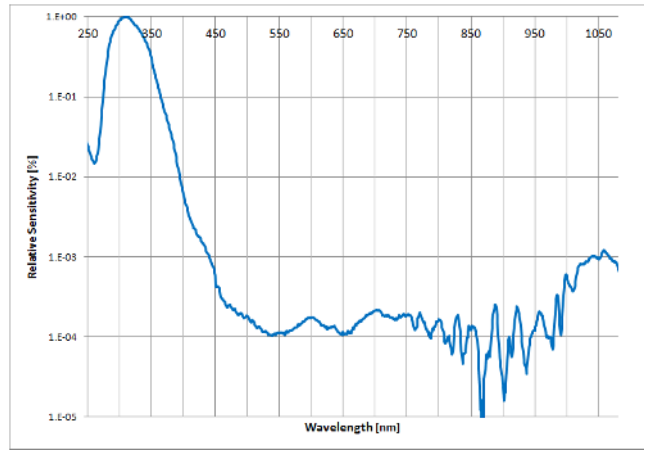
**Figure 2.6 ALS Typical Dark Count vs. Temperature**



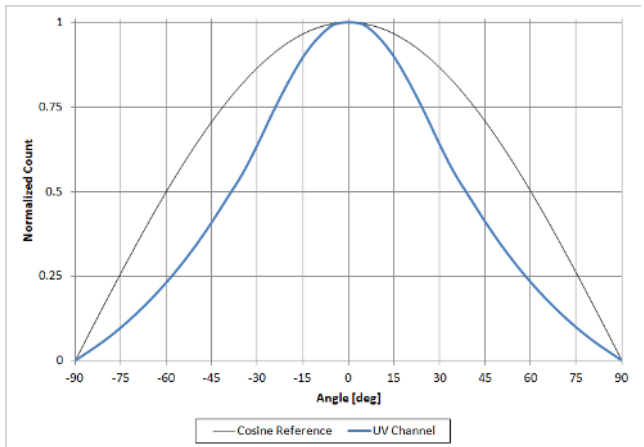
**Figure 2.7 Spectral Response UVBS, Linear**



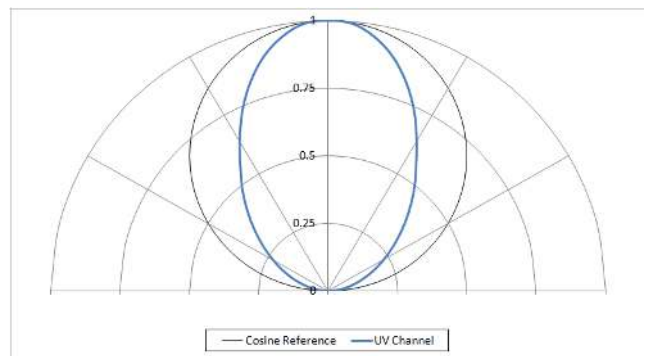
**Figure 2.8 Spectral Response UVBS, Logarithmic**



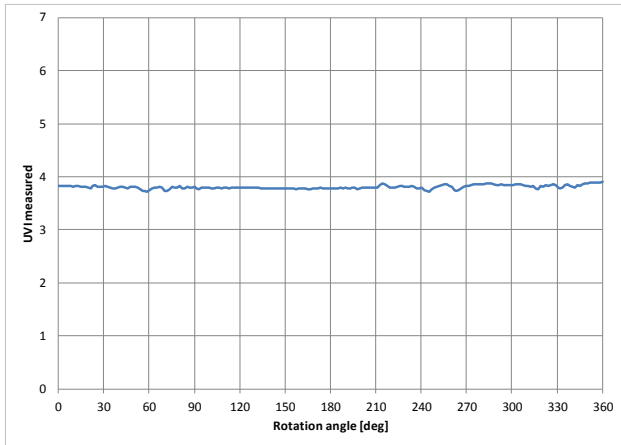
**Figure 2.9 UVBS Sensitivity vs. Angle of Incidence**  
310nm LED



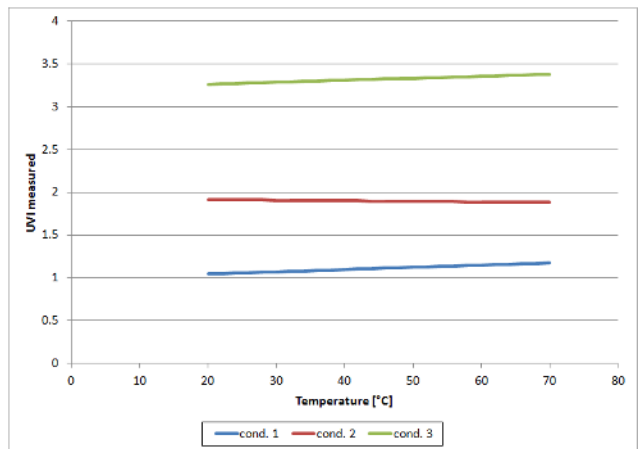
**Figure 2.10 UVBS Sensitivity vs. Angle of Incidence (Polar)**



**Figure 2.11 UVBS Rotation in Horizontal Plane**

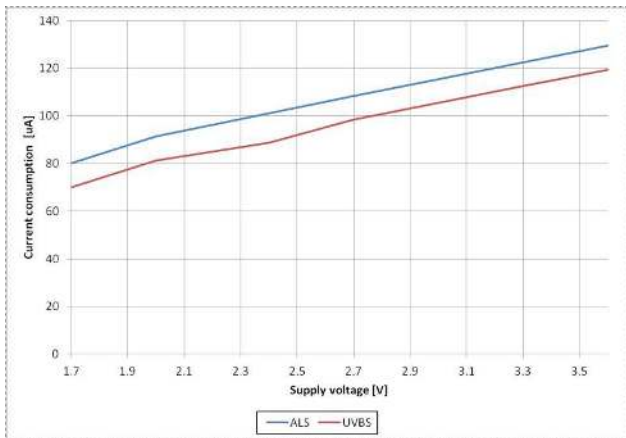


**Figure 2.12 UVBS Temperature Behavior for Several Sunlight Conditions**

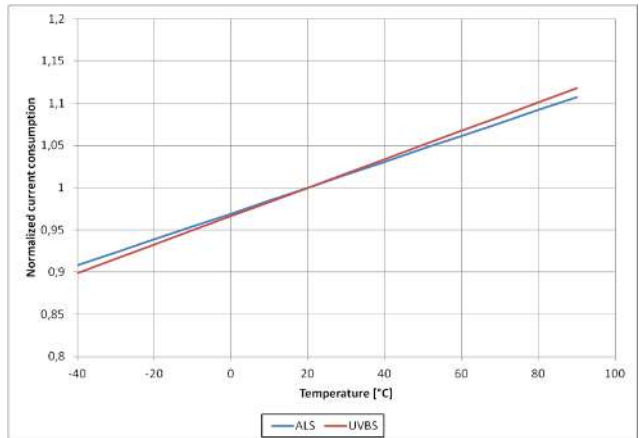


**Figure 2.13 Active Current vs. Supply Voltage**

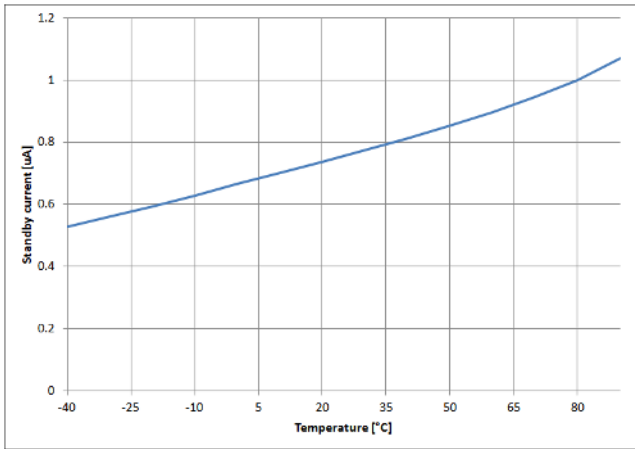
*ALS: default setting, UVBS: default setting*



**Figure 2.14 Normalized Active Current vs. Temperature**



**Figure 2.15 Standby Current vs. Temperature**

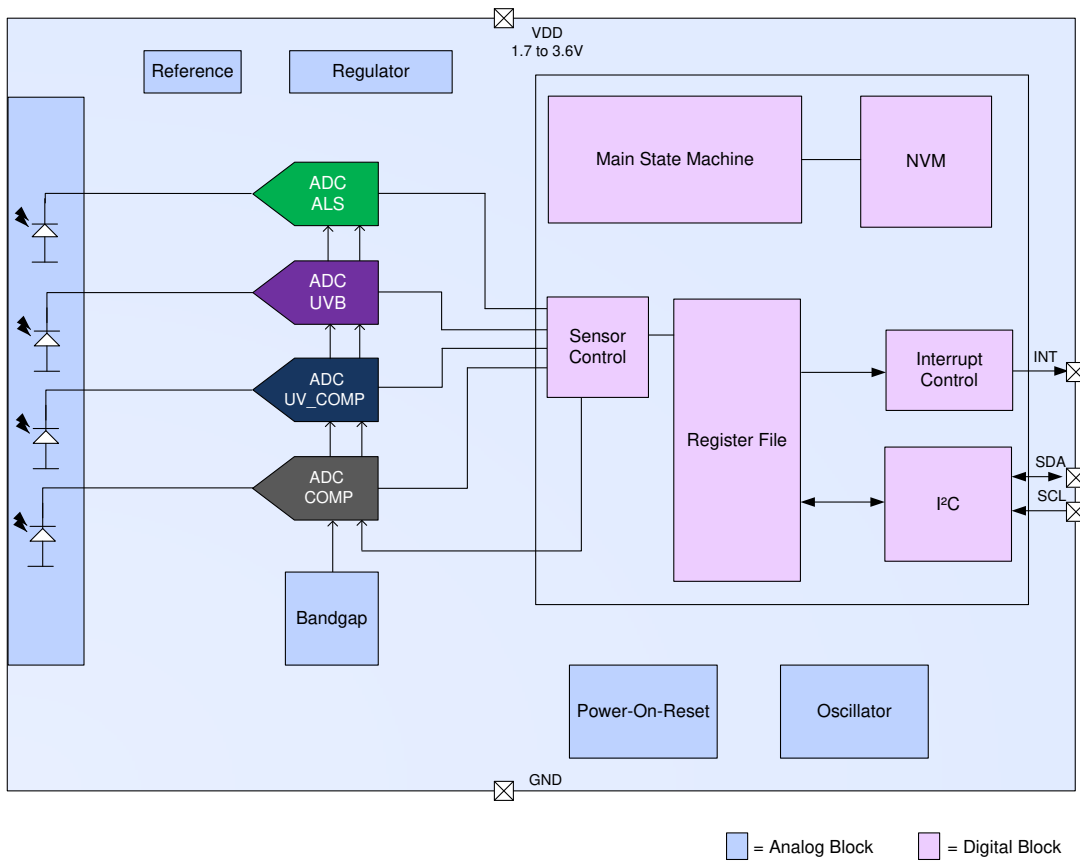


### 3. Detailed Description

The ZOPT2201 contains 4 different photodiode channels for ambient light measurement, UVB energy level measurement, and temperature compensation. The sensor diodes are arranged in a matrix array. The photodiode currents are converted to digital values by ADCs. The ZOPT2201 also includes some peripheral circuits such as an internal oscillator, current source, voltage reference, and internal one-time programmable non-volatile memory (NVM) to store trimming information.

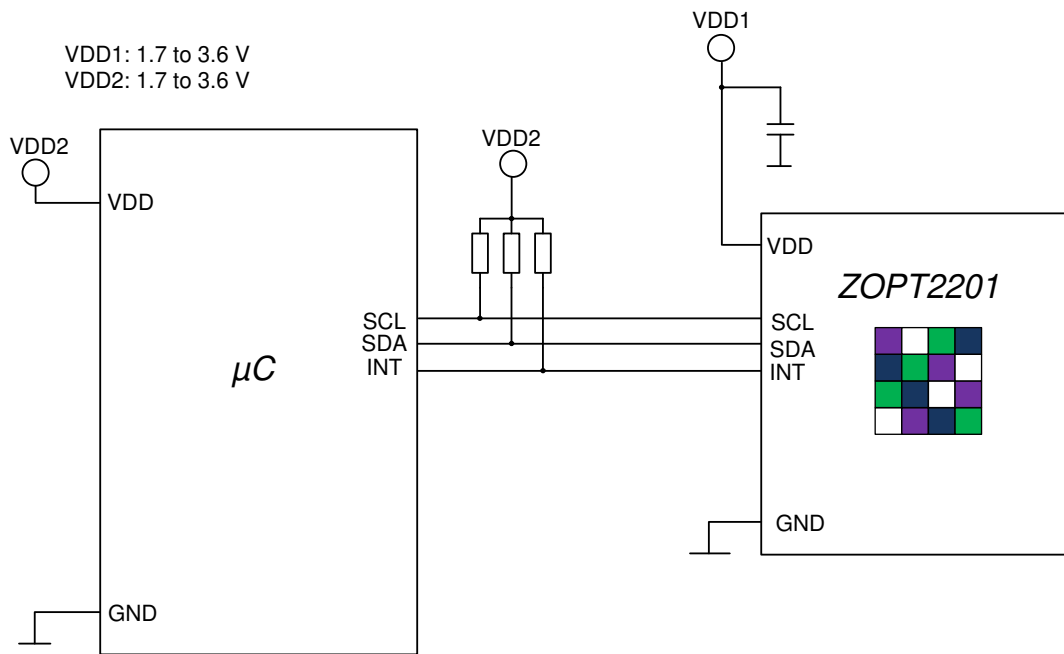
#### 3.1 Block Diagram of the ZOPT2201

Figure 3.1 Simplified ZOPT2201 Block Diagram



### 3.2 Application Circuit

Figure 3.2 Typical Application Circuit



### 3.3 Pin Description

For pin layout and package dimensions, refer to sections 4.1 and 4.2 for the LGA6 and TSV packages respectively.

**Table 3.1 Pin Description (LGA6)**

Number	Pin Name	I/O Type	Description
1	SCL	IN	I <sup>2</sup> C serial clock line
2	SDA	IN/OUT	I <sup>2</sup> C serial data line
3	VDD	SUPPLY	Digital/analog power supply
4	INT	OUT	Interrupt pin
5	GND	GROUND	Digital/analog ground
6	N.C.	-	Not connected

**Table 3.2 Pin Description (TSV)**

Number	Pin Name	I/O Type	Description
A1	INT	OUT	Interrupt pin
A2	SDA	IN/OUT	I <sup>2</sup> C serial data line
A3	N.C.	-	Not connected
B1	GND	GROUND	Digital/analog ground
B2	VDD	SUPPLY	Digital/analog power supply
B3	SCL	IN	I <sup>2</sup> C serial clock line

### 3.4 Device Operation Modes

**Table 3.3 Operational Mode Descriptions**

Mode Number	Mode Name	Description
1	Standby	Default mode after power-up. In this mode, the oscillator, all internal support blocks, and the ADCs are switched off but I <sup>2</sup> C communication is fully supported.
2	ALS	<p><u>Active ADC Channels:</u> ALS, COMP</p> <p>ALS Mode allows measurement of ambient light intensity. The sensor response is closely matched to human eye response to guarantee high lux value accuracy. Temperature compensation for the sensor elements is carried out internally via the COMP channel.</p> <ul style="list-style-type: none"> <li>▪ ALS Mode is activated by setting the <i>LS_EN</i> bit to 1, the <i>LS_Mode</i> bit to 0 and the <i>RawMode_SEL</i> bit to 0 in the <i>MAIN_CTRL</i> register (see section 3.11.1). <ul style="list-style-type: none"> <li>• Write 02<sub>HEX</sub> to register 00<sub>HEX</sub></li> </ul> </li> <li>▪ Internal temperature compensation runs following calculation before sensor data is stored in output register: <ul style="list-style-type: none"> <li>• <math>ALS = ALS\_raw - COMP</math></li> </ul> </li> </ul>
3	UVBS	<p><u>Active ADC Channels:</u> UVB, UV_COMP</p> <p>UVBS Mode allows high precision measurements of UVB energy intensity. The sensor response is chosen such that it can be used to calculate the UV index directly.</p> <p>Temperature and stray light compensation for the sensor channel is performed internally via the UV_COMP channel.</p> <ul style="list-style-type: none"> <li>▪ UVBS Mode is activated by setting the <i>LS_EN</i> bit and the <i>LS_Mode</i> bit to 1 in the <i>MAIN_CTRL</i> register (see section 3.11.1) <ul style="list-style-type: none"> <li>• Write 0A<sub>HEX</sub> to register 00<sub>HEX</sub></li> </ul> </li> <li>▪ Internal temperature compensation runs following calculation before sensor data is stored in the output register: <ul style="list-style-type: none"> <li>• <math>UVB = UVB\_raw - UV\_COMP</math></li> </ul> </li> </ul>



Mode Number	Mode Name	Description
4	ALS/UVBS_Raw	<p><u>Active ADC Channels:</u> ALS, UVB, UV_COMP, COMP</p> <p>ALS/UVBS_Raw Mode allows optimum temperature and stray light compensation for ALS and UVBS output data by external post-processing.</p> <ul style="list-style-type: none"> <li>▪ ALS/UVBS_Raw Mode uses a special operation mode of the ZOPT2201. It requires a specific sequence to initialize after power up.</li> <li>▪ The following commands must be sent via I<sup>2</sup>C <i>single byte</i> access to activate the special operation mode of ZOPT2201: <ul style="list-style-type: none"> <li>• Write B5<sub>HEX</sub> to register 31<sub>HEX</sub></li> <li>• Write DF<sub>HEX</sub> to register 30<sub>HEX</sub></li> <li>• Write 04<sub>HEX</sub> to register 31<sub>HEX</sub></li> </ul> </li> <li>▪ ALS/UVBS_Raw operation is activated (after the sequence above has been sent) by setting the <i>LS_EN</i> and <i>RawMode_SEL</i> bits to 1 and setting the <i>LS_Mode</i> bit to 0 in the <i>MAIN_CTRL</i> register (see section 3.11.1) <ul style="list-style-type: none"> <li>• Write 06<sub>HEX</sub> to register 00<sub>HEX</sub></li> </ul> </li> <li>▪ No internal temperature and stray light compensation is carried out. All channel data registers (see Table 3.10) carry the <i>uncompensated raw data</i> as received from the ADCs.</li> <li>▪ Important: Proper temperature and stray light <i>compensation must be done on the application level</i> applying following formulas: <ul style="list-style-type: none"> <li>• ALS = ALS<sub>raw</sub> – COMP</li> <li>• UVB = UVB<sub>raw</sub> – UV_COMP</li> </ul> </li> </ul> <p>Important: The internal digital trimming factors are not applied to the output data in the ALS/UVBS_Raw Mode. If this mode is used, contact IDT for the related application note (see contact information on last page).</p>

**Table 3.4 Channel Activation vs. Operation Mode**

Mode Number	Mode Name	ALS		UVB		UV_COMP		COMP	
		Inactive	Active	Inactive	Active	Inactive	Active	Inactive	Active
1	Standby	✓		✓		✓		✓	
2	ALS		✓	✓		✓			✓
3	UVBS	✓			✓		✓	✓	
4	ALS/UVBS_Raw		✓		✓		✓		✓

### 3.5 Conversion Control State Machine

#### 3.5.1 Start Up after Power-On or Software Reset

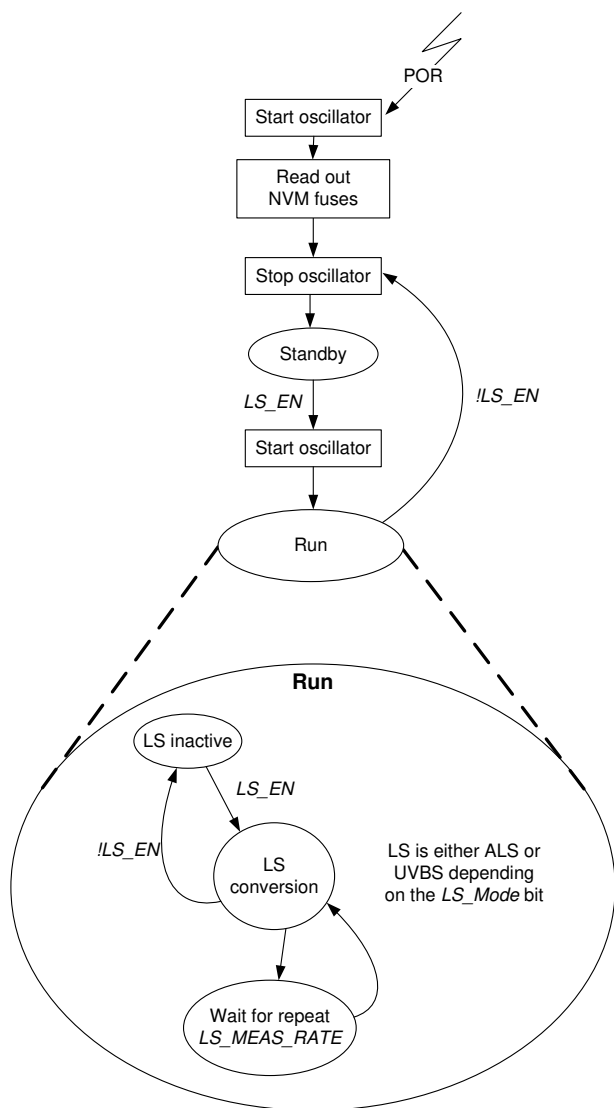
The main state machine is set to “Start State” during a power-on or software reset. As soon as the reset is released, the internal oscillator is started and the programmed I<sup>2</sup>C address and the trim values are read from the internal NVM trimming data block. The ZOPT2201 enters Standby Mode as soon as the Idle State is reached (see Figure 3.3).

NOTE: If the I<sup>2</sup>C address has not yet been read, the device will respond with NACK to any I<sup>2</sup>C command and ignore any request to avoid responding to an incorrect I<sup>2</sup>C address.

If any of the sensor operation modes becomes activated through an I<sup>2</sup>C command (i.e., the *LS\_EN* bit is set to 1 and the sensor mode is selected with the respective bits in the *MAIN\_CTRL* register), the internal support blocks are immediately powered on. Once the voltages and currents are settled (typical after 500µs), the state machine checks for trigger events from a measurement scheduler to start conversions according to the selected measurement repeat rates (see section 3.11.2).

When the user resets the *LS\_EN* bit to 0, a running conversion will be completed and the relevant ADCs and support blocks will move to Standby Mode thereafter.

**Figure 3.3 Main State Machine**



### 3.6 Light Sensor Sensitivity Configuration

#### 3.6.1 Gain Modes, Resolution, and Measurement Time

There are five analog gain modes to adjust the sensitivity of the ZOPT2201 device to the needs of the application. The microcontroller can calculate the ambient light in lux by multiplying the ADC count value of the ALS channel with the appropriate output-scaling coefficient. A similar method can be used for UVI determination via UVBS channel.

If ALS/UVBS\_Raw Mode is used, temperature and stray light compensation must be carried out in the microcontroller before output scaling coefficients are applied (see Table 3.3 for the ALS/UVBS\_Raw Mode description).

Selected analog gain settings as well as resolution and measurement time settings are valid for all active ADC converter channels at the same time. The gain, resolution, and measurement time cannot be simultaneously set to different settings for different channels. If different gain or resolution settings are required for different channels, conversions must be performed consecutively with modified settings.

**Table 3.5 ALS Detection Ranges**

Effective Output Resolution [Bits]	Measurement Time [ms]	Gain Mode 1			Gain Mode 3		
		Minimum Detection [lux]	Maximum Detection [lux]	Result Resolution [lux/Count]	Minimum Detection [lux]	Maximum Detection [lux]	Result Resolution [lux/Count]
13	3.125	19.2000	157286	19.2000	6.4000	52429	6.4000
16	25	2.4000	157286	2.4000	0.8000	52429	0.8000
17	50	1.2000	157286	1.2000	0.4000	52429	0.4000
<b>18 (default)</b>	<b>100</b>	<b>0.6000</b>	<b>157286</b>	<b>0.6000</b>	<b>0.2000</b>	<b>52429</b>	<b>0.2000</b>
19	200	0.3000	157286	0.3000	0.1000	52429	0.1000
20	400	0.1500	157286	0.1500	0.0500	52429	0.0500

Effective Output Resolution [Bits]	Measurement Time [ms]	Gain Mode 6			Gain Mode 9		
		Minimum Detection [lux]	Maximum Detection [lux]	Result Resolution [lux/Count]	Minimum Detection [lux]	Maximum Detection [lux]	Result Resolution [lux/Count]
13	3.125	3.2000	26214	3.2000	2.1333	17476	2.1333
16	25	0.4000	26214	0.4000	0.2667	17476	0.2667
17	50	0.2000	26214	0.2000	0.1333	17476	0.1333
<b>18 (default)</b>	<b>100</b>	<b>0.1000</b>	<b>26214</b>	<b>0.1000</b>	<b>0.0667</b>	<b>17476</b>	<b>0.0667</b>
19	200	0.0500	26214	0.0500	0.0333	17476	0.0333
20	400	0.0250	26214	0.0250	0.0167	17476	0.0167

		Gain Mode 18		
Effective Output Resolution [Bits]	Measurement Time [ms]	Minimum Detection [lux]	Maximum Detection [lux]	Result Resolution [lux/Count]
13	3.125	1.0667	8738	1.0667
16	25	0.1333	8738	0.1333
17	50	0.0667	8738	0.0667
<b>18 (default)</b>	<b>100</b>	<b>0.0333</b>	<b>8738</b>	<b>0.0333</b>
19	200	0.0167	8738	0.0167
20	400	0.0083	8738	0.0083

**Table 3.6 UVBS Sensitivities**

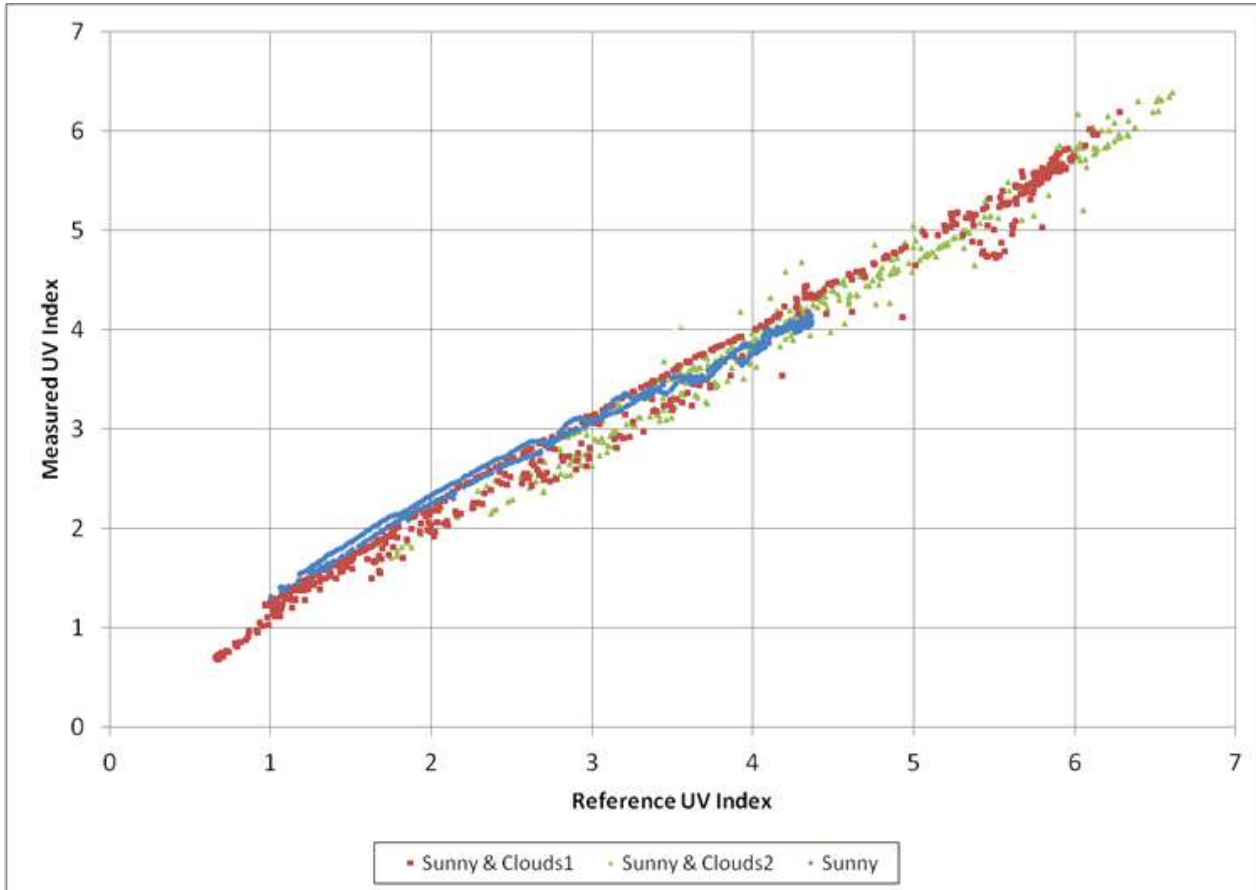
Note: See section 3.11.3 for further details.

		Gain Mode 1	Gain Mode 3	Gain Mode 6	Gain Mode 9	Gain Mode 18
Effective Output Resolution [Bits]	Measurement Time [ms]	Sensitivity $\left[\frac{\text{counts}}{\mu\text{W}/\text{cm}^2}\right]$	Sensitivity $\left[\frac{\text{counts}}{\mu\text{W}/\text{cm}^2}\right]$	Sensitivity $\left[\frac{\text{counts}}{\mu\text{W}/\text{cm}^2}\right]$	Sensitivity $\left[\frac{\text{counts}}{\mu\text{W}/\text{cm}^2}\right]$	Sensitivity $\left[\frac{\text{counts}}{\mu\text{W}/\text{cm}^2}\right]$
13	3.125	0.022	0.065	0.130	0.195	0.391
16	25	0.174	0.521	1.042	1.563	3.125
17	50	0.347	1.042	2.083	3.125	6.250
<b>18 (default)</b>	<b>100</b>	<b>0.694</b>	<b>2.083</b>	<b>4.167</b>	<b>6.250</b>	<b>12.500</b>
19	200	1.389	4.167	8.333	12.500	25.000
20	400	2.778	8.333	16.667	25.000	50.000

### 3.7 UVB Sensor Match to UVI

Due to the specifically designed spectral sensitivity of the UVB sensor, a very good match between sensor readings and reference UVI meter readings is achieved for different weather conditions.

**Figure 3.4 Measured UV Index vs. Reference UVI Meter**



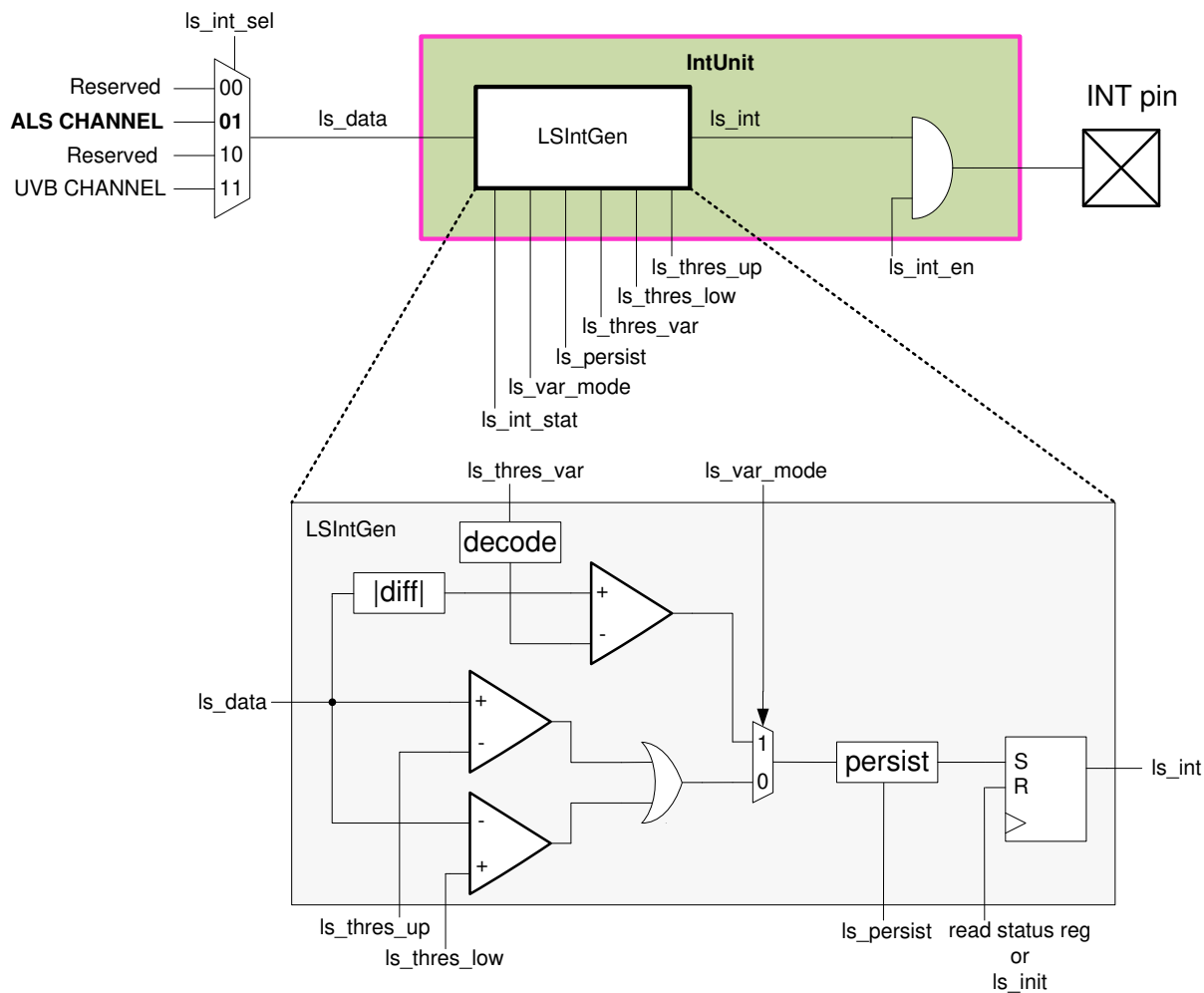
### 3.8 Interrupt Features

The ZOPT2201 can generate an interrupt signal on a user-selected sensor channel. Interrupts will be triggered if upper or lower threshold values are crossed or if the output count variation of consecutive conversions has exceeded a defined limit.

An interrupt can be displayed at the INT pin as an active-low signal or via a status register flag. Interrupt conditions are always evaluated after completion of a new conversion on the selected sensor channel.

The *ls\_int* signal (output of LSIntGen in Figure 3.5) is also stored in the *MAIN\_STATUS* register as the *LS interrupt status* (see section 3.11.5) flag. The flag is cleared by reading the *MAIN\_STATUS* register. A cleared *LS interrupt status* flag will also clear the interrupt signal on the INT pin.

**Figure 3.5 Interrupt Unit**



The interrupt is configured by the bits in the *INT\_CFG* register (see section 3.11.10). It can function as either threshold triggered (*LS\_VAR\_MODE* = 0) or variance triggered (*LS\_VAR\_MODE* = 1).

The interrupt source generator is configurable to be one of the following input channels: ALS or UVBS. The interrupt source is selected by the *LS\_INT\_SEL* bits in the *INT\_CFG* register (see section 3.11.10).

The threshold interrupt is enabled with  $LS\_INT\_EN = 1$  and  $LS\_VAR\_MODE = 0$ . The interrupt is set when the respective \*\_DATA register value of the selected interrupt source channel is above the upper or below the lower threshold configured in the  $LS\_THRES\_UP$  and  $LS\_THRES\_LOW$  registers (see sections 3.11.12 and 3.11.13 respectively) for a specified number of consecutive measurements as configured in the  $INT\_PST$  register ( $1 + LS\_PERSIST$ ; see section 3.11.11).

The variance interrupt is enabled with  $LS\_INT\_EN = 1$  and  $LS\_VAR\_MODE = 1$ . It is set when the absolute value difference between the preceding and the current output data of the selected interrupt source channel is above the decoded variance threshold (see section 3.11.14) for a specified number of consecutive measurements ( $1 + LS\_PERSIST$ ).

### 3.9 I<sup>2</sup>C Interface

The ZOPT2201 is equipped with an I<sup>2</sup>C interface for control and data communication. The chip always operates as a slave. The device offers two different 7-bit slave addresses that are selectable via NVM programming. A read/write bit must be appended to the slave address by the master device to properly communicate with the device.

The interface is compatible with standard mode (100kHz) and fast mode (400kHz) I<sup>2</sup>C communication.

**Table 3.7 Supported I<sup>2</sup>C Clock Frequencies**

Mode	Frequency	Transient Noise Filter
Standard	100kHz	50ns
Fast	400kHz	50ns

The I<sup>2</sup>C circuitry is always active (Standby or Active Mode of the ZOPT2201). If the I<sup>2</sup>C address is not yet read from the memory block, the device will respond with “NACK” to any request and ignore the possible commands. An attempt to read or write to non-existing addresses will be answered with “NACK.”

#### 3.9.1 I<sup>2</sup>C Address Decoding

The I<sup>2</sup>C address decoding is done during start up after a power-on-reset or software reset. Two different I<sup>2</sup>C addresses can be selected through NVM programming (see Table 3.8).

**Table 3.8 I<sup>2</sup>C Address**

Address NVM Level	I <sup>2</sup> C Address		
	7 Bits	Write	Read
0 – Default	1010 011 <sub>XBIN</sub>	A6 <sub>HEX</sub>	A7 <sub>HEX</sub>
1 – Programmed	1010 010 <sub>XBIN</sub>	A4 <sub>HEX</sub>	A5 <sub>HEX</sub>

#### 3.9.2 I<sup>2</sup>C Register Read

The ZOPT2201 registers can be read individually or in block read mode. When two or more bytes are read in block read mode, reserved register addresses are skipped and the next valid address is referenced. If the last valid address has been reached, but the master continues with the block read, the address counter in the ZOPT2201 will not roll over and the ZOPT2201 returns 00<sub>HEX</sub> for every subsequent byte read.

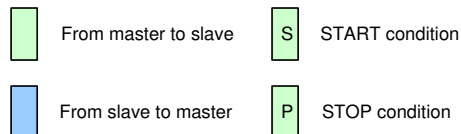
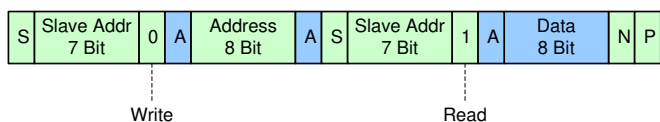
The block read operation is the only way to ensure correct data read out of multi-byte registers and to avoid splitting of results with HIGH and LOW bytes originating from different conversions. During block read access on LS result registers, the result update is blocked.

If a read access is started on an address belonging to a non-readable register, the ZOPT2201 will return NACK until the I<sup>2</sup>C operation is ended.

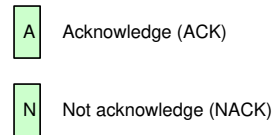
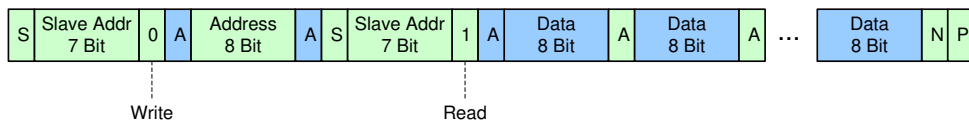
Read operations must follow the timing diagram in Figure 3.6.

**Figure 3.6 I<sup>2</sup>C Register Read**

**Register Read (I<sup>2</sup>C™ Read)**



**Register Block Read (I<sup>2</sup>C™ Read)**



**3.9.3 Register Write**

The ZOPT2201 registers can be written to individually or in block write mode. When two or more bytes are written in block write mode; reserved registers and read-only registers are skipped. The transmitted data is automatically applied to the next writable register. If a register includes read (R) and read/write (RW) bits, the register is not skipped. Data written to read-only bits are ignored.

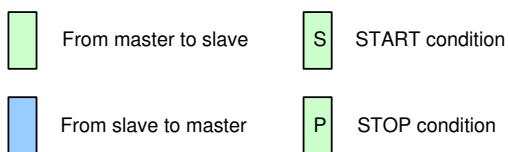
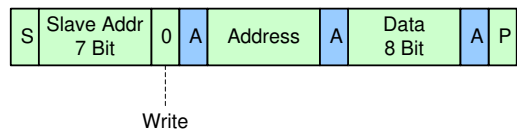
If the last valid address of the ZOPT2201's address range is reached but the master attempts to continue the block write operation, the address counter of the ZOPT2201 will not roll over. The ZOPT2201 will return NACK for every following byte sent by the master until the I<sup>2</sup>C operation is ended.

If a write access is started on an address belonging to a non-writeable register, the ZOPT2201 will return NACK until the I<sup>2</sup>C operation is ended.

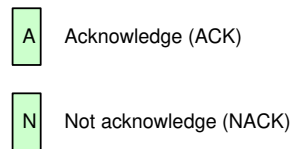
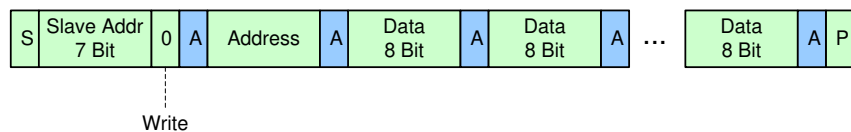
Write operations must follow the timing diagram in Figure 3.7.

**Figure 3.7 I<sup>2</sup>C Register Write**

**Register Write (I<sup>2</sup>C™ Write)**



**Register Block Write (I<sup>2</sup>C™ Write)**





3.9.4 I<sup>2</sup>C Interface—Bus Timing

Figure 3.8 Bus Timing

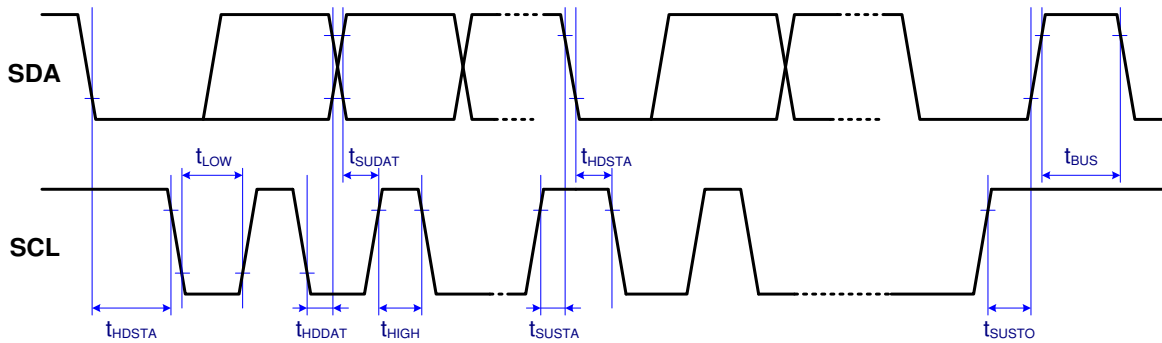


Table 3.9 Bus Timing Characteristic

Parameter	Symbol	Standard Mode	Fast Mode	Units
Maximum SCL clock frequency	$f_{SCL}$	100	400	kHz
Minimum START condition hold time relative to SCL edge	$t_{HDSTA}$	4		$\mu s$
Minimum SCL clock low width	$t_{LOW}$	4.7		$\mu s$
Minimum SCL clock high width	$t_{HIGH}$	4		$\mu s$
Minimum START condition setup time relative to SCL edge	$t_{SUSTA}$	4.7		$\mu s$
Minimum data hold time on SDA relative to SCL edge	$t_{HDDAT}$	0		$\mu s$
Minimum data setup time on SDA relative to SCL edge	$t_{SUDAT}$	0.1	0.1	$\mu s$
Minimum STOP condition setup time on SCL	$t_{SUSTO}$	4		$\mu s$
Minimum bus free time between stop condition and start condition	$t_{BUS}$	4.7		$\mu s$

### 3.10 Summary of Internal Registers

**Table 3.10 Register Overview**

Address	Type	Name	Default Value	Description
00 <sub>HEX</sub>	RW	MAIN_CTRL	00 <sub>HEX</sub>	LS operation mode control, software (SW) reset
04 <sub>HEX</sub>	RW	LS_MEAS_RATE	22 <sub>HEX</sub>	LS measurement rate and resolution in Active Mode
05 <sub>HEX</sub>	RW	LS_GAIN	01 <sub>HEX</sub>	LS analog gain range
06 <sub>HEX</sub>	R	PART_ID	B2 <sub>HEX</sub>	Part number ID and revision ID
07 <sub>HEX</sub>	R	MAIN_STATUS	20 <sub>HEX</sub>	Power-on status, interrupt status, data status
0D <sub>HEX</sub>	R	ALS_DATA_0	00 <sub>HEX</sub>	ALS – ADC measurement data, LSB
0E <sub>HEX</sub>	R	ALS_DATA_1	00 <sub>HEX</sub>	ALS – ADC measurement data
0F <sub>HEX</sub>	R	ALS_DATA_2	00 <sub>HEX</sub>	ALS – ADC measurement data, MSB
10 <sub>HEX</sub>	R	UVB_DATA_0	00 <sub>HEX</sub>	UVBS – ADC measurement data, LSB
11 <sub>HEX</sub>	R	UVB_DATA_1	00 <sub>HEX</sub>	UVBS – ADC measurement data
12 <sub>HEX</sub>	R	UVB_DATA_2	00 <sub>HEX</sub>	UVBS – ADC measurement data, MSB
13 <sub>HEX</sub>	R	UV_COMP_DATA_0	00 <sub>HEX</sub>	UVBS – COMP ADC measurement data, LSB
14 <sub>HEX</sub>	R	UV_COMP_DATA_1	00 <sub>HEX</sub>	UVBS – COMP ADC measurement data
15 <sub>HEX</sub>	R	UV_COMP_DATA_2	00 <sub>HEX</sub>	UVBS – COMP ADC measurement data, MSB
16 <sub>HEX</sub>	R	COMP_DATA_0	00 <sub>HEX</sub>	COMP – ADC measurement data, LSB
17 <sub>HEX</sub>	R	COMP_DATA_1	00 <sub>HEX</sub>	COMP – ADC measurement data
18 <sub>HEX</sub>	R	COMP_DATA_2	00 <sub>HEX</sub>	COMP – ADC measurement data, MSB
19 <sub>HEX</sub>	RW	INT_CFG	10 <sub>HEX</sub>	Interrupt configuration
1A <sub>HEX</sub>	RW	INT_PST	00 <sub>HEX</sub>	Interrupt persist setting
21 <sub>HEX</sub>	RW	LS_THRES_UP_0	FF <sub>HEX</sub>	LS interrupt upper threshold, LSB
22 <sub>HEX</sub>	RW	LS_THRES_UP_1	FF <sub>HEX</sub>	LS interrupt upper threshold, intervening bits
23 <sub>HEX</sub>	RW	LS_THRES_UP_2	0F <sub>HEX</sub>	LS interrupt upper threshold, MSB
24 <sub>HEX</sub>	RW	LS_THRES_LOW_0	00 <sub>HEX</sub>	LS interrupt lower threshold, LSB
25 <sub>HEX</sub>	RW	LS_THRES_LOW_1	00 <sub>HEX</sub>	LS interrupt lower threshold, intervening bits
26 <sub>HEX</sub>	RW	LS_THRES_LOW_2	00 <sub>HEX</sub>	LS interrupt lower threshold, MSB
27 <sub>HEX</sub>	RW	LS_THRES_VAR	00 <sub>HEX</sub>	LS interrupt variance threshold
2F <sub>HEX</sub>	RW	DEVICE_CONFIG	00 <sub>HEX</sub>	Control bit for I <sup>2</sup> C address
30 <sub>HEX</sub>	RW	SPECIAL_MODE_1		Special operation mode register 1
31 <sub>HEX</sub>	RW	SPECIAL_MODE_2		Special operation mode register 2

### 3.11 Detailed Description of Registers

#### 3.11.1 MAIN\_CTRL

Address 00<sub>HEX</sub>  
 Default value 00<sub>HEX</sub>  
 Register access RW

Bit	7	6	5	4	3	2	1	0
00 <sub>HEX</sub>	0	0	0	SW reset	LS_Mode	RawMode_SEL	LS_EN	0

Bit[4] *SW reset*: If bit is set to 1, a software reset will be triggered.

Bit[3] *LS\_Mode*: This bit is only checked if LS\_EN is active.

0 (default)	ALS Mode:	ALS + COMP channels activated, UVB and UV_COMP channels deactivated
1	UVBS Mode:	UVB + UV_COMP channels activated, ALS and COMP channels deactivated Mode takes precedence over other operation modes

Bit[2] *RawMode\_SEL*: This bit is only checked if LS\_EN is active.

0 (default)	ALS Mode:	ALS + COMP channels activated, UVBS and UV_COMP channels deactivated
1	ALS/UVBS Raw_Mode:	ALS, UVB, UV_COMP, and COMP channels activated. (Further actions are needed; see Table 3.3 for details.)

Bit[1] *LS\_EN*

1	Light sensor active
0 (default)	Light sensor standby

Bit[0] Reserved

Writing to this register stops the ongoing measurements and starts new measurements (depending on the respective enable bits).

### 3.11.2 LS\_MEAS\_RATE

Address 04<sub>HEX</sub>  
 Default value 22<sub>HEX</sub>  
 Register access RW

Bit	7	6	5	4	3	2	1	0
04 <sub>HEX</sub>	0	LS Resolution / Bit Width			0	LS Measurement Rate		

Bit[6:4] *Light Sensor Resolution/ Bit Width*. The resolution selected via this register will have an effect on the measurement time and the accuracy of the measurement:

000 <sub>BIN</sub>	20-bit; 400ms
001 <sub>BIN</sub>	19-bit; 200ms
010 <sub>BIN</sub>	18-bit; 100ms <b>(default)</b>
011 <sub>BIN</sub>	17-bit; 50ms
100 <sub>BIN</sub>	16-bit; 25ms
101 <sub>BIN</sub>	13-bit; 3.125ms
110 <sub>BIN</sub>	Reserved
111 <sub>BIN</sub>	Reserved

Bit[2:0] *LS Measurement Rate*. This bit field controls the timing of the periodic measurements of the light sensor in Active Mode.

000 <sub>BIN</sub>	25ms
001 <sub>BIN</sub>	50ms
010 <sub>BIN</sub>	100ms <b>(default)</b>
011 <sub>BIN</sub>	200ms
100 <sub>BIN</sub>	500ms
101 <sub>BIN</sub>	1000ms
110 <sub>BIN</sub>	2000ms
111 <sub>BIN</sub>	2000ms



**Note:** When the measurement repeat rate is programmed to be faster than possible for the specified ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register stops the ongoing measurements and starts new measurements (depending on the respective enable bits).

### 3.11.3 LS\_GAIN

Address 05<sub>HEX</sub>  
 Default value 01<sub>HEX</sub>  
 Register access RW

Bit	7	6	5	4	3	2	1	0
05 <sub>HEX</sub>	0	0	0	0	0	LS Gain Range		

Note: The following ALS / UVBS detection ranges apply to the default resolution of 18-bit (measurement time = 100ms); see Table 3.5 and Table 3.6 respectively for details.

#### LS Detection Ranges

ALS Mode:

Bit[2:0]	ALS (temperature compensated):		
000 <sub>BIN</sub>	Gain: 1		0.6 to 157286 lux
001 <sub>BIN</sub>	Gain: 3		0.2 to 52429 lux ( <b>default</b> )
010 <sub>BIN</sub>	Gain: 6		0.1 to 26214 lux
011 <sub>BIN</sub>	Gain: 9		0.0667 to 17476 lux
100 <sub>BIN</sub>	Gain: 18		0.0333 to 8738 lux

UVBS Mode:

Bit[2:0]	UVBS (temperature compensated):		
000 <sub>BIN</sub>	Gain: 1		1.44 to 377487 $\mu\text{W}/\text{cm}^2$
001 <sub>BIN</sub>	Gain: 3		0.48 to 125829 $\mu\text{W}/\text{cm}^2$ ( <b>default</b> )
010 <sub>BIN</sub>	Gain: 6		0.24 to 62915 $\mu\text{W}/\text{cm}^2$
011 <sub>BIN</sub>	Gain: 9		0.16 to 41943 $\mu\text{W}/\text{cm}^2$
100 <sub>BIN</sub>	Gain: 18		0.08 to 20972 $\mu\text{W}/\text{cm}^2$ ( <b>recommended for application</b> )

Writing to this register stops the ongoing measurements and starts new measurements (depending on the respective enable bits).

### 3.11.4 PART\_ID

Address 06<sub>HEX</sub>  
 Default value B2<sub>HEX</sub>  
 Register access R

Bit	7	6	5	4	3	2	1	0
06 <sub>HEX</sub>	Part Number ID				Revision ID			

Bit[7:4] *Part Number ID*  
 Bit[3:0] *Revision ID* of the component. The value increases by one each time a new silicon revision is manufactured

### 3.11.5 MAIN\_STATUS

Address 07<sub>HEX</sub>  
 Default value 20<sub>HEX</sub>  
 Register access R

Bit	7	6	5	4	3	2	1	0
07 <sub>HEX</sub>	0	0	Power-On status	LS interrupt status	LS data status	0	0	0

Bit[5] *Power-On status*. If set to 1, the part has had a power-up event, either because the part was turned on or because there was a power-supply voltage disturbance

**A value of 1 is the default for the first register read after power-on reset.**

**Note:** All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if the *Power-On status* flag is set. In the event of a power-up event while in the ALS/UVBS\_Raw Mode, this special operation mode is turned off. To restore this mode, the initialization sequence described in Table 3.3 must be repeated before the mode can be reactivated.

**The flag is cleared after the register is read.**

Bit[4] *LS interrupt status* (updated even if the interrupt pin is disabled)  
 0 interrupt condition has not occurred (**default**)  
 1 interrupt condition has occurred (cleared after read)

Bit[3] *LS data status*  
 0 old data, already read (**default**)  
 1 new data, not yet read (cleared after read)

Bit[2:0] Reserved

### 3.11.6 ALS\_DATA

Address                0D<sub>HEX</sub> and 0E<sub>HEX</sub> and 0F<sub>HEX</sub>  
 Default value        00<sub>HEX</sub> and 00<sub>HEX</sub> and 00<sub>HEX</sub>  
 Register access      R

Bit	7	6	5	4	3	2	1	0
0D <sub>HEX</sub>	ALS_DATA_0[7:0]							
0E <sub>HEX</sub>	ALS_DATA_1[15:8]							
0F <sub>HEX</sub>	0	0	0	0	ALS_DATA_2[19:16]			

ALS channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

Register data is already temperature compensated. See Table 3.3 for details.

When an I<sup>2</sup>C read operation is active and points to an address in the range 07<sub>HEX</sub> to 18<sub>HEX</sub>, all registers in this range are locked until the I<sup>2</sup>C read operation is completed or this address range is left.

This guarantees that the data in the registers belongs to the same measurement cycle. New measurement data is stored into temporary registers and the actual \*\_DATA registers are updated as soon as there is no on-going I<sup>2</sup>C read operation to the address range 07<sub>HEX</sub> to 18<sub>HEX</sub>.

Register 0D <sub>HEX</sub>	Bit[7:0]	ALS diode data least significant data byte
Register 0E <sub>HEX</sub>	Bit[7:0]	ALS diode data intervening data byte
Register 0F <sub>HEX</sub>	Bit[3:0]	ALS diode data most significant data byte

### 3.11.7 UVB\_DATA

Address 10<sub>HEX</sub> and 11<sub>HEX</sub> and 12<sub>HEX</sub>  
 Default value 00<sub>HEX</sub> and 00<sub>HEX</sub> and 00<sub>HEX</sub>  
 Register access R

Bit	7	6	5	4	3	2	1	0
10 <sub>HEX</sub>	UVB_DATA_0[7:0]							
11 <sub>HEX</sub>	UVB_DATA_1[15:8]							
12 <sub>HEX</sub>	0	0	0	0	UVB_DATA_2[19:16]			

UVB channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

Register data is already temperature compensated. See Table 3.3 for details.

When an I<sup>2</sup>C read operation is active and points to an address in the range 07<sub>HEX</sub> to 18<sub>HEX</sub>, all registers in this range are locked until the I<sup>2</sup>C read operation is completed or this address range is left.

This guarantees that the data in the registers belongs to the same measurement cycle. New measurement data is stored into temporary registers and the actual \*\_DATA registers are updated as soon as there is no on-going I<sup>2</sup>C read operation to the address range 07<sub>HEX</sub> to 18<sub>HEX</sub>.

Register 10<sub>HEX</sub> Bit[7:0] UVB diode data least significant data byte  
 Register 11<sub>HEX</sub> Bit[7:0] UVB diode data intervening data byte  
 Register 12<sub>HEX</sub> Bit[3:0] UVB diode data most significant data byte



### 3.11.8 UV\_COMP\_DATA

Address                    13<sub>HEX</sub> and 14<sub>HEX</sub> and 15<sub>HEX</sub>  
 Default value            00<sub>HEX</sub> and 00<sub>HEX</sub> and 00<sub>HEX</sub>  
 Register access         R

Bit	7	6	5	4	3	2	1	0
13 <sub>HEX</sub>	UV_COMP_DATA_0[7:0]							
14 <sub>HEX</sub>	UV_COMP_DATA_1[15:8]							
15 <sub>HEX</sub>	0	0	0	0	UV_COMP_DATA_2[19:16]			

UVBS compensation (UV\_COMP) channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

Register carries UVBS temperature compensation data. See Table 3.3 for details.

When an I<sup>2</sup>C read operation is active and points to an address in the range 07<sub>HEX</sub> to 18<sub>HEX</sub>, all registers in this range are locked until the I<sup>2</sup>C read operation is completed or this address range is left.

This guarantees that the data in the registers belongs to the same measurement cycle. New measurement data is stored into temporary registers and the actual \*\_DATA registers are updated as soon as there is no on-going I<sup>2</sup>C read operation to the address range 07<sub>HEX</sub> to 18<sub>HEX</sub>.

Register 13 <sub>HEX</sub>	Bit[7:0]	UV_COMP diode data least significant data byte
Register 14 <sub>HEX</sub>	Bit[7:0]	UV_COMP diode data intervening data byte
Register 15 <sub>HEX</sub>	Bit[3:0]	UV_COMP diode data most significant data byte

### 3.11.9 COMP\_DATA

Address                16<sub>HEX</sub> and 17<sub>HEX</sub> and 18<sub>HEX</sub>  
 Default value        00<sub>HEX</sub> and 00<sub>HEX</sub> and 00<sub>HEX</sub>  
 Register access      R

Bit	7	6	5	4	3	2	1	0
16 <sub>HEX</sub>	COMP_DATA_0[7:0]							
17 <sub>HEX</sub>	COMP_DATA_1[15:8]							
18 <sub>HEX</sub>	0	0	0	0	COMP_DATA_2[19:16]			

ALS compensation channel (COMP) digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

Register carries ALS temperature compensation data. See Table 3.3 for details.

When an I<sup>2</sup>C read operation is active and points to an address in the range 07<sub>HEX</sub> to 18<sub>HEX</sub>, all registers in this range are locked until the I<sup>2</sup>C read operation is completed or this address range is left.

This guarantees that the data in the registers belongs to the same measurement cycle. New measurement data is stored into temporary registers and the actual \*\_DATA registers are updated as soon as there is no on-going I<sup>2</sup>C read operation to the address range 07<sub>HEX</sub> to 18<sub>HEX</sub>.

Register 16 <sub>HEX</sub>	Bit[7:0]	COMP diode data least significant data byte
Register 17 <sub>HEX</sub>	Bit[7:0]	COMP diode data intervening data byte
Register 18 <sub>HEX</sub>	Bit[3:0]	COMP diode data most significant data byte

### 3.11.10 INT\_CFG

Address 19<sub>HEX</sub>  
 Default value 10<sub>HEX</sub>  
 Register access RW

Bit	7	6	[5:4]	3	2	1	0
19 <sub>HEX</sub>	0	0	LS_INT_SEL	LS_VAR_MODE	LS_INT_EN	0	0

Bit[5:4] *LS\_INT\_SEL* Light sensor (LS) interrupt source select  
 00 Reserved  
 01 ALS channel (**default**)  
 10 Reserved  
 11 UVB channel

Bit[3] *LS\_VAR\_MODE* Light sensor variation interrupt mode  
 0 LS Threshold Interrupt Mode (**default**)  
 1 LS Variation Interrupt Mode

Bit[2] *LS\_INT\_EN* Light sensor interrupt enable  
 0 LS interrupt disabled (**default**)  
 1 LS interrupt enabled

### 3.11.11 INT\_PST

Address 1A<sub>HEX</sub>  
 Default value 00<sub>HEX</sub>  
 Register access RW

Bit	7	6	5	4	3	2	1	0
1A <sub>HEX</sub>	LS_PERSIST				0	0	0	0

Bit[7:4] *LS\_PERSIST* sets the number of similar consecutive LS interrupt events that must occur before the interrupt is asserted.  
 0000<sub>BIN</sub> Every LS value out of threshold range asserts an interrupt (**default**).  
 0001<sub>BIN</sub> 2 consecutive LS values out of threshold range assert an interrupt.  
 ...  
 1111<sub>BIN</sub> 16 consecutive LS values out of threshold range assert an interrupt.

Bit[3:0] Reserved.

### 3.11.12 LS\_THRES\_UP

Address 21<sub>HEX</sub> and 22<sub>HEX</sub> and 23<sub>HEX</sub>  
 Default value FF<sub>HEX</sub> and FF<sub>HEX</sub> and 0F<sub>HEX</sub>  
 Register access RW

Bit	7	6	5	4	3	2	1	0
21 <sub>HEX</sub>	LS_THRES_UP_0							
22 <sub>HEX</sub>	LS_THRES_UP_1							
23 <sub>HEX</sub>	0	0	0	0	LS_THRES_UP_2			

LS\_THRES\_UP\_x sets the upper threshold value for the LS interrupt. The interrupt controller compares the value in LS\_THRES\_UP\_x against the measured data in the \*\_DATA\_x registers of the selected LS interrupt channel. It generates an interrupt event if \*\_DATA\_x exceeds the threshold level.

The data format for LS\_THRES\_UP\_x must match that of the \*\_DATA\_x registers.

Register 21<sub>HEX</sub> Bit[7:0] LS upper interrupt threshold value, LSB  
 Register 22<sub>HEX</sub> Bit[7:0] LS upper interrupt threshold value, intervening byte  
 Register 23<sub>HEX</sub> Bit[3:0] LS upper interrupt threshold value, MSB

### 3.11.13 LS\_THRES\_LOW

Address 24<sub>HEX</sub> and 25<sub>HEX</sub> and 26<sub>HEX</sub>  
 Default value 00<sub>HEX</sub> and 00<sub>HEX</sub> and 00<sub>HEX</sub>  
 Register access RW

Bit	7	6	5	4	3	2	1	0
24 <sub>HEX</sub>	LS_THRES_LOW_0							
25 <sub>HEX</sub>	LS_THRES_LOW_1							
26 <sub>HEX</sub>	0	0	0	0	LS_THRES_LOW_2			

LS\_THRES\_LOW\_x sets the lower threshold value for the LS interrupt. The interrupt controller compares the value in LS\_THRES\_LOW\_x against the measured data in the \*\_DATA\_x registers of the selected LS interrupt channel. It generates an interrupt event if the \*\_DATA\_x is below the threshold level.

The data format for LS\_THRES\_LOW\_x must match that of the \*\_DATA\_x registers.

Register 24<sub>HEX</sub> Bit[7:0] LS lower interrupt threshold value, LSB  
 Register 25<sub>HEX</sub> Bit[7:0] LS lower interrupt threshold value, intervening byte  
 Register 26<sub>HEX</sub> Bit[3:0] LS lower interrupt threshold value, MSB

**3.11.14 LS\_THRES\_VAR**

Address 27<sub>HEX</sub>  
 Default value 00<sub>HEX</sub>  
 Register access RW

Bit	7	6	5	4	3	2	1	0
27 <sub>HEX</sub>	0	0	0	0	0	LS_THRES_VAR		

Bit[2:1] LS variance threshold

Code	Interrupt generated when
000 <sub>BIN</sub>	new DATA_x varies by <b>8 counts</b> compared to previous result ( <b>default</b> )
001 <sub>BIN</sub>	new DATA_x varies by <b>16 counts</b> compared to previous result
010 <sub>BIN</sub>	new DATA_x varies by <b>32 counts</b> compared to previous result
011 <sub>BIN</sub>	new DATA_x varies by <b>64 counts</b> compared to previous result
100 <sub>BIN</sub>	new DATA_x varies by <b>128 counts</b> compared to previous result
101 <sub>BIN</sub>	new DATA_x varies by <b>256 counts</b> compared to previous result
110 <sub>BIN</sub>	new DATA_x varies by <b>512 counts</b> compared to previous result
111 <sub>BIN</sub>	new DATA_x varies by <b>1024 counts</b> compared to previous result

**3.11.15 DEVICE\_CONFIG**

Address            2F<sub>HEX</sub>  
 Default value    00<sub>HEX</sub>  
 Register access   RW

Bit	7	6	5	4	3	2	1	0
2F <sub>HEX</sub>	0	0	0	0	Reserved	Reserved	I <sup>2</sup> C Address	Reserved

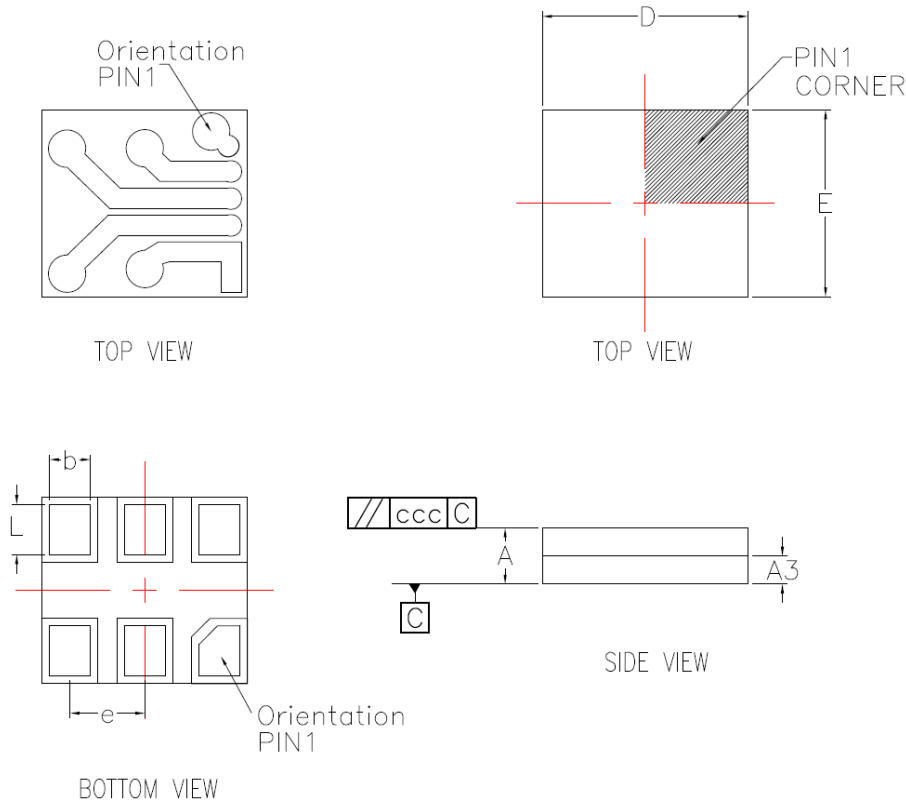
Bit[1]            I<sup>2</sup>C address

0 (default)	7-bit format (no R/W bit consideration):	53 <sub>HEX</sub>
	8-bit format (with R/W bit consideration):	A6 <sub>HEX</sub> / A7 <sub>HEX</sub>
1	7-bit format (no R/W bit consideration):	52 <sub>HEX</sub>
	8-bit format (with R/W bit consideration):	A4 <sub>HEX</sub> / A5 <sub>HEX</sub>

## 4. Packages

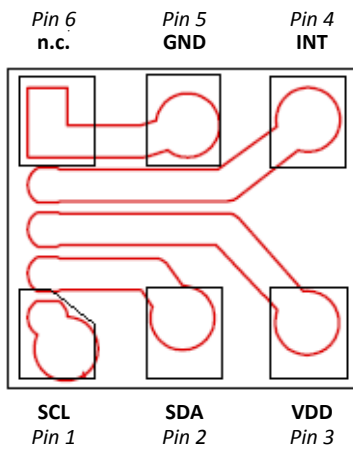
### 4.1 LGA6 Package (2.0 × 2.2 × 0.7 mm)

#### 4.1.1 Mechanical Dimensions

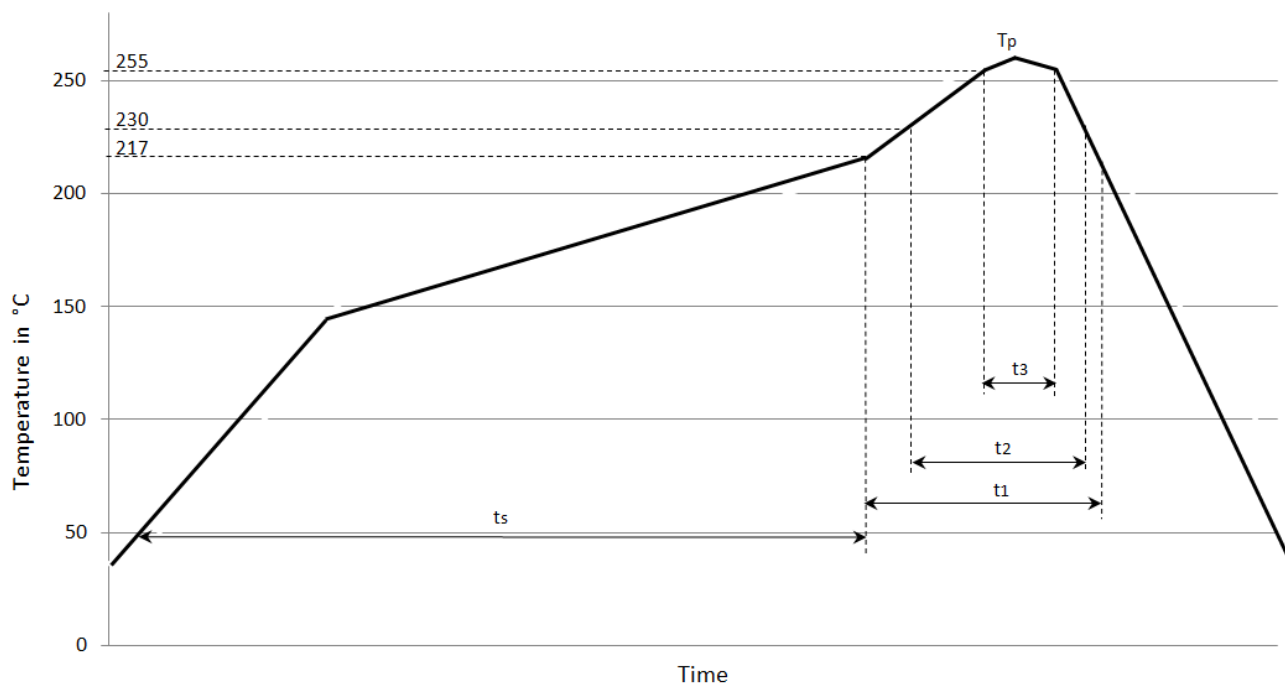


SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	0.65	0.70	0.75
A3	0.35	0.40	0.45
b	0.39	0.44	0.49
L	0.49	0.54	0.59
D	2.10	2.20	2.30
E	1.90	2.00	2.10
e	0.80 BSC		
ccc	0.01		

#### 4.1.2 Pin Assignment (Top View)



### 4.1.3 Reflow Profile

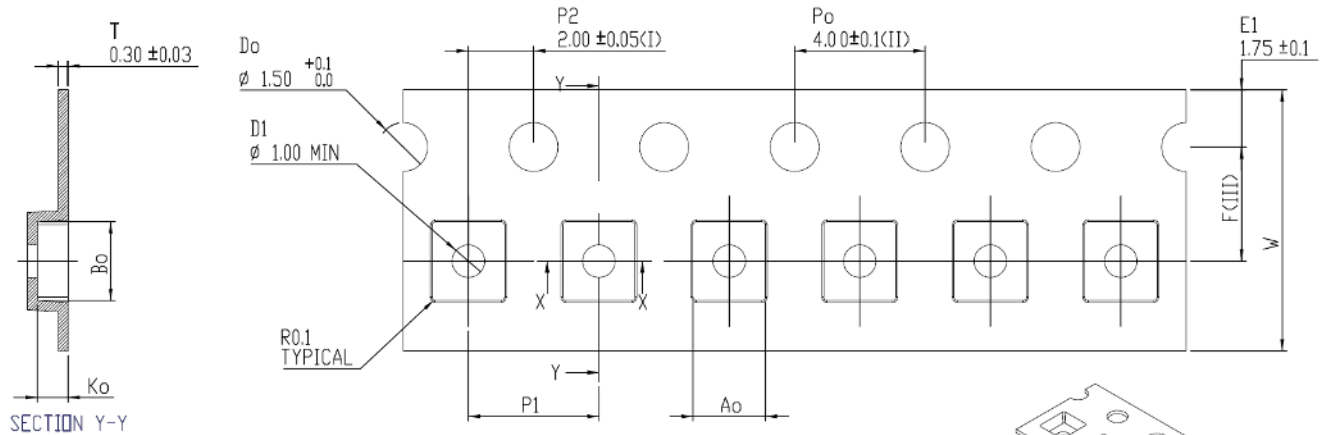


**Table 4.1 Reflow Profile Specification**

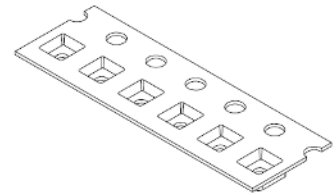
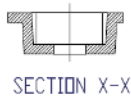
Parameter	Legend	Component
Time above 217°C	$t_1$	$\leq 60$ sec
Time above 230°C	$t_2$	$\leq 50$ sec
Time above 255°C	$t_3$	$\leq 15$ sec
Peak Temp	$T_p$	$\leq 260^\circ\text{C}$
Soak Time (50°C – 217°C)	$t_s$	$\leq 180$ sec
Temperature Gradient Preheating		$< 3$ °C/sec
Temperature Gradient Cooling		$< 5$ °C/sec



4.1.4 Tape Packaging Information



Ao	2.22 +/- 0.1
Bo	2.42 +/- 0.1
Ko	0.95 +/- 0.1
F	3.50 +/- 0.05
P1	4.00 +/- 0.1
W	8.00 +0.3/-0.1



NOTES : (UNLESS OTHERWISE SPECIFIED)

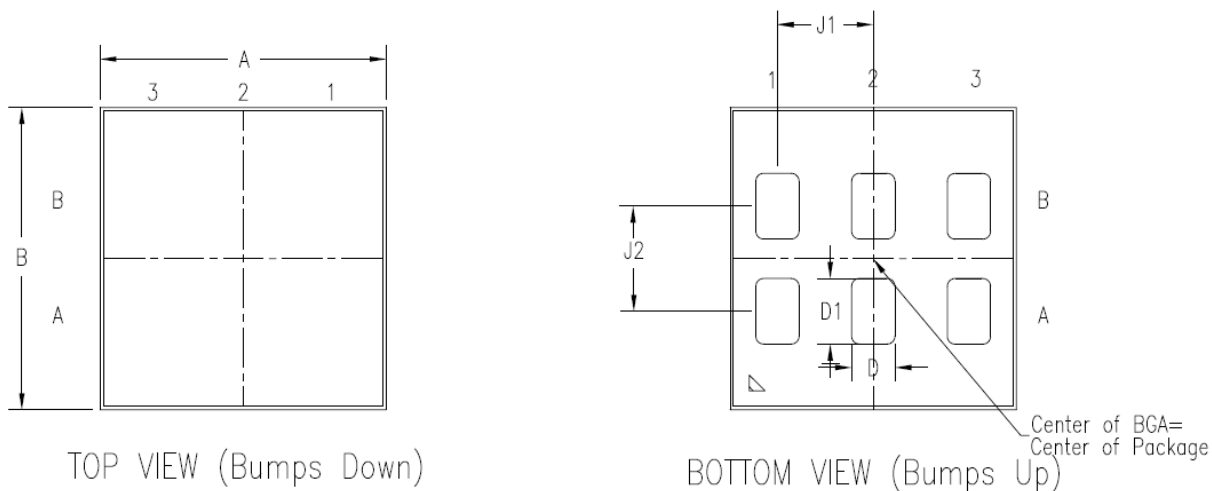
1. SUPPLIER : C-PAK
2. SUPPLIER PART NUMBER : DDFN-2x2.2x0.7 (EM1089-16)
3. Po 10 PITCHES CUMULATIVE TOLERANCE ON TAPE : ±0.20 mm
4. REFER TO MSA-3018 FOR THE ALLOWABLE CAMBER REQUIREMENT.
5. MATERIAL : BLACK CONDUCTIVE POLYSTYRENE.
6. Ao AND Bo MEASURED FROM THE BOTTOM OF THE POCKET.
7. Ko MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER.
8. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
9. POCKET CENTER AND POCKET HOLE CENTER MUST BE SAME POSITION.
10. REFER TO MAA-3092 & MSA-3018 FOR THE IDT STANDARD REQUIREMENT FOR CARRIER TAPE.
11. ALL THE DIMENSIONS ARE IN MILLIMETERS (MM).
12. LENGTH PER ROLL = 500 METERS.
13. ALLOWABLE CAMBER TO BE 2/250 MM MAXIMUM.

## 4.2 TSV Package (1.1 × 1.2 × 0.26 mm)

### 4.2.1 Mechanical Dimensions

Note: In the following mechanical diagram, the symbol N refers to the number of pins, N1 refers to the number of pin columns, and N2 refers to the number of rows.

Mechanical Diagram



SYMBOL	PACKAGE DIMENSIONS		
	MIN	NOM	MAX
A	1065	1090	1115
B	1125	1150	1175
C	203	263	323
C1	5	10	15
C2	218	263	308
C3	125	145	165
D	135	165	195
D1	250	280	310
N	6 (INC)		
N1	3		
N2	2		
J1		365	
J2		400	

**NOTE:**

1. DIMENSIONS in  $\mu\text{m}$ .
2. The thickness of Bond-1 glass is 100  $\mu\text{m}$  (green glass x 1pcs).
3. The material of solder printing is SAC305.

## 5. Part Order Information

Product Sales Code	Description	Delivery Package
ZOPT2201AC5R	ZOPT2201 LGA6 – Temperature range: -40 to +90°C	Reel
ZOPT2201AC9R	ZOPT2201 TSV – Temperature range: -40 to +90°C	Reel
ZOPT2201KIT V1.0	ZOPT2201 Evaluation Kit, including ZOPT Control Board, mini-USB cable, and 1 ZOPT2201 sample mounted on the LGA6 Sensor Board; kit software is available for free download – see the <i>ZOPT Evaluation Kit Quick Start Guide</i> included in the kit for instructions.	

## 6. Glossary

Term	Description
ADC	Analog-to-Digital Converter
ALS	Ambient Light Sensor
LGA	Land-Grid Array (package type)
LS	Light Sensor (can be either ALS or UVBS depending on the ZOPT2201 configuration)
NVM	Non-volatile Memory
SDA	Serial Data
SCL	Serial Clock
SW	Software
TSV	Through-Silicon Vias (package type)
UVBS	UVB Energy Sensor

## 7. Document Revision History

Revision Date	Description
September 2, 2016	<ul style="list-style-type: none"> <li>▪ Update for UVBS sensitivity.</li> <li>▪ Addition of ALS/UVBS_Raw Mode as described in sections 3.4, 3.6, and 3.11.1; addition of ALS/UVBS_Raw Mode current consumption specifications in section 1.3.</li> <li>▪ Updates for Figure 3.3 and Figure 3.5.</li> <li>▪ Revision of name for bit 3 in the MAIN_CTRL register from <i>UVBS_Mode</i> to <i>LS_Mode</i>.</li> <li>▪ Addition of new package type TSV and TSV package information (see new section 4.2).</li> <li>▪ Addition of reflow profile for LGA6 package.</li> <li>▪ Update for “Mechanical Dimensions” drawing for LGA6.</li> <li>▪ Added new section 4.1.4 for tape packaging information.</li> <li>▪ Minor edits for clarity and formatting.</li> </ul>
April 4, 2016	Rebranding for IDT. Revision number is replaced by release date.
March 7, 2016 (Revision 1.00)	First release.

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