MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Low Supply Voltage Range: 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption**
  - **Active Mode: 220 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.5 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Five Power-Saving Modes**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies**
  - **Internal Very-Low-Power Low-Frequency (LF) Oscillator**
  - **32-kHz Crystal** (1)
  - **External Digital Clock Source**
- **One 16-Bit Timer_A With Three Capture/Compare Registers**
- **Up to 16 Touch-Sense Enabled I/O Pins**
- **Universal Serial Interface (USI) Supporting SPI and I2C (see Table 1)**
- **10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan (see Table 1)**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Logic With Spy-Bi-Wire Interface**
- **Family Members are Summarized in Table 1**
- **Package Options**
  - **TSSOP: 20 Pin**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Extended (–40°C to 125°C) Temperature Range** (2)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Crystal oscillator cannot be operated beyond 105°C

(2) Custom temperature ranges available

DESCRIPTION

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G2332 series of microcontrollers are ultra-low-power mixed signal microcontrollers with built-in 16-bit timers, and up to 16 I/O touch sense enabled pins and built-in communication capability using the universal serial communication interface. The MSP430G2332 series have a 10-bit A/D converter. For configuration details, see Table 1. Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

Table 1. Available Options

Device	EEM	Flash (kB)	RAM (B)	Timer_A	ADC10 Channel	USI	CLOCK	I/O	Package Type
MSP430G2332QPW2EP	1	4	256	1x TA3	8	1	LF, DCO, VLO	16	20-TSSOP

Table 2. ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER		TOP-SIDE MARKING	VID NUMBER
–40°C to 125°C	TSSOP - PW	MSP430G2332QPW2REP	Tape and Reel, 2000	G2332EP	V62/12625-01XE
		MSP430G2332QPW2EP	Tube, 70		V62/12625-01XE-T

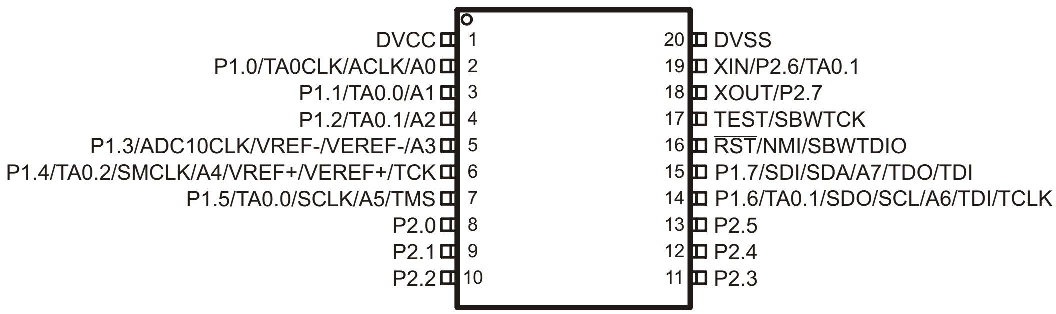
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

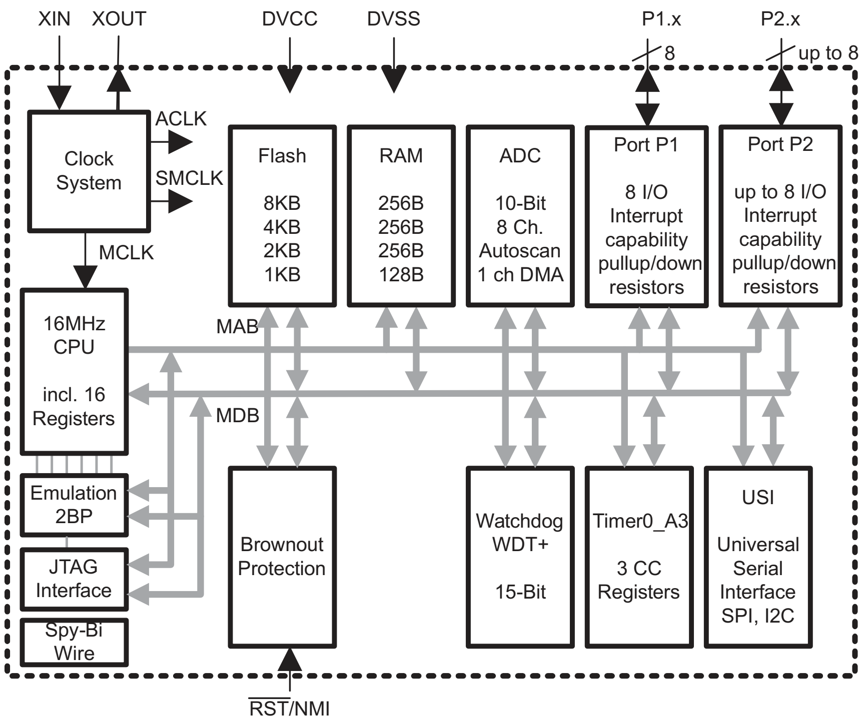
DEVICE PINOUTS

PW PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAMS

Functional Block Diagram



NOTE: Port P2: Two pins are available on the 14-pin package option. Eight pins are available on the 20-pin package option.

TERMINAL FUNCTIONS

Table 3. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO. PW20		
P1.0/ TA0CLK/ ACLK/ A0	2	I/O	General-purpose digital I/O pin Timer0_A, clock signal TACLK input ACLK signal output ADC10 analog input A0
P1.1/ TA0.0/ A1	3	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI0A input, compare: Out0 output ADC10 analog input A1
P1.2/ TA0.1/ A2	4	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI1A input, compare: Out1 output ADC10 analog input A2
P1.3/ ADC10CLK/ A3/ VREF-/VEREF	5	I/O	General-purpose digital I/O pin ADC10, conversion clock output ADC10 analog input A3 ADC10 negative reference voltage
P1.4/ TA0.2/ SMCLK/ A4/ VREF+/VEREF+/ TCK	6	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI2A input, compare: Out2 output SMCLK signal output ADC10 analog input A4 ADC10 positive reference voltage JTAG test clock, input terminal for device programming and test
P1.5/ TA0.0/ A5/ SCLK/ TMS	7	I/O	General-purpose digital I/O pin Timer0_A, compare: Out0 output ADC10 analog input A5 USI: clk input in I2C mode; clk in/output in SPI mode JTAG test mode select, input terminal for device programming and test
P1.6/ TA0.1/ A6/ SDO/ SCL/ TDI/ TCLK	14	I/O	General-purpose digital I/O pin Timer0_A, compare: Out1 output ADC10 analog input A6 USI: Data output in SPI mode USI: I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/ A7/ SDI/ SDA/ TDO/TDI [1]	15	I/O	General-purpose digital I/O pin ADC10 analog input A7 USI: Data input in SPI mode USI: I2C data in I2C mode JTAG test data output terminal or test data input during programming and test
P2.0	8	I/O	General-purpose digital I/O pin
P2.1	9	I/O	General-purpose digital I/O pin
P2.2	10	I/O	General-purpose digital I/O pin
P2.3	11	I/O	General-purpose digital I/O pin
P2.4	12	I/O	General-purpose digital I/O pin
P2.5	13	I/O	General-purpose digital I/O pin

(1) TDO or TDI is selected via JTAG instruction.

Table 3. Terminal Functions (continued)

TERMINAL NAME	NO. PW20	I/O	DESCRIPTION
XIN/ P2.6/ TA0.1	19	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer0_A, compare: Out1 output
XOUT/ P2.7	18	I/O	Output terminal of crystal oscillator(2) General-purpose digital I/O pin
$\overline{\text{RST}}$/ NMI/ SBWTDIO/	16	I	Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	17	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DVCC	1	NA	Supply voltage
AVCC	NA	NA	Supply voltage
DVSS	20	NA	Ground reference
AVSS	NA	NA	Ground reference
NC	-	NA	Not connected
QFN Pad	-	NA	QFN package pad connection to VSS recommended.

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

SHORT-FORM DESCRIPTION

CPU

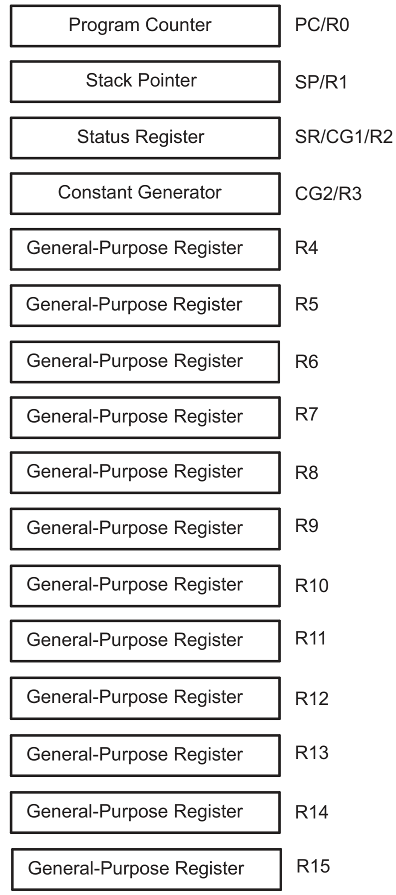
The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 4 shows examples of the three types of instruction formats; Table 5 shows the address modes.

Table 4. Instruction Word Formats

FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 5. Address Mode Descriptions(1)

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source, D = destination

Operating Modes

The MSP430 devices have one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, if flash is not programmed) the CPU goes into LPM4 immediately after power-up.

Table 6. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
			0FFFAh	29
			0FFF8h	28
			0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TACCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TACCR2 TACCR1 CCIFG. TAIFGTable 4(4)	maskable	0FFF0h	24
			0FFEEh	23
			0FFECh	22
ADC10	ADC10IFG(4)	maskable	0FFEAh	21
USI	USIIFG, USISTTIFG(2)(4)	maskable	0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (5)			0FFDEh to 0FFC0h	15 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
	(shaded)	SFR bit is not present in device.

Table 7. Interrupt Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
00h			**ACCVIE**	**NMIIE**			**OFIE**	**WDTIE**
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE Oscillator fault interrupt enable

NMIIE (Non)maskable interrupt enable

ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

Table 8. Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				**NMIIFG**	**RSTIFG**	**PORIFG**	**OFIFG**	**WDTIFG**
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault.

PORIFG Power-On Reset interrupt flag. Set on V_{CC} power-up.

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.

NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h								

Memory Organization

Table 9. Memory Organization

		MSP430G2332
Memory	Size	4kB
Main: interrupt vector	Flash	0xFFFF to 0xFFC0
Main: code memory	Flash	0xFFFF to 0xF000
Information memory	Size	256 Byte
	Flash	010FFh to 01000h
RAM	Size	256 B
		0x02FF to 0x0200
Peripherals	16-bit	01FFh to 0100h
	8-bit	0FFh to 010h
	8-bit SFR	0Fh to 00h

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

Calibration Data Stored in Information Memory Segment A

Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value structure.

Table 10. Tags Used by the ADC Calibration Tags

NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at V_{CC} = 3 V and T_A = 30°C at calibration
TAG_ADC10_1	0x10DA	0x10	ADC10_1 calibration tag
TAG_EMPTY	-	0xFE	Identifier for empty memory areas

Table 11. Labels Used by the ADC Calibration Tags

LABEL	CONDITION AT CALIBRATION / DESCRIPTION	SIZE	ADDRESS OFFSET
CAL_ADC_25T85	INCHx = 0x1010, REF2_5 = 1, T_A = 85°C	word	0x0010
CAL_ADC_25T30	INCHx = 0x1010, REF2_5 = 1, T_A = 30°C	word	0x000E
CAL_ADC_25VREF_FACTOR	REF2_5 = 1, T_A = 30°C, $I_{(VREF+)}$ = 1 mA	word	0x000C
CAL_ADC_15T85	INCHx = 0x1010, REF2_5 = 0, T_A = 85°C	word	0x000A
CAL_ADC_15T30	INCHx = 0x1010, REF2_5 = 0, T_A = 30°C	word	0x0008
CAL_ADC_15VREF_FACTOR	REF2_5 = 0, T_A = 30°C, $I_{(VREF+)}$ = 0.5 mA	word	0x0006
CAL_ADC_OFFSET	External VREF = 1.5 V, $f_{(ADC10CLK)}$ = 5 MHz	word	0x0004
CAL_ADC_GAIN_FACTOR	External VREF = 1.5 V, $f_{(ADC10CLK)}$ = 5 MHz	word	0x0002
CAL_BC1_1MHz	-	byte	0x0009
CAL_DCO_1MHz	-	byte	0x00008
CAL_BC1_8MHz	-	byte	0x0007
CAL_DCO_8MHz	-	byte	0x0006
CAL_BC1_12MHz	-	byte	0x0005
CAL_DCO_12MHz	-	byte	0x0004
CAL_BC1_16MHz	-	byte	0x0003
CAL_DCO_16MHz	-	byte	0x0002

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There are two 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition(port P1 and port P2 only) is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and port P2, if available.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.
- Each I/O has an individually programmable pin-oscillator enable bit to enable low-cost touch sensing.

WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer0_A3

Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. Timer0_A3 Signal Connections(1)

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
PW20					PW20
P1.0-2	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
PinOsc		INCLK			
P1.1-3	TA0.0	CCI0A	CCR0	TA0	P1.1-3
	ACLK	CCI0B			P1.5-7
	V_{SS}	GND			
	V_{CC}	V_{CC}			
P1.2-4	TA0.1	CCI1A	CCR1	TA1	P1.2-4
	CAOUT	CCI1B			P1.6-14
	V_{SS}	GND			P2.6-19
	V_{CC}	V_{CC}			
P1.4-6	TA0.2	CCI2A	CCR2	TA2	P1.4-6
PinOsc	TA0.2	CCI2B			
	V_{SS}	GND			
	V_{CC}	V_{CC}			

(1) Only one pin-oscillator must be enabled at a time.

USI

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

Peripheral File Map

Table 13. Peripherals With Word Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
ADC10	ADC data transfer start address	ADC10SA	01BCh
	ADC memory	ADC10MEM	01B4h
	ADC control register 1	ADC10CTL1	01B2h
	ADC control register 0	ADC10CTL0	01B0h
Timer0_A3	Capture/compare register	TACCR2	0176h
	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control	TACCTL2	0166h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

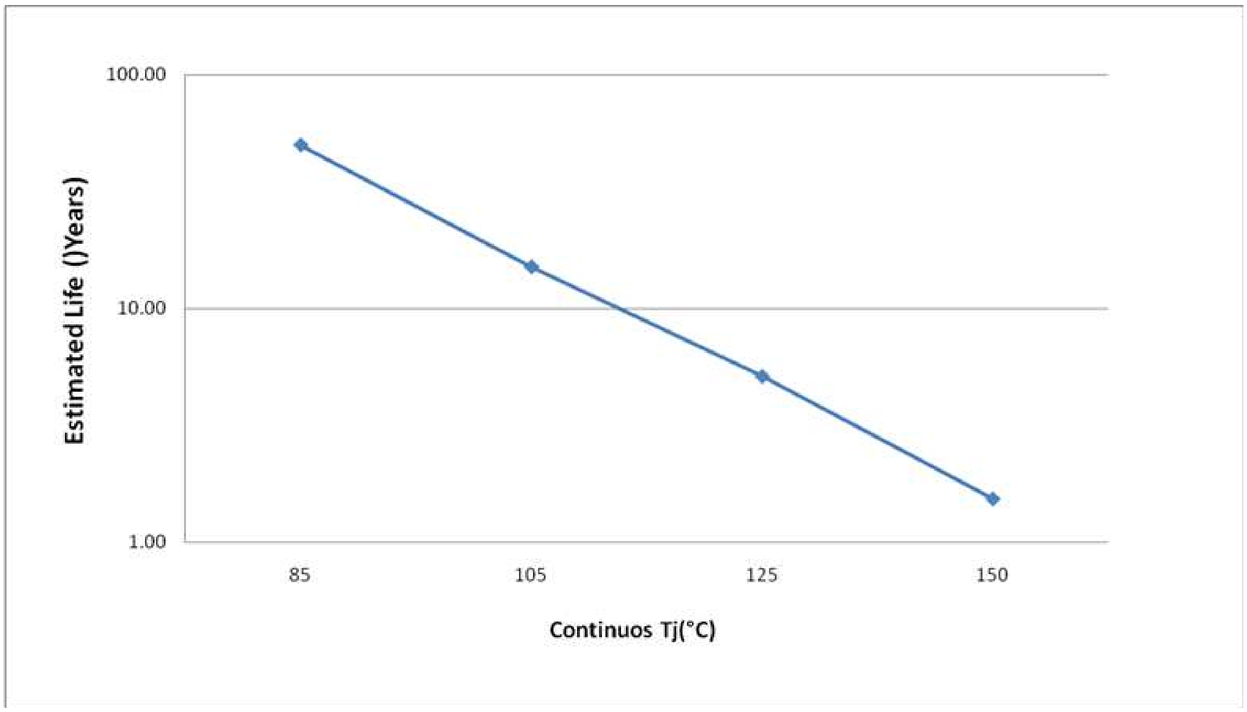
Table 14. Peripherals With Byte Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
ADC10	Analog enable 0	ADC10AE0	04Ah
	ADC data transfer control register 1	ADC10DTC1	049h
	ADC data transfer control register 0	ADC10DTC0	048h
USI	USI control 0	USICTL0	078h
	USI control 1	USICTL1	079h
	USI clock control	USICKCTL	07Ah
	USI bit counter	USICNT	07Bh
	USI shift register	USISR	07Ch
Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P2	Port P2 selection 2	P2SEL2	042h
	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection 2	P1SEL2	041h
	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

Absolute Maximum Ratings(1)

Voltage applied at V_{CC} to V_{SS}		–0.3 V to 4.1 V
Voltage applied to any pin(2)		–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin		±2 mA
Storage temperature range, T_{stg}(3)	Unprogrammed device	–55°C to 150°C
	Programmed device	–55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.



A. See data sheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 110°C junction temperature (does not include package interconnect life).

C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 1. Operating Life Derating Chart

THERMAL INFORMATION

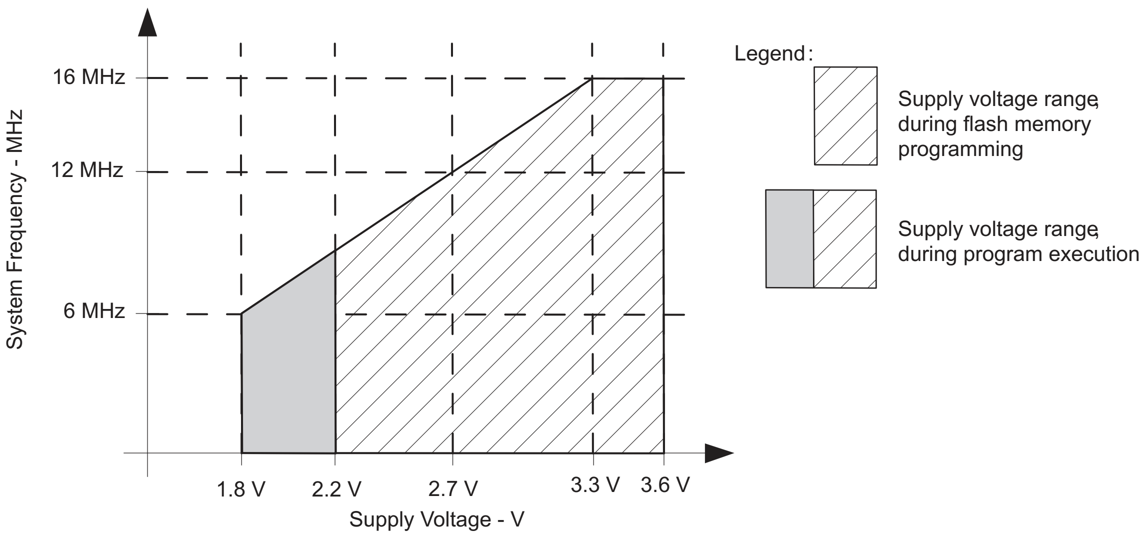
THERMAL METRIC[1]		MSP430G2332-EP PW 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	98.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	26.8	
θ_{JB}	Junction-to-board thermal resistance[4]	41.2	
ψ_{JT}	Junction-to-top characterization parameter[5]	1.1	
ψ_{JB}	Junction-to-board characterization parameter[6]	40.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution	1.8		3.6	V
		During flash programming/erase	2.2		3.6	
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature		-40		125	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency using the USART module)(1)(2)	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc		12	
		V_{CC} = 3.3 V, Duty cycle = 50% ± 10%	dc		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 2. Safe Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	2.2 V		220		µA
			3 V		320	400	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics – Active Mode Supply Current (Into V_{CC})

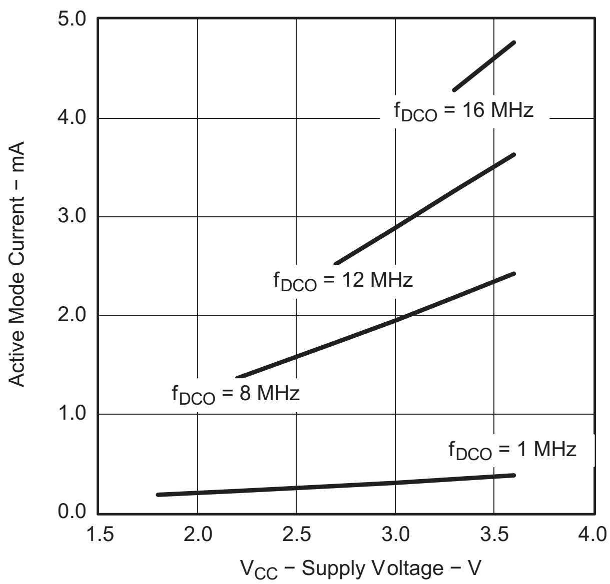


Figure 3. Active Mode Current vs V_{CC}, T_A = 25°C

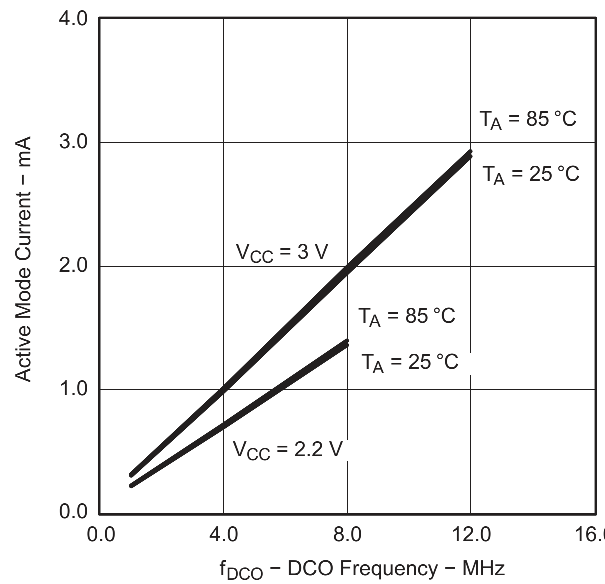


Figure 4. Active Mode Current vs DCO Frequency

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current[2]	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		55		µA
I_{LPM2}	Low-power mode 2 (LPM2) current[3]	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22		µA
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current[3]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.7	1.5	µA
			125°C				24	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3)[3]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	0.7	µA
			125°C			3	9.3	
I_{LPM4}	Low-power mode 4 (LPM4) current[4]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	0.5	µA
			85°C			0.8	1.5	µA
			125°C			3	8	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for brownout and WDT clocked by SMCLK included.
(3) Current for brownout and WDT clocked by ACLK included.
(4) Current for brownout included.

Typical Characteristics Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

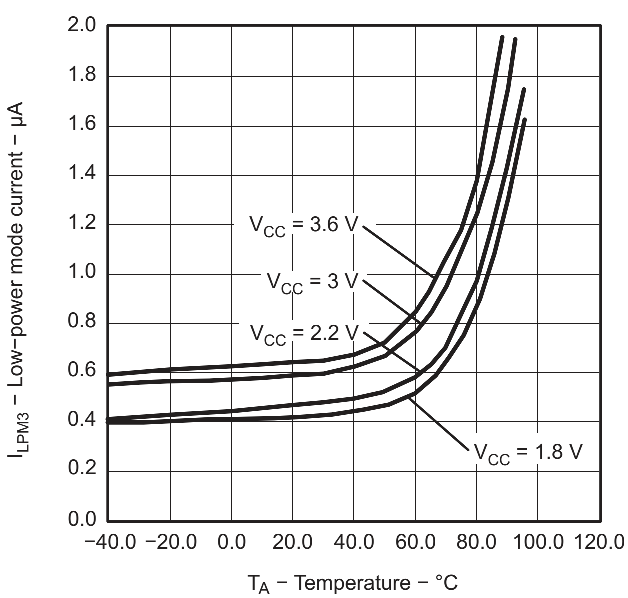


Figure 5. LPM3 Current vs Temperature

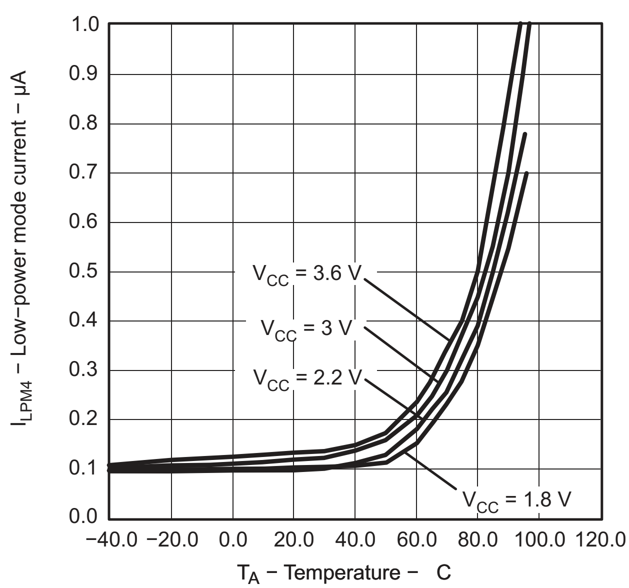


Figure 6. LPM4 Current vs Temperature

Schmitt-Trigger Inputs – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		3 V	0.3		1	V
R_{Pull}	Pullup/pulldown resistor	For pullup: V_{IN} = V_{SS} For pulldown: V_{IN} = V_{CC}	3 V	20	35	50	kΩ
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}			5		pF

Leakage Current – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current(1)(2)	T_A = -40°C to 85°C	3 V		±50	nA
		T_A = 125°C(1)(2)			±120	

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input, and the pullup/pulldown resistor is disabled.

Outputs – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –6 mA(1)	3 V		V_{CC} – 0.3		V
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 6 mA(1)	3 V		V_{SS} + 0.3		V

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y, C_L = 20 pF, R_L = 1 kΩ(1) (2)	3 V		12		MHz
f_{Port_CLK}	Clock output frequency	Px.y, C_L = 20 pF(2)	3 V		16		MHz

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

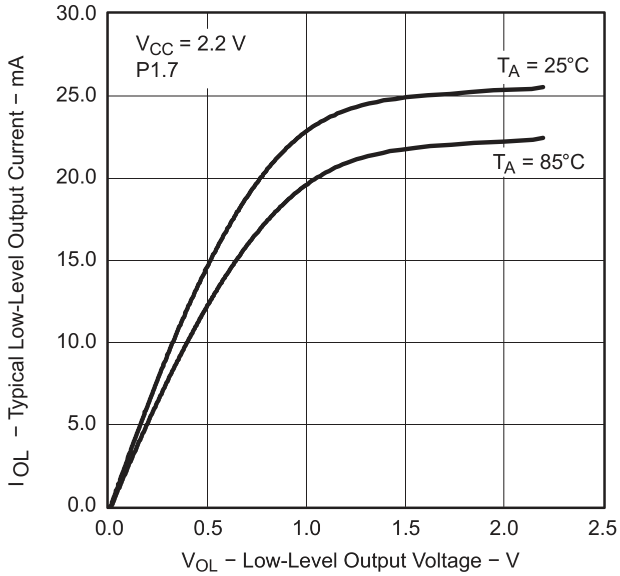


Figure 7.

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

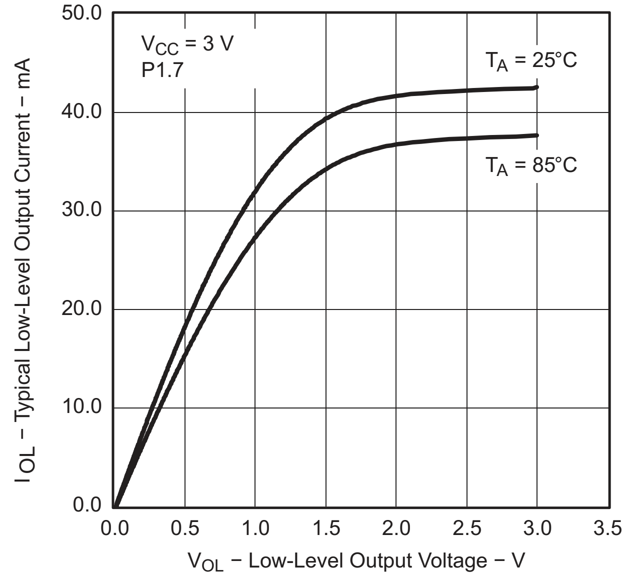


Figure 8.

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

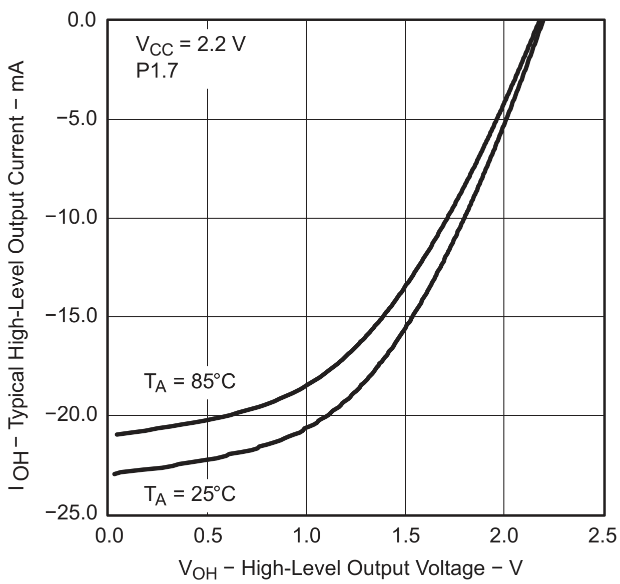


Figure 9.

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

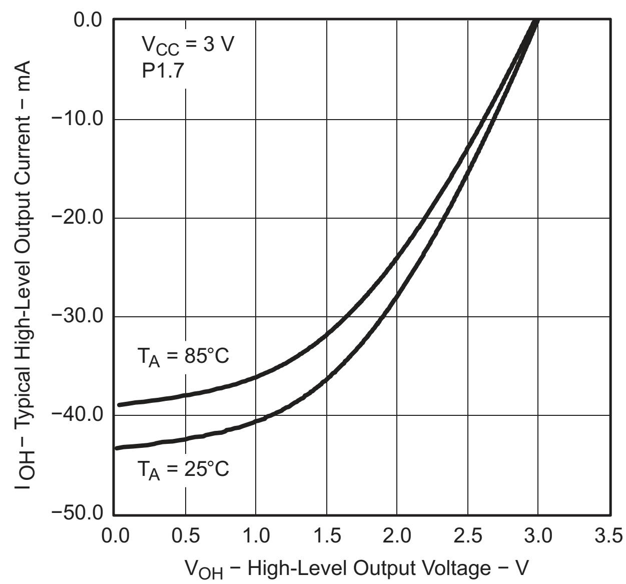


Figure 10.

Pin-Oscillator Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$fo_{P1.x}$	Port output oscillation frequency	P1.y, C_L = 10 pF, R_L = 100 kΩ (1) (2)	3 V		1400		kHz
		P1.y, C_L = 20 pF, R_L = 100 kΩ (1) (2)			900		
$fo_{P2.x}$	Port output oscillation frequency	P2.0 to P2.5, C_L = 10 pF, R_L = 100 kΩ (1) (2)	3 V		1800		kHz
		P2.0 to P2.5, C_L = 20 pF, R_L = 100 kΩ (1) (2)			1000		
$fo_{P2.6/7}$	Port output oscillation frequency	P2.6 and P2.7, C_L = 20 pF, R_L = 100 kΩ (1) (2)	3 V		700		kHz

(1) A resistive divider with two 100-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage oscillates with a typical amplitude of 700 mV at the specified toggle frequency.

Typical Characteristics – Pin-Oscillator Frequency

TYPICAL OSCILLATING FREQUENCY
vs
LOAD CAPACITANCE

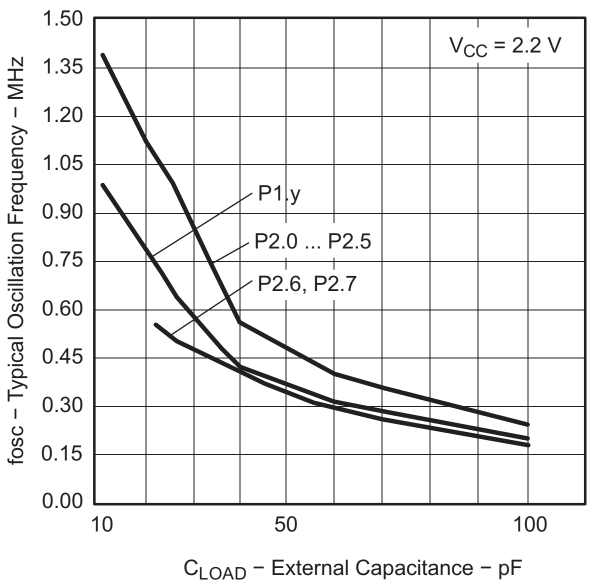


Figure 11.

TYPICAL OSCILLATING FREQUENCY
vs
LOAD CAPACITANCE

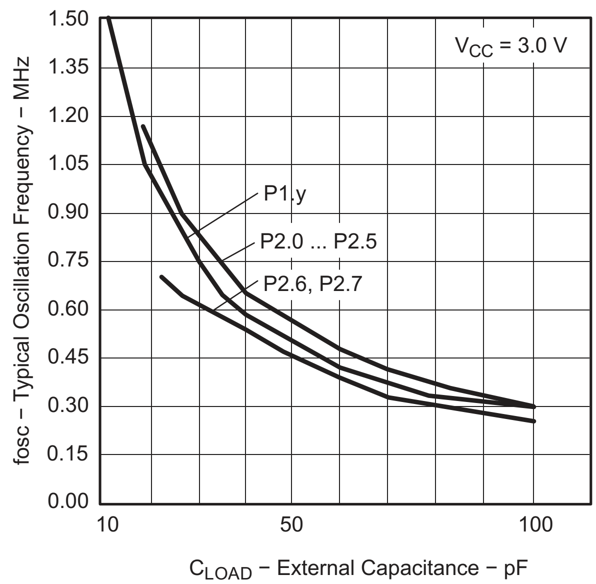


Figure 12.

POR/Brownout Reset (BOR)[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 13	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 13 through Figure 15	$dV_{CC}/dt \le 3$ V/s			1.40		V
$V_{hys(B\_IT-)}$	See Figure 13	$dV_{CC}/dt \le 3$ V/s			140		mV
$t_{d(BOR)}$	See Figure 13					2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally[2]		2.2 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
(2) Minimum and maximum parameters are characterized up to T_A = 105°C, unless otherwise noted.

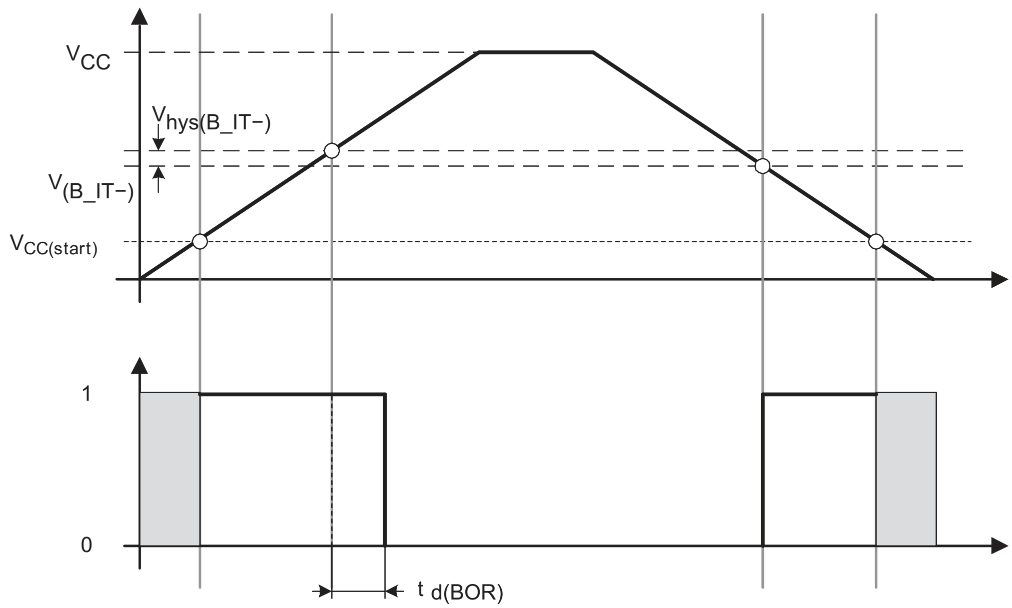


Figure 13. POR/Brownout Reset (BOR) vs Supply Voltage

Typical Characteristics – POR/Brownout Reset (BOR)

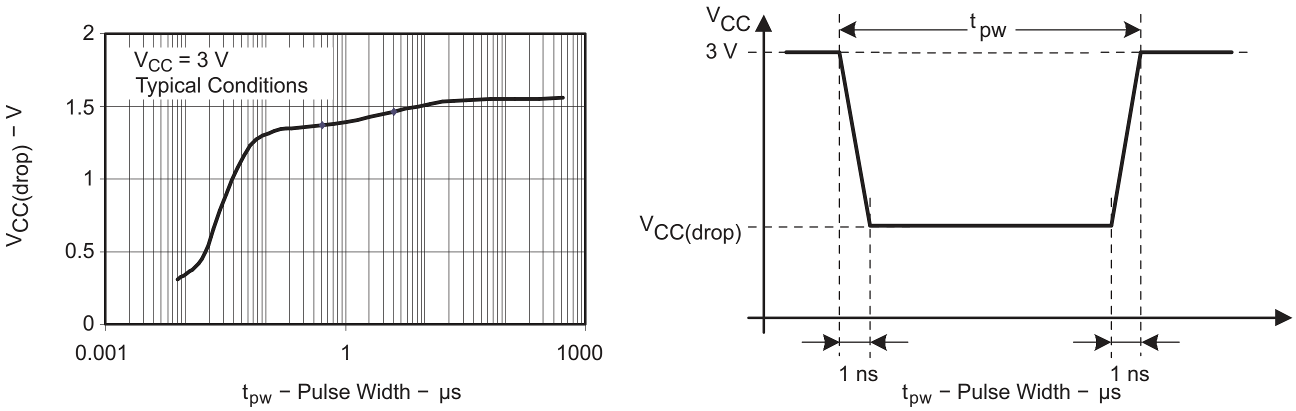


Figure 14. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

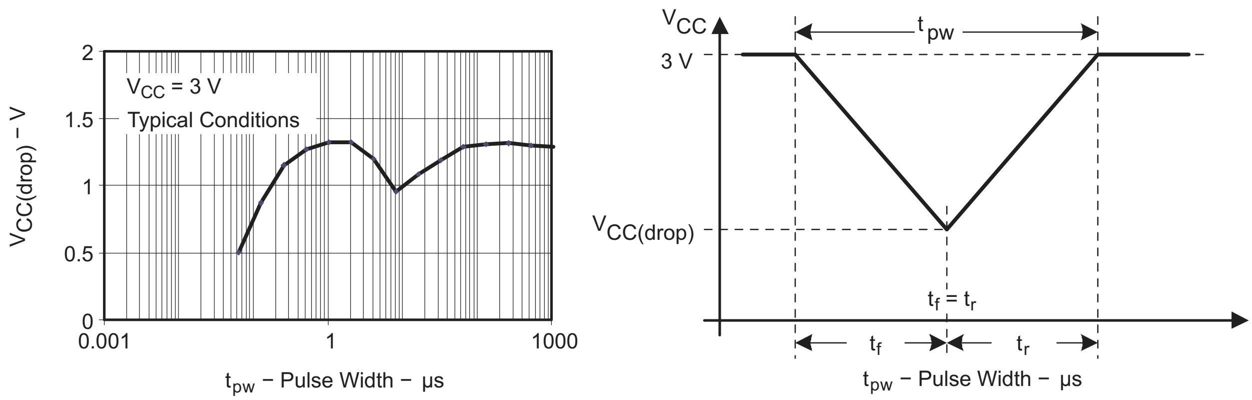


Figure 15. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	V
		RSELx = 15		3		3.6	V
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3 V		0.15		MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3 V		0.21		MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3 V		0.30		MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3 V		0.41		MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3 V		0.58		MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3 V		1.6		MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3 V		2.3		MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3 V		3.4		MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3 V		4.25		MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	3 V		1.35		ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	3 V		1.08		ratio
Duty cycle		Measured at SMCLK output	3 V		50		%

Calibrated DCO Frequencies – Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature(1)	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	-40°C to 125°C	3 V	-3	±0.5	+3	%
1-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	30°C	1.8 V to 3.6 V	-3	±2	+3	%
1-MHz tolerance overall	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	-40°C to 125°C	1.8 V to 3.6 V	-6	±3	+6	%
8-MHz tolerance over temperature(1)	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	-40°C to 125°C	3 V	-3	±0.5	+3	%
8-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	30°C	2.2 V to 3.6 V	-3	±2	+3	%
8-MHz tolerance overall	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	-40°C to 125°C	2.2 V to 3.6 V	-6	±3	+6	%
12-MHz tolerance over temperature(1)	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	-40°C to 125°C	3 V	-3	±0.5	+3	%
12-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	30°C	2.7 V to 3.6 V	-3	±2	+3	%
12-MHz tolerance overall	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	-40°C to 125°C	2.7 V to 3.6 V	-6	±3	+6	%
16-MHz tolerance over temperature(1)	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	-40°C to 125°C	3.3 V	-3	±0.5	+3	%
16-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	30°C	3.3 V to 3.6 V	-3	±2	+3	%
16-MHz tolerance overall	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	-40°C to 125°C	3.3 V to 3.6 V	-6	±3	+6	%

(1) This is the frequency change from the measured frequency at 30°C over temperature.

Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	3 V		1.5		µs
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (2)				$1/f_{MCLK} + t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4

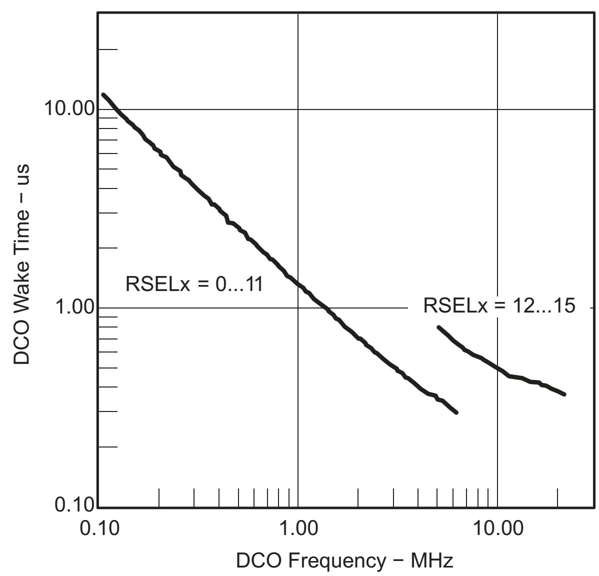


Figure 16. DCO Wake-Up Time From LPM3 vs DCO Frequency

Crystal Oscillator, XT1, Low-Frequency Mode(1) (2)

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3, T_A = -40°C to 125°C	1.8 V to 3.6 V		32768		Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(3)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
Duty cycle	LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(4)	XTS = 0, XCAPx = 0, LFXT1Sx = 3(5)	2.2 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 (a) Keep the trace between the device and the crystal as short as possible.
 (b) Design a good ground plane around the oscillator pins.
 (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Crystal oscillator cannot be operated beyond 105°C. Parameters are characterized up to T_A = 105°C, unless otherwise noted.

(3) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
 Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(4) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(5) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	3 V	4	12	20	kHz
		125°C				23	
df_{VLO}/d_T	VLO frequency temperature drift(1)	-40°C to 125°C	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(2)	25°C	1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method: (MAX(-40°C to 125°C) - MIN(-40°C to 125°C)) / MIN(-40°C to 125°C) / (125°C - (-40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) - MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V - 1.8 V)

Timer_A

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	SMCLK Duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$t_{TA,cap}$	Timer_A capture timing(1)	TA0, TA1	3 V	20			ns

(1) Parameter characterized up to T_A = 105°C, unless otherwise noted.

USI, Universal Serial Interface(1)

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USI}	USI module clock frequency	External: SCLK, Duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$f_{(SCLK)}$	Serial clock frequency, slave mode	SPI slave mode	3 V			6	MHz
$V_{OL,I2C}$	Low-level output voltage on SDA and SCL	USI module in I2C mode, $I_{(OLmax)}$ = 1.5 mA	3 V	V_{SS}		V_{SS} + 0.4	V

(1) Parameters are characterized up to T_A = 105°C, unless otherwise noted.

Typical Characteristics – USI Low-Level Output Voltage on SDA and SCL

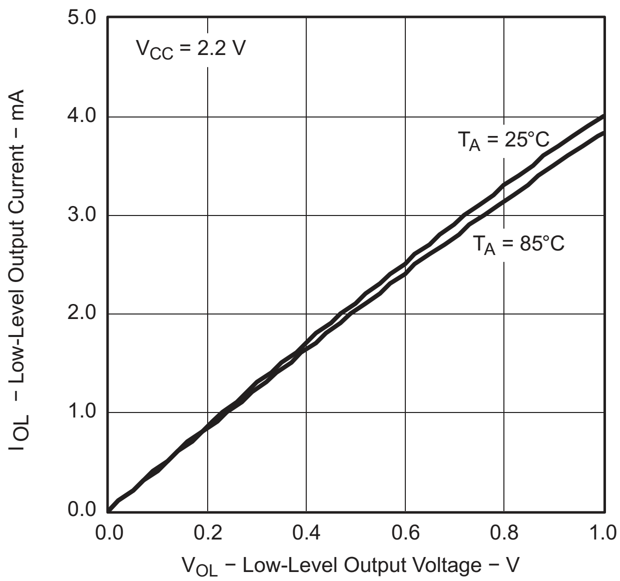


Figure 17. USI Low-Level Output Voltage vs Output Current

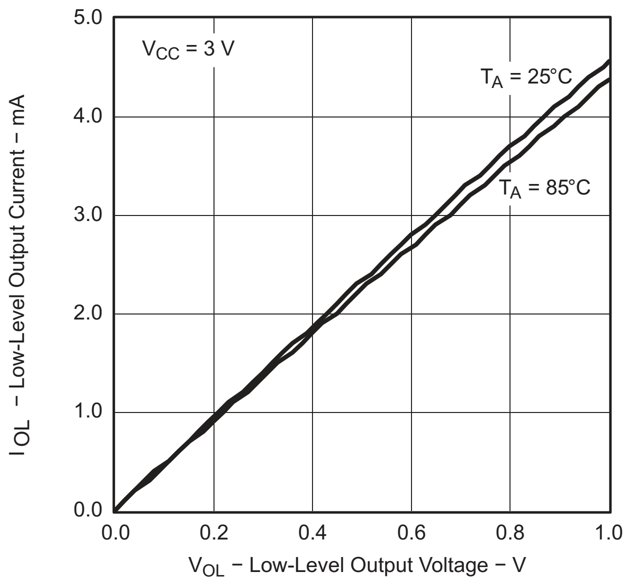


Figure 18. USI Low-Level Output Voltage vs Output Current

10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[(1)]

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage[(2)]	All Ax terminals, Analog inputs selected in ADC10AE register		3 V	0		V_{CC}	V
I_{ADC10}	ADC10 supply current[(3)]	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	-40°C to 125°C	3 V		0.6		mA
I_{REF+}	Reference supply current, reference buffer disabled[(4)]	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	-40°C to 125°C	3 V		0.25		mA
		$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0				0.25		
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0[(4)]	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	-40°C to 125°C	3 V		1.1		mA
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1[(4)]	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	-40°C to 125°C	3 V		0.5		mA
C_I	Input capacitance	Only one terminal Ax can be selected at one time	-40°C to 125°C	3 V			27	pF
R_I	Input MUX ON resistance	0 V ≤ V_{Ax} ≤ V_{CC}	-40°C to 125°C	3 V		1000		Ω

(1) The leakage current is defined in the leakage current table with Px.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
(4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	I_{VREF+} ≤ 1 mA, REF2_5V = 0		2.2			V
		I_{VREF+} ≤ 1 mA, REF2_5V = 1		3			
V_{REF+}	Positive built-in reference voltage	I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 0	3 V	1.37	1.5	1.61	V
		I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 1		2.29	2.5	2.7	
$I_{LD,VREF+}$	Maximum VREF+ load current(1)		3 V			±1	mA
	VREF+ load regulation(1)	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage V_{Ax} ≈ 0.75 V, REF2_5V = 0	3 V			±2	LSB
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage V_{Ax} ≈ 1.25 V, REF2_5V = 1				±2	
	V_{REF+} load regulation response time	I_{VREF+} = 100 µA→900 µA, V_{Ax} ≈ 0.5 × VREF+, Error of conversion result ≤ 1 LSB, ADC10SR = 0	3 V			400	ns
C_{VREF+}	Maximum capacitance at pin VREF+(1)	I_{VREF+} ≤ ±1 mA, REFON = 1, REFOUT = 1	3 V			100	pF
TC_{REF+}	Temperature coefficient	I_{VREF+} = const with 0 mA ≤ I_{VREF+} ≤ 1 mA	3 V			±170	ppm/°C
t_{REFON}	Settling time of internal reference voltage to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1	3.6 V			30	µs
$t_{REFBURST}$	Settling time of reference buffer to 99.9% VREF(1)	I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0	3 V			2	µs

(1) Minimum and maximum parameters are characterized up to T_A = 105°C, unless otherwise noted.

10-Bit ADC, External Reference[1]

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
VEREF+	Positive external reference input voltage range[2]	VEREF+ > VEREF–, SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		VEREF– ≤ VEREF+ ≤ V_{CC} – 0.15 V, SREF1 = 1, SREF0 = 1 [3]		1.4		3	
VEREF–	Negative external reference input voltage range[4]	VEREF+ > VEREF–		0		1.2	V
ΔVEREF	Differential external reference input voltage range, ΔVEREF = VEREF+ – VEREF–	VEREF+ > VEREF– [5]		1.4		V_{CC}	V
I_{VEREF+}	Static input current into VEREF+	0 V ≤ VEREF+ ≤ V_{CC}, SREF1 = 1, SREF0 = 0	3 V		±1		µA
		0 V ≤ VEREF+ ≤ V_{CC} – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1[3]			0		
$I_{VEREF–}$	Static input current into VEREF–	0 V ≤ VEREF– ≤ V_{CC}	3 V		±1		µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45		6.3	MHz
			ADC10SR = 1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	3.35		6.9	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0				13 × ADC10DIV × 1/$f_{ADC10CLK}$		
$t_{ADC10ON}$	Turn-on settling time of the ADC	See [1]					100	ns

(1) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		3 V			±1	LSB
E_D	Differential linearity error		3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	3 V			±1	LSB
E_G	Gain error		3 V		±1.1	±2	LSB
E_T	Total unadjusted error		3 V		±2	±5	LSB

10-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current[1]	REFON = 0, INCHx = 0Ah, T_A = 25°C	3 V		60		µA
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah [2]	3 V		3.55		mV/°C
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected [3]	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	3 V	30			µs
I_{VMID}	Current into divider at channel 11	ADC10ON = 1, INCHx = 0Bh	3 V			[4]	µA
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, V_{MID} ≈ 0.5 × V_{CC}	3 V		1.5		V
$t_{VMID(sample)}$	Sample time required if channel 11 is selected [5]	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	3 V	1220			ns

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
(2) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) No additional current is needed. The V_{MID} is used during sampling.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

Flash Memory[1][2]

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V, 3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V, 3.6 V		1	7	mA
t_{CPT}	Cumulative program time[3]		2.2 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V, 3.6 V	20			ms
	Program and erase endurance	-40°C ≤ T_J ≤105°C		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See [4]			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	See [4]			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	See [4]			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	See [4]			6		t_{FTG}
$t_{Mass Erase}$	Mass erase time	See [4]			10593		t_{FTG}
$t_{Seg Erase}$	Segment erase time	See [4]			4819		t_{FTG}

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(2) Additional flash retention documentation located in application report SLAA392.
(3) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(4) These values are hardwired into the flash controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage [(1)]	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		2.2 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length		2.2 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge[(1)])		2.2 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time	T_A = -40°C to 105°C	2.2 V	15		100	µs
f_{TCK}	TCK input frequency[(2)]		2.2 V	0		5	MHz
$R_{Internal}$	Internal pulldown resistance on TEST	T_A = -40°C to 105°C	2.2 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse[(1)]

T_A = 25°C, over recommended ranges of supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

PIN SCHEMATICS

Port P1 Pin Schematic: P1.0 to P1.2, Input/Output With Schmitt Trigger

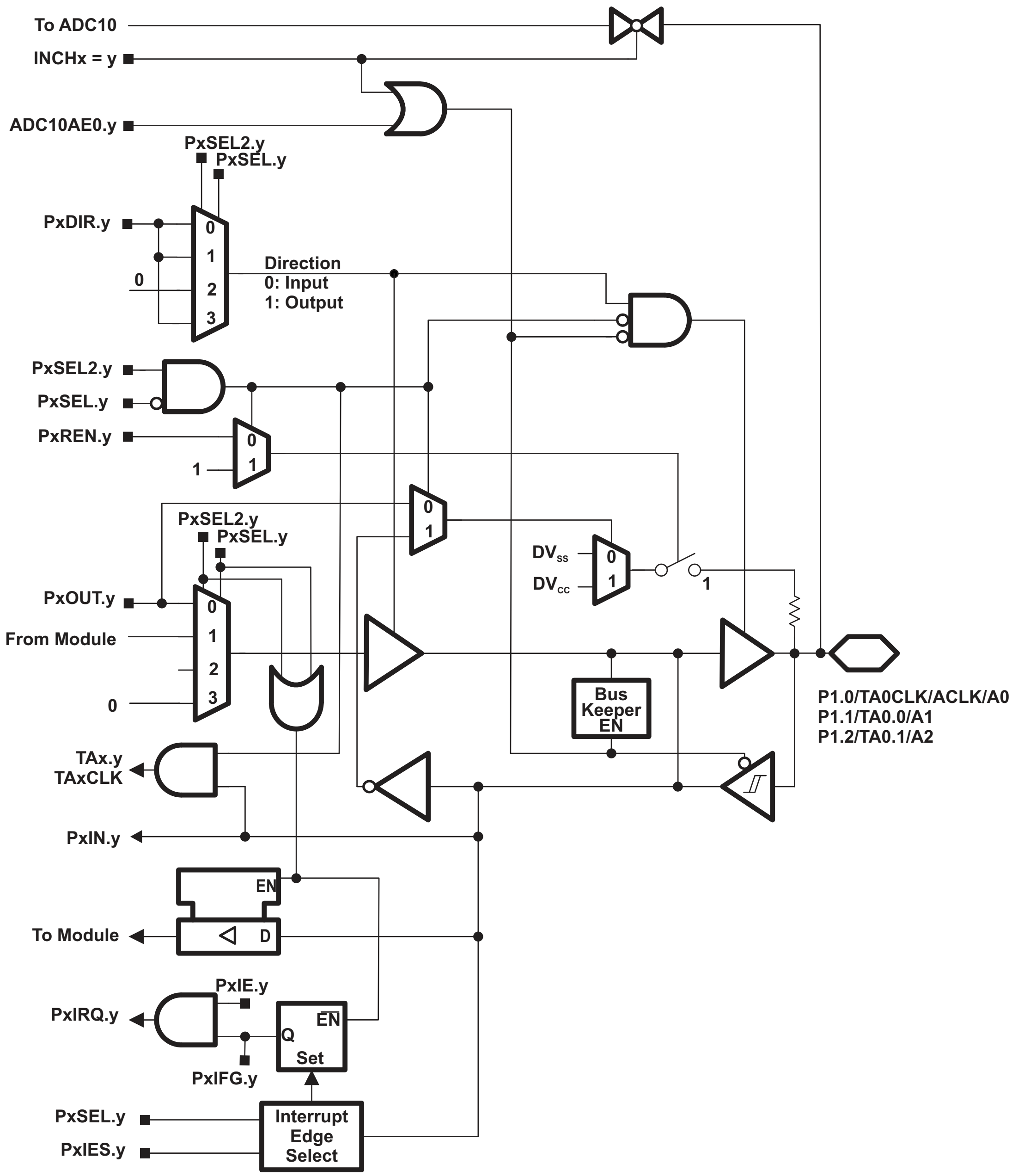


Table 15. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[(1)]		
			P1DIR.x	P1SEL.x	P1SEL2.x
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0
TA0CLK/		TA0.TACLK	0	1	0
ACLK/		ACLK	1	1	0
A0/		A0	X	X	X
Pin Osc		Capacitive sensing	x	0	1
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0
TA0.0/		TA0.0	1	1	0
		TA0.CCI0A	0	1	0
A1/		A1	X	X	X
Pin Osc		Capacitive sensing	X	0	1
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0
TA0.1/		TA0.1	1	1	0
		TA0.CCI1A	0	1	0
A2/		A2	X	X	X
Pin Osc		Capacitive sensing	X	0	1

(1) X = don't care

Port P1 Pin Schematic: P1.3, Input/Output With Schmitt Trigger

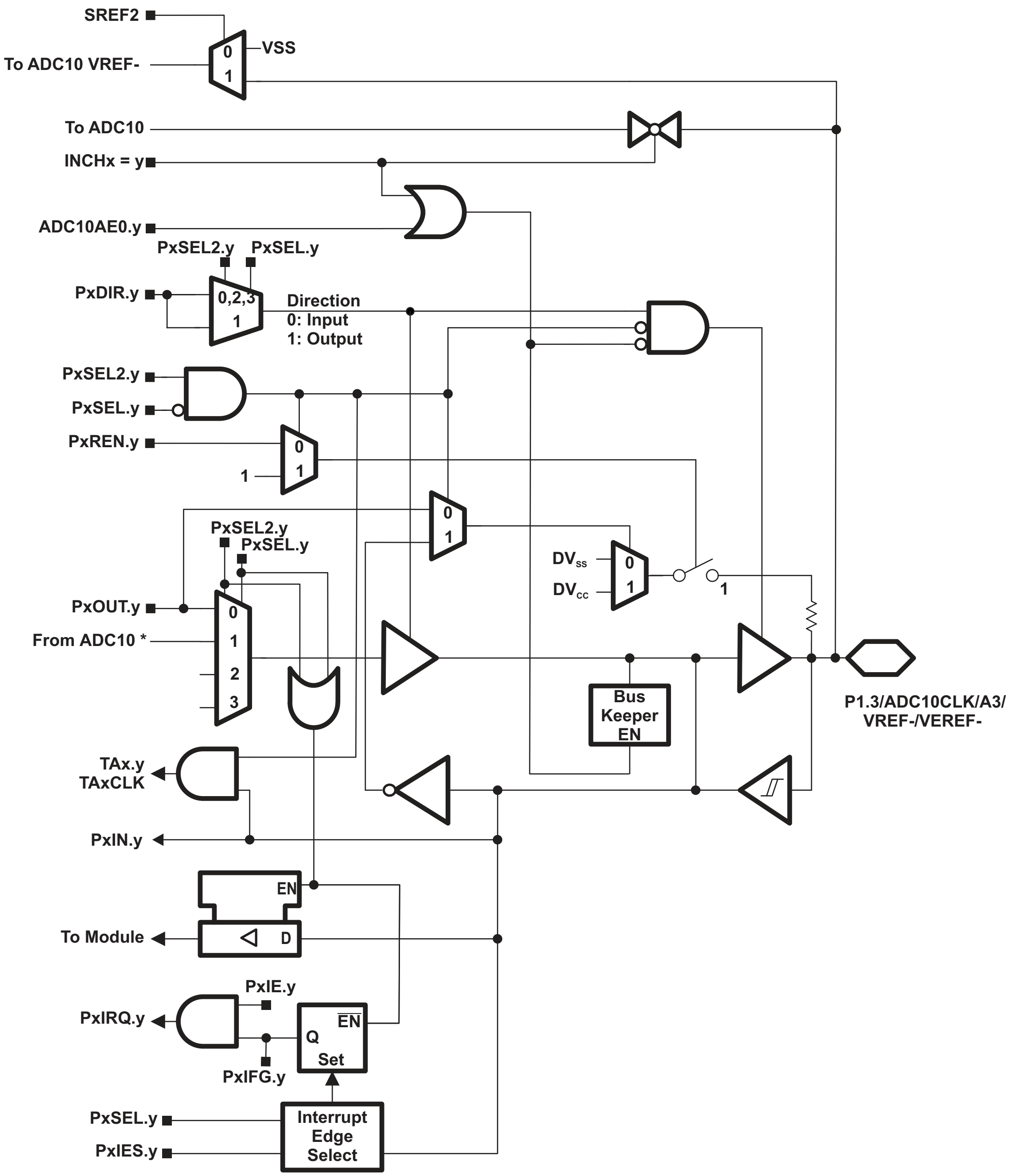


Table 16. Port P1 (P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)			
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x (INCH.x=1)
P1.3/	3	P1.x (I/O)	I: 0; O: 1	0	0	0
ADC10CLK/		ADC10CLK	1	1	0	0
A3/		A3	X	X	X	1 (y = 3)
VREF-/		VREF-	X	X	X	1
VEREF-/		VEREF-	X	X	X	1
Pin Osc		Capacitive sensing	X	0	1	0

(1) X = don't care

Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger

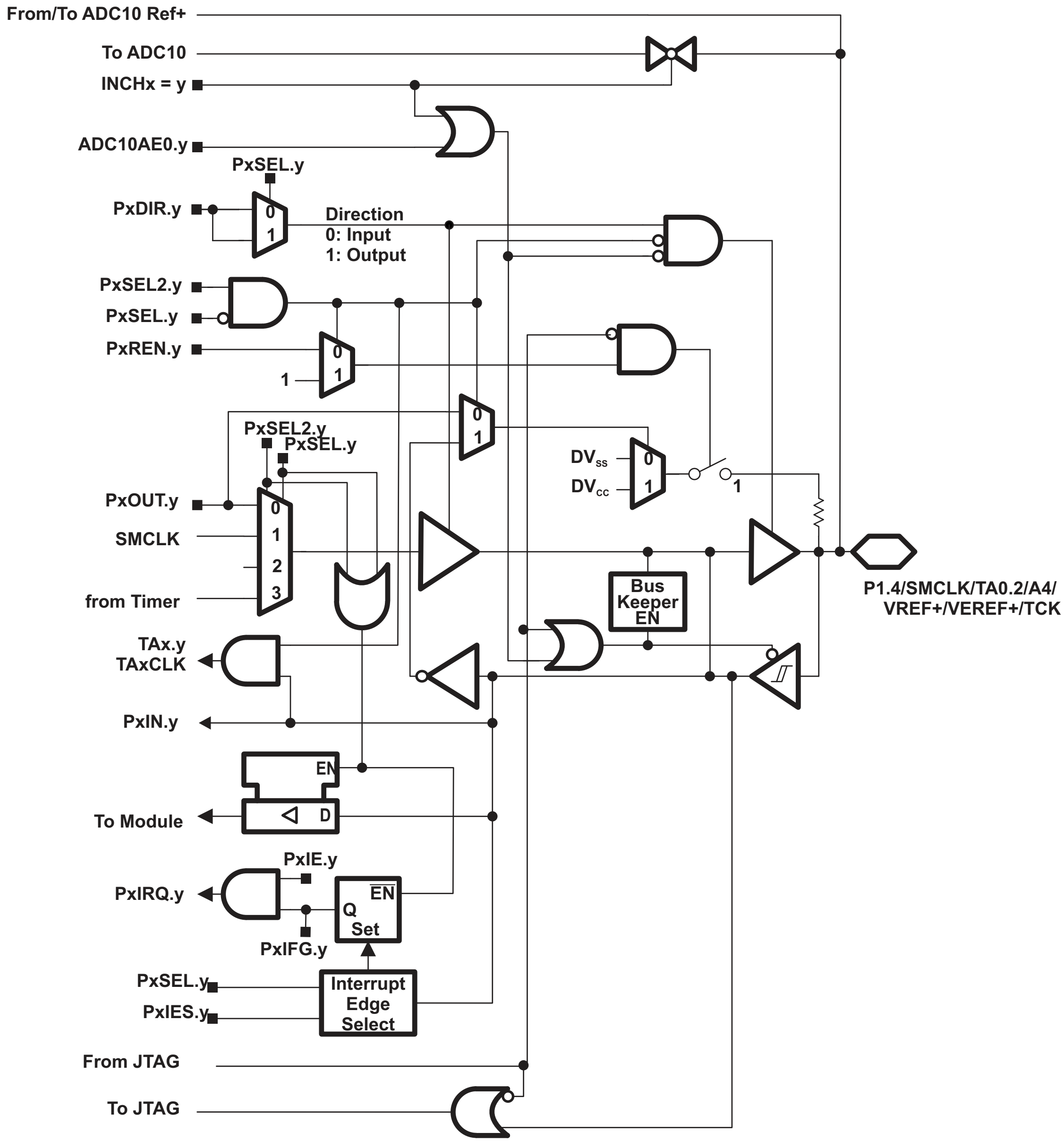


Table 17. Port P1 (P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x (INCH.x=1)	JTAG Mode
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0	0	0
SMCLK/		SMCLK	1	1	0	0	0
TA0.2/		TA0.2	1	1	1	0	0
		TA0.CCI2A	0	1	1	0	0
VREF+/		VREF+	X	X	X	1	0
VEREF+/		VEREF+	X	X	X	1	0
A4/		A4	X	X	X	1 (y = 4)	0
TCK/		TCK	X	X	X	0	1
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care

Port P1 Pin Schematic: P1.5 to P1.7, Input/Output With Schmitt Trigger

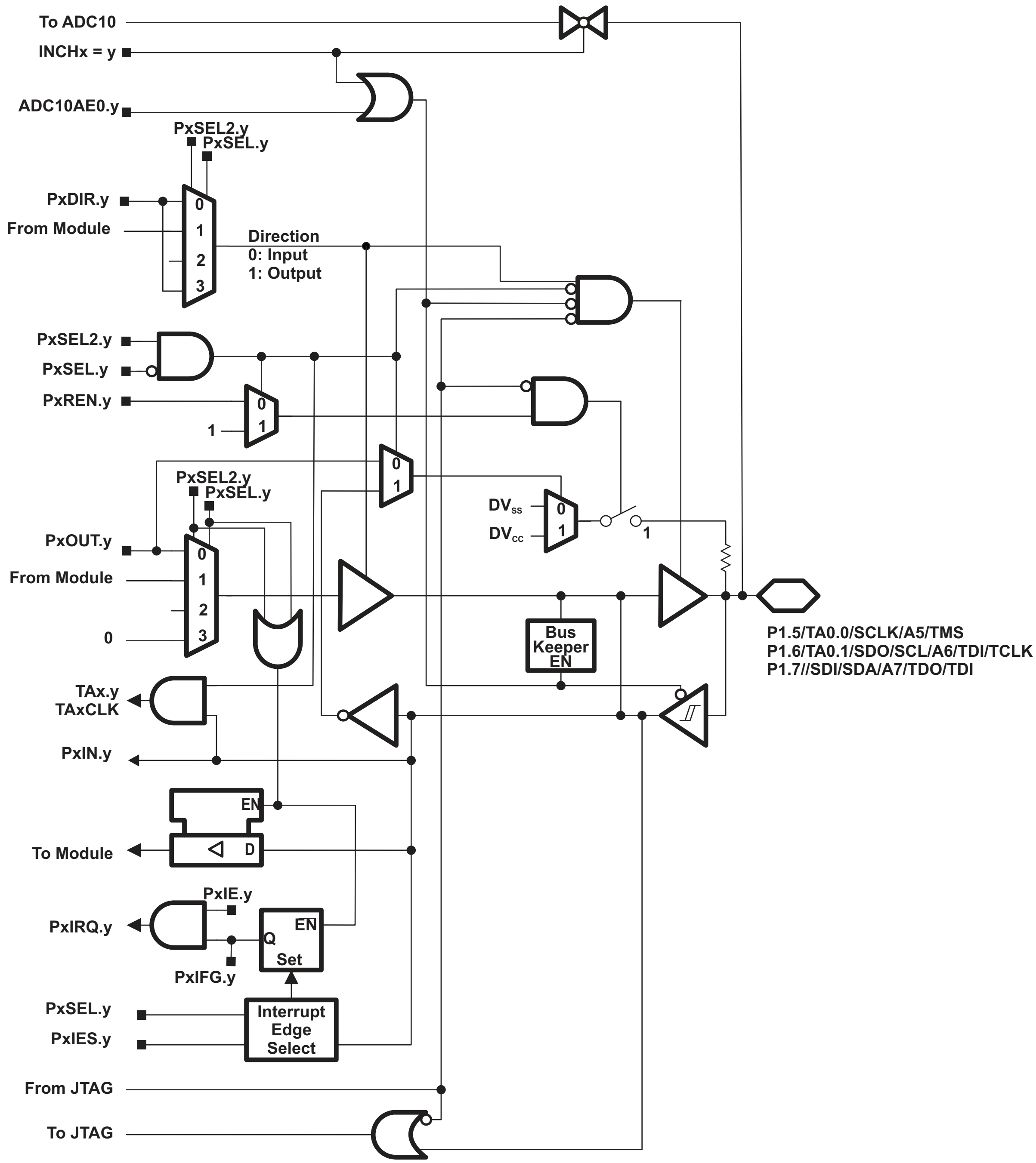


Table 18. Port P1 (P1.5 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)					
			P1DIR.x	P1SEL.x	P1SEL2.x	USIP.x	JTAG Mode	ADC10AE.x (INCH.x=1)
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0	0
SCLK/		SPI mode	from USI	1	0	1	0	0
A5/		A5	X	X	X	0	0	1 (y = 5)
TMS/		TMS	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0	0
SDO/		SPI mode	from USI	1	0	!	0	0
SCL/		I2C mode	from USI	1	0	!	0	0
A6/		A6	X	X	X	0	0	1 (y = 6)
TDI/TCLK/		TDI/TCLK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
SDI/		SPI mode	from USI	1	0	1	0	0
SDA/		SPI mode	from USI	1	0	1	0	0
A7/		A7	X	X	X	0	0	1 (y = 7)
TDO/TDI/		TDO/TDI	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care

Port P2 Pin Schematic: P2.0 to P2.5, Input/Output With Schmitt Trigger

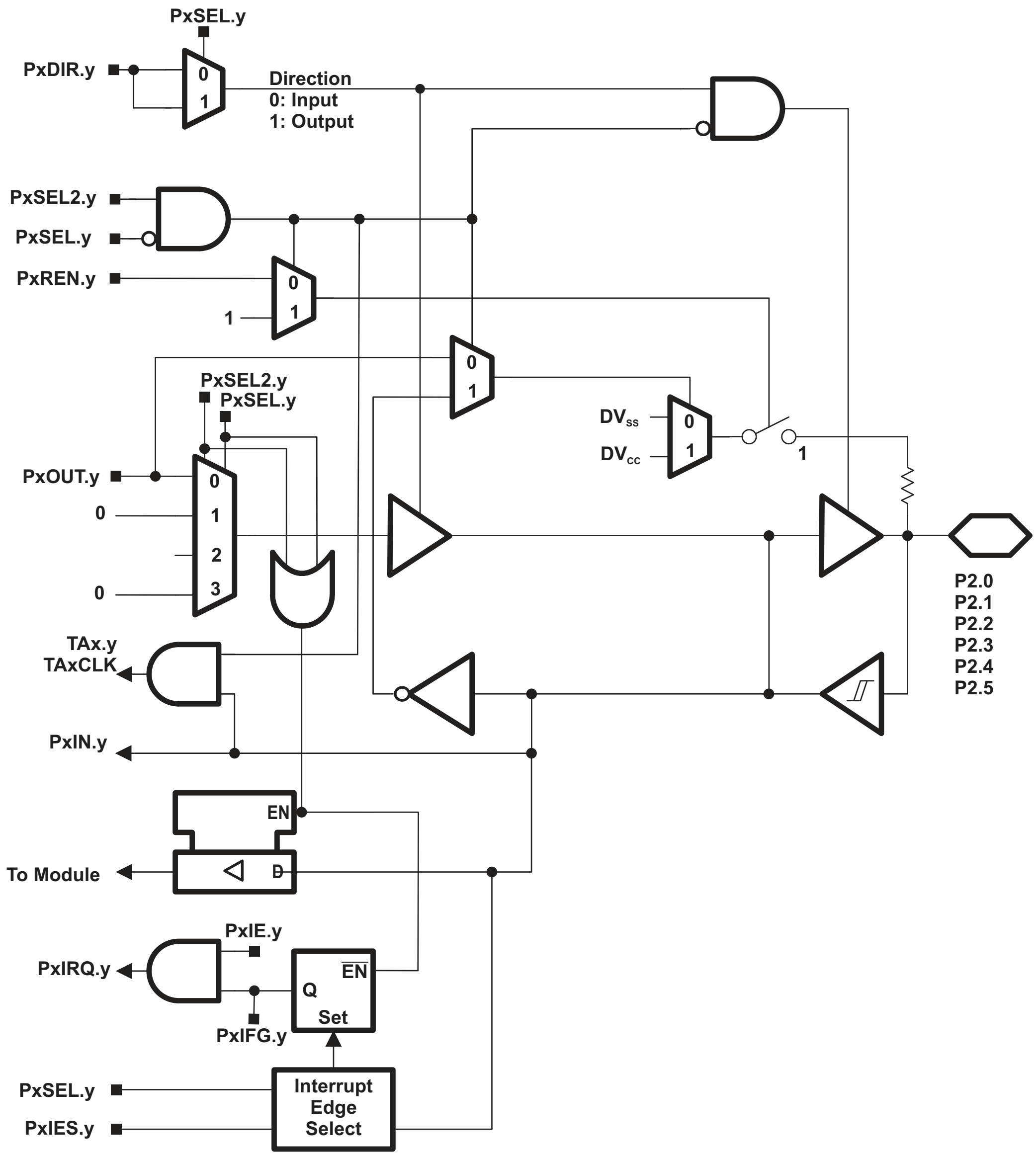


Table 19. Port P2 (P2.0 to P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P2DIR.x	P2SEL.x	P2SEL2.x
P2.0/	0	P2.x (I/O)	I: 0; O: 1	0	0
Pin Osc		Capacitive sensing	X	0	1
P2.1/	1	P2.x (I/O)	I: 0; O: 1	0	0
Pin Osc		Capacitive sensing	X	0	1
P2.2/	2	P2.x (I/O)	I: 0; O: 1	0	0
Pin Osc		Capacitive sensing	X	0	1
P2.3/	3	P2.x (I/O)	I: 0; O: 1	0	0
Pin Osc		Capacitive sensing	X	0	1
P2.4/	4	P2.x (I/O)	I: 0; O: 1	0	0
Pin Osc		Capacitive sensing	X	0	1
P2.5/	5	P2.x (I/O)	I: 0; O: 1	0	0
Pin Osc		Capacitive sensing	X	0	1

(1) X = don't care

Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger

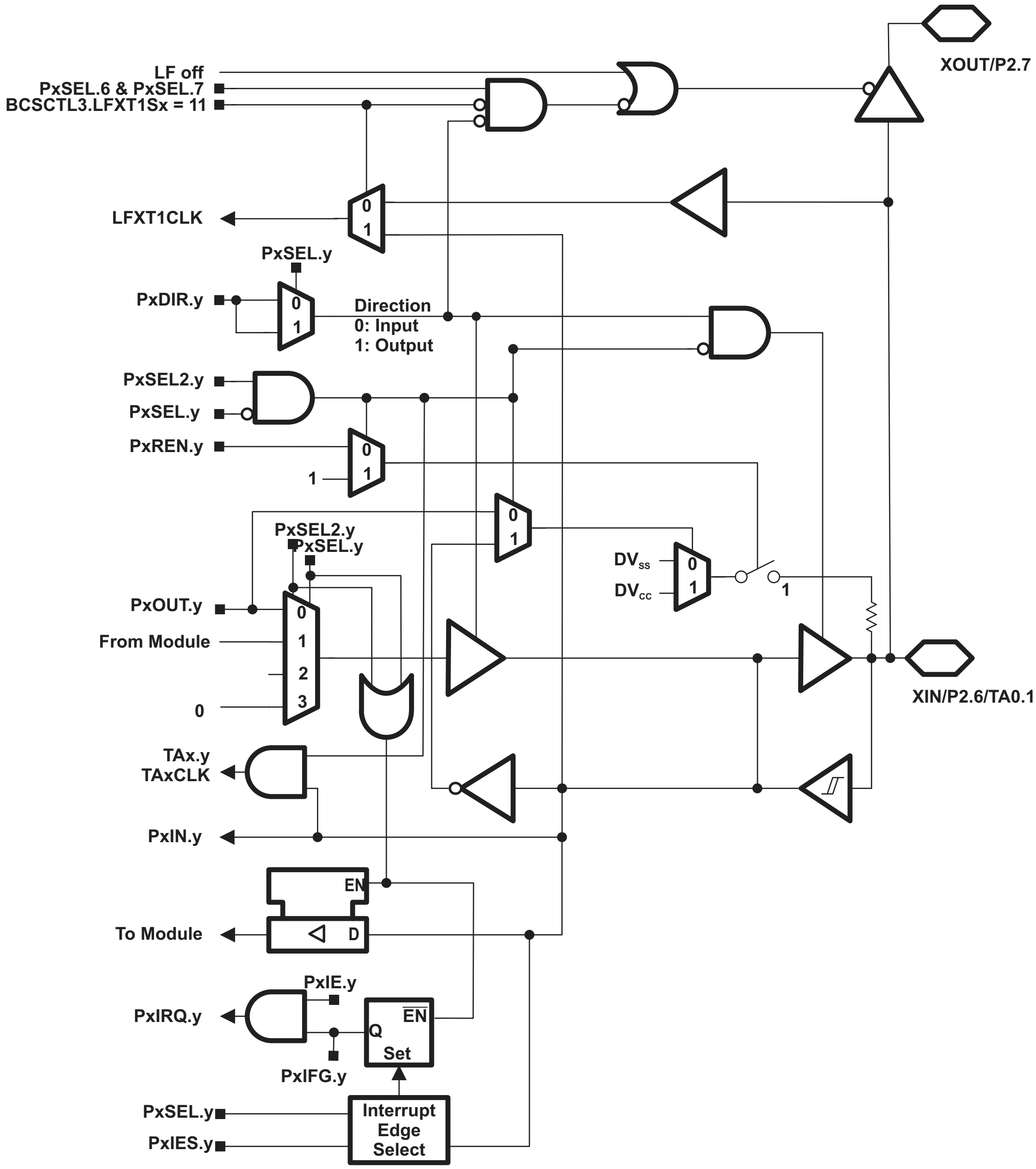


Table 20. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL2.6 P2SEL2.7
XIN/	6	XIN	0	1 1	0 0
P2.6/		P2.x (I/O)	I: 0; O: 1	0 X	0 0
TA0.1/		Timer0_A3.TA1	1	1 0	0 0
Pin Osc		Capacitive sensing	X	0 X	1 X

(1) X = don't care

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger

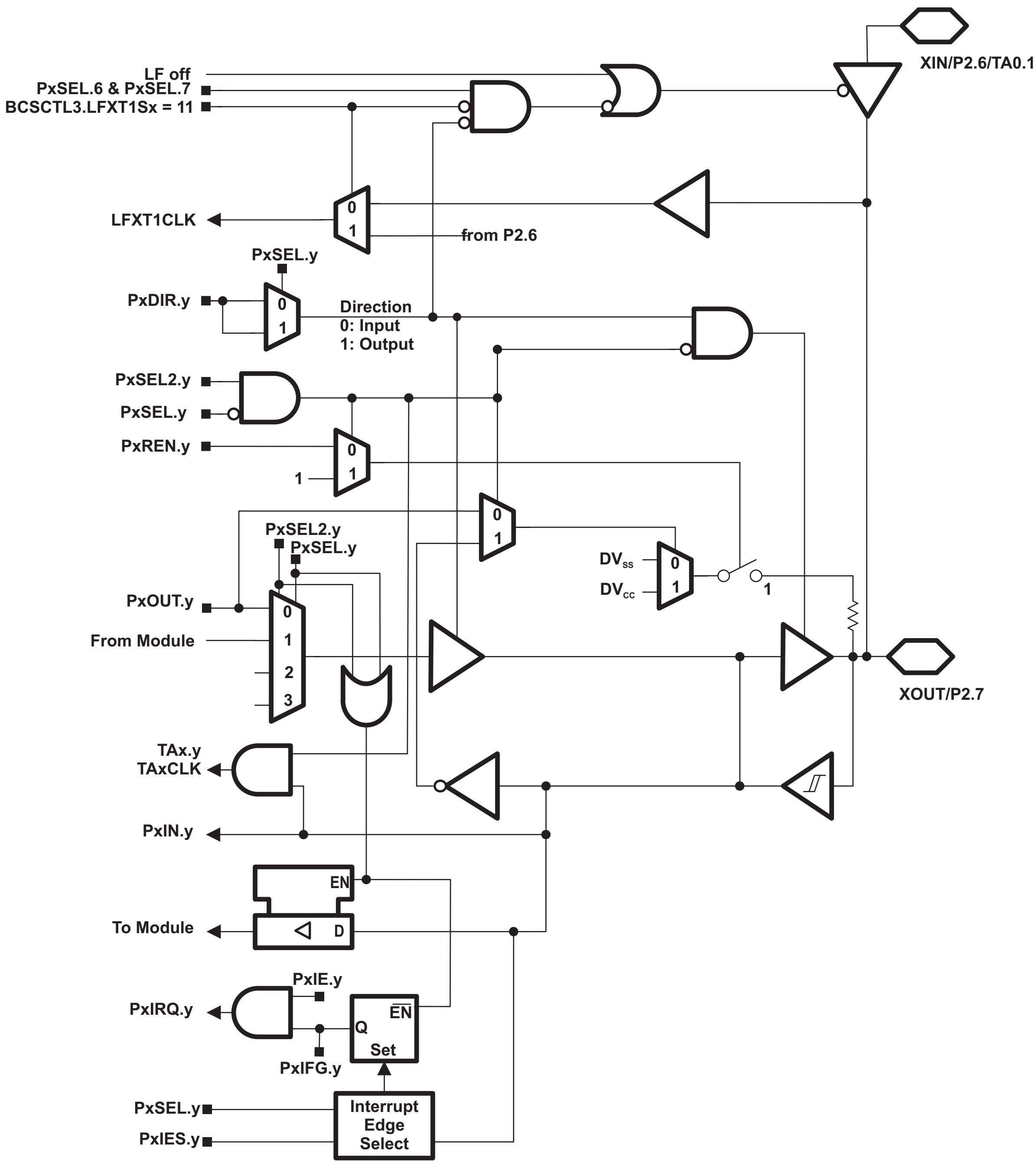


Table 21. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[(1)]		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL2.6 P2SEL2.7
XOUT/	7	XOUT	X	1 1	0 0
P2.7/		P2.x (I/O)	I: 0; O: 1	X 0	0 0
Pin Osc		Capacitive sensing	X	X 0	X 1

(1) X = don't care

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2332QPW2EP	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	G2332EP	Samples
MSP430G2332QPW2REP	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	G2332EP	Samples
V62/12625-01XE	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	G2332EP	Samples
V62/12625-01XE-T	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	G2332EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF MSP430G2332-EP :

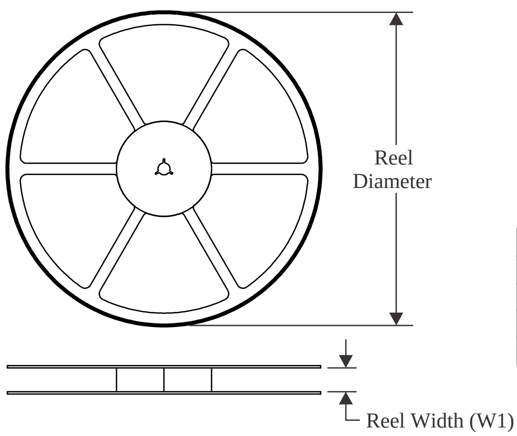
- Catalog: MSP430G2332

NOTE: Qualified Version Definitions:

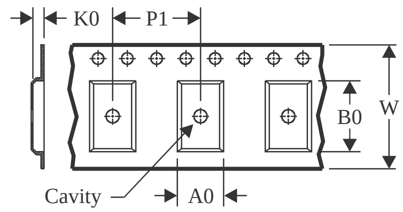
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

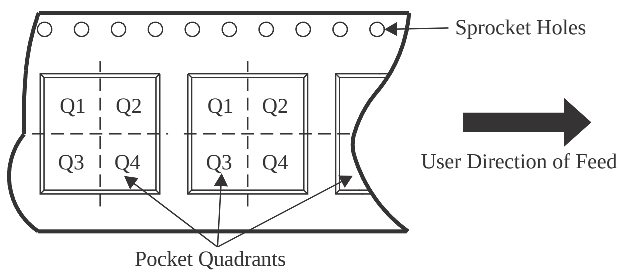


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

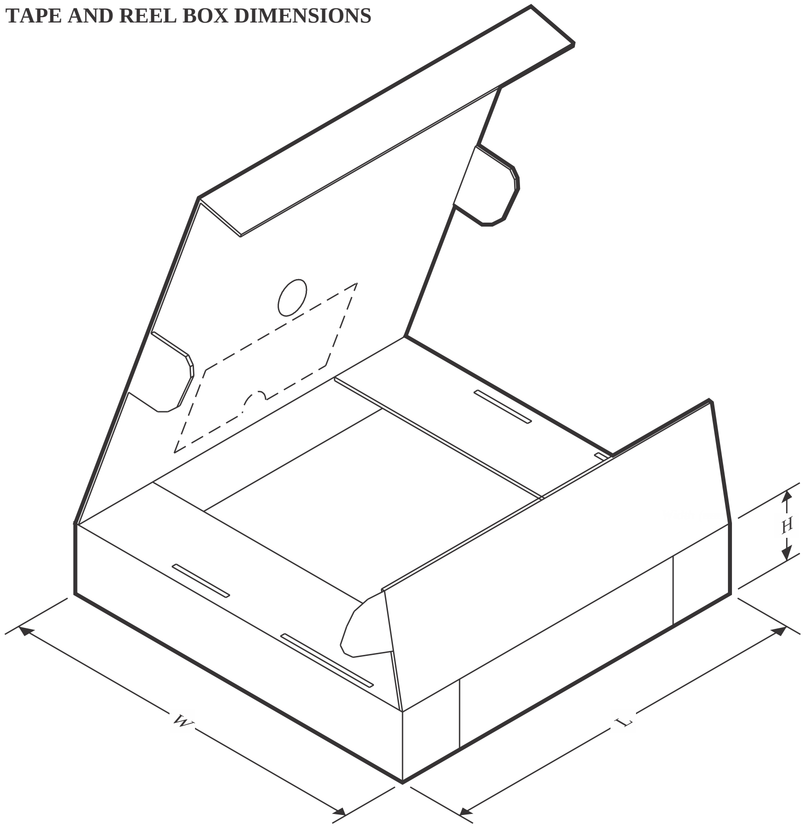
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430G2332QPW2REP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

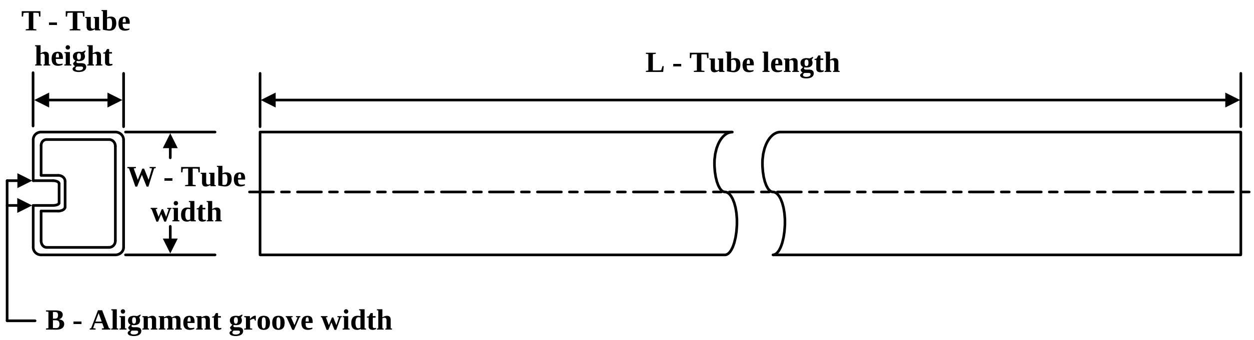
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

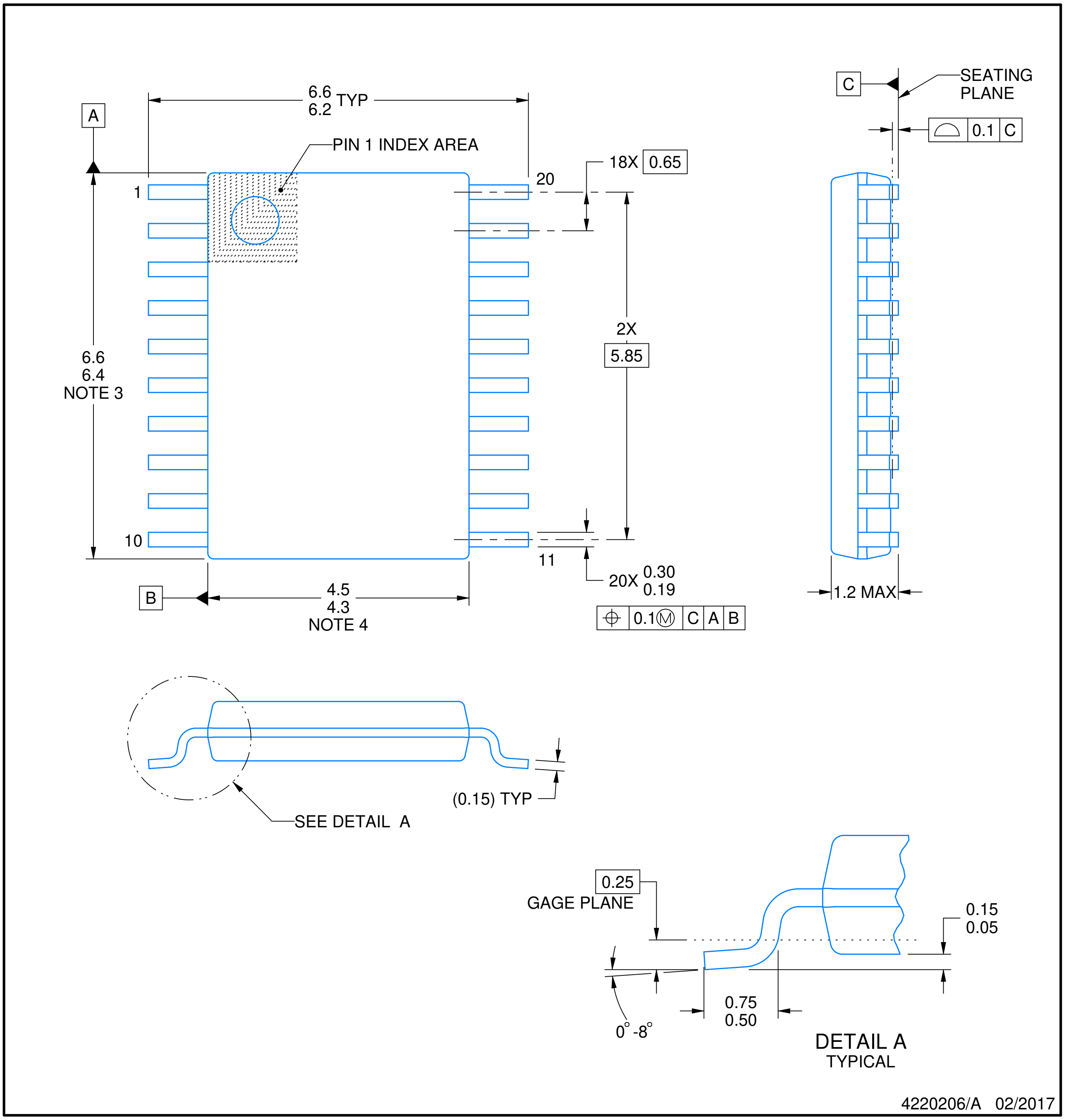
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430G2332QPW2REP	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



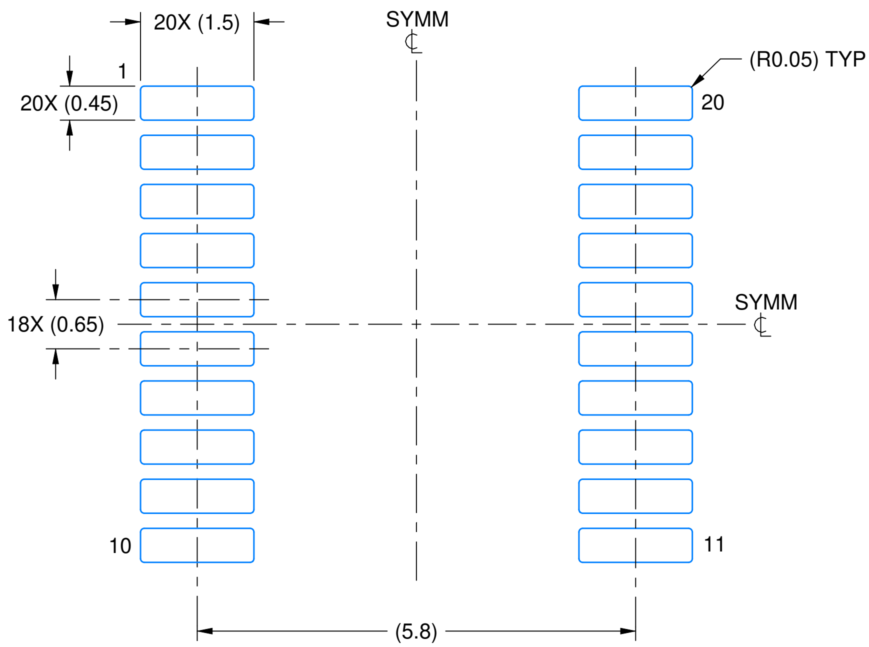
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430G2332QPW2EP	PW	TSSOP	20	70	530	10.2	3600	3.5
V62/12625-01XE-T	PW	TSSOP	20	70	530	10.2	3600	3.5

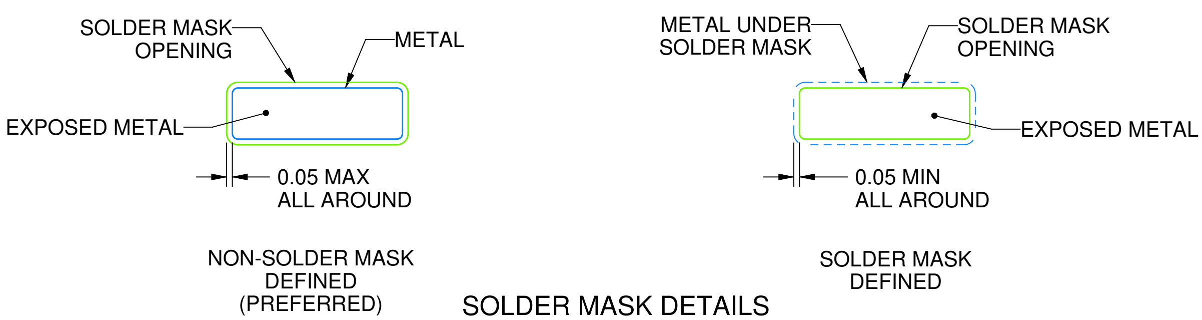


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

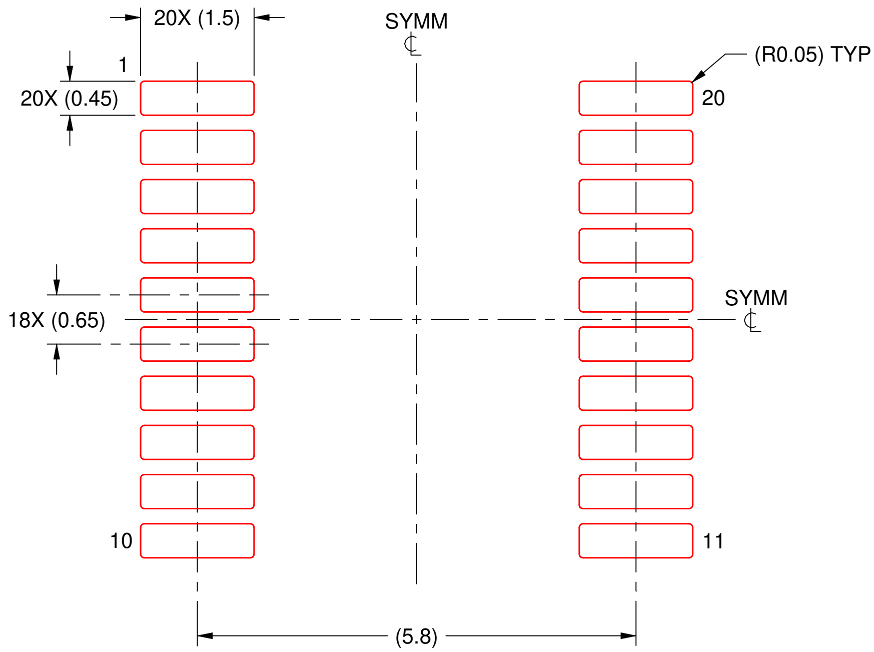


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



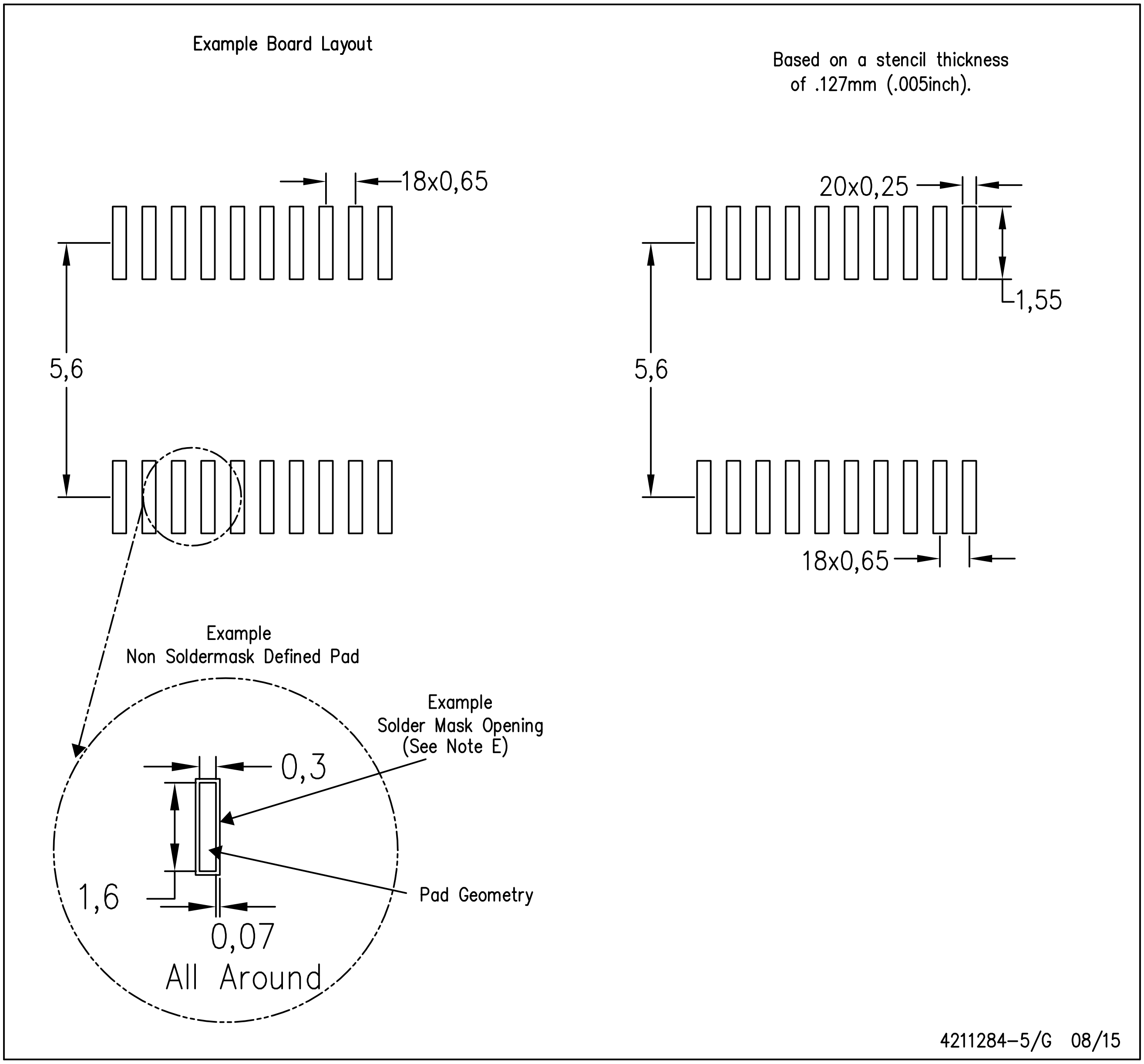
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.