

**uPG2301TQ**

**InGaP / GaAs HBT PA IC**

**for Bluetooth Class1**

Application Information

August 2004

# CEL Power Amplifier for Bluetooth Class 1

## uPG2301TQ

### Features

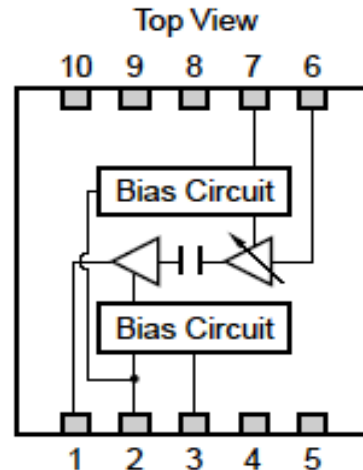
- Low Current Consumption
- 20dB Variable Gain Control
- Shut Down Function

### Application

- Bluetooth Class 1

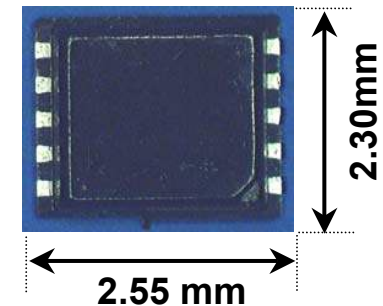
### RF Performance

- Operating Frequency: 2.4 to 2.5GHz
- Supply voltage:  $V_{CC1,2} = V_{bias} = 3.3V$ ,  
 $V_{enable} = 2.9V$
- Output Power : 23dBm typ.  
@  $V_{cont} = 2.5V$ ,  $P_{in} = +4dBm$
- Gain Control Range: 23dB typ.  
@  $V_{cont} = 0$  to  $2.5V$ ,  $P_{in} = +4dBm$
- Operating Current: 120mA typ. @  $P_{in} = +4dBm$ ,  $V_{cont} = 2.5V$



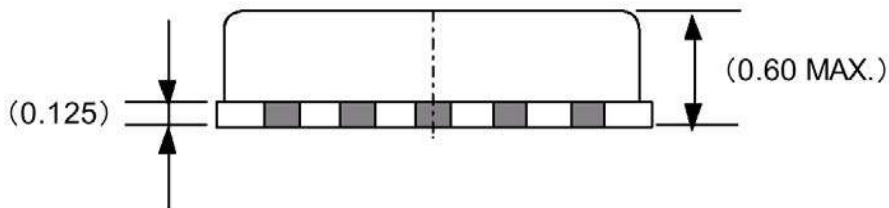
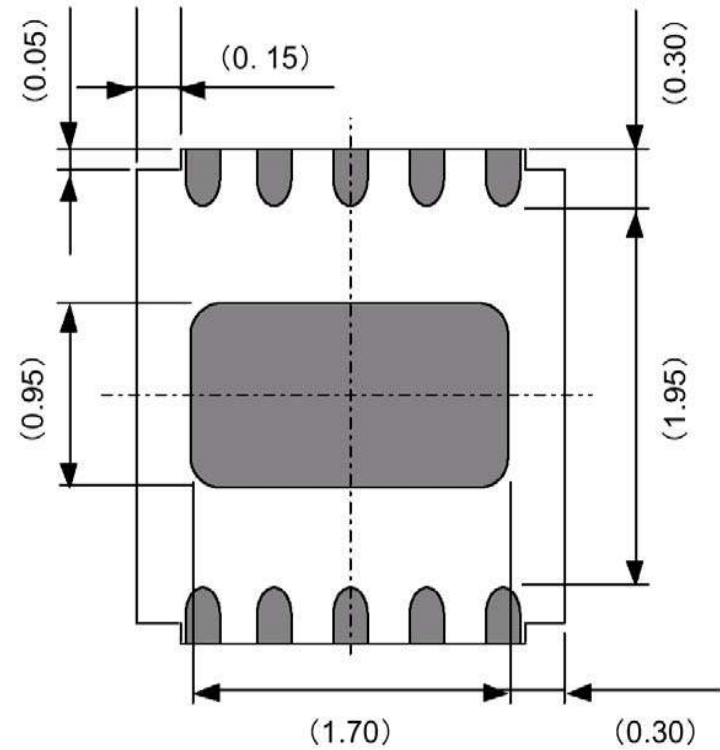
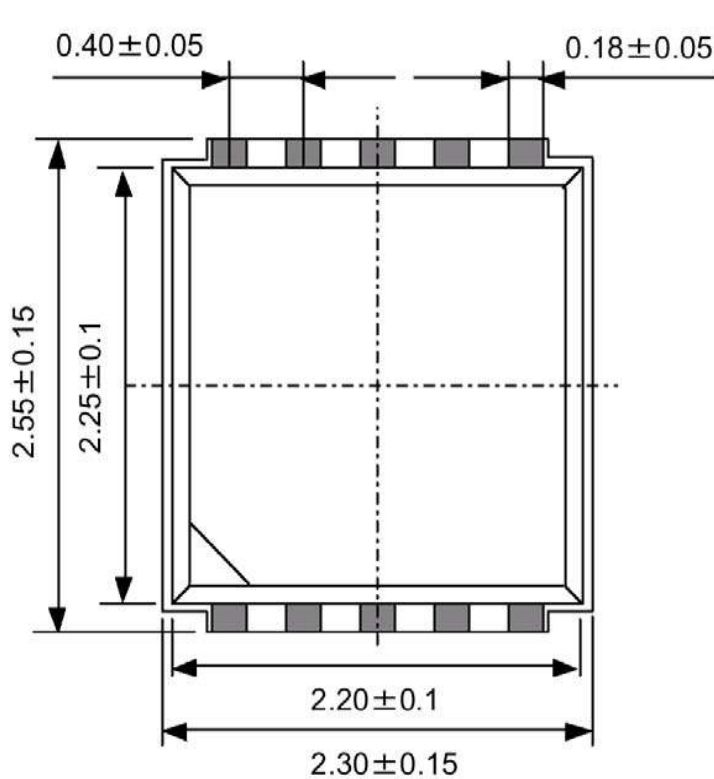
In Mass Production

10pin TSON PKG



Thickness: 0.6mm MAX  
Lead Pitch: 0.4mm

# Package Dimensions



**( Unit : mm )**

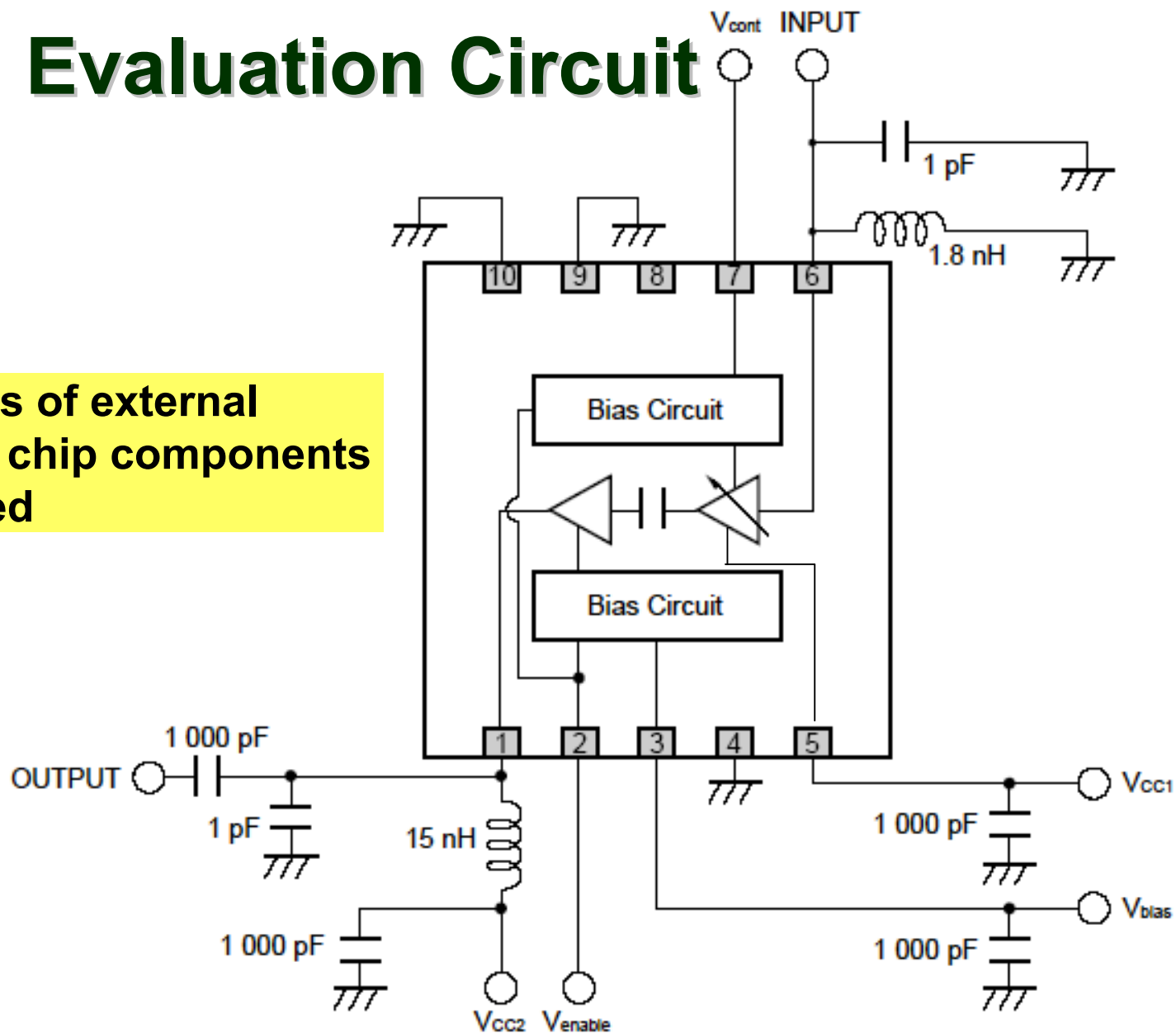
| Pin No. | Pin Name             | Applied Voltage (V) | Pin Voltage (V) | Function and Applications  | Internal Equivalent Circuit |
|---------|----------------------|---------------------|-----------------|--|-----------------------------|
| 1       | OUT/V <sub>CC2</sub> | 2.7 to 3.6          | –               | <p>Supply voltage and output pin of final stage amplifier.</p> <p>This collector output pin should supply voltage through external inductor, optimize external LC value for matching impedance and couple with capacitor to obtain output power.</p> |                             |
| 9       | GND                  | 0                   | –               | <p>GND pin of final stage amplifier.</p> <p>Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.</p>   |                             |

|   |              |            |   |  |   |
|---|--------------|------------|---|--|---|
| 2 | $V_{enable}$ | 0 to 3.1   | - | <p><b>Enable pin.</b></p> <p>This pin can control the operation of bias circuit and gain control circuit. The applied voltage should be minimized to shut down the operation. The worst current into this pin is approximately 1 mA.</p> | <p>Gain control of 1st stage amplifier</p> <p>Bias for interstage</p> |
| 3 | $V_{bias}$   | 2.7 to 3.6 | - | <p><b>Bias pin.</b></p> <p>Apply voltage to the bias circuit via this pin.</p>   |   |
| 7 | $V_{cont}$   | 0 to 3.6   | - | <p><b>Gain control pin of 1st stage amplifier.</b></p> <p>Since this device is a reverse control type, AGC control voltage should be maximized to get maximum gain. Current into this pin is approximately 0.3 mA.</p>                   |   |

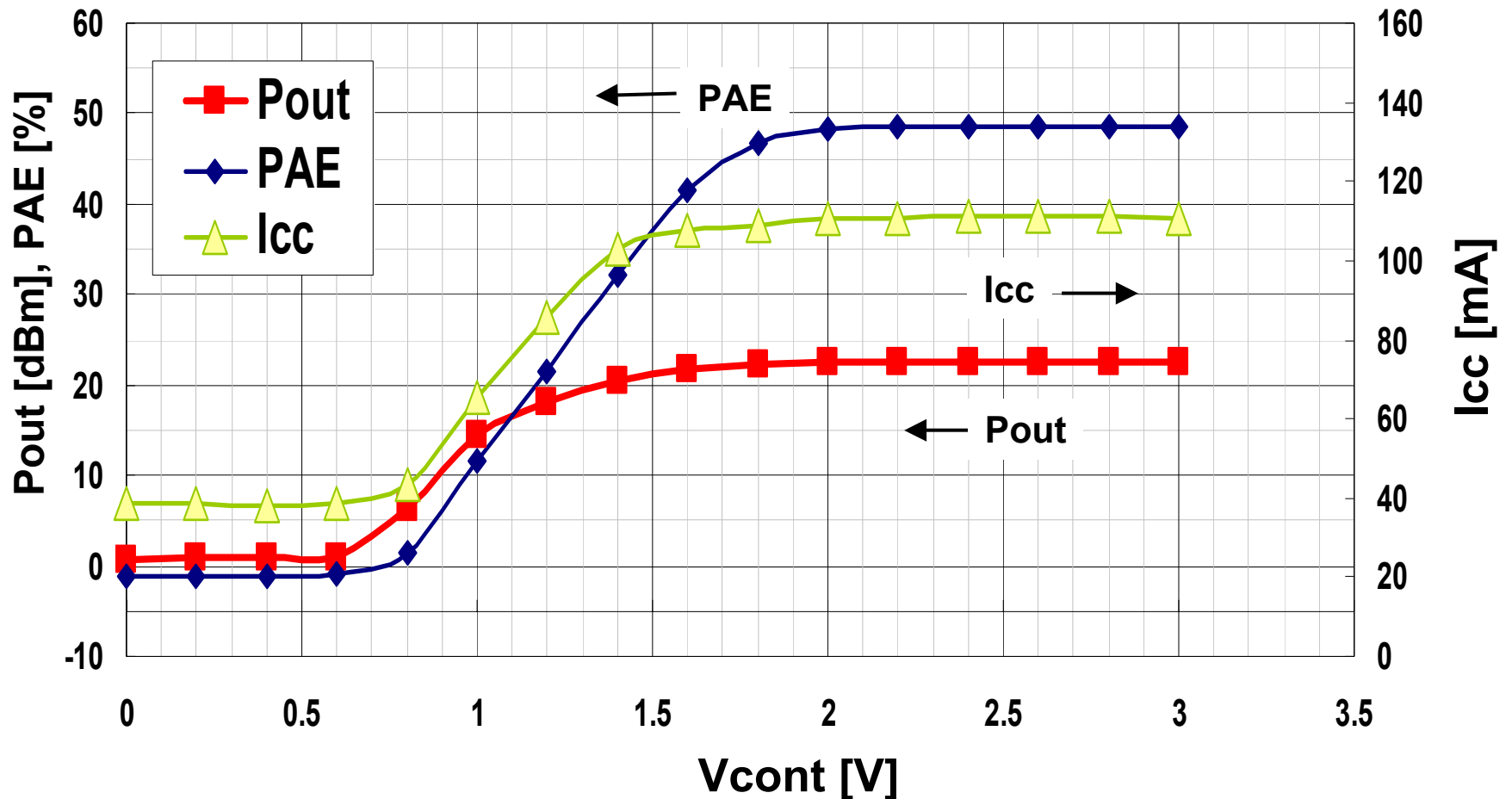
|   |                  |            |   |  |  |
|---|------------------|------------|---|--|--|
| 4 | GND              | 0          | - | <p>GND pin of 1st stage amplifier.</p> <p>Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.</p> |  |
| 5 | V <sub>CC1</sub> | 2.7 to 3.6 | - | <p>Supply voltage pin of 1st stage amplifier.</p> <p>This pin should be externally equipped with bypass capacitor (example: 1 000 pF) to minimize its impedance.</p>                           |  |
| 6 | INPUT            | -          | - | <p>Input pin of RF signal.</p> <p>This port is internally coupled with capacitor for DC blocking. The impedance matching circuit is externally needed.</p>                                     |  |

# Evaluation Circuit

Only 8 pcs of external 0603 size chip components are needed

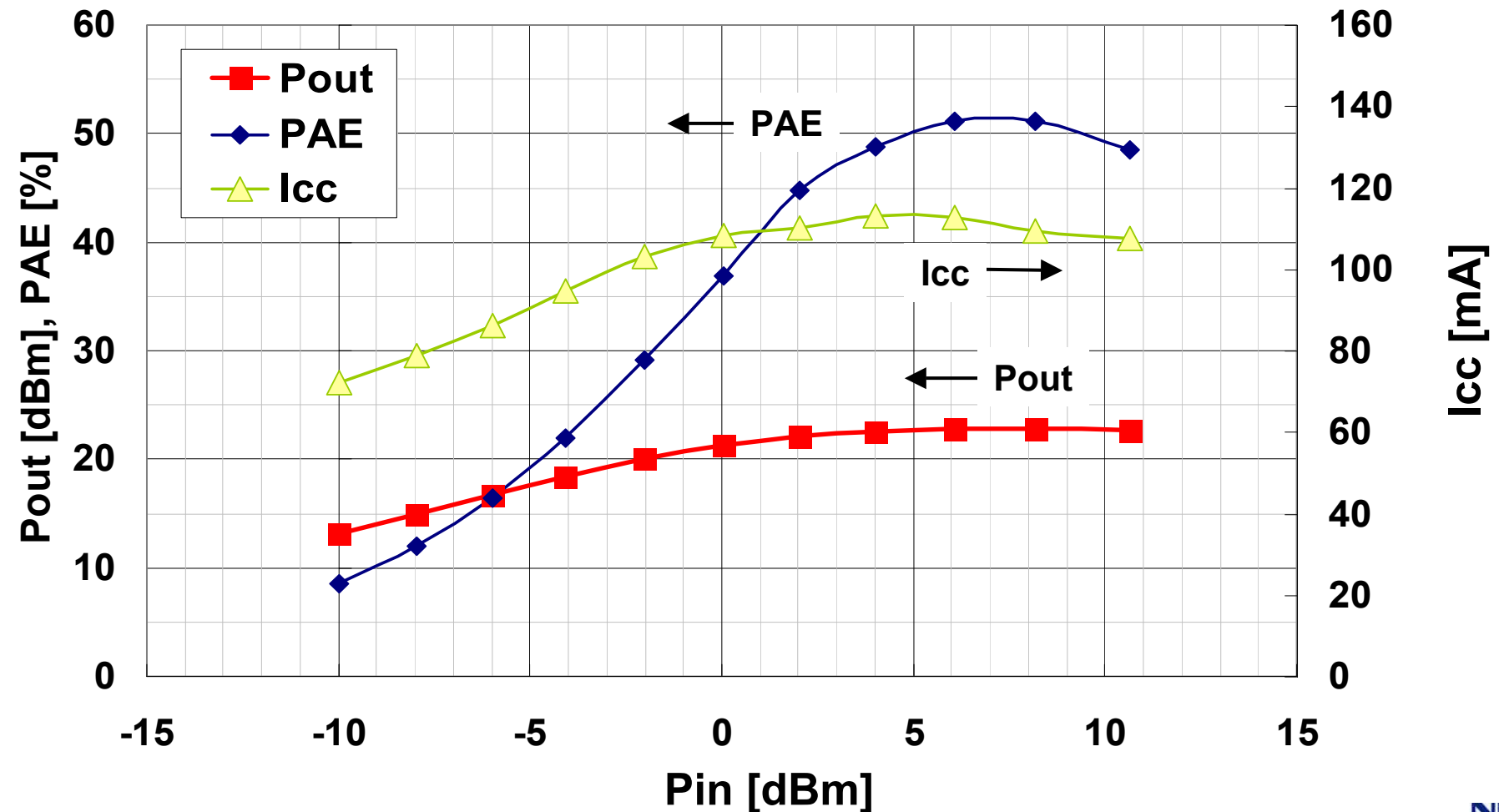


**Test Conditions** :  $f = 2450\text{MHz}$ ,  $V_{cc1}=V_{cc2}=V_{bias}=3.3\text{V}$ ,  $V_{enable}=2.9\text{V}$ ,  
 $P_{in}=+4\text{dBm}$ , with external input & output matching circuits

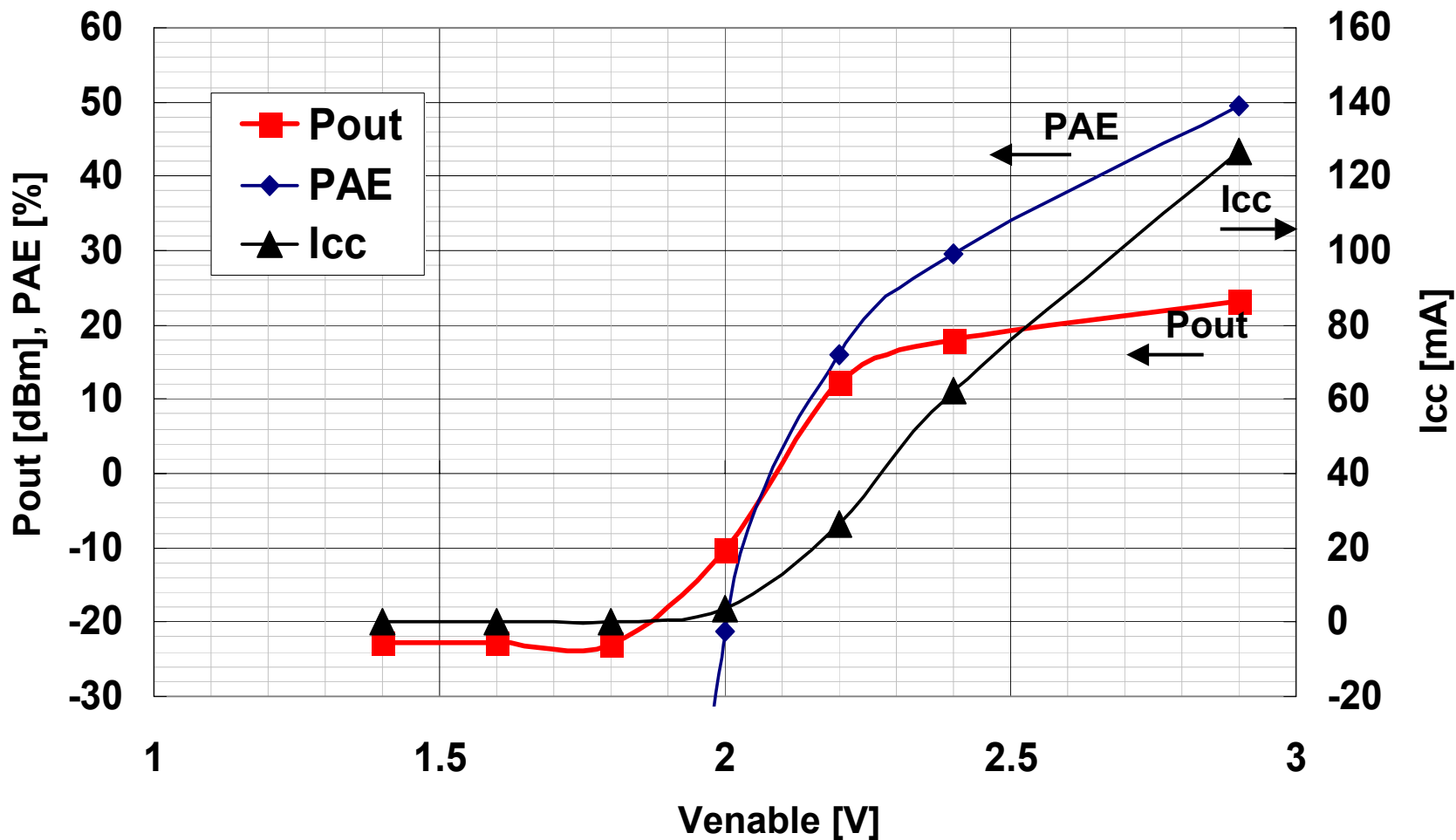




**Test Conditions** :  $f = 2450\text{MHz}$ ,  $V_{cc1}=V_{cc2}=V_{bias}=3.3\text{V}$ ,  $V_{enable}=2.9\text{V}$ ,  
 $V_{cont}=2.5\text{V}$ , with external input & output matching circuits

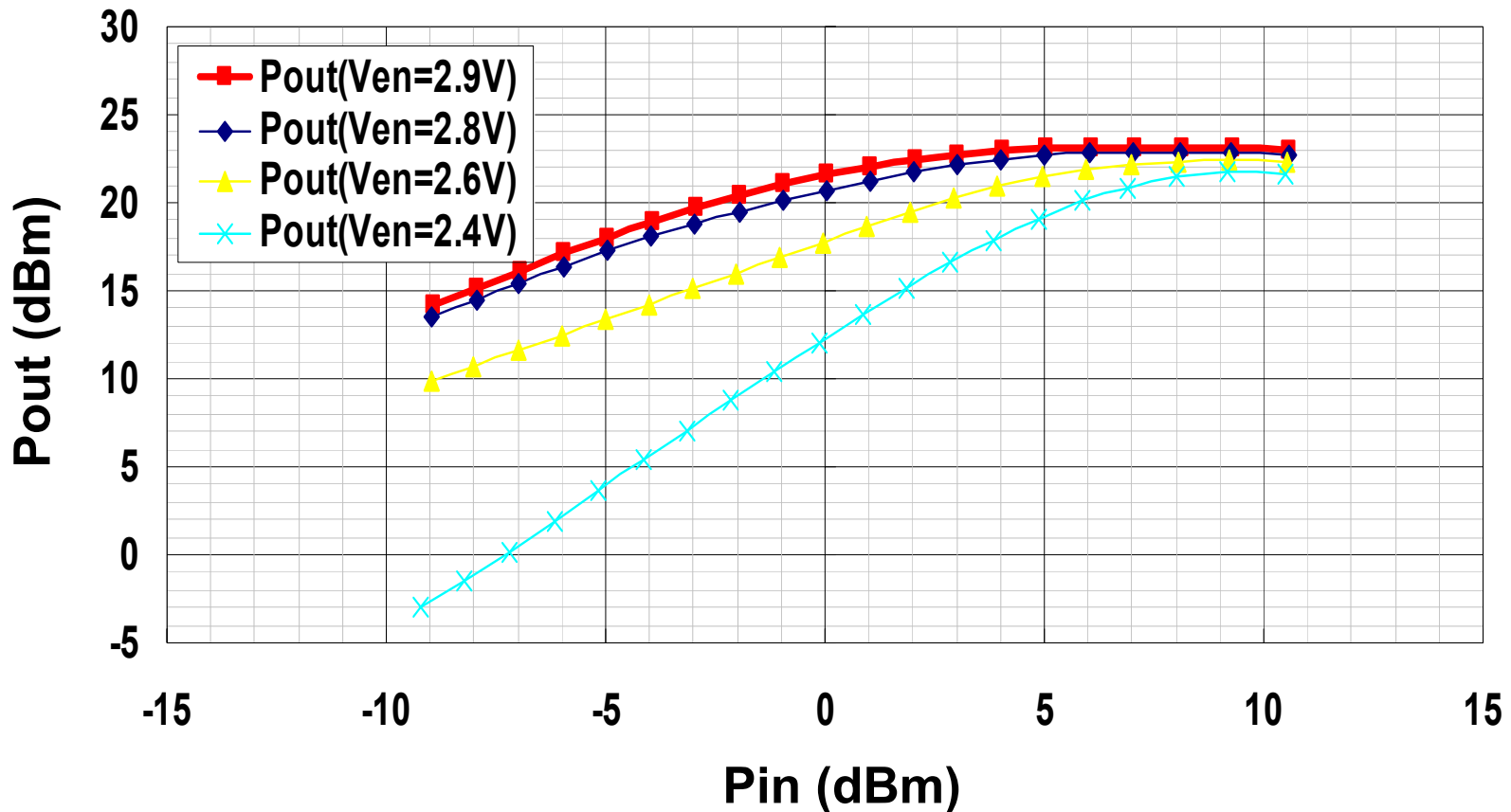


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 With external input & output matching circuits

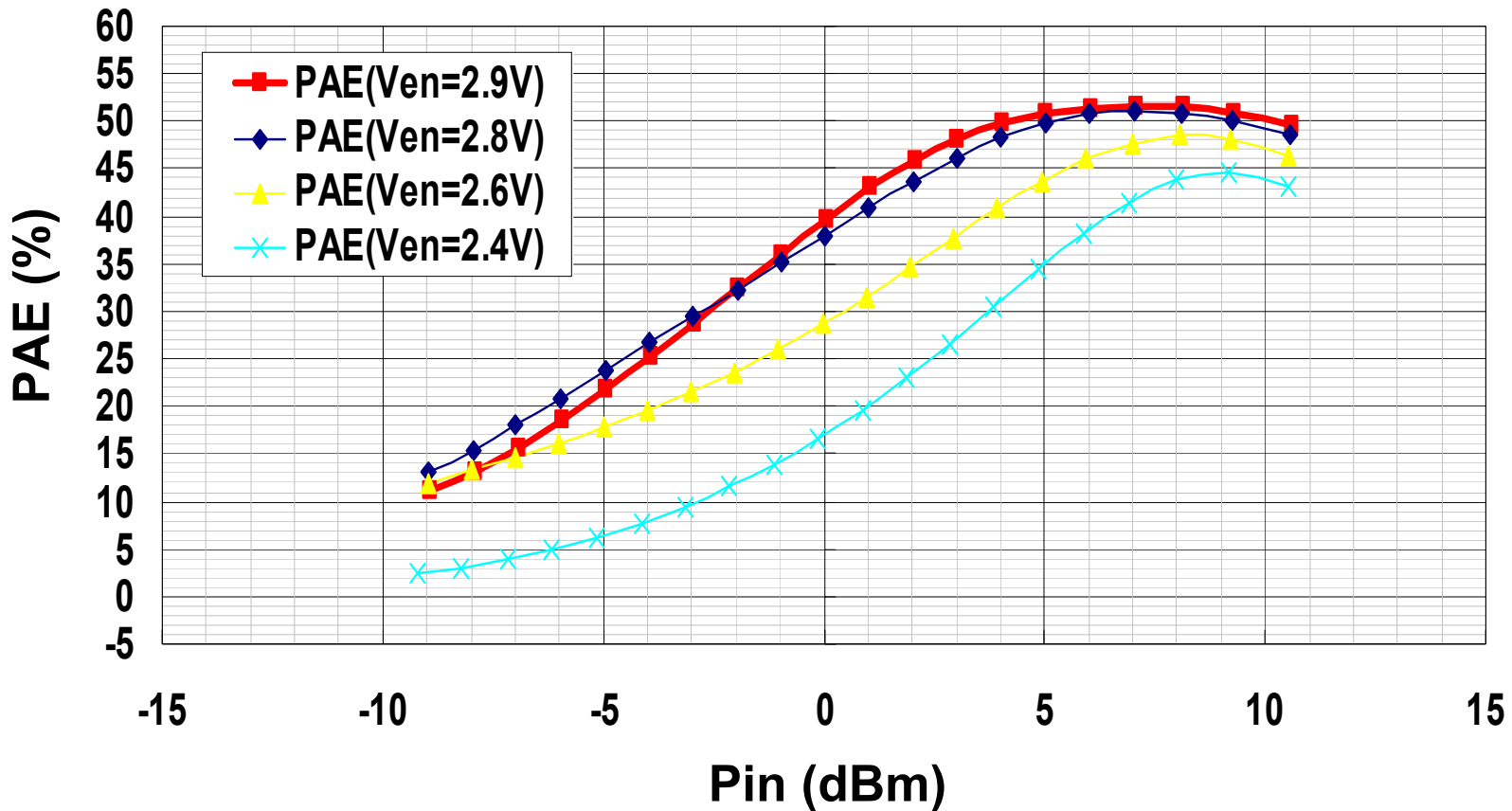


# CEL Venable Dependency for Pin vs. Pout

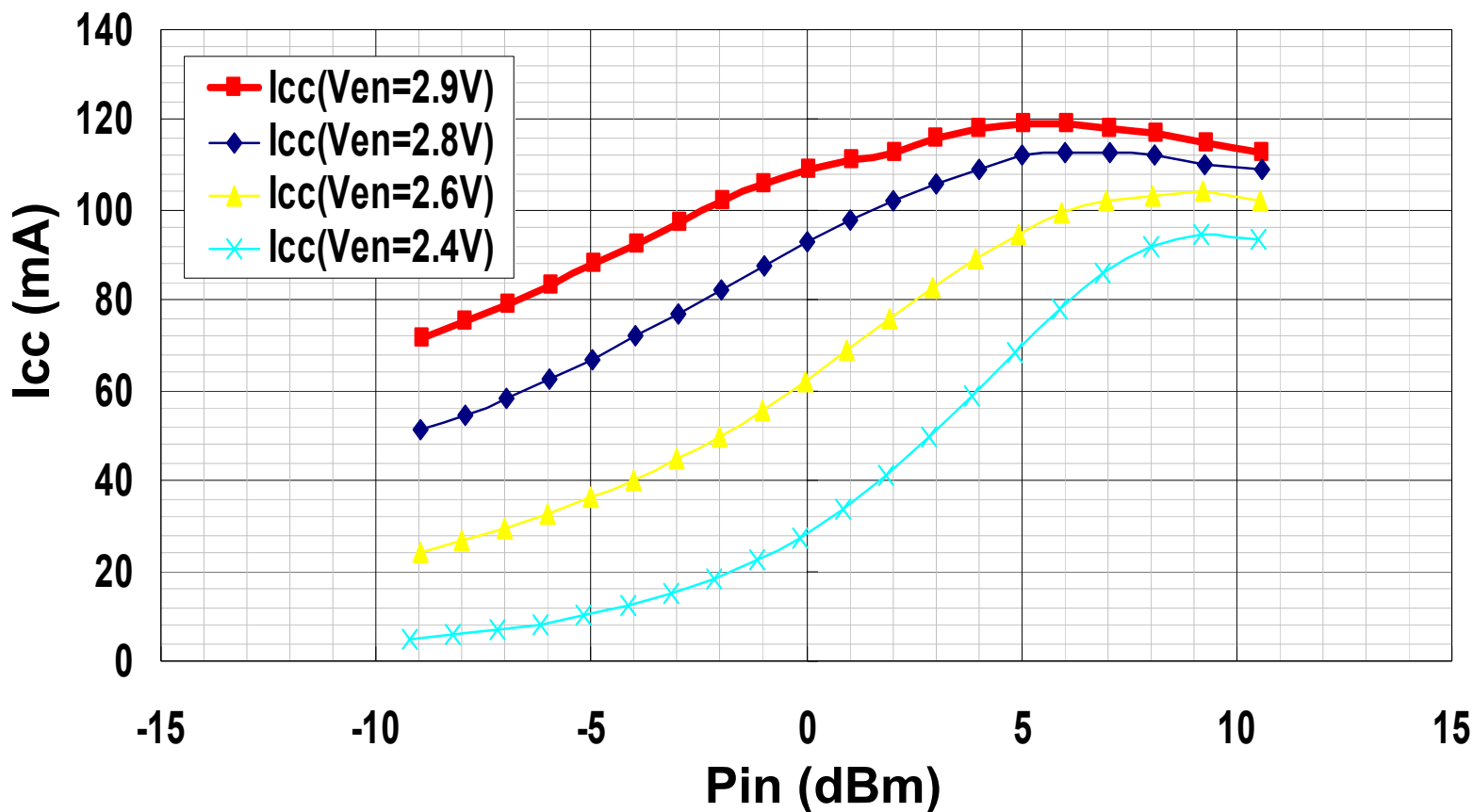
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**Test Conditions** :  $f = 2450\text{MHz}$ ,  $V_{cc1}=V_{cc2}=V_{bias}=3.3\text{V}$ ,  $V_{cont}=2.5\text{V}$ ,  
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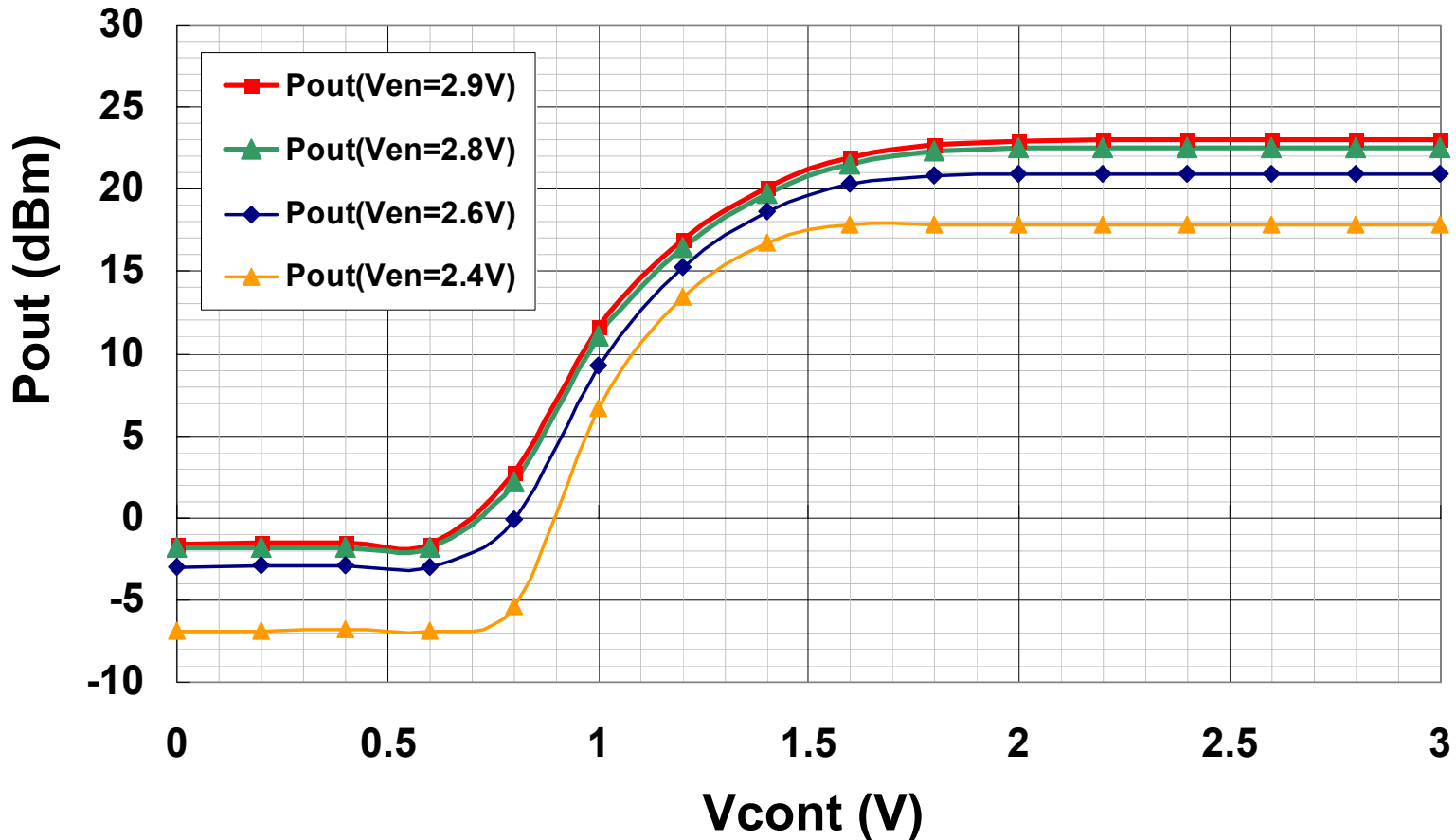


**Test Conditions** :  $f = 2450\text{MHz}$ ,  $V_{cc1}=V_{cc2}=V_{bias}=3.3\text{V}$ ,  $V_{cont}=2.5\text{V}$ ,  
with external input & output matching circuits

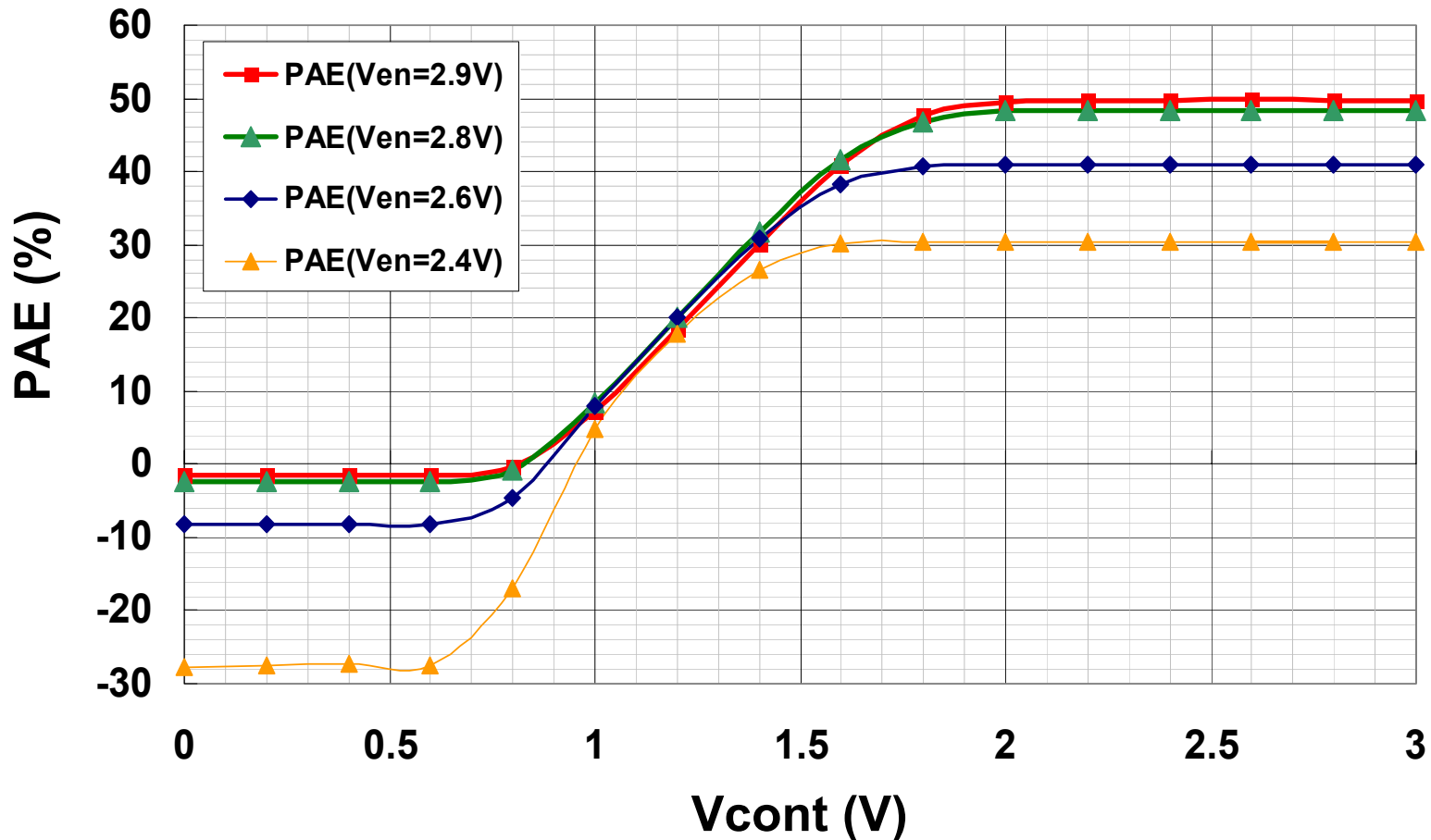


# Venable Dependency for Vcont vs. Pout

**Test Conditions** :  $f = 2450\text{MHz}$ ,  $V_{cc1}=V_{cc2}=V_{bias}=3.3\text{V}$ ,  $P_{in}=+4\text{dBm}$ ,  
with external input & output matching circuits



**Test Conditions** :  $f = 2450\text{MHz}$ ,  $V_{cc1}=V_{cc2}=V_{bias}=3.3\text{V}$ ,  $P_{in}=+4\text{dBm}$ ,  
with external input & output matching circuits



**Test Conditions** :  $f = 2450\text{MHz}$ ,  $V_{cc1}=V_{cc2}=V_{bias}=3.3\text{V}$ ,  $P_{in}=+4\text{dBm}$ ,  
with external input & output matching circuits

