

# MOSFET - Power, Single N-Channel 60 V, 9 mΩ, 48 A NVLJWS011N06CL

#### **Features**

- Small Footprint for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	60	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain	Steady	T <sub>C</sub> = 25°C	I <sub>D</sub>	48	Α
Current R <sub>θJC</sub> (Notes 1, 3)		T <sub>C</sub> = 100°C		34	
Power Dissipation	State	T <sub>C</sub> = 25°C	$P_{D}$	46	W
R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 100°C		23	
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	12	Α
Current R <sub>θJA</sub> (Notes 1, 2, 3)	Steady	T <sub>A</sub> = 100°C		8.5	
Power Dissipation	State	T <sub>A</sub> = 25°C	$P_{D}$	2.9	W
R <sub>θJA</sub> (Notes 1, 2)		T <sub>A</sub> = 100°C		1.4	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I <sub>DM</sub>	233	Α
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	38	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 2.3 A)			E <sub>AS</sub>	103	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

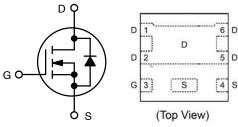
#### THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case	$R_{\theta JC}$	3.3	°C/W
Junction-to-Ambient	$R_{\theta JA}$	52	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX	
60 V	9 mΩ @ 10 V	48 A	
	13 mΩ @ 4.5 V	4074	

# **ELECTRICAL CONNECTION**



**N-CHANNEL MOSFET** 



#### WDFNW6 (2.05x2.05) CASE 515AD

## MARKING DIAGRAM



XXXX = Specific Device Code

A = Assembly Location

L = Wafer Lot Y = Year

W = Work Week

# **ORDERING INFORMATION**

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

## **ELECTRICAL CHARACTERISTICS**

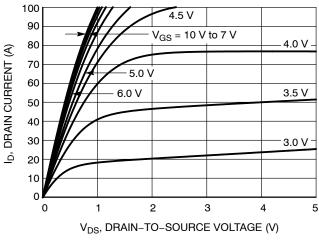
Parameter	Symbol	Test Conditions		Min	Тур	Max	Unit
OFF CHARACTERISTICS	<u> </u>				•		•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /				27.5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$ ,	T <sub>J</sub> = 25°C			10	μΑ
		V <sub>DS</sub> = 60 V	T <sub>J</sub> = 125°C			100	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS}$	= 20 V			100	nA
ON CHARACTERISTICS (Note 4)					-		
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A			7.7	9	mΩ
					10.7	13	1
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D$	= 34 μΑ	1.2		2.0	V
Gate Threshold Voltage Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-5.6		mV/°C
Forward Transconductance	9FS	V <sub>DS</sub> =6 V, I <sub>D</sub>	= 10 A		39		S
CHARGES AND CAPACITANCES					-		
Input Capacitance	C <sub>ISS</sub>				912		pF
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V			460		]
Reverse Transfer Capacitance	C <sub>RSS</sub>				8		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>DS</sub> = 48 V; I <sub>D</sub> = 10 A, V <sub>GS</sub> = 4.5 V			6.3		nC
Total Gate Charge	Q <sub>G(TOT)</sub>				13.6		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{DS} = 48 \text{ V}; I_D = 10 \text{ A},$ $V_{GS} = 10 \text{ V}$			1.4		
Gate-to-Source Charge	Q <sub>GS</sub>				2.5		
Gate-to-Drain Charge	$Q_{GD}$				1.4		
Plateau Voltage	V <sub>GP</sub>				2.7		V
SWITCHING CHARACTERISTICS (Note 5	)						
Turn-On Delay Time	t <sub>d(ON)</sub>				8.1		ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub>	<sub>S</sub> = 48 V,		23.3		]
Rise Time	t <sub>r</sub>	$I_D = 10 A, R_G$	$V_{GS}$ = 10 V, $V_{DS}$ = 48 V, $I_D$ = 10 A, $R_G$ = 6 $\Omega$		3.0		
Fall Time	t <sub>f</sub>				3.6		
SOURCE-TO-DRAIN DIODE CHARACTE	RISTICS						
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.82	1.2	V
			T <sub>J</sub> = 125°C		0.69		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dl/dt = 100 Α/μs, I <sub>SD</sub> = 10 A, V <sub>DS</sub> = 48 V			32		ns
Charge Time	ta				15.8		]
Discharge Time	t <sub>b</sub>				16		
Reverse Recovery Charge	Q <sub>RR</sub>				20		nC

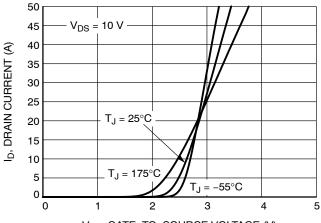
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

#### TYPICAL CHARACTERISTICS





V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V) Figure 2. Transfer Characteristics



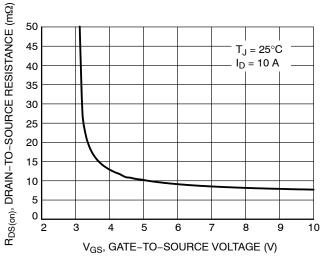


Figure 3. On-Resistance vs. Gate-to-Source Voltage

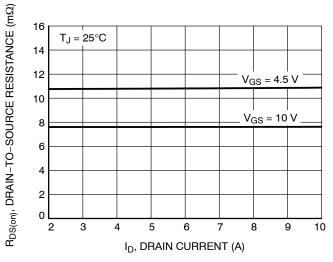


Figure 4. On-Resistance vs. Drain Current and **Gate Voltage** 

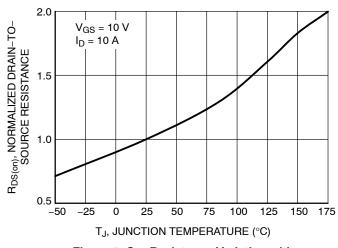


Figure 5. On-Resistance Variation with **Temperature** 

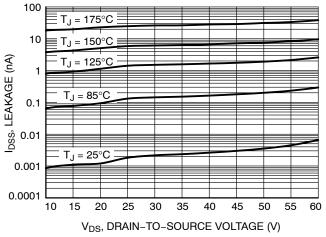
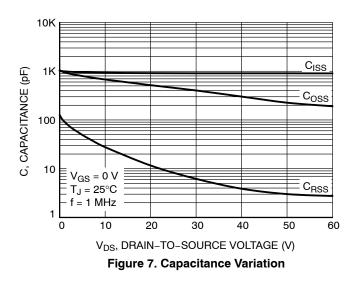


Figure 6. Drain-to-Source Leakage Current vs. Voltage

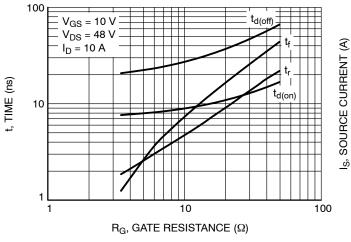
#### **TYPICAL CHARACTERISTICS**



0 2 4 6 8 10 12 14

QG, TOTAL GATE CHARGE (nC)

Figure 8. Gate-to-Source Voltage vs. Total Charge



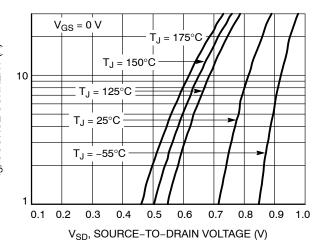
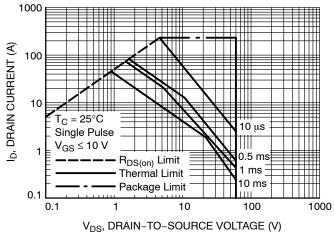


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current



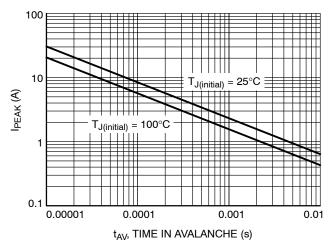


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Drain Current vs. Time in Avalanche

## **TYPICAL CHARACTERISTICS**

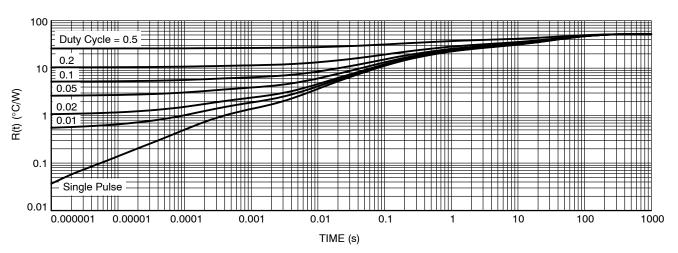


Figure 13. Transient Thermal Impedance

#### **DEVICE ORDERING INFORMATION**

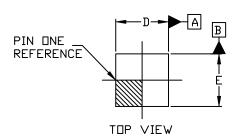
Device	Marking	Package	Shipping <sup>†</sup>
NVLJWS011N06CLTAG	011N	WDFNW6 (Pb-Free, Wettable Flanks)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

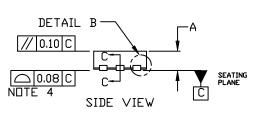
#### WDFNW6 2.05x2.05, 0.65P

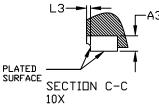
CASE 515AD **ISSUE O** 

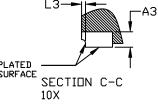


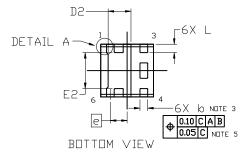
#### NOTES:

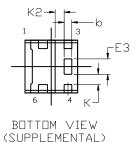
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M,
- 2009.
  CONTROLLING DIMENSION: MILLIMETERS
  DIMENSION & APPLIES TO PLATED TERMINALS AND IS
  MEASURED BETWEEN 0.15 AND 0.30MM FROM THE
- TERMINAL TIP.
  COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL
  AS THE TERMINALS.
  POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD
  AS WELL AS THE TERMINALS.



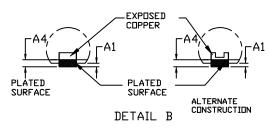


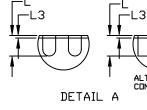


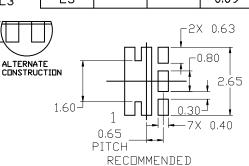




	MILLIMETERS			
DIM	MIN.	N□M.	MAX.	
Α	0.70	0.75	0.80	
A1	0.00		0.05	
A3	(	0.20 REF	_	
Α4	0.10	-		
ھ	0.25	0.30	0.35	
D	1.95	2.05	2.15	
D2	0.84	0.89	0.94	
Е	1.95	2.05	2.15	
E2	1.35	1.40	1,45	
E3	0.55	0.60	0.65	
e	0.65 BSC			
К	0.40 REF			
К2	0.35 REF			
L	0.275	0.325	0.375	
L3			0.09	







MOUNTING FOOTPRINT For additional information on our Pb-Free strategy and soldering details, please download the IIN Seniconductor Soldering and Mounting Techniques Reference Manual, SILLERRHYD.

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