TPS53124 Dual Synchronous Step-Down Controller For Low-Voltage Power Rails

1 Features

- High Efficiency, Low-Power Consumption
- D-Cap Mode Enables Fast Transient Response
- High Initial Reference Accuracy
- Low Output Ripple
- Wide Input Voltage Range: 4.5 V to 24 V
- Output Voltage Range: 0.76 V to 5.5 V
- Low-Side $R_{DS(on)}$ Loss-less Current Sensing
- Adaptive Gate Drivers with Integrated Boost Diode
- Internal 1.2-ms Voltage-Servo Soft Start
- Built-In 5-V Linear Regulator

2 Applications

- Digital TV Power Supply
- Networking Home Terminal
- Digital STB

3 Description

The TPS53124 is a dual, Adaptive on-time DCAP™ mode synchronous controller. The part enables system designers to cost effectively complete the suite of digital TV power bus regulators with the absolute lowest external component count and lowest standby consumption. The main control loop for the TPS53124 uses the D-CAP™ mode that optimized for low ESR output capacitors such as POSCAP or SP-CAP promises fast transient response with no external compensation. The part provides a convenient and efficient operation with conversion voltages from 4.5 V to 24 V and output voltage from 0.76 V to 5.5 V.

The TPS53124 is available in the 24-pin RGE package and in the 28-pin PW package and is specified from -40°C to 85°C ambient temperature range.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
TPS53124	PW (28)	9.70 mm x 6.40 mm
TPS53124	QFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematics

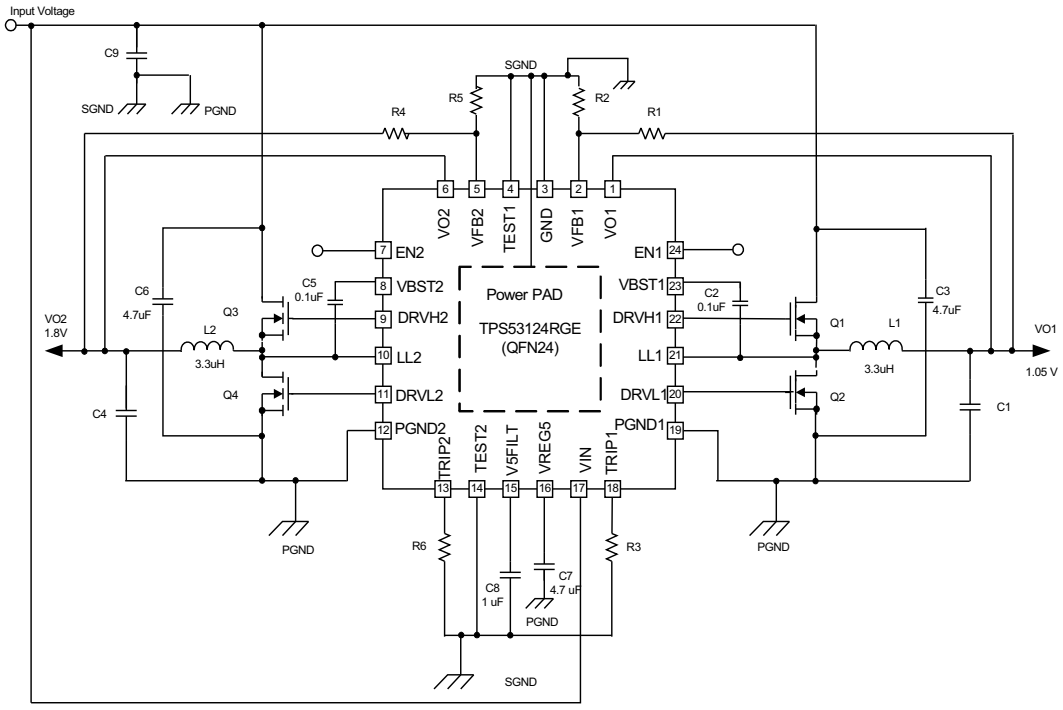
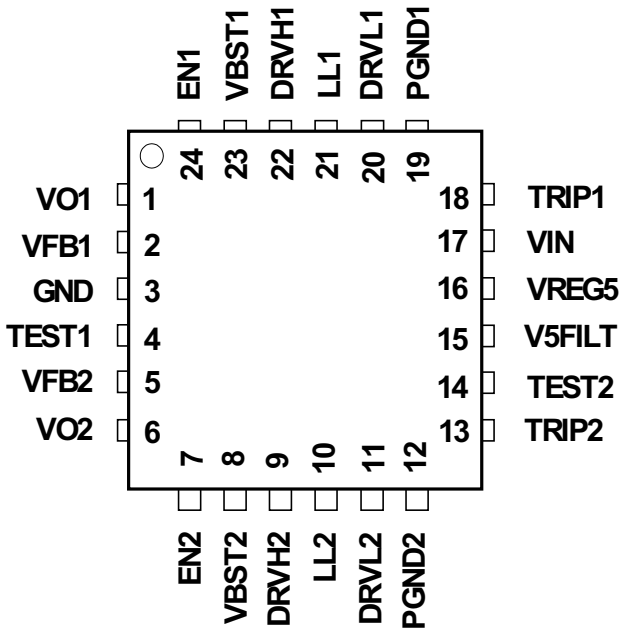


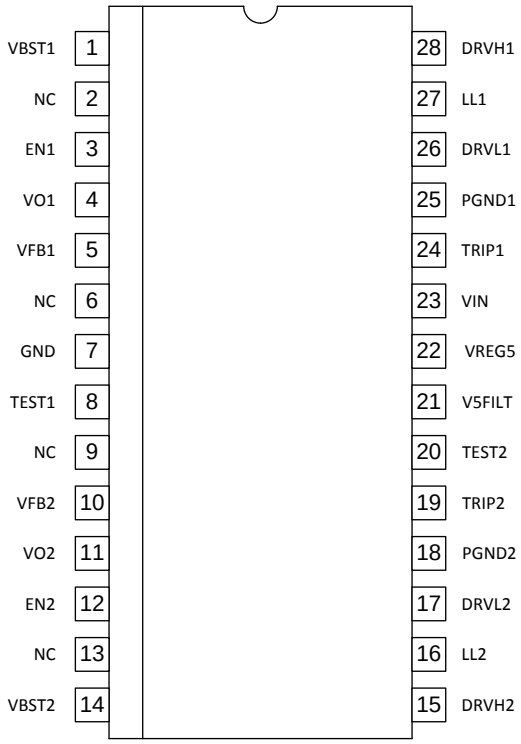
Table of Contents

5 Pin Configuration and Functions

QFN Package
24 Pins
Top View



TSSOP Package
28 Pins



Pin Functions

PIN			I/O	DESCRIPTION
NAME	GFN24	TSSOP28		
VBST1, VBST2	23, 8	1, 14	I	Supply input for high-side NFET driver (boost terminal). Connect capacitor from this pin to respective LL terminals. An internal PN diode is connected between VREG5 to each of these pins. User can add external schottky diode if forward drop is critical to drive the NFET.
EN1, EN2	24, 7	3, 12	I	Channel 1 and Channel 2 enable pins.
VO1, VO2	1, 6	4, 11	I	Output connections to SMPS. These terminals serve ON-time adjustment, output discharge.
VFB1, VFB2	2, 5	5, 10	I	SMPS feedback inputs. Connect with feedback resistor divider.
GND	3	7	I	Signal ground pin.
DRVH1, DRVH2	22, 9	28, 15	O	High-side NFET driver outputs. LL referenced floating drivers. The gate drive voltage is defined by the voltage across VBST to LL node flying capacitor.
LL1, LL2	21, 10	27, 16	I/O	Switch-node connections for high-side drivers. Also serve as input to current comparators.
DRVL1, DRVL2	20, 11	26, 17	O	Synchronous NFET driver outputs. PGND referenced drivers. The gate drive voltage is defined by VREG5 voltage.
PGND1, PGND2	19, 12	25, 18	I/O	Ground returns for DRVL1 and DRVL2. Also serve as input of current comparators. Connect PGND1, PGND2 and GND strongly together near the device.
TRIP1, TRIP2	18, 13	24, 19	I	Over-current trip point set input. Connect resistor from this pin to GND to set threshold for synchronous $R_{DS(on)}$ sense. Voltage across this pin and GND is compared to voltage across PGND and LL at over current comparator.
VIN	17	23	I	Supply Input for 5-V linear regulator.
V5FILT	15	21	I	5-V supply input for the entire control circuit except the NFET drivers. Connect capacitor (typical 1 µF) from GND to V5FILT. V5FILT is connected to VREG5 via internal resistor.
VREG5	16	20	O	5-V power supply output. VREG5 is connected to V5FILT via internal resistor.
TEST1, TEST2	4, 14	8, 20	I/O	Used for test only. Pin should be connected to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage Range	VIN,EN1,EN2	–0.3	26	V
	VBST1,VBST2	–0.3	32	
	VBST1,VBST2(wrt LLx)	–0.3	6	
	V5FILT,VFB1,VFB2,TRIP1,TRIP2,VO1,VO2, TEST1,TEST2	–0.3	6	
Output Voltage Range	DRVH1, DRVH2	–1	32	V
	DRVH1, DRVH2 (wrt LLx)	–0.3	6	
	LL1,LL2	–2	26	
	DRVL1,DRVL2,VREG5	–0.3	6	
	PGND1, PGND2	–0.3	0.3	
Operating ambient temperature range, T_A		–40	85	°C
Junction Temperature Range, T_J		–40	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply Input Voltage Range	VIN	4.5		24	V
		V5FILT	4.5		5.5	
	Input Voltage Range	VBST1, VBST2	–0.1		30	V
		VBST1, VBST2 (wrt LLx)	–0.1		5.5	
		VFB1, VFB2, VO1, VO2	–0.1		5.5	
		TRIP1, TRIP2	–0.1		0.3	
		EN1, EN2	–0.1		24	
	Output Voltage Range	DRVH1, DRVH2	–0.1		30	V
		VBST1, VBST2 (wrt LLx)	–0.1		5.5	
		LL1, LL2	1.8		24	
		DRVL1, NCDRVL2, VREG5	–0.11		5.5	
		PGND1, PGND2	–0.1		0.1	
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	

6.4 Thermal Information

THERMAL METRIC(1)		TPS53124 TSSOP (PW) 28 PINS	TPS53124 RGE (QFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.3	35.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.0	39.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	13.6	
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.5	
ψ_{JB}	Junction-to-board characterization parameter	37.8	13.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
I_{IN}	VIN supply current	VIN current, T_A = 25°C, VREG5 tied to V5FLT, EN1 = EN2 = 5 V, VFB1 = VFB2 = 0.8 V, LL1 = LL2 = 0.5 V		450	800	µA
I_{VINSDN}	VIN shutdown current	VIN current, T_A = 25°C, no load, EN1 = EN2 = 0 V			10	
VFB Voltage and Discharge Resistance						
V_{BG}	Bandgap initial regulation accuracy	T_A = 25°C	–1%		1%	
V_{VFBTH}	VFB threshold voltage	T_A = 25°C	755	765	775	mV
		T_A = -40°C to 85°C	752		778	
I_{VFB}	VFB input current	VFBx = 0.8 V, T_A = 25°C		–0.01	±0.1	µA
R_{DISCHG}	V_O discharge resistance	ENx = 0 V, VOx = 0.5 V,T_A = 25°C		40	80	Ω
VREG5 Output						
V_{VREG5}	VREG5 output voltage	T_A = 25°C ,5.5 V < VIN < 24 V, 0 < I_{VREG5} < 10 mA	4.6	5	5.2	V
V_{LN5}	Line regulation	5.5 V < VIN < 24 V, I_{VREG5} = 10 mA			20	mV
V_{LD5}	Load regulation	1 mA < I_{VREG5} < 10 mA			40	
I_{VREG5}	Output current	VIN = 5.5 V, VREG5 = 4.0 V, T_A = 25°C		170		mA
Output: N-Channel MOSFET Gate Drivers						
R_{DRVH}	DRVH resistance	Source, I_{DRVHx} = -100 mA		5.5	11	Ω
		Sink, I_{DRVHx} = 100 mA		2.5	5	
R_{DRVL}	DRVL resistance	Source, I_{DRVLx} = –100 mA		4	12	Ω
		Sink, I_{DRVLx} = 100 mA		2	4	
T_D	Dead time	DRVHx-low to DRVLx-on	20	50	80	ns
		DRVLx-low to DRVHx-on	20	40	80	
Internal BST Diode						
V_{FBST}	Forward voltage	$V_{VREG5-VBSTx}$, I_F = 10 mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	VBST = 29 V, LL = 24 V, T_A = 25°C		0.1	1	µA
ON-Time Timer Control						
T_{ON1}	CH1 ON time	LL1 = 12 V, VO1 = 1.5 V		390		ns
T_{ON2}	CH2 ON time	LL2 = 12 V, VO2 = 1.05 V		210		
$T_{ON(min)}$	CH2 ON time	LL2 = 12 V, VO2 = 0.76 V		160		
$T_{OFF(min)}$	CH1/CH2 min OFF time	LL = 0.7 V T_A = 25°C, VFB = 0.7 V		390		
Soft Start						
T_{SS}	Internal SS time	Internal soft start VFB = 0.735 V	0.85	1.2	1.4	ms

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
$V_{UV5VFILT}$	V5FILT UVLO threshold	Wake up	3.7	4	4.3	V
		Hysteresis	0.2	0.3	0.4	
LOGIC Threshold						
V_{ENH}	ENx H-level input voltage	EN 1/2	2			V
V_{ENL}	ENx L-level input voltage	EN 1/2			0.3	
Current Sense						
I_{TRIP}	TRIP source current	VTRIPx = 0.1 V, T_A = 25°C	8.5	10	11.5	µA
TC_{ITRIP}	I_{TRIP} temperature coefficient	On the basis of 25°C		4000		ppm/°C
$V_{OCL(off)}$	OCP compensation offset	($V_{TRIPx-GND}$ - $V_{PGNDx-LLx}$) voltage,$V_{TRIPx-GND}$ = 60 mV, T_A = 25°C	–10	0	10	mV
		($V_{TRIPx-GND}$ - $V_{PGNDx-LLx}$) voltage, $V_{TRIPx-GND}$ = 60 mV	–15		15	
$V_{R(trip)}$	Current limit threshold setting range	$V_{TRIPx-GND}$ voltage	30		200	
Output Undervoltage and Overvoltage Protection						
V_{OVP}	Output OVP trip threshold	OVP detect	110%	115%	120%	
T_{OVPDEL}	Output OVP prop delay			1.5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis (recovery < 20 µs)		10%		
T_{UVPDEL}	Output UVP delay		17	30	40	µs
T_{UVPEN}	Output UVP enable delay		1.2	2	2.5	ms
Thermal Shutdown						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		150		°C
		Hysteresis(1)		20		

(1) Ensured by design. Not production tested.

6.6 Typical Characteristics

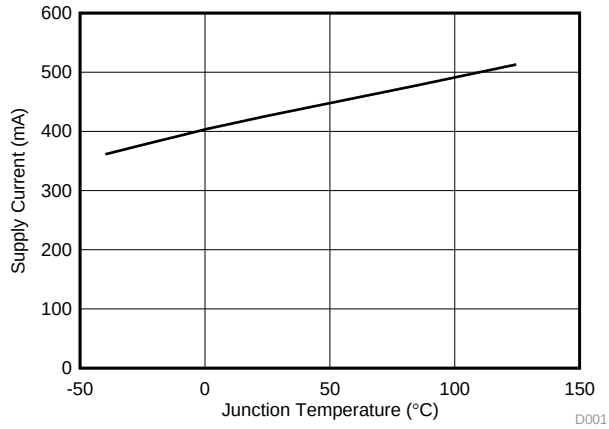


Figure 1. VIN Supply Current vs Junction Temperature

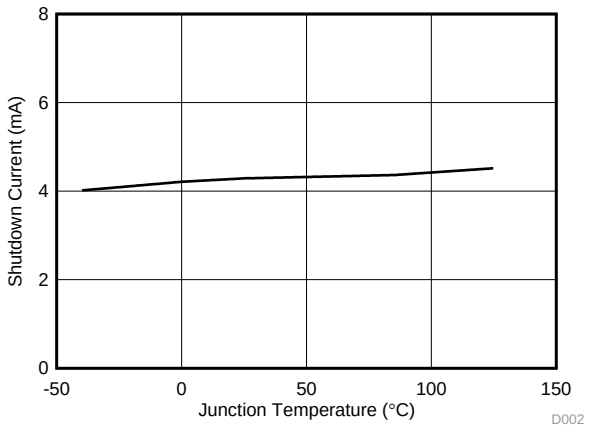


Figure 2. VIN Shutdown Current vs Junction Temperature

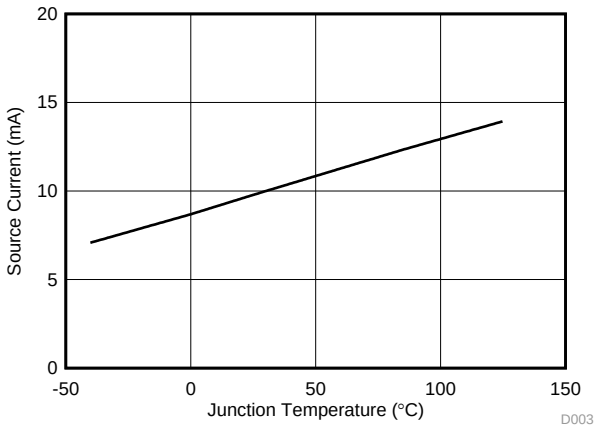


Figure 3. ITRIP Source Current vs Junction Temperature

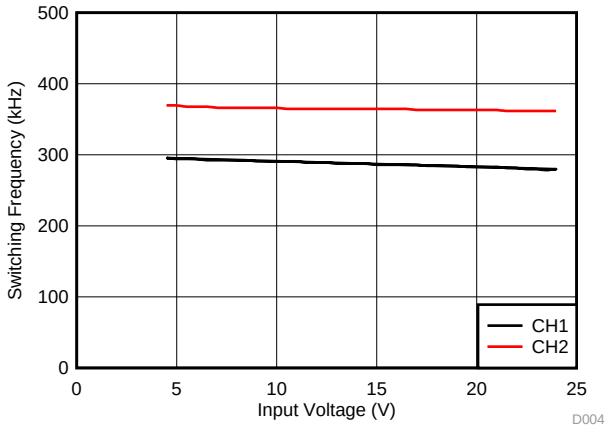


Figure 4. Switching Frequency vs Input Voltage

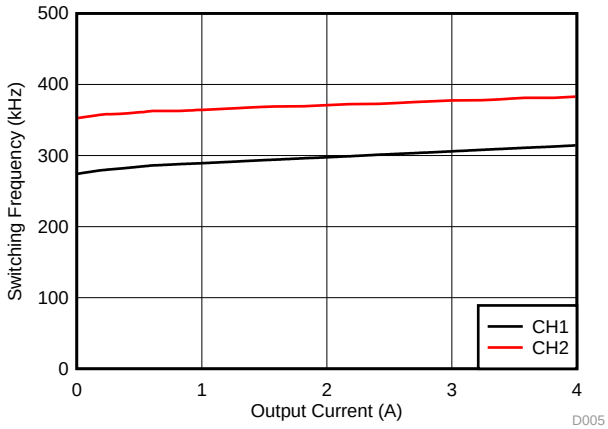


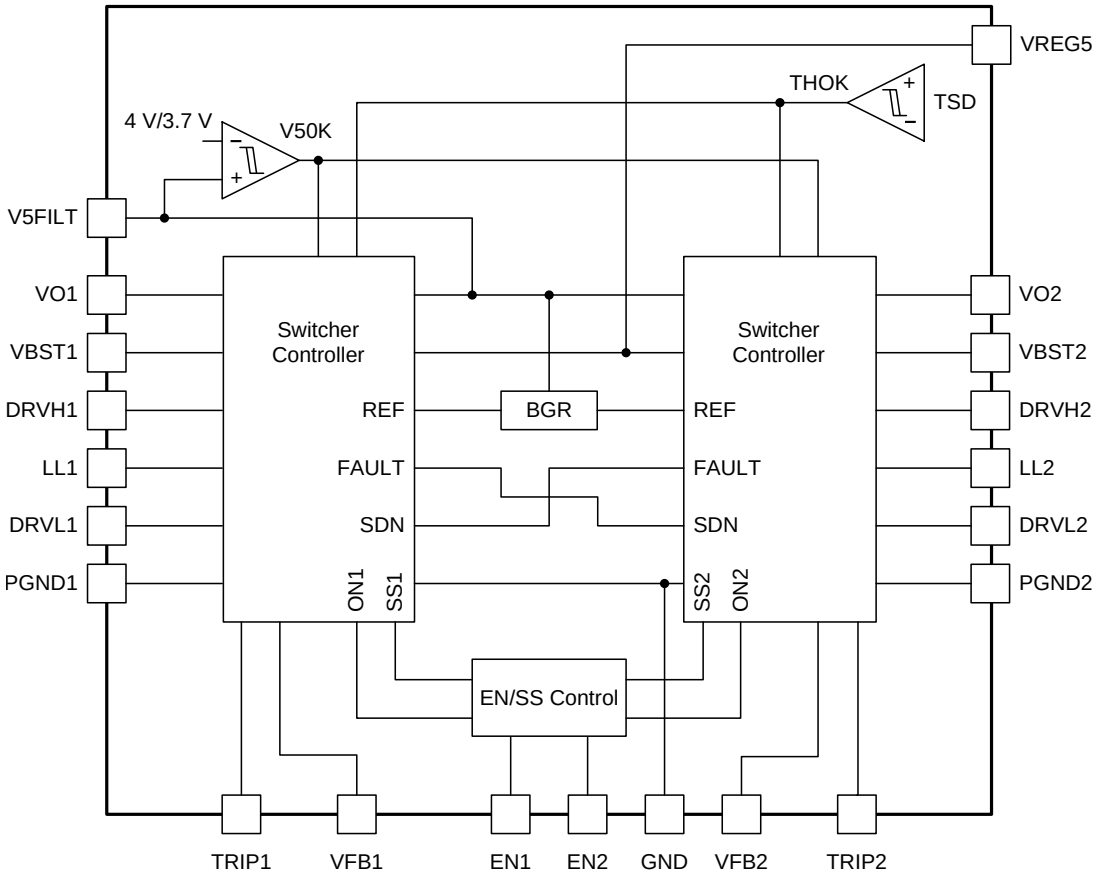
Figure 5. Switching Frequency vs Output Current

7 Detailed Description

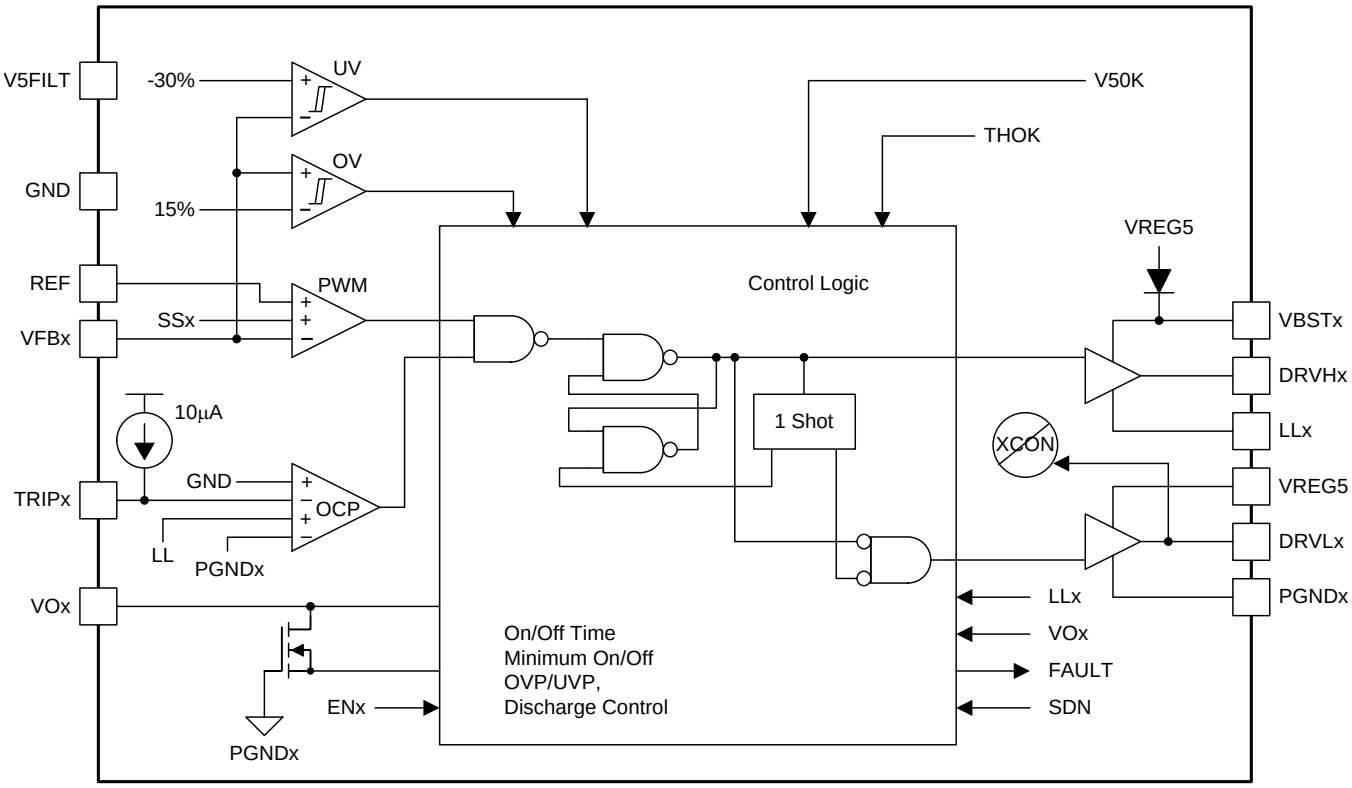
7.1 Overview

The TPS53124 is a dual, Adaptive on-time DCAP™ mode synchronous controller. The part enables system designers to cost effectively complete the suite of digital TV power bus regulators with the absolute lowest external component count and lowest standby consumption. The main control loop for the TPS53124 uses the D-CAP™ mode that optimized for low ESR output capacitors such as POSCAP or SP-CAP promises fast transient response with no external compensation. The part provides a convenient and efficient operation with conversion voltages from 4.5 V to 24 V and output voltage from 0.76 V to 5.5 V.

7.2 Functional Block Diagram



Functional Block Diagram (continued)



7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the switching mode power supply (SMPS) is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports a proprietary D-CAP™ Mode. D-CAP™ Mode uses internal compensation circuit and is suitable for low external component count configuration with appropriate amount of ESR at the output capacitor(s). The output ripple bottom voltage is monitored at a feedback point voltage.

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or becomes ON state. This MOSFET is turned off, or becomes OFF state, after internal one-shot timer expires. This one shot is determined by the converter's input voltage ,VIN, and the output voltage ,VOUT, to keep frequency fairly constant over the input voltage range, hence it is called adaptive on-time control. The high-side MOSFET is turned on again when feedback information indicates insufficient output voltage. Repeating operation in this manner, the controller regulates the output voltage.

7.3.2 Low-Side Driver

The low-side driver is designed to drive high current low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. 5-V bias voltage is delivered from internal regulator VREG5 output. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND. The average drive current is equal to the gate charge at V_{GS} = 5 V times switching frequency. This gate drive current as well as the high-side gate drive current times 5 V makes the driving power which need to be dissipated from TPS53124 package.

7.3.3 High-Side Driver

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from VREG5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5 V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBSTx and LLx pins. The drive capability is represented by its internal resistance.

7.3.4 PWM Frequency and Adaptive On-Time Control

TPS53124 employs adaptive on-time control scheme and does not have a dedicated oscillator on board. However, the part runs with pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The on-time is controlled inverse proportional to the input voltage and proportional to the output voltage so that the duty ratio will be kept as VOUT/VIN technically with the same cycle time.

7.3.5 Soft Start

The TPS53124 has an internal, 1.2 ms, voltage servo soft start for each channel. When the ENx pin becomes high, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up. As TPS53124 shares one DAC with both channels, if ENx pin is set to high while another channel is starting up, soft start is postponed until another channel soft start has completed. If both of EN1 and EN2 are set high at a same time, both channels start up at same time.

7.3.6 Output Discharge Control

TPS53124 discharges the output when ENx is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). TPS53124 discharges outputs using an internal 40-Ω MOSFET which is connected to VOx and PGNDx. The external low-side MOSFET is not turned on for the output discharge operation to avoid the possibility of causing negative voltage at the output.

This discharge ensures that, on start, the regulated voltage always start from zero volts.

Feature Description (continued)

7.3.7 Current Protection

TPS53124 has cycle-by-cycle over current limiting control. The inductor current is monitored during the 'OFF' state and the controller keeps the OFF state during the inductor current is larger than the over-current trip level. In order to provide both good accuracy and cost effective solution, TPS53124 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. TRIPx pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. TRIPx terminal sources 10-µA I_{TRIP} current at the ambient temperature and the trip level is set to the OCL trip voltage V_{TRIP} as below:

$$V_{TRIP}(mV) = R_{TRIP}(k\Omega) \times 10(\mu A) \quad (1)$$

The trip level should be in the range of 30 mV to 200 mV over all operational temperature. The inductor current is monitored by the voltage between PGNDx pin and LLx pin. I_{TRIP} has 4000ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. PGNDx is used as the positive current sensing node so that PGNDx should be connected to the source terminal of the bottom MOSFET.

As the comparison is done during the OFF state, V_{TRIP} sets valley level of the inductor current. Thus, the load current at over-current threshold, I_{OCP}, can be calculated as follows:

$$I_{OCP} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up with crossing the under voltage protection threshold and shutdown.

7.3.8 Over/Under Voltage Protection

TPS53124 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 30 µs, TPS53124 latches OFF both top and bottom MOSFET drivers, and shut off both drivers of another channel. This function is enabled approximately 2.0 ms.

7.3.9 UVLO Protection

TPS53124 has V5FILT Under Voltage Lock Out protection (UVLO). When the V5FILT voltage is lower than UVLO threshold voltage TPS53124 is shut off. This is non-latch protection.

7.3.10 Thermal Shutdown

TPS53124 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the switchers will be shut off as both DRVH and DRVL at low, the output discharge function enabled. Then TPS53124 is shut off. This is non-latch protection.

7.4 Device Functional Modes

The TPS53124 has two operating modes. The TPS53124 is in shut down mode when the EN1 and EN2 pins are low. When the EN1 and EN2 pins is pulled high, the TPS53124 enters the normal operating mode.

8 Application and Implementation

8.1 Application Information

The TPS53124 is a dual, Adaptive on-time DCAP™ mode synchronous controller. The part enables system designers to cost effectively complete the suite of digital TV power bus regulators with the absolute lowest external component count and lowest standby consumption. The main control loop for the TPS53124 uses the D-CAP™ mode that optimized for low ESR output capacitors such as POSCAP or SP-CAP promises fast transient response with no external compensation. The part provides a convenient and efficient operation with conversion voltages from 4.5 V to 24 V and output voltage from 0.76 V to 5.5 V.

8.2 Typical Application

The TPS53124 is a Step-Down Controller in a realistic cost-sensitive application. Providing both a low core-type 1.05 V and I/O type 1.8 V output from a loosely regulated 12 V source. Idea applications are: Digital TV Power Supply, Networking Home Pin and Digital Set-Top Box (STB).

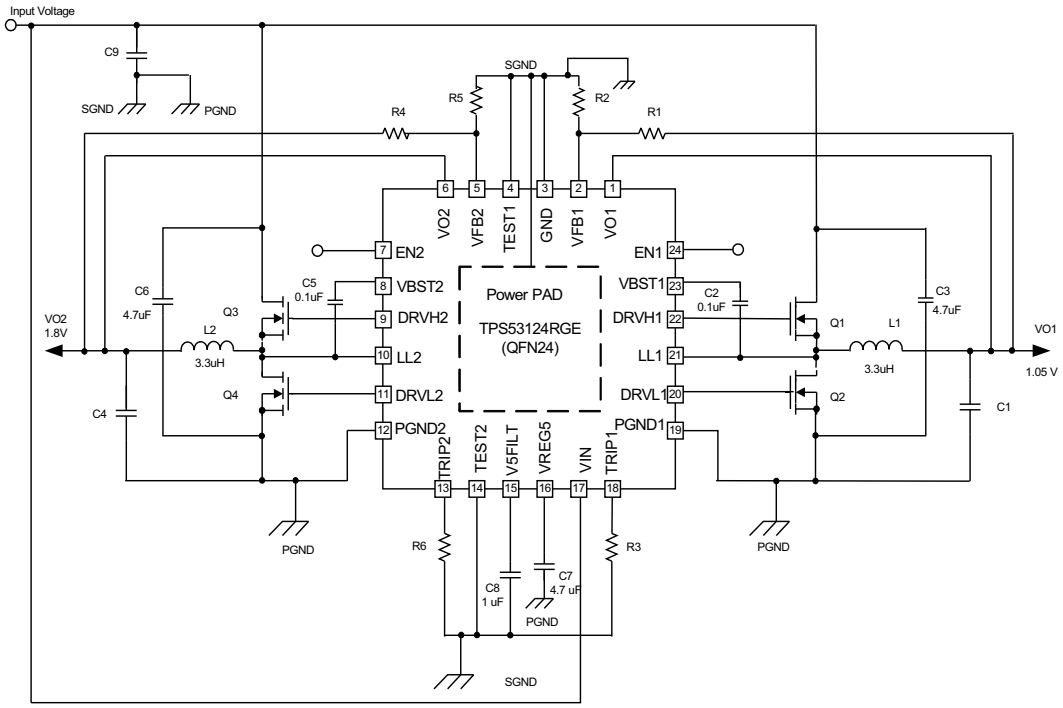


Figure 6. TPS53124 Typical Application Circuit (QFN)

Typical Application (continued)

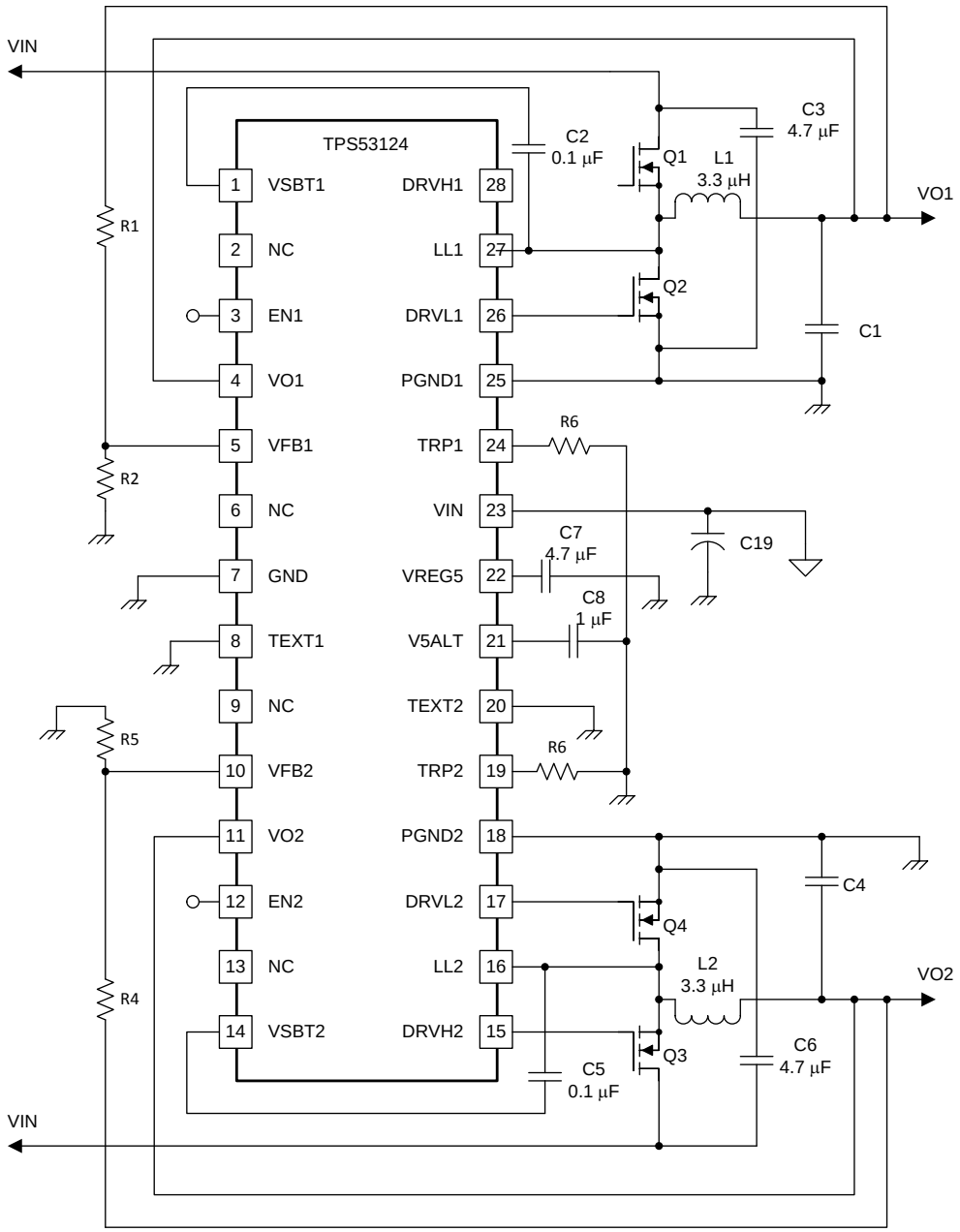


Figure 7. TSSOP

Typical Application (continued)

8.2.1 Design Requirements

Table 1. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input voltage	12 V
Output voltage	VO1 = 1.8 V, VO2 = 1.05 V

8.2.2 Detailed Design Procedure

8.2.2.1 Choose Inductor

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation.

Equation 3 can be used to calculate L1.

$$L1 = \frac{\left(V_{IN(MAX)} - V_O1\right)}{I_{L1(RIPPLE)} \times f_{SW}} \times \frac{V_O1}{V_{IN(MAX)}} = \frac{\left(V_{IN(MAX)} - V_O1\right)}{0.3 \times I_O1 \times f_{SW}} \times \frac{V_O1}{V_{IN(MAX)}} \quad (3)$$

The inductors current ratings needs to support both the RMS (thermal) current and the Peak (saturation) current. The RMS and peak inductor current can be estimated as follows.

$$I_{L1(RIPPLE)} = \frac{\left(V_{IN(MAX)} - V_O1\right)}{L1 \times f_{SW}} \times \frac{V_O1}{V_{IN(MAX)}} \quad (4)$$

$$I_{L1(PEAK)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L1(RIPPLE)} \quad (5)$$

$$I_{L1(RMS)} = \sqrt{I_O1^2 + \frac{1}{12}\left(I_{L1(RIPPLE)}\right)^2} \quad (6)$$

NOTE

The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

8.2.2.2 Loop Compensation and External Parts Selection

A buck converter system using D-CAP™ Mode can be simplified as below.

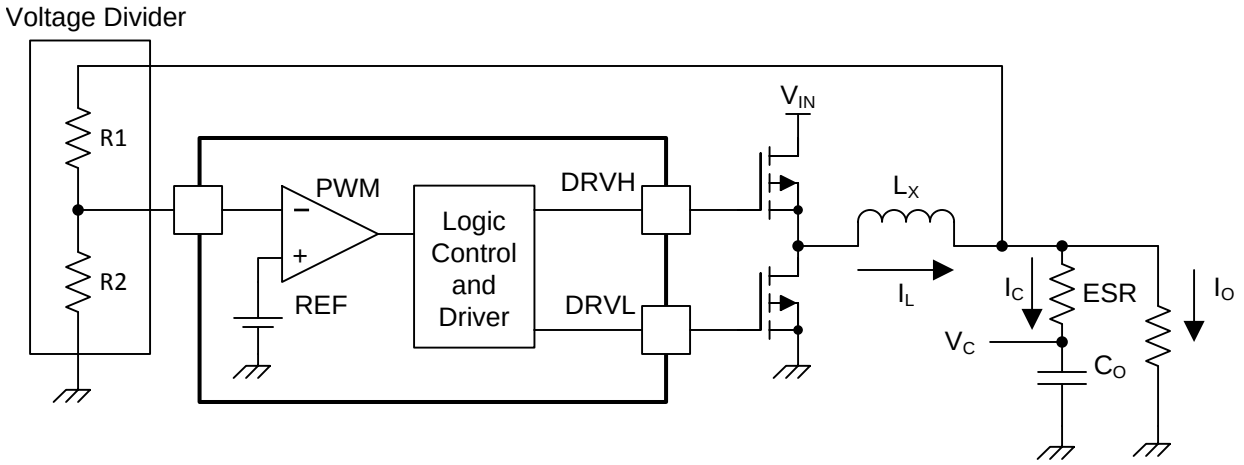


Figure 8. Simplifying the Modulator

The output voltage is compared with internal reference voltage after divider resistors, R1 and R2. The PWM comparator determines the timing to turn on top MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increase.

For the loop stability, the 0-dB frequency, f_0, defined below need to be lower than 1/3 of the switching frequency.

$$f_O = \frac{1}{2\pi \times ESR \times C_O} \leq \frac{f_{SW}}{3} \tag{7}$$

Although D-CAP™ Mode provides many advantages such as ease-of-use, minimum external components configuration and extremely short response time, a sufficient amount of feedback signal needs to be provided by external circuit to reduce jitter level. This is due to not employing an error amplifier in the loop. The required signal level is approximately 10 mV at the comparing point (VFB terminal). This gives Vripples at the output node becomes Equation 8.The output capacitor's ESR should meet this requirement.

$$V_{RIPPLE} = \frac{V_{OUT}}{V_{FBx}} \times 10mV \tag{8}$$

8.2.2.3 Choose Input Capacitor

The TPS53124 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-µF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.4 Choose Bootstrap Capacitor

The TPS53124 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1-µF high-quality ceramic capacitor is recommended. The voltage rating should be greater than 10 V.

8.2.2.5 Choose VREG5 and V5FILT Capacitor

The TPS53124 requires both the VREG5 regulator and V5FILT input are bypassed. A minimum 4.7-µF high-quality ceramic capacitor must be connected between the VREG5 and GND for proper operation. A minimum 1-µF high-quality ceramic capacitor must be connected between the V5FILT and GND for proper operation. Both of these capacitors' voltage ratings should be greater than 10 V.

8.2.2.6 Choose Output Voltage Set Point Resistors

The output voltage is set with a resistor divider from the output voltage node to the VFBx pin. It is recommended to use 1% tolerance or better resisters. Select R2 between 10 kΩ and 100 kΩ and use Equation 9 or Equation 10 to calculate R1.

$$V_{swinj} = (V_{IN} - V_O1 \times 0.5875) \times \left(\frac{1}{f_{SW}}\right) \times \left(\frac{V_O1}{V_{IN}}\right) \times 4975 \quad (9)$$

$$R1 = \left(\frac{V_O1}{V_{FB} + \frac{V_{FB(RIPPLE)} + V_{swinj}}{2}} - 1\right) \times R2 \quad (10)$$

Where

$V_{FB(RIPPLE)}$ = Ripple voltage at VFB
V_{swinj} = Ripple voltage at error comparator

8.2.2.7 Choose Over Current Set Point Resistor

$$V_{TRIP} = \left(I_{OCL} - \frac{(V_{IN} - V_O)}{2 \times L1 \times f_{SW}} \times \frac{V_O}{V_{IN}}\right) \times R_{DS(ON)} \quad (11)$$

$$V_{TRIP} = \left(I_{OCL} - \frac{(V_{IN} - V_O)}{2 \times L1 \times f_{SW}} \times \frac{V_O}{V_{IN}}\right) \times R_{DS(ON)} \quad (12)$$

Where

$R_{DS(ON)}$ = Low-side FET on-resistance
$I_{TRIP(min)}$ = TRIP pin source current (8.5 µA)
V_{OCL0ff} = Minimum over current limit offset voltage (–20 mV)
I_{OCL} = Over current limit

8.2.2.8 Choose Soft Start Capacitor

Soft-start time equation is as follows.

$$C_{SS} = \frac{T_{SS} \times I_{SSC}}{V_{FB}} \quad (13)$$

8.2.3 Application Curves (QFN)

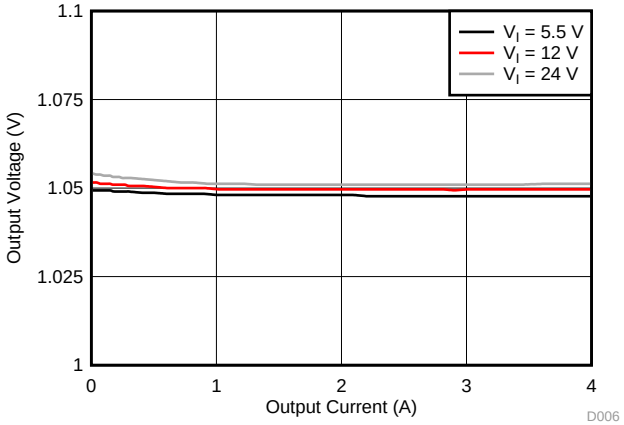


Figure 9. CH1 Output Voltage vs Output Current

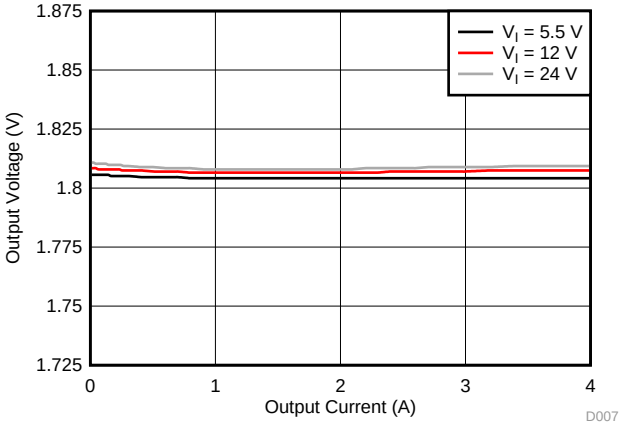


Figure 10. CH2 Output Voltage vs Output Current

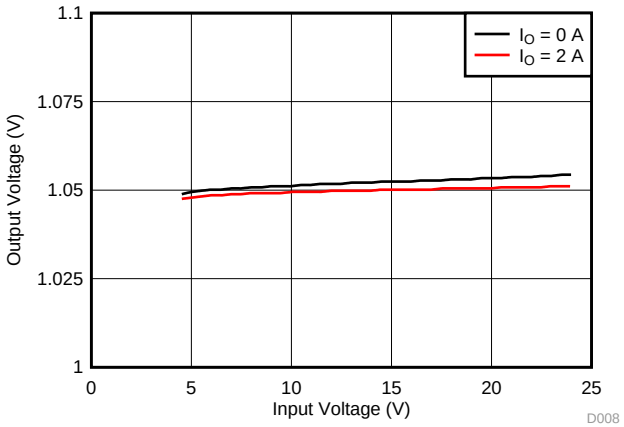


Figure 11. CH1 Output Voltage vs Input Voltage

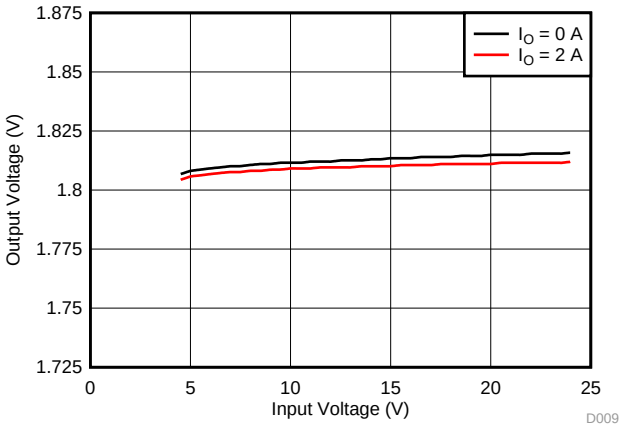


Figure 12. CH2 Output Voltage vs Input Voltage

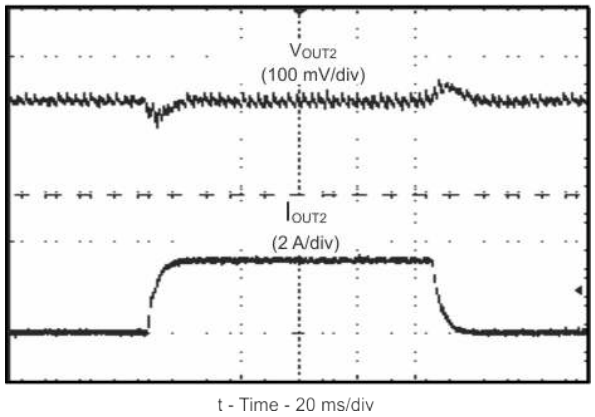


Figure 13. CH1 Load Step Response

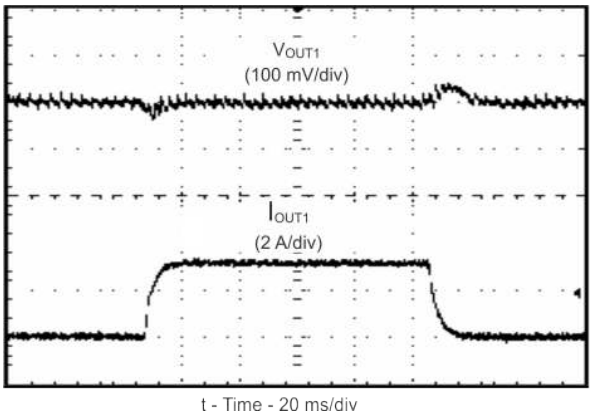


Figure 14. CH2 Load Step Response

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 24 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS53124 device additional 0.1 µF ceramic capacitance may be required in addition to the ceramic bypass capacitors, 10 µF.

10 Layout

10.1 Layout Guidelines

- Keep the input switching current loop as small as possible. (VIN ≥ C3 ≥ PNGD ≥ Sync FET ≥ SW ≥ Control FET)
- Place the input capacitor (C3) close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback terminal (FBx) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.
- DRVH and DRVL line should not run close to SW node or minimize it.
- GND terminals for capacitors of SSx and V5FILT and resistors of feedback and TRIPx should be connected to SGND.
- GND terminals for capacitors of VREG5 and VIN should be connected to PGND.
- Signal lines should not run under/near output inductor or minimize it.

10.2 Layout Example

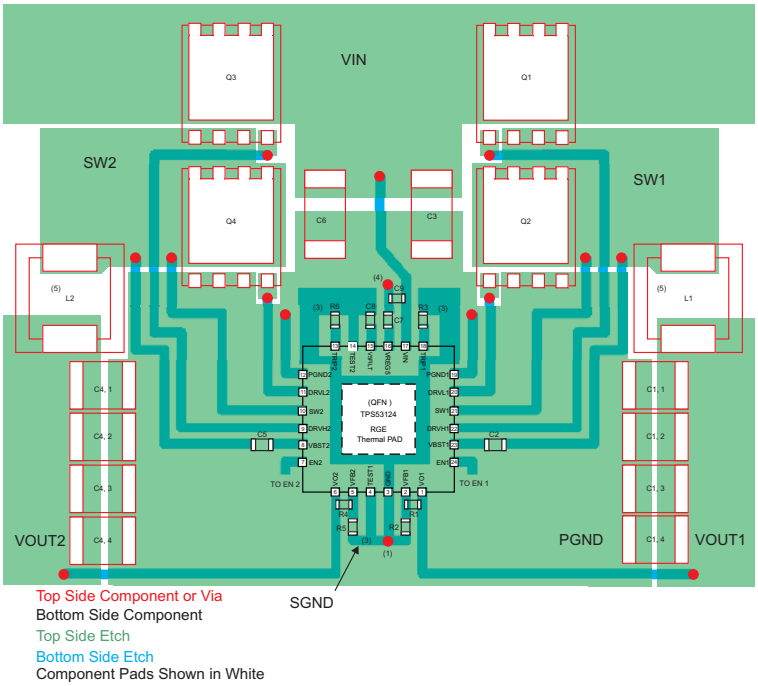


Figure 15. Layout Example for QFN

11 Revision History

Changes from Original (February 2008) to Revision C	Page
• Changed LSL on VREG5 from 4.8 V to 4.6 V.	7
• Changed USL on $R_{DS(on)}$ (R_{DRVL} / Source = –100 ma) from 8 Ω to 12 Ω.	7

12 Device and Documentation Support

12.1 Trademarks

DCAP is a trademark of Texas Instruments.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

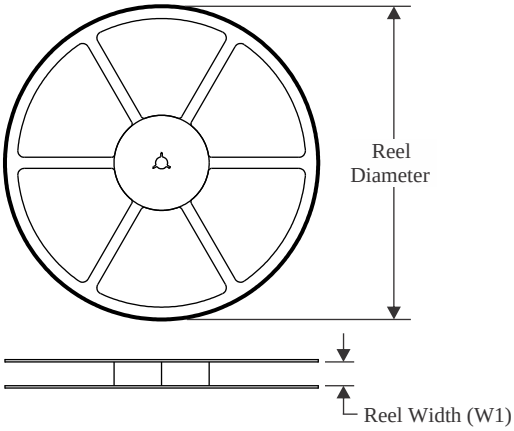
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

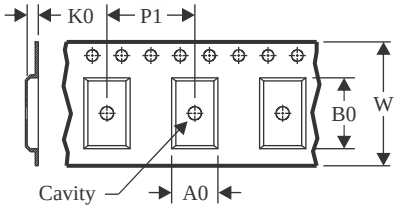
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

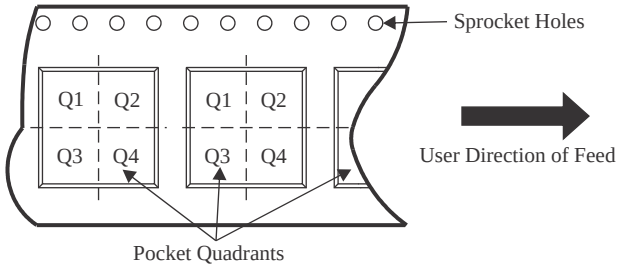


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

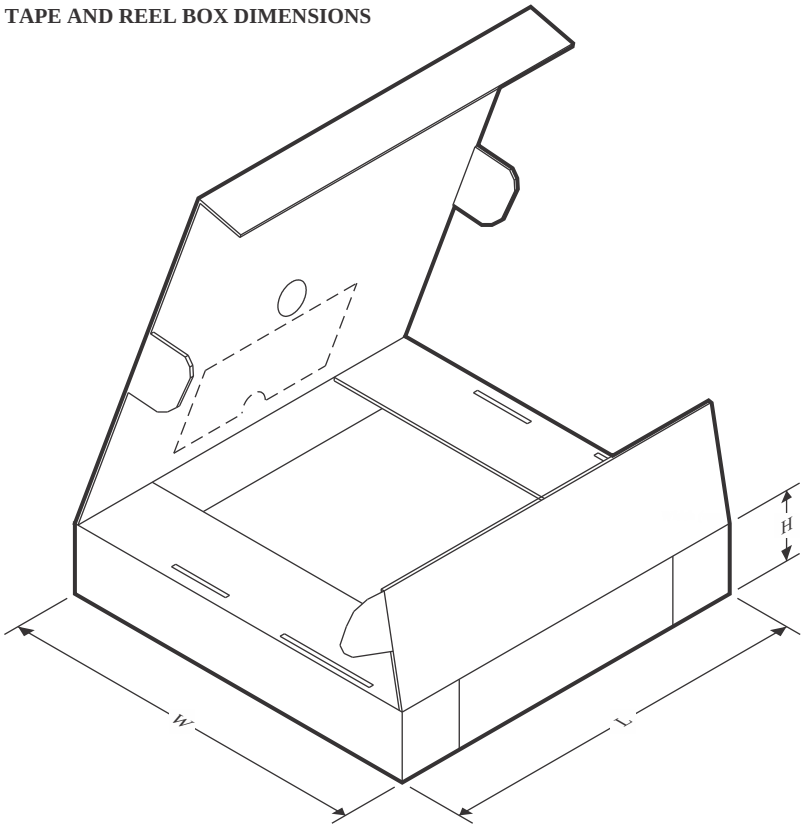
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53124RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53124RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

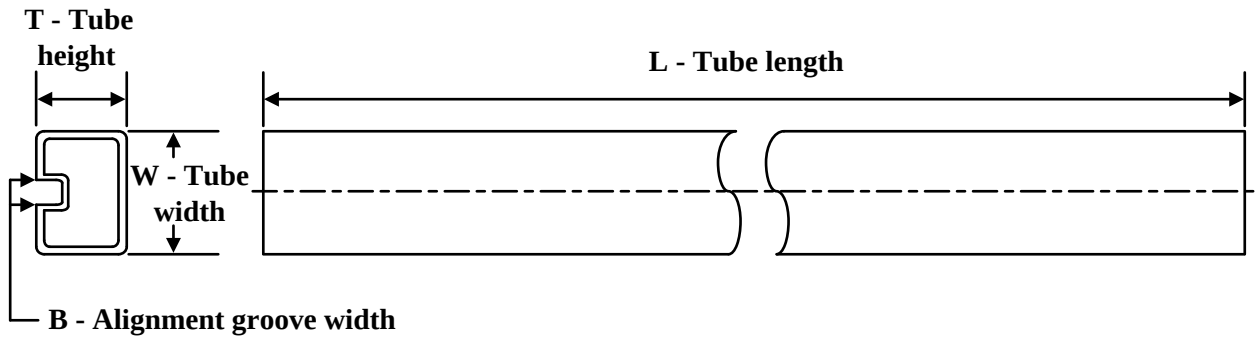
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53124RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS53124RGET	VQFN	RGE	24	250	210.0	185.0	35.0

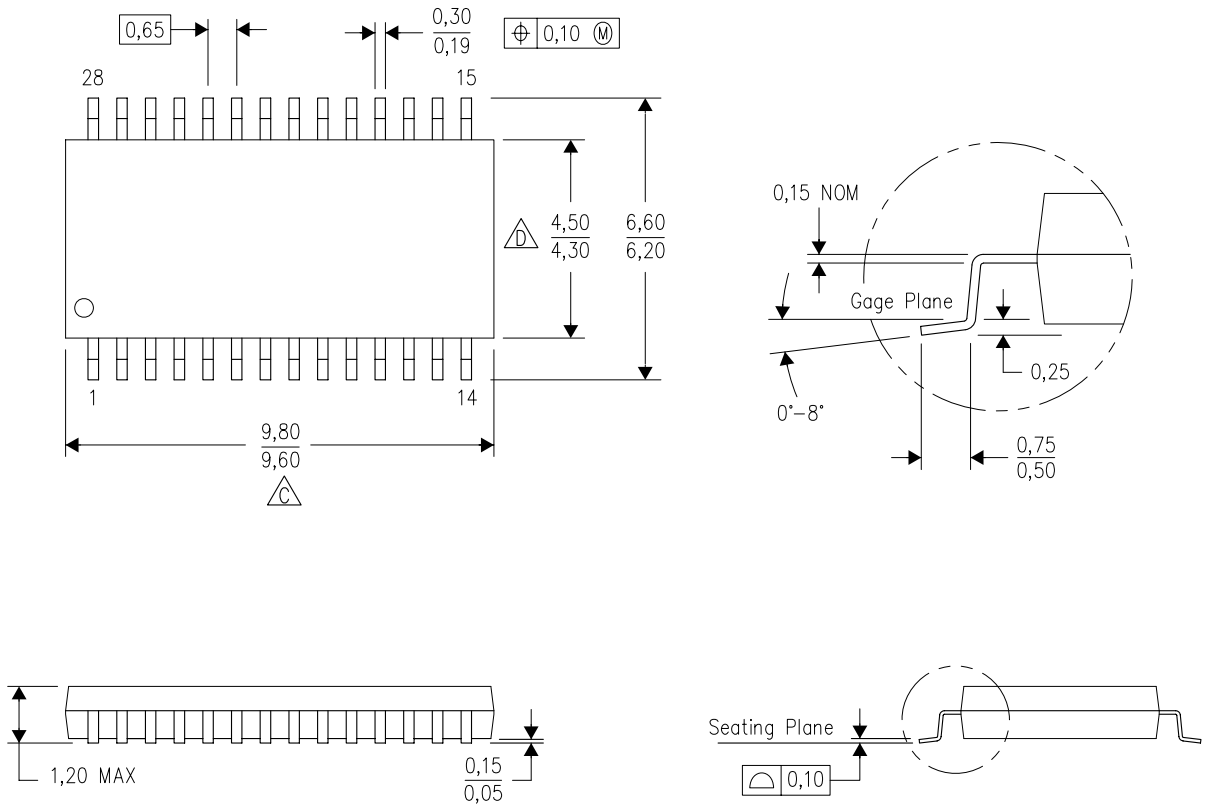
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS53124PW	PW	TSSOP	28	50	530	10.2	3600	3.5

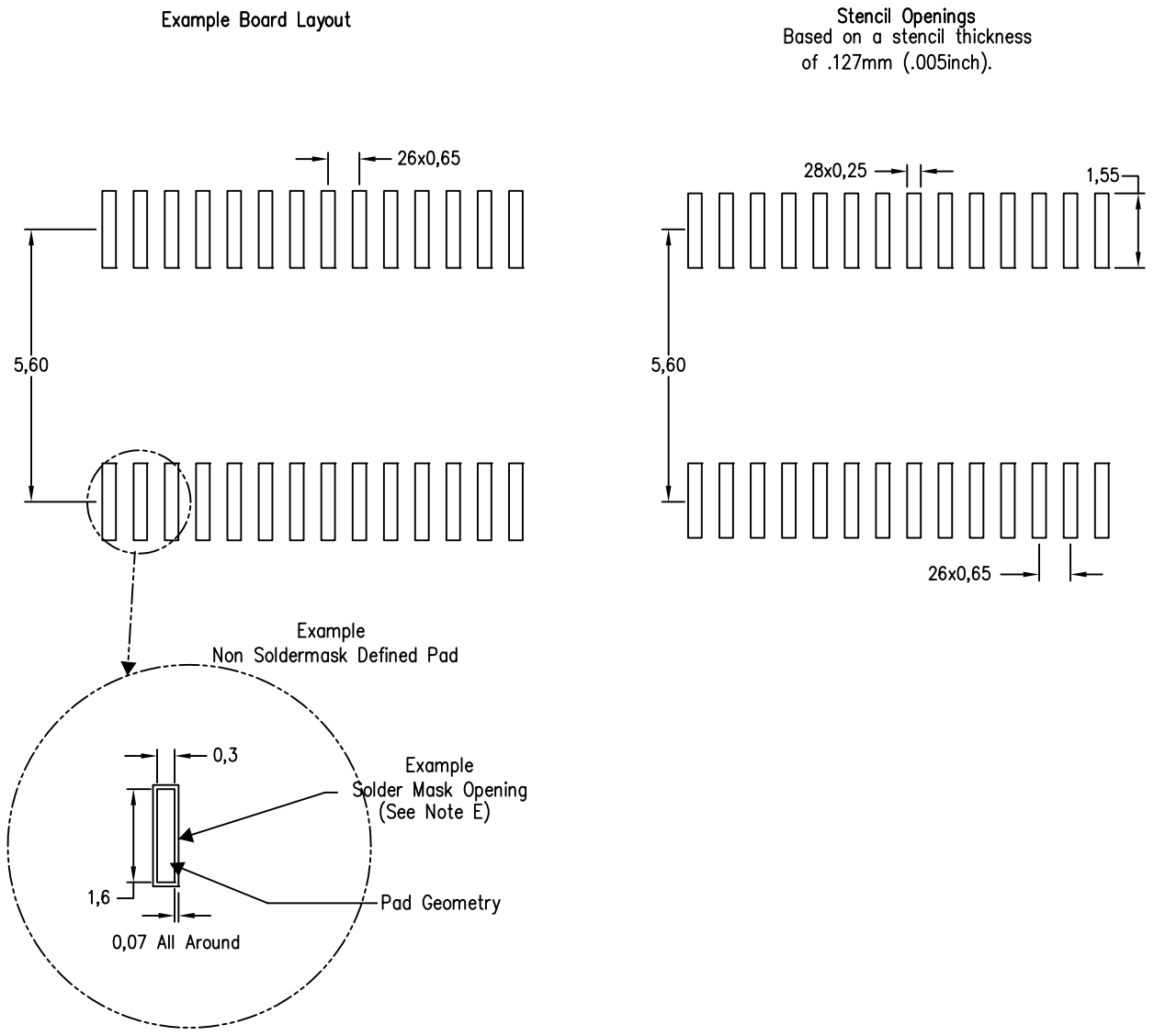
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE

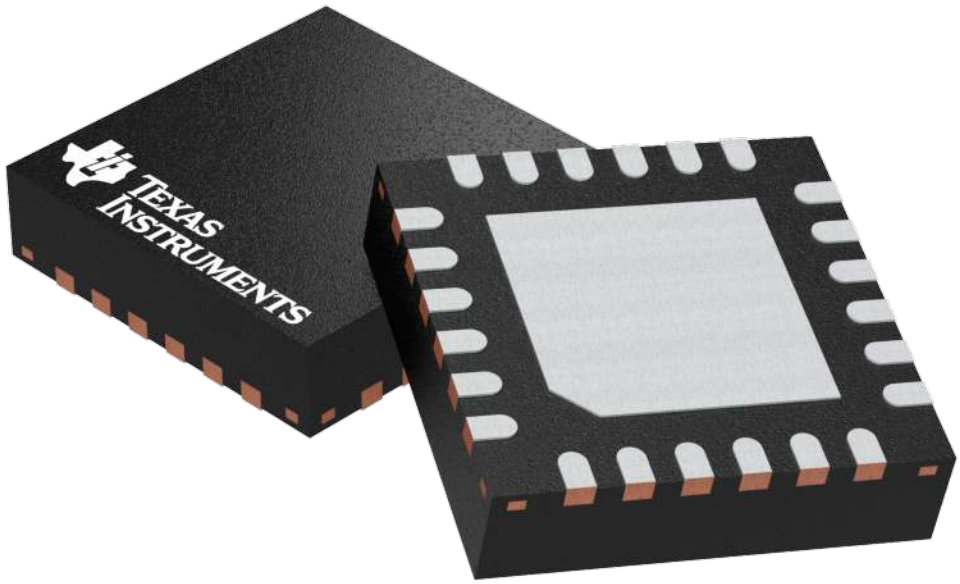


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



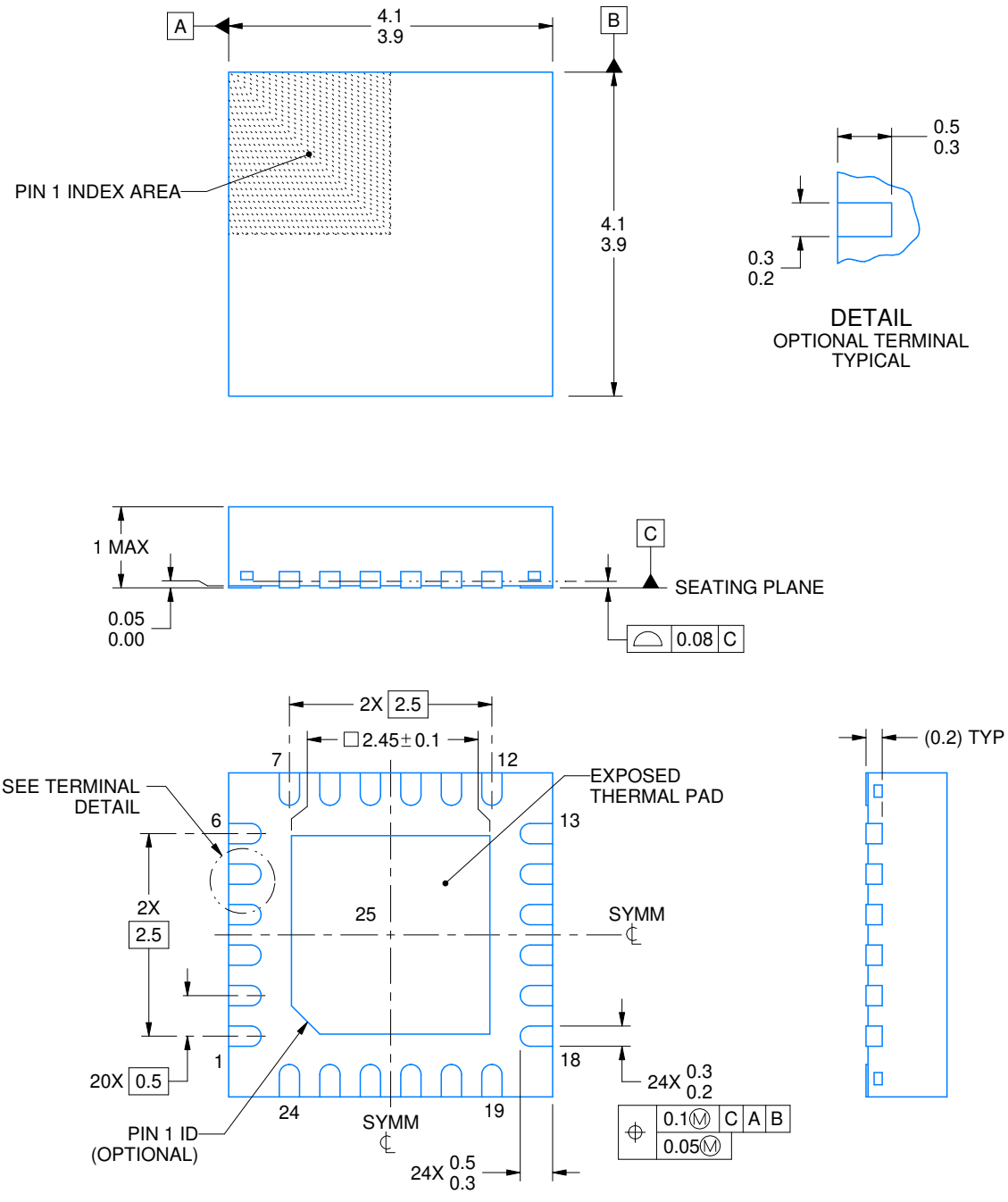
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024B

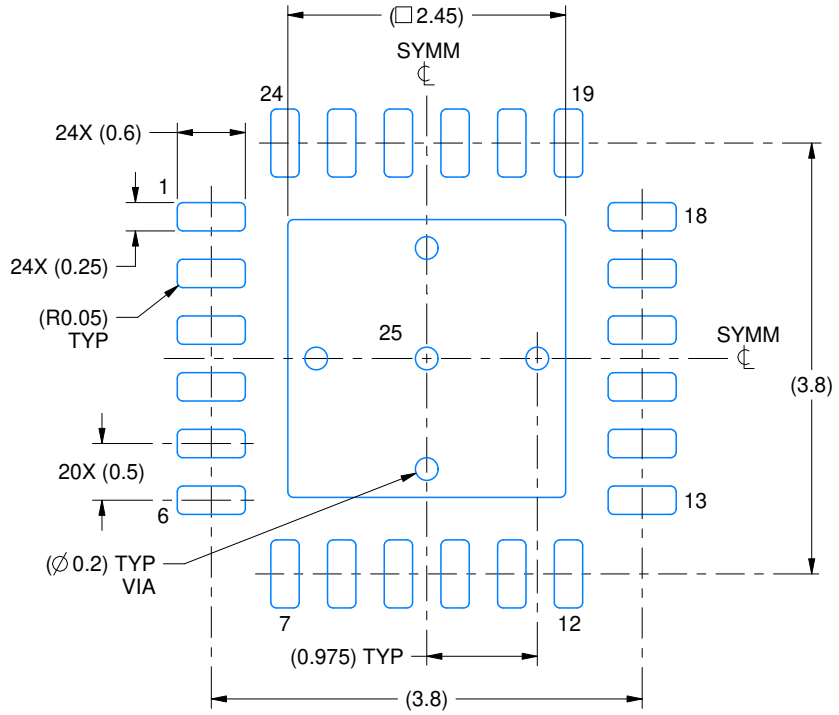
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

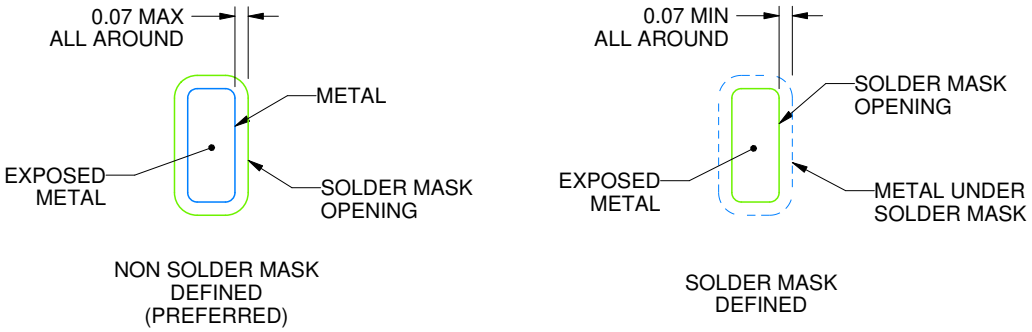


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

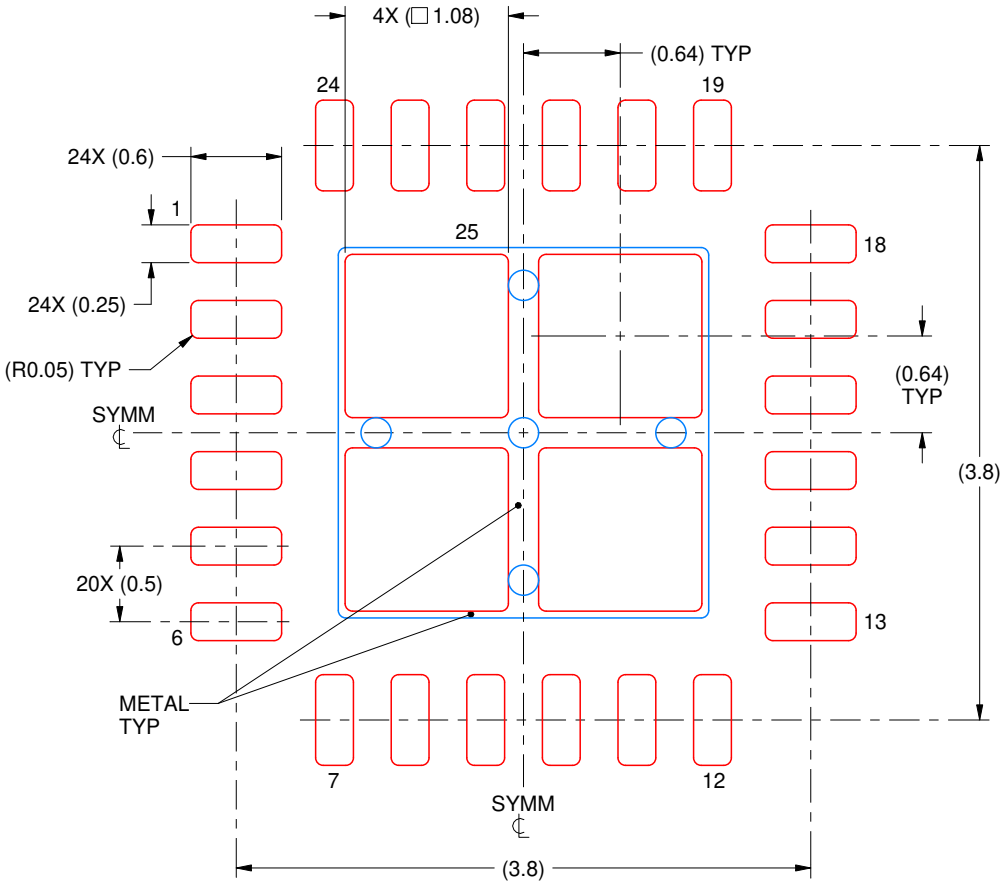
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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