4006B
18-STAGE STATIC SHIFT REGISTER

DESCRIPTION – The 4006B is an 18-stage Shift Register arranged as two 4-stage and two 5-stage shift regsiters with a common Clock Input ($\overline{CP}$). The two 4-stage shift registers, each have a Data Input (D_a, D_b) and a Data Output (Q_{3a}, Q_{3b}); the two 5-stage shift registers each have a Data Input (D_c, D_d) and Data Outputs from the fourth and fifth stages (Q_{3c}, Q_{4c}, Q_{3d}, Q_{4d}).

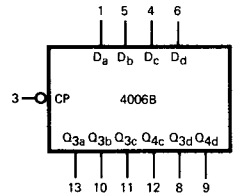
The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data is shifted into the first register position of each register from the Data Inputs (D_a-D_d) and all the data in each register is shifted one position to the right on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$).

- **CLOCK EDGE-TRIGGERED ON A HIGH-TO-LOW TRANSITION**
- **CASCADABLE**
- **SERIAL-TO-SERIAL DATA TRANSFER**

PIN NAMES

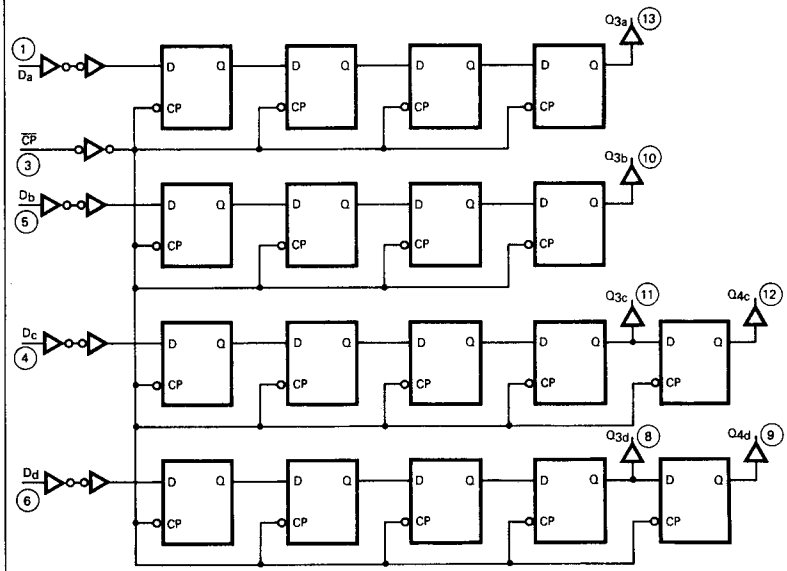
D_a-D_d	Data Inputs
$\overline{CP}$	Clock Input (H→L Edge-Triggered)
Q_{3a}-Q_{3d}, Q_{4c}, Q_{4d}	Data Outputs

LOGIC SYMBOL



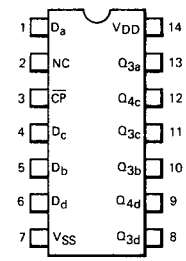
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 2

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 2
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

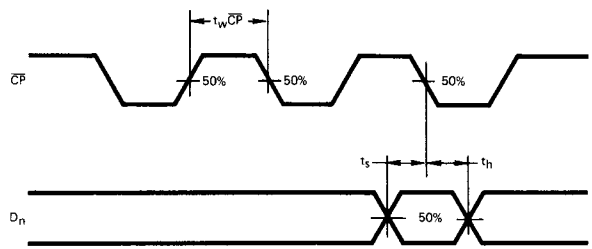
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to any Q_n		90	200		39	100		30	80	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			90	200		35	100		25	80		
t_{TLH}	Output Transition Time		60	135		30	75		20	45	ns	
t_{THL}			60	135		30	75		20	45		
$t_W\overline{CP}$	$\overline{CP}$ Minimum Pulse Width	100	50		50	20		40	13		ns	
t_s	Set-Up Time, D_n to $\overline{CP}$	30	12		15	5		15	5		ns	
t_h	Hold Time, D_n to $\overline{CP}$	30	1		15	4		10	4			
f_{MAX}	Maximum Input Clock Frequency (Note 3)	8	19		15	30		18	36		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D_n TO $\overline{CP}$

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.