User's Guide
SLVUA14–February 2014

TPS40170 with NexFETs 24-V Input, 5 V at 10-A Output Synchronous Buck EVM

The TPS40170EVM-597 evaluation module (EVM) is a synchronous buck design providing a fixed 5-V output at up to 10-A load from a 10-V to 36-V input bus. The module uses the TPS40170 high-performance, wide-input voltage, synchronous buck controller with CSD18537NQ5A and CSD18563Q5A power MOSFETs. This user's guide contains information for the TPS40170EVM-597 evaluation module (PWR597) including the performance specifications, schematic, and the bill of materials.

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1 Introduction

A photo of the TPS40170EVM-597 board is shown in Figure 1.

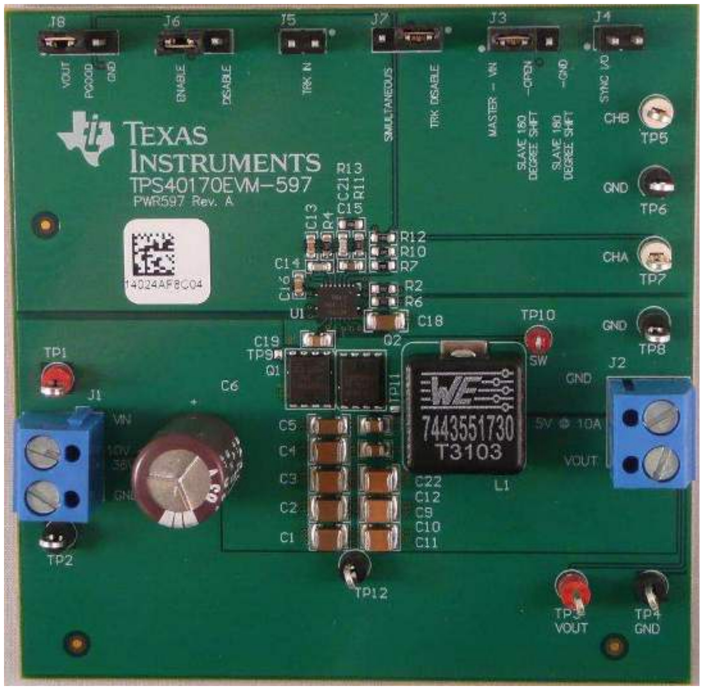


Figure 1. TPS40170EVM-597 Board

1.1 Background

The TPS40170 DC-DC synchronous buck controller is designed for high efficiency from an input voltage source of 4.5 V to 60 V. The CSD18537NQ5A and CSD18563Q5A NexFET power MOSFETs are designed to minimize losses in power conversion applications. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the TPS40170, CSD18537NQ5A, and CSD18563Q5A in a typical wide-input bus converter application while providing a number of non-invasive test points to evaluate the performance and capabilities.

The control and gate drive circuitry is incorporated inside the TPS40170 package. The switching frequency is externally set at a nominal 300 kHz with a resistor to ground at the RT pin to reduce the size of output filter components. The hiccup current limit is externally set with an external resistor to ground at the ILIM pin and uses voltage sensing across the low-side MOSFET. The compensation components are external to the integrated circuit (IC), and an external resistor divider allows for an adjustable output voltage. Additionally, the TPS40170 provides an adjustable undervoltage lockout with hysteresis through an external resistor divider at the UVLO pin and adjustable soft-start with an external capacitor at the SS pin. The TRK pin can also be used to have the output voltage track an external reference. Lastly, the PGOOD pin is an integrated open drain output power good signal. The TPS40170EVM-597 has been evaluated up to a maximum input of 40 V.

For more details on the TPS40170 (SLUS970), CSD18537NQ5A (SLPS391), and CSD18563Q5A (SLPS444), refer to the device datasheets.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS40170EVM-597	V_{IN} = 10 V to 36V	I_{OUT} = 0 A to 10A

1.2 Performance Specification Summary

A summary of the TPS40170EVM-597 (EVM) performance specifications is provided in Table 2. Specifications are given for all input voltages, all load currents, an output voltage of 5 V, and an ambient temperature of 25°C, unless otherwise specified. This EVM is designed and tested for V_{IN} = 10 V to 36 V.

Table 2. TPS40170EVM-597 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} voltage range			10	24	36	V
Full load input current	V_{IN} = 24 V			2.26		A
No load input current	V_{IN} = 24 V			26		mA
UVLO start threshold				9		V
UVLO stop threshold				8		V
Output voltage set point				5		V
Output current range	V_{IN} = 10 V to 36 V		0		10	A
Line regulation	I_{OUT} = 10 A, V_{IN} = 10 V to 36 V			±0.05%		
Load regulation	V_{IN} = 12 V, I_{OUT} = 0 A to 10 A			±0.1%		
Load transient response	V_{IN} = 24 V, I_{OUT} = 2.5 A to 7.5 A	Voltage change		–200		mV
		Recovery time		60		µs
	V_{IN} = 24 V, I_{OUT} = 7.5 A to 2.5 A	Voltage change		120		mV
		Recovery time		60		µs
Loop bandwidth	V_{IN} = 24 V, I_{OUT} = 10 A			56		kHz
Phase margin	V_{IN} = 24 V, I_{OUT} = 10 A			61		°
Input voltage ripple	V_{IN} = 24 V, I_{OUT} = 10 A			400		mVpp
Output voltage ripple	V_{IN} = 24 V, I_{OUT} = 10 A			18		mVpp
Output rise time	10% to 90%			4		ms
Operating frequency				300		kHz
Peak efficiency	TPS40170EVM-597, V_{IN} = 24 V, I_{OUT} = 6 A			92.3%		

1.3 Schematic

The TPS40170EVM-597 schematic is illustrated in Figure 2.

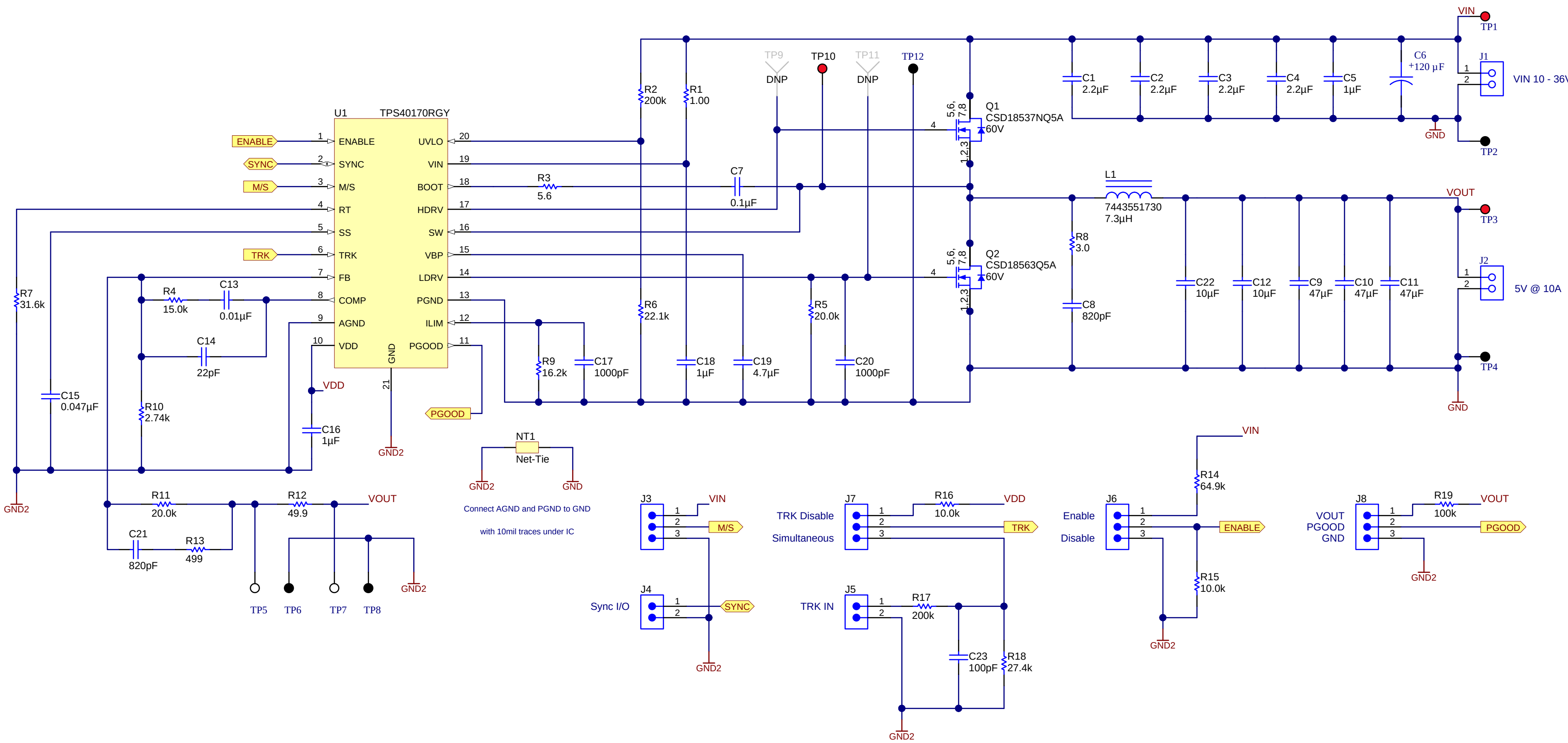


Figure 2. TPS40170EVM-597 Schematic

1.4 Modifications

This evaluation module is designed to provide access to the features of the TPS40170 and allow users to modify it for their own application. Component selection for any modifications can be done with the aid of the equations in the TPS40170 datasheet (SLUS970) or WEBENCH.

2 Test Setup

This section describes how to properly connect, set up, and use the EVM.

2.1 I/O Connection Summary

This EVM includes I/O connectors and test points as shown in Table 3. A power supply capable of supplying at least 5.4 A must be connected to J1 through a pair of 16-AWG wires. The load must be connected to J2 through a pair of 16-AWG wires. The maximum load-current capability must be at least 10 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

Table 3. EVM Connectors and Test points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	V_{OUT}, 5 V at 10-A
J3	M/S pin jumper
J4	SYNC pin jumper
J5	TRK in jumper
J6	ENABLE pin jumper
J7	TRK disable/enable jumper
J8	PGOOD jumper
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	Output voltage test point at V_{OUT} connector
TP4	GND test point at V_{OUT} connector
TP5	Test point for Channel B of loop response measurement
TP6	Ground test point for Channel B of loop response measurement
TP7	Test point for Channel A of loop response measurement
TP8	Ground test point for Channel A of loop response measurement
TP9	Measurement test point for high-side gate driver voltage
TP10	Measurement test point for switching node voltage
TP11	Measurement test point for low-side gate driver voltage
TP12	Ground test point for switch node and gate drive voltages

2.2 Synchronization Jumpers – J3, J4

TPS40170EVM-597 is designed with a synchronization mode jumper (J3) using a 3-pin, 0.1-inch spacing header and shunt. Installing a shunt in J3 in the master position connects the M/S (master/slave) pin to VIN and programs the master synchronization mode. The TPS40170 controller outputs a 50% duty cycle 3.3-V SYNC signal to the SYNC I/O connector (J4). The rising edge of the SYNC signal is synchronized to the rising edge of the high-side FET (Q1).

Installing a shunt in J3 in the SLAVE 180 position connects the M/S pin to GND and programs Slave 180 synchronization mode. In this mode, the SYNC I/O connector is used as an input, and the TPS40170 controller synchronizes the rising edge of the high-side FET (Q1) to the falling edge of the SYNC I/O input.

Removing the shunt from J3 leaves the M/S pin floating and programs Slave 0 synchronization mode. In this mode, the SYNC I/O connector is used as an input and the TPS40170 controller synchronizes the turnon of the high-side FET (Q1) to the rising edge of the SYNC I/O input.

In SLAVE mode, SYNC frequency must be between 270 kHz and 330 kHz. If no signal is provided at the SYNC I/O connector, switching returns to the RT programmed frequency of 300 kHz.

2.3 Tracking Jumpers – J7, J5

The TPS40170EVM-597 is designed with a tracking enable/disable jumper (J7) using a 3-pin, 0.1-inch spacing header and shunt. Installing a shunt in J7 in the SIMULTANEOUS position connects the TRK pin to TRK IN (J5) through a matched divider. This forces VOUT to track the lower of TRK IN or the programmed output voltage (5 V).

Installing a shunt in J7 in the TRK DISABLE position connects TRK to VDD and disables the tracking feature. J7 must be set in this position if no input is present on the TRK IN input.

2.4 Enable Jumper - J6

The TPS40170EVM-597 is designed with an Enable jumper (J6) using a 3-pin, 0.1-inch spacing header and shunt. Installing a shunt in the J6 Enable position connects the Enable pin to VIN and enables the TPS40170 controller. When the shunt is removed or installed in the Disable position, the ENABLE pin is pulled to ground. This forces the output into a high-impedance state (approximately 22 kΩ to GND).

2.5 Power Good Jumper – J8

The TPS40170EVM-597 is designed with a Power Good mode jumper (J8) using a 3-pin, 0.1-inch spacing header and shunt. Placing a shunt in J8 in the VOUT position connects Power Good to VOUT via a 100-kΩ resistor.

Removing the shunt from the J8 position leaves the PGOOD and GND pins available to connect PGOOD to the enable input of another EVM board with no active pullup.

3 Test Results

This section includes test results typical for the EVM covering efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start up, and shutdown. Measurements were taken at an ambient temperature of 25°C.

3.1 Efficiency and Output Voltage Regulation

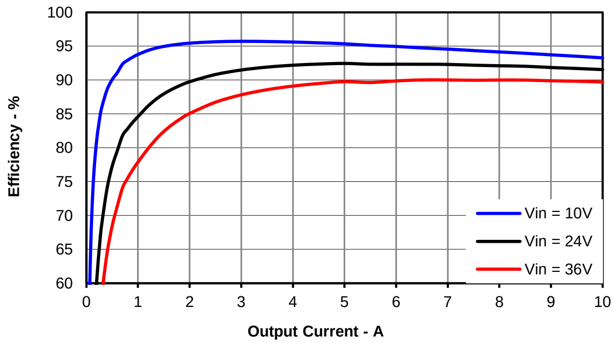


Figure 3. Efficiency Versus Output Current

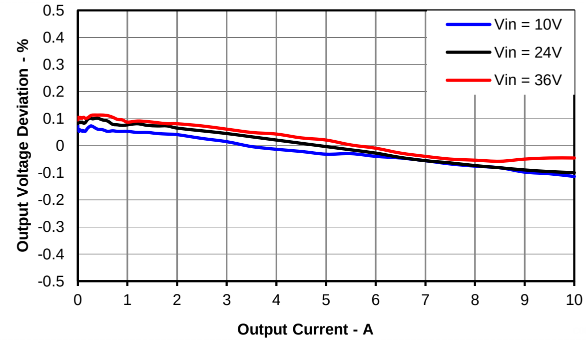
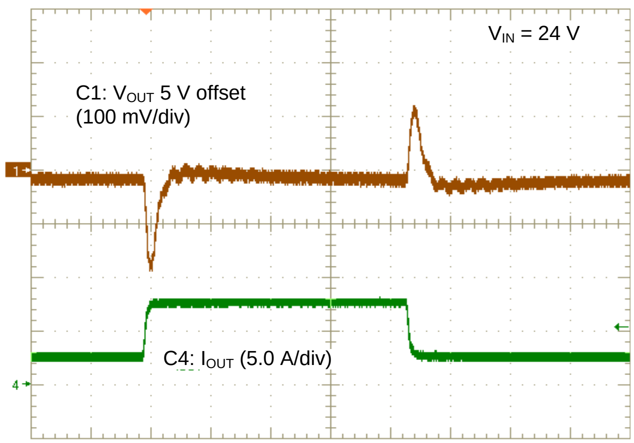


Figure 4. Regulation Versus Output Current

3.2 Load Transients and Loop Response



Time: 100 µs/div

Figure 5. Load Transient Response

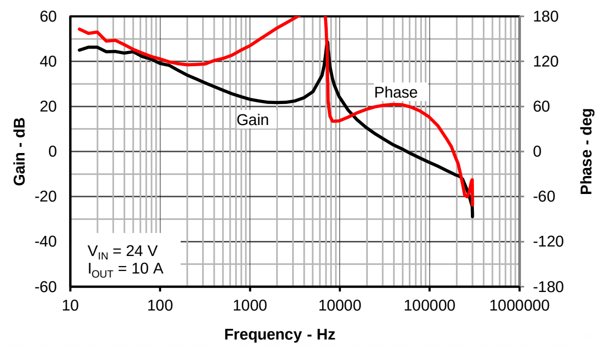
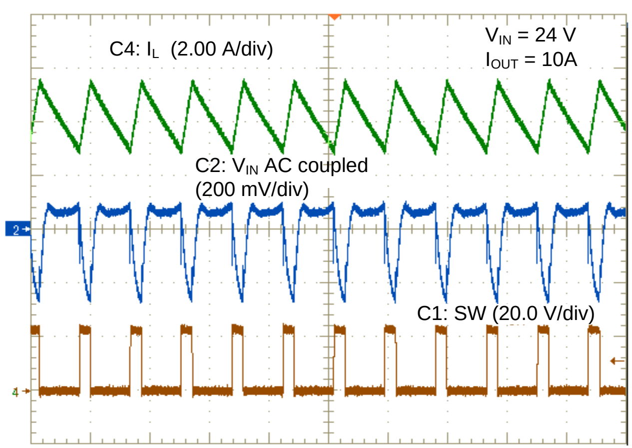


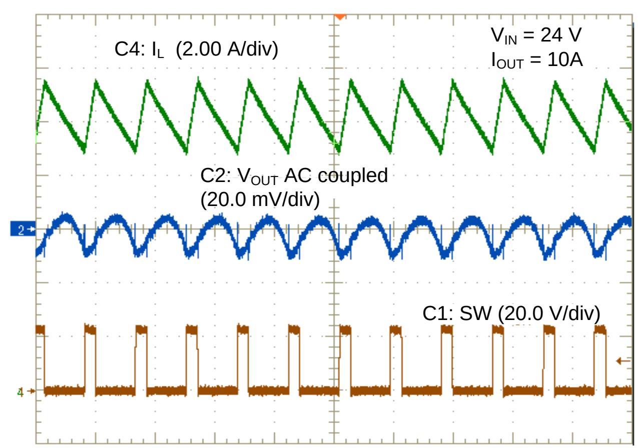
Figure 6. Loop Response

3.3 Input and Output Voltage Ripple



Time: 4.0 µs/div

Figure 7. Input Voltage Ripple



Time: 4.0 µs/div

Figure 8. Output Voltage Ripple

3.4 Start Up

The start up waveforms are shown in Figure 9, Figure 10, and Figure 11. The input voltage for these plots is 24 V and there is a resistive load on the output. In Figure 9 the input voltage is initially applied by turning on the input supply. When the input reaches the undervoltage lockout threshold set by the resistor divider at the UVLO pin, the start up sequence begins and the output ramps up toward the set value of 5 V.

In Figure 10 the input voltage is initially applied with EN held low. When EN is released, the start up sequence begins and the output ramps up toward the set value of 5 V.

In Figure 11 the input voltage is initially applied with EN held low. An external voltage is supplied to V_{OUT}. When EN is released, the start up sequence begins and the internal reference ramps up from 0 V with the internal soft-start. When the internal reference reaches the FB voltage the output begins ramping toward the set value of 5 V.

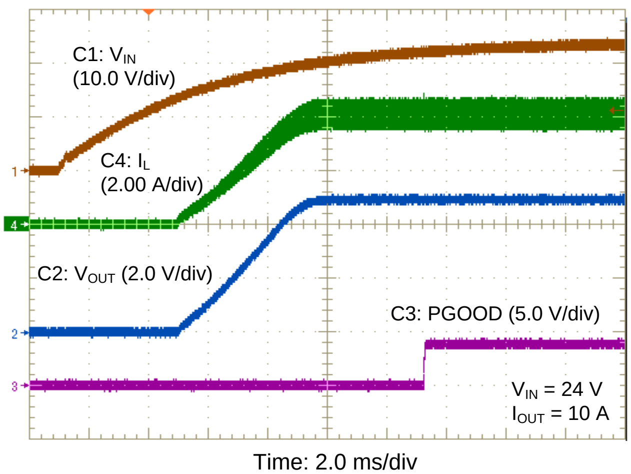


Figure 9. Start Up Relative to V_{IN}

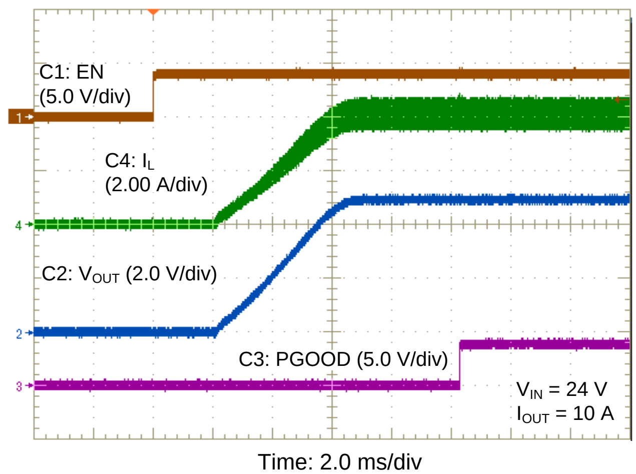


Figure 10. Start Up Relative to EN

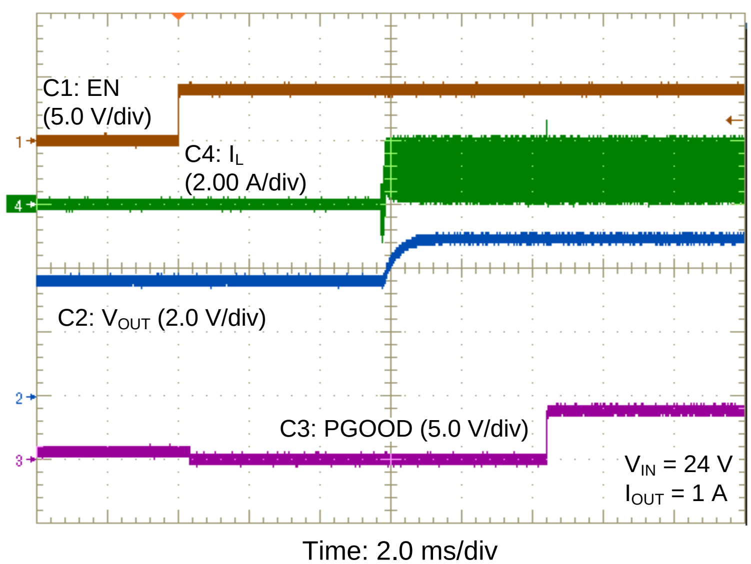


Figure 11. Prebias Start Up Relative to EN

3.5 Shutdown

The shutdown waveforms are shown in Figure 12 and Figure 13. The input voltage for these plots is 24 V with a 10-A resistive load. In Figure 12 the input power supply is turned off. When the input falls below the undervoltage lockout threshold set by the resistor divider at the UVLO pin, the TPS40170 shuts down and the output falls to ground.

In Figure 13, the input voltage is held at 24 V and EN is shorted to ground disabling the internal regulators of the TPS40170. The VBP and VDD outputs begin discharging. When the voltage of either one falls below its UVLO, the TPS40170 stops switching and output voltage discharges to ground.

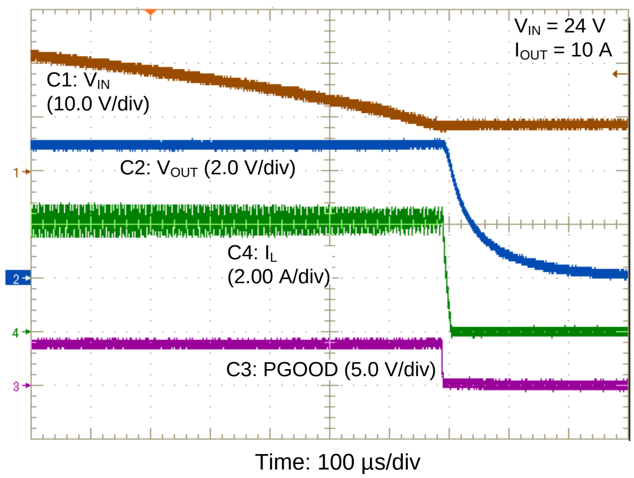


Figure 12. Shutdown Relative to V_{IN}

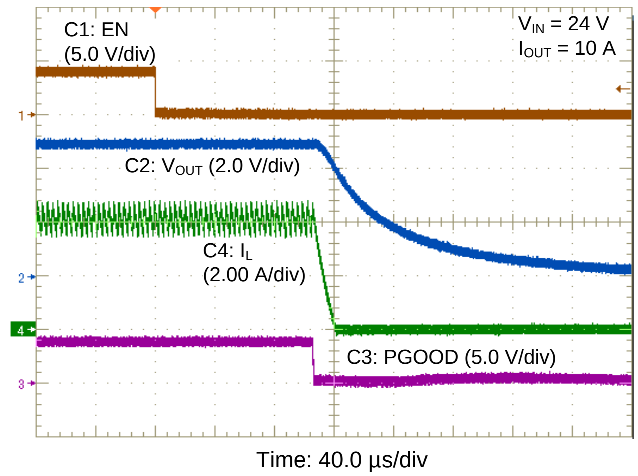


Figure 13. Shutdown Relative to EN

4 Board Layout

4.1 Layout

The board layout for the EVM is shown in Figure 14 through Figure 19. The EVM has been designed using a 4-layer, 3 inch x 3 inch, 2-oz copper-clad circuit board with all power components on the top to allow the user to easily view, probe, and evaluate the TPS40170 control IC in a practical application. Moving power components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

Recommended layout guidelines are as follows:

- Ensure the layout allows a continuous flow of the power planes.
- Connect the 1-µF VIN bypass capacitor next to the VIN pin with a short return to the PGND pin.
- Connect the VBP bypass capacitor next to the VBP pin with a short return to the PGND pin as it provides the instantaneous charge for the low-side FET gate driver.
- Keep the BOOT to SW bypass capacitor near both pins as it provides the instantaneous charge for the high-side FET gate driver.
- Minimize the distance between the VIN node of the input ceramic capacitor and the drain pin of the high-side control FET. Minimize the distance between the PGND node of the input ceramic capacitor and the source pin of the low-side FET.
- Keep the HDRV, SW and LDRV traces as short as is practically possible as these carry high peak currents during the turn on and turn off of the external FETs.
- Provide a direct and wide connection of the low-side FET's source to the GND of the VBP capacitor.
- When using an RC snubber, it should be kept close to the drain and the source of the low-side FET to be most effective.
- Connect the ILIM bypass capacitor close to the ILIM pin with short return to the PGND pin for best noise immunity.
- Connect the VDD bypass capacitor directly next to the VDD pin and AGND pin.
- Carefully connect the noise sensitive signals such as RT, SS, FB, and COMP as close to the IC as practically possible and connect to AGND as shown.
- The AGND and PGND should be connected at a single point at the PowerPad.
- The PowerPad should be connected to any internal PCB ground planes using multiple vias directly under the IC for best thermal performance.

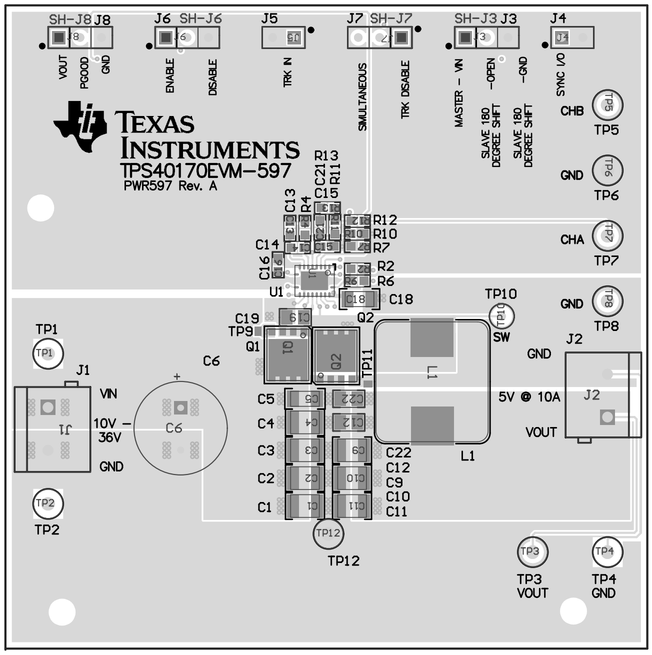


Figure 14. TPS40170EVM-597 Top Assembly and Silkscreen

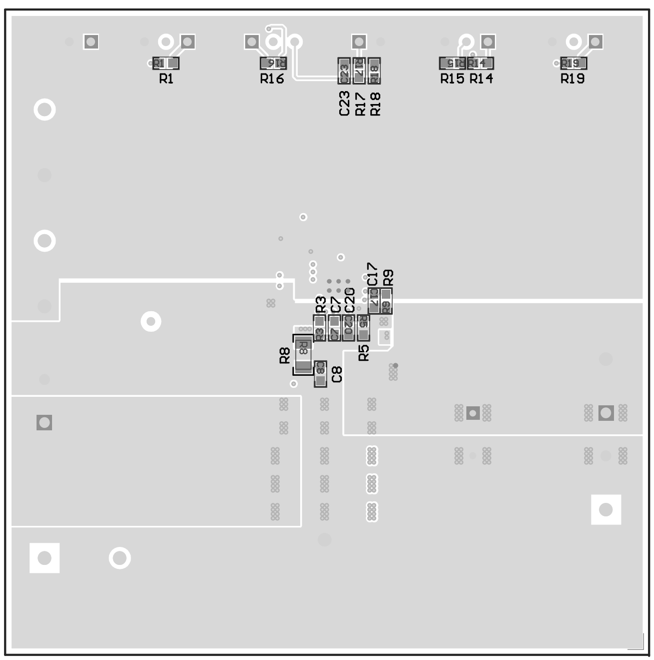


Figure 15. TPS40170EVM-597 Bottom Assembly and Silkscreen (Viewed from Bottom)

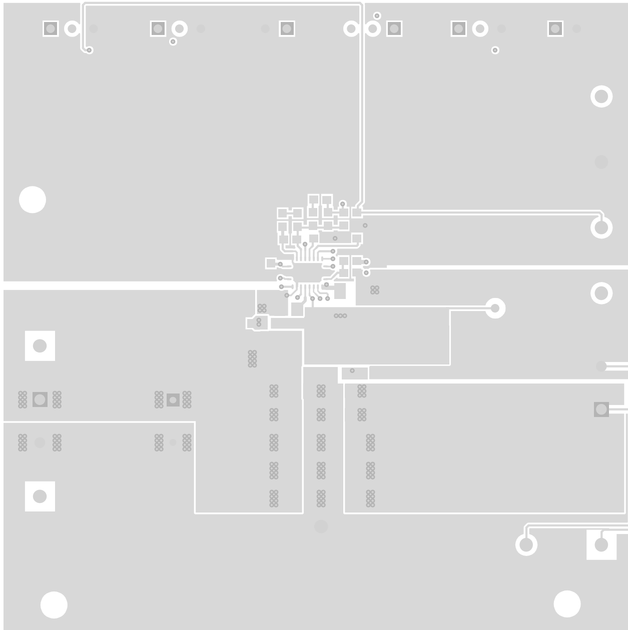


Figure 16. TPS40170EVM-597 Top Layer Layout

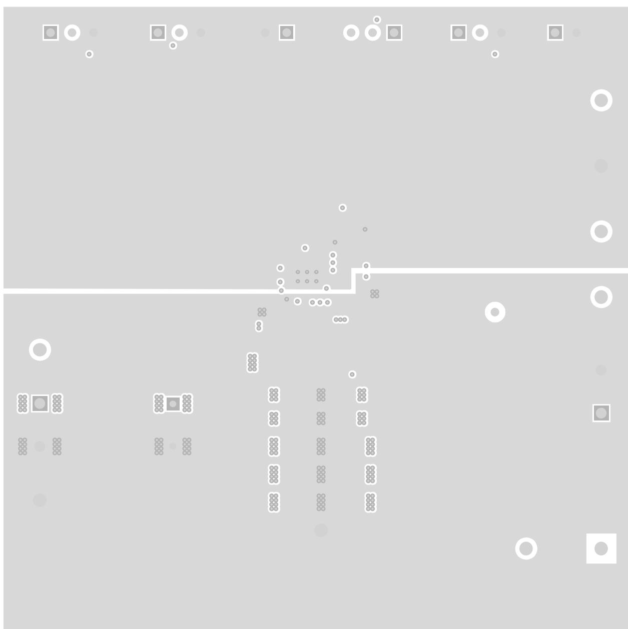


Figure 17. TPS40170EVM-597 Mid-Layer 1 Layout

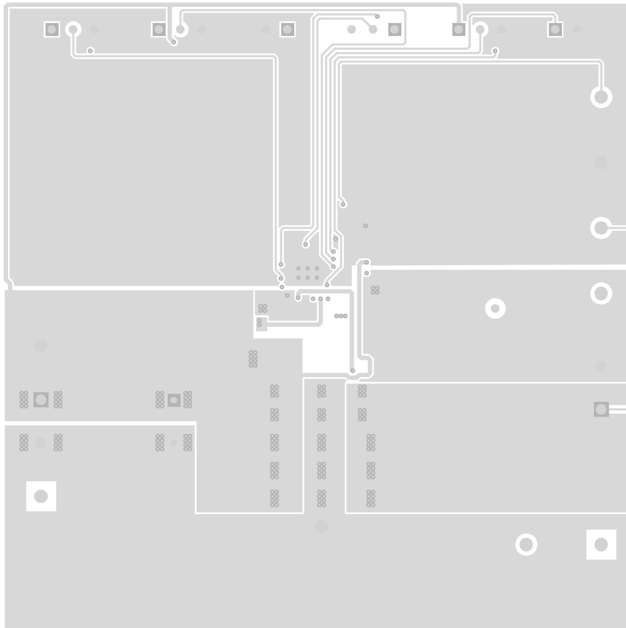


Figure 18. TPS40170EVM-597 Mid-Layer 2 Layout

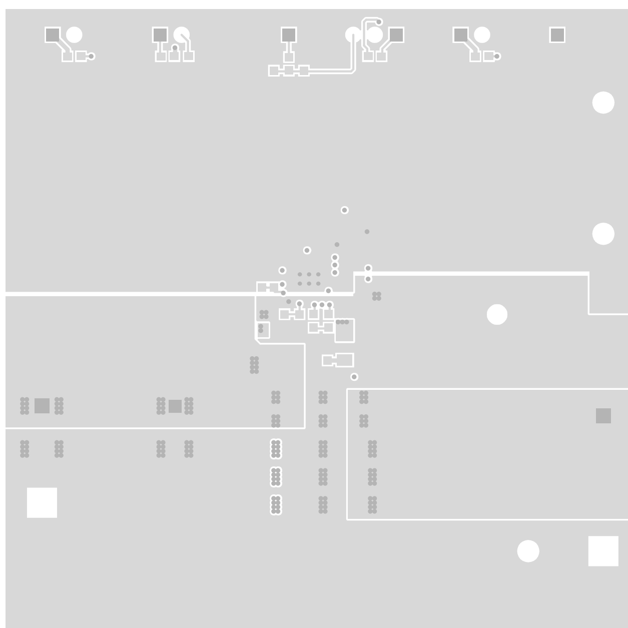


Figure 19. TPS40170EVM-597 Bottom Layer Layout (Viewed from Top)

5 Bill of Materials

Table 4 shows the BOM for the TPS40170EVM-597.

Table 4. TPS40170EVM-597 Bill of Materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
PCB	1		Printed Circuit Board		PWR597	Any
C1, C2, C3, C4	4	2.2uF	CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210	1210	STD	STD
C5, C18	2	1uF	CAP, CERM, 1uF, 100V, +/-10%, X7R, 1206	1206	STD	STD
C6	1	120 µF	Capacitor, Aluminum, 63V, 20%, KZE Series	10.00 mm Dia	KZE63VB121M10X16LL	Chemi-Con
C7	1	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	0603	STD	STD
C8	1	820pF	CAP, CERM, 820pF, 100V, +/-10%, X7R, 0603	0603	STD	STD
C9, C10, C11	3	47uF	CAP, CERM, 47uF, 10V, +/-10%, X7R, 1210	1210	STD	STD
C12, C22	2	10uF	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805	0805	STD	STD
C13	1	0.01uF	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0603	0603	STD	STD
C14	1	22pF	CAP, CERM, 22pF, 50V, +/-5%, C0G/NP0, 0603	0603	STD	STD
C15	1	0.047uF	CAP, CERM, 0.047uF, 50V, +/-10%, X7R, 0603	0603	STD	STD
C16	1	1uF	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	0603	STD	STD
C17, C20	2	1000pF	CAP, CERM, 1000pF, 50V, +/-10%, X7R, 0603	0603	STD	STD
C19	1	4.7uF	CAP, CERM, 4.7uF, 16V, +/-10%, X5R, 0805	0805	STD	STD
C21	1	820pF	CAP, CERM, 820pF, 50V, +/-5%, C0G/NP0, 0603	0603	STD	STD
C23	1	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	0603	STD	STD
J1, J2	2		TERMINAL BLOCK 5.08MM VERT 2POS, TH	TERM_BLK, 2pos, 5.08mm	ED120/2DS	On-Shore Technology
J3, J6, J7, J8	4		Header, 100mil, 3x1, Tin plated, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
J4, J5	2		Header, 100mil, 2x1, Tin plated, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions
L1	1	7.3uH	Inductor, Shielded Drum Core, WE-Perm, 7.3uH, 12A, 0.0059 ohm, SMD	WE-HCA1	7443551730	Wurth Elektronik eiSos
Q1	1	60V	MOSFET, N-CH, 60V, 50A, SON 5x6mm	SON 5x6mm	CSD18537NQ5A	Texas Instruments
Q2	1	60V	MOSFET, N-CH, 60V, 100A, SON 5x6mm	SON 5x6mm	CSD18563Q5A	Texas Instruments
R1	1	1.00	RES, 1.00 ohm, 1%, 0.1W, 0603	0603	STD	STD
R2, R17	2	200k	RES, 200k ohm, 1%, 0.1W, 0603	0603	STD	STD
R3	1	5.6	RES, 5.6 ohm, 5%, 0.1W, 0603	0603	STD	STD
R4	1	15.0k	RES, 15.0k ohm, 1%, 0.1W, 0603	0603	STD	STD
R5, R11	2	20.0k	RES, 20.0k ohm, 1%, 0.1W, 0603	0603	STD	STD
R6	1	22.1k	RES, 22.1k ohm, 1%, 0.1W, 0603	0603	STD	STD
R7	1	31.6k	RES, 31.6k ohm, 1%, 0.1W, 0603	0603	STD	STD
R8	1	3.0	RES, 3.0 ohm, 5%, 0.25W, 1206	1206	STD	STD
R9	1	16.2k	RES, 16.2k ohm, 1%, 0.1W, 0603	0603	STD	STD
R10	1	2.74k	RES, 2.74k ohm, 1%, 0.1W, 0603	0603	STD	STD
R12	1	49.9	RES, 49.9 ohm, 1%, 0.1W, 0603	0603	STD	STD
R13	1	499	RES, 499 ohm, 1%, 0.1W, 0603	0603	STD	STD
R14	1	64.9k	RES, 64.9k ohm, 1%, 0.1W, 0603	0603	STD	STD
R15, R16	2	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	0603	STD	STD
R18	1	27.4k	RES, 27.4k ohm, 1%, 0.1W, 0603	0603	STD	STD
R19	1	100k	RES, 100k ohm, 1%, 0.1W, 0603	0603	STD	STD
SH-J3, SH-J6, SH-J7, SH-J8	4	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP3	2	Red	Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP2, TP4, TP6, TP8, TP12	5	Black	Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP5, TP7	2	White	Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
TP10	1	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
U1	1		4.5-v to 60-v wide-input synchronous PWM buck controller, RGY0020A	RGY0020A	TPS40170RGY	Texas Instruments

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l’autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d’usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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