

74F114

Dual JK Negative Edge-Triggered Flip-Flop with Common Clocks and Clears

General Description

The 'F114 contains two high-speed JK flip-flops with common Clock and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on \bar{S}_D or \bar{C}_D prevents clocking and forces Q or \bar{Q} HIGH, respectively. Simultaneous LOW signals on \bar{S}_D and \bar{C}_D force both Q and \bar{Q} HIGH.

Asynchronous Inputs:

- LOW input to \bar{S}_D sets Q to HIGH level
- LOW input to \bar{C}_D sets Q to LOW level
- Clear and Set are independent of Clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

Features

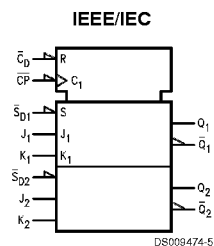
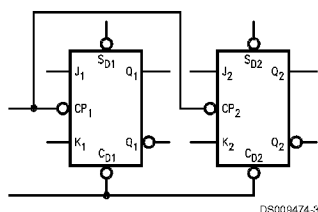
- Guaranteed 4000V minimum ESD protection

Ordering Code:

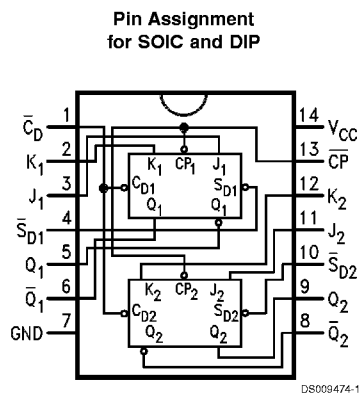
Commercial	Package Number	Package Description
74F114PC	N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
74F114SC (Note 1)	M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20 μA / -0.6 mA
\overline{CP}	Clock Pulse Input (Active Falling Edge)	1.0/8.0	20 μA / -4.8 mA
$\overline{C_D}$	Direct Clear Input (Active LOW)	1.0/10.0	20 μA / -6.0 mA
$\overline{S_{D1}}, \overline{S_{D2}}$	Direct Set Inputs (Active LOW)	1.0/5.0	20 μA / -3.0 mA
$Q_1, Q_2, \overline{Q_1}, \overline{Q_2}$	Outputs	50/33.3	-1 mA / 20 mA

Truth Table

Inputs					Outputs	
$\overline{S_D}$	$\overline{C_D}$	\overline{CP}	J	K	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	\sim	h	h	$\overline{Q_0}$	Q_0
H	H	\sim	l	h	L	H
H	H	\sim	h	l	H	L
H	H	\sim	l	l	Q_0	$\overline{Q_0}$

H = HIGH Voltage Level

L = LOW Voltage Level

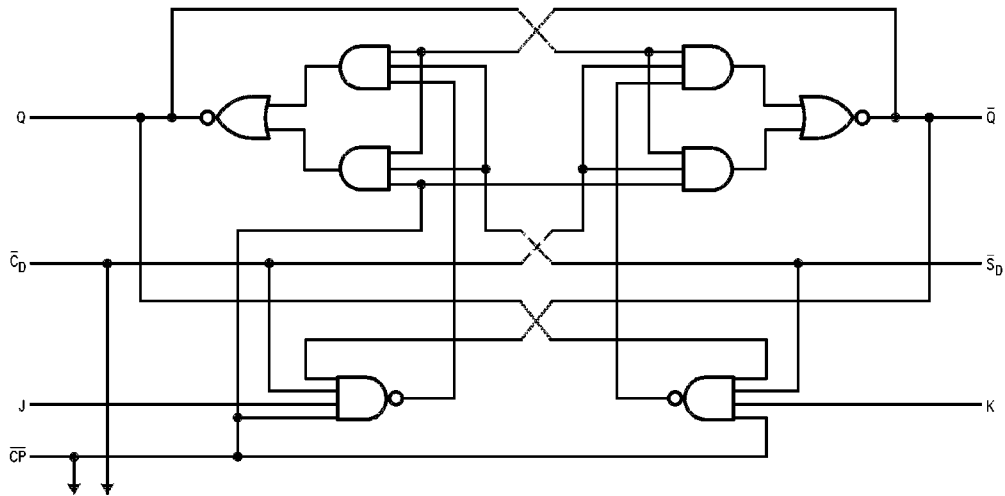
X = Immaterial

\sim = HIGH-to-LOW Clock Transition

Q_0 ($\overline{Q_0}$) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram (one half shown)



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	74F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current	74F		5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output High Leakage Current	74F		50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -3.0 -4.8 -6.0	mA	Max	V _{IN} = 0.5V (J _n , K _n) V _{IN} = 0.5V (\overline{S}_{Dn}) V _{IN} = 0.5V ($\overline{C}\overline{P}$) V _{IN} = 0.5V ($\overline{C}\overline{Dn}$)
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		12.0	19.0	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		12.0	19.0	mA	Max	V _O = LOW

AC Electrical Characteristics

Symbol	Parameter	74F			74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	75	95		70		MHz

AC Electrical Characteristics (Continued)

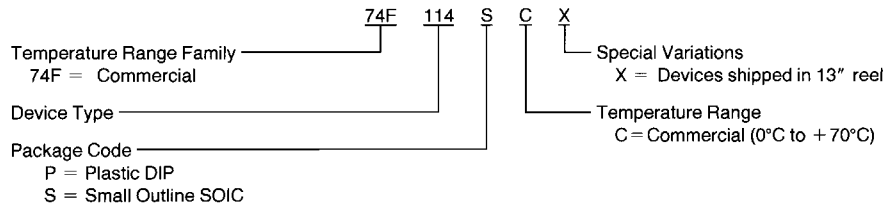
Symbol	Parameter	74F			74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay CP̄ to Q _n or Q̄ _n	3.0	5.0	6.5	3.0	7.5	ns
t _{PHL}	CP̄ to Q _n or Q̄ _n	3.0	5.5	7.5	3.0	8.5	
t _{PLH}	Propagation Delay C̄ _{Dn} or S̄ _{Dn} to Q _n or Q̄ _n	3.0	4.5	6.5	3.0	7.5	ns
t _{PHL}	C̄ _{Dn} or S̄ _{Dn} to Q _n or Q̄ _n	3.0	4.5	6.5	3.0	7.5	

AC Operating Requirements

Symbol	Parameter	74F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Com		
		Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW	4.0		5.0		ns
t _s (L)	J _n or K _n to CP̄	3.0		3.5		
t _h (H)	Hold Time, HIGH or LOW	0		0		ns
t _h (L)	J _n or K _n to CP̄	0		0		
t _w (H)	CP̄ Pulse Width	4.5		5.0		ns
t _w (L)	HIGH or LOW	4.5		5.0		
t _w (L)	C̄ _{Dn} or S̄ _{Dn} Pulse Width, LOW	4.5		5.0		ns
t _{rec}	Recovery Time S̄ _{Dn} , C̄ _{Dn} , to CP̄	4.0		5.0		ns

Ordering Information

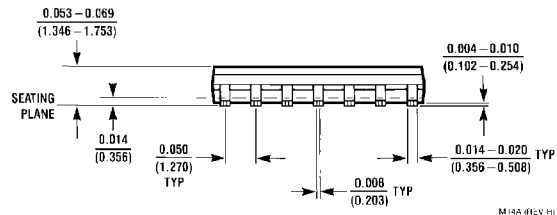
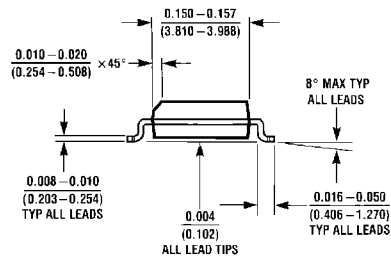
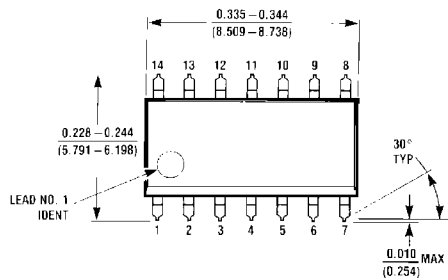
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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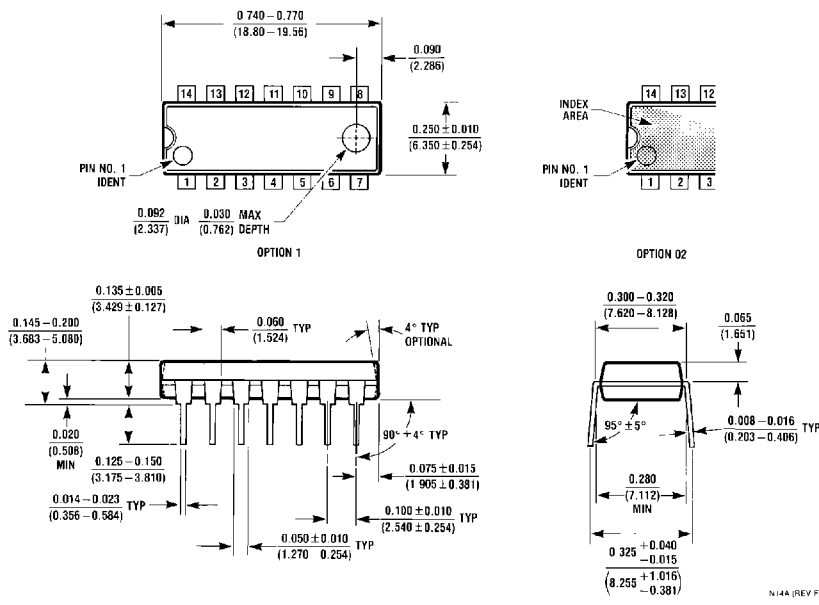
Physical Dimensions

inches (millimeters) unless otherwise noted



14-Lead (0.150" Wide) Molded Small Outline Package (S)
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead (0.150" Wide) Molded Dual-In-Line Package (P)
Package Number N14A**

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