# 3-W STEREO CLASS-D AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

## FEATURES

- **3 W Per Channel into 3-Ω Speakers (THD+N = 10%)**
  - **< 0.045% THD at 1.5 W, 1 kHz, 3-Ω Load**
- **DC Volume Control With 2-dB Steps From -38 dB to 20 dB**
- **Filter Free Modulation Scheme Operates Without a Large and Expensive LC Output Filter**
- **Extremely Efficient Third Generation 5-V Class-D Technology**
  - **Low Supply Current, 7 mA**
  - **Low Shutdown Control, 1 µA**
  - **Low Noise Floor, -80 dBV**
  - **Maximum Efficiency into 3 Ω, 78%**
  - **Maximum Efficiency into 8 Ω, 88%**
  - **PSRR, -70 dB**
- **Integrated Depop Circuitry**
- **Operating Temperature Range, -40°C to 85°C**
- **Space-Saving, Surface Mount PowerPAD™ Package**

## APPLICATIONS

- **LCD Projectors**
- **LCD Monitors**
- **Powered Speakers**
- **Battery Operated and Space Constrained Systems**

## DESCRIPTION

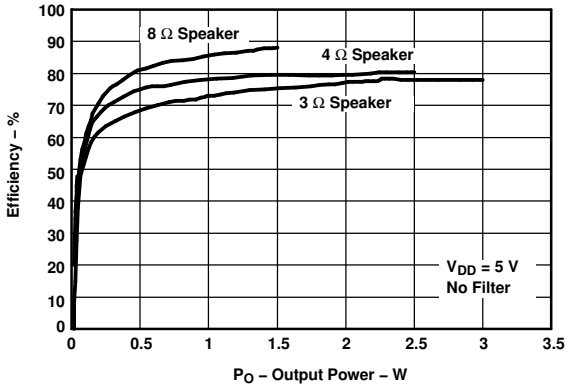
The TPA2008D2 is a third generation 5-V class-D amplifier from Texas Instruments. Improvements to previous generation devices include: dc volume control, lower supply current, lower noise floor, higher efficiency, smaller packaging, and fewer external components. Most notably, a new filter-free class-D modulation technique allows the TPA2008D2 to directly drive the speakers, without needing a low-pass output filter consisting of two inductors and three capacitors per channel. Eliminating this output filter saves approximately 30% in system cost and 75% in PCB area.

The improvements and functionality make this device ideal for LCD projectors, LCD monitors, powered speakers, and other applications that demand more battery life, reduced board space, and functionality that surpasses currently available class-D devices.

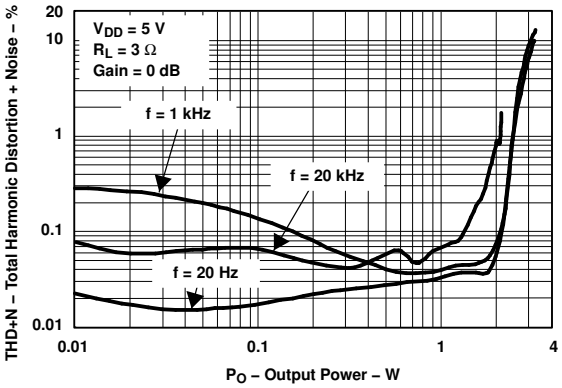
A chip-level shutdown control limits total supply current to 1 µA, making the device ideal for battery-powered applications. Protection circuitry increases device reliability: thermal and short circuit. Undervoltage shutdown saves battery power for more essential devices when battery voltage drops to low levels.

The TPA2008D2 is available in a 24-pin TSSOP PowerPAD™package.

**EFFICIENCY vs OUTPUT POWER**




**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER**

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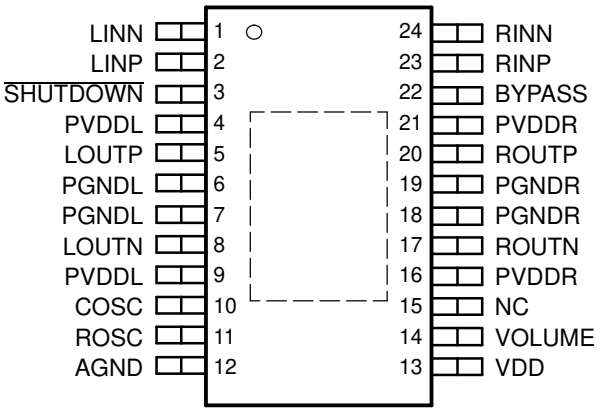
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTIONS

| | TSSOP PowerPAD (PWP)(1) |
|---|---|
| Device | TPA2008D2PWP(1) |
| Package Designator | PWP(1) |

(1) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA2008D2PWPR).

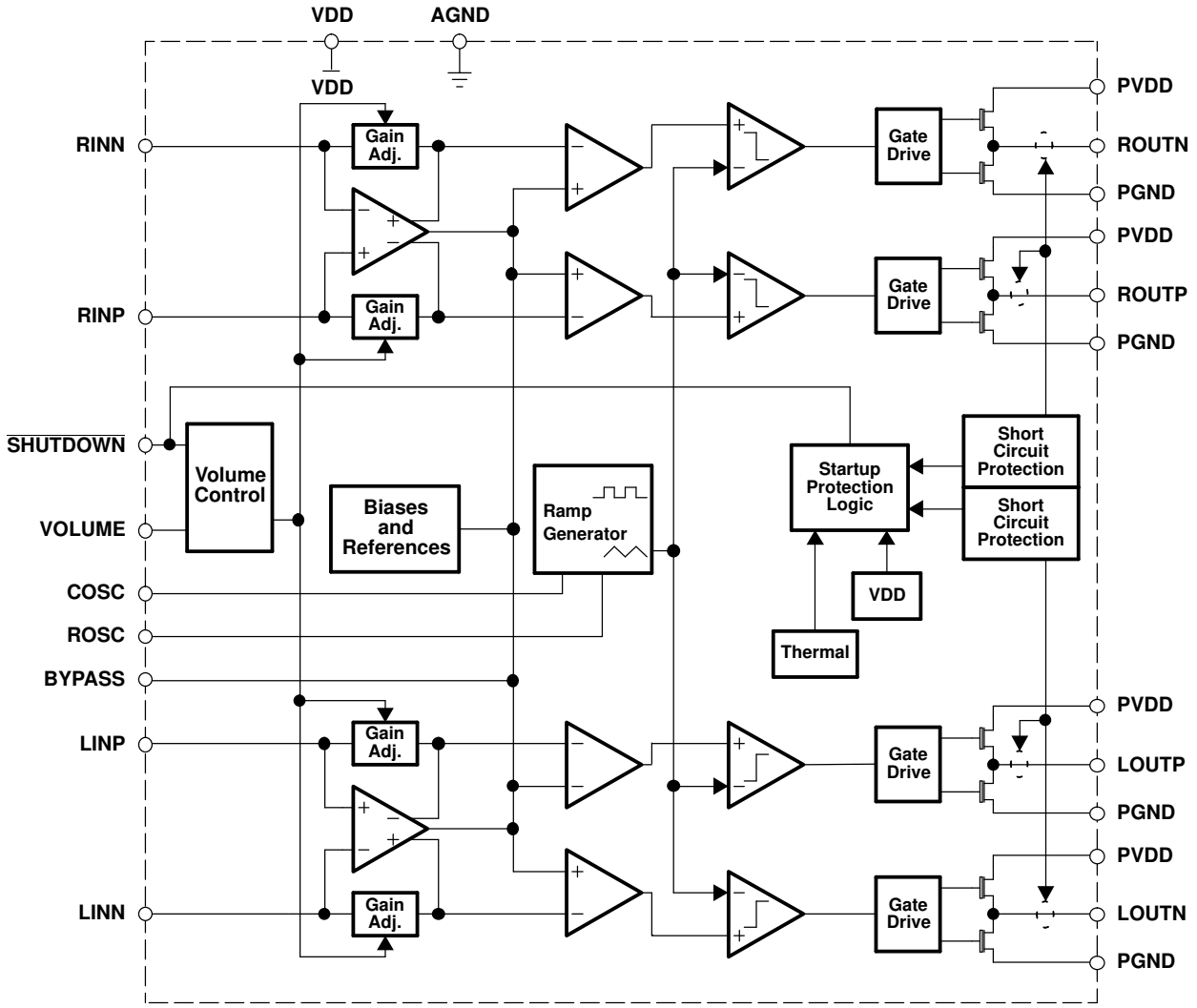
**PWP PACKAGE**
**(TOP VIEW)**



## TERMINAL FUNCTIONS

| TERMINAL NO. | TERMINAL NAME | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 12 | - | Analog ground |
| BYPASS | 22 | I | Tap to voltage divider for internal mid-supply bias generator used for internal analog reference. |
| COSC | 10 | I | A capacitor connected to this terminal sets the oscillation frequency in conjunction with ROSC. For proper operation, connect a 220-pF capacitor from COSC to ground. |
| LINN | 1 | I | Negative differential audio input for left channel |
| LINP | 2 | I | Positive differential audio input for left channel |
| LOUTN | 8 | O | Negative audio output for left channel |
| LOUTP | 5 | O | Positive audio output for left channel |
| NC | 15 | I | No connection |
| PGNDL | 6, 7 | - | Power ground for left channel H-bridge |
| PGNDR | 18, 19 | - | Power ground for right channel H-bridge |
| PVDDL | 4, 9 | | Power supply for left channel H-bridge |
| PVDDR | 16, 21 | | Power supply for right channel H-bridge |
| RINN | 24 | I | Positive differential audio input for right channel |
| RINP | 23 | I | Negative differential audio input for right channel |
| ROSC | 11 | I | A resistor connected to the ROSC terminal sets the oscillation frequency in conjunction with COSC. For proper operation, connect a 120-kΩ resistor from ROSC to ground. |
| ROUTN | 17 | O | Negative output for right channel |
| ROUTP | 20 | O | Positive output for right channel |
| $\overline{\text{SHUTDOWN}}$ | 3 | I | Places the amplifer in shutdown mode if a TTL logic low is placed on this terminal; normal operation if a TTL logic high is placed on this terminal. |
| VDD | 13 | - | Analog power supply |
| VOLUME | 14 | I | DC volume control for setting the gain on the internal amplifiers. The dc voltage range is 0 to VDD. |
| Thermal Pad | - | - | Connect to analog ground and the power grounds must be soldered down in all applications to properly secure device on the PCB. |

## FUNCTIONAL BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

| | | UNIT |
|---|---|---|
| $V_{DD}$,$PV_{DD}$ | Supply voltage range | -0.3 V to 6 V |
| $V_I$ (RINN, RINP, LINN, LINP, VOLUME) | Input voltage range | 0 V to $V_{DD}$ |
| | Continuous total power dissipation | See Dissipation Rating Table |
| $T_A$ | Operating free-air temperature range | -40°C to 85°C |
| $T_J$ | Operating junction temperature range | -40°C to 150°C |
| $T_{stg}$ | Storage temperature range | -65°C to 85°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS TABLE

| PACKAGE | $T_A \leq 25°C$ | DERATING FACTOR | $T_A = 70°C$ | $T_A = 85°C$ |
|---|---|---|---|---|
| PWP | 2.18 W | 21.8 mW/°C | 1.2 W | 872 mW |

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 4.5 | 5.5 | V |
| | Volume terminal voltage | | 0 | $V_{DD}$ | V |
| $V_{IH}$ | High-level input voltage | $\overline{SHUTDOWN}$ | 2 | | V |
| $V_{IL}$ | Low-level input voltage | $\overline{SHUTDOWN}$ | | 0.8 | V |
| | PWM frequency | | 200 | 300 | kHz |
| $T_A$ | Operating free-air temperature | | -40 | 85 | °C |
| $T_J$ | Operating junction temperature | | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

$T_A$= 25°C, $V_{DD}$ = $PV_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\lvert V_{OS} \rvert$ | Output offset voltage (measured differentially) | $V_I$ = 0 V, $A_V$ = 20 dB, $R_L$ = 8Ω | | | 5 | 25 | mV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = $PV_{DD}$ = 4.5 V to 5.5 V | | | -70 | | dB |
| $\lvert I_{IH} \rvert$ | High-level input current | $V_{DD}$ = $PV_{DD}$ = 5.5 V, VI= $V_{DD}$ = $PV_{DD}$ | | | | 1 | µA |
| $\lvert I_{IL} \rvert$ | Low-level input current | $V_{DD}$ = $PV_{DD}$ = 5.5 V, $V_I$ = 0 V | | | | 1 | µA |
| $I_{DD}$ | Supply current | No filter (no load) | | | 7 | 15 | mA |
| $I_{DD(max)}$ | RMS supply current at max power | $R_L$ = 3 Ω, $P_O$ = 2.5 W/channel (stereo) | | | 1.8 | | A |
| $I_{DD(SD)}$ | Supply current in shutdown mode | $\overline{SHUTDOWN}$ = 0 V | | | 50 | 1000 | nA |
| $r_{ds(on)}$ | Drain-source on-state resistance | $V_{DD}$ = 5 V, $I_O$ = 500 mA, $T_J$= 25°C | High side | | 450 | 600 | mΩ |
| | | | Low side | | 450 | 600 | |

## OPERATING CHARACTERISTICS

$T_A$= 25°C, $V_{DD}$ = $PV_{DD}$ = 5 V, $R_L$ = 3 Ω, Gain = 0 dB (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $P_O$ | Output power | f = 1 kHz, $R_L$ = 3 Ω, Stereo operation | THD+N = 1% | | 2.5 | | W |
| | | | THD+N = 10% | | 3 | | |
| THD+N | Total harmonic distortion plus noise | $P_O$ = 2.2 W, f = 20 Hz to 20 kHz | | | <0.3% | | |
| | | $P_O$ = 1.5 W, f = 1 kHz | | | 0.045% | | |
| BOM | Maximum output power bandwidth | THD = 5% | | | 20 | | kHz |
| SNR | Signal-to-noise ratio | Maximum output at THD+N <0.5% | | | 96 | | dB |
| | Thermal trip point | | | | 150 | | °C |
| | Thermal hysteresis | | | | 20 | | °C |
| $V_n$ | Integrated noise floor | 20 Hz to 20 kHz, inputs ac grounded | Volume = 0 dB | | 42 | | $\mu V_{rms}$ |
| | | | Volume = 20 dB | | 85 | | |

**Table 1. TYPICAL DC VOLUME CONTROL**

| VOLTAGE ON VOLUME PIN (V) (INCREASING OR FIXED GAIN) | VOLTAGE ON VOLUME PIN (V) (DECREASING GAIN) | TYPICAL GAIN OF AMPLIFIER (dB) (1) |
|---|---|---|
| 0-0.33 | 0.31-0 | -38 (2) |
| 0.34-0.42 | 0.43-0.32 | -37 |
| 0.43-0.52 | 0.54-0.44 | -35 |
| 0.53-0.63 | 0.64-0.55 | -33 |
| 0.64-0.75 | 0.75-0.65 | -31 |
| 0.76-0.86 | 0.86-0.76 | -29 |
| 0.87-0.97 | 0.97-0.87 | -27 |
| 0.98-1.07 | 1.08-0.98 | -25 |
| 1.08-1.18 | 1.19-1.09 | -23 |
| 1.19-1.30 | 1.32-1.20 | -21 |
| 1.31-1.41 | 1.42-1.33 | -19 |
| 1.42-1.52 | 1.53-1.43 | -17 |
| 1.53-1.63 | 1.63-1.54 | -15 |
| 1.64-1.75 | 1.75-1.64 | -13 |
| 1.76-1.85 | 1.84-1.76 | -12 |
| 1.86-1.96 | 1.96-1.85 | -10 |
| 1.97-2.07 | 2.09-1.97 | -8 |
| 2.08-2.18 | 2.19-2.10 | -6 |
| 2.19-2.30 | 2.33-2.20 | -4 |
| 2.31-2.40 | 2.43-2.34 | -2 |
| 2.41-2.52 | 2.49-2.44 | 0 (2) |
| 2.53-2.63 | 2.62-2.50 | 2 |
| 2.64-2.75 | 2.75-2.63 | 4 |
| 2.76-2.87 | 2.85-2.76 | 6 |
| 2.88-2.98 | 2.99-2.86 | 8 |
| 2.99-3.10 | 3.12-3.00 | 10 |
| 3.11-3.22 | 3.25-3.13 | 12 |
| 3.23-3.33 | 3.36-3.26 | 14 |
| 3.34-3.47 | 3.48-3.37 | 16 |
| 3.48-3.69 | 3.64-3.49 | 18 |
| 3.70-$V_{DD}$ | $V_{DD}$-3.65 | 20 (2) |

(1) The typical part-to-part gain variation can be as large as ±2 dB (one gain step).
(2) Tested in production.

The volume control circuitry of the TPA2008D2 is internally referenced to the VDD and AGND terminals. Any common-mode noise between the VOLUME terminal and these terminals will be sensed by the volume control circuitry. If the noise exceeds the step size voltage, the gain will change. In order to minimize this effect, care must be taken to ensure the signal driving the VOLUME terminal is referenced to the VDD and AGND terminals of the TPA2008D2. See section titled, “Special Layout Considerations” for more details.

## TYPICAL CHARACTERISTICS

### TABLE OF GRAPHS

| | | | FIGURE |
|---|---|---|---|
| | Efficiency | vs Output power | 1, 2 |
| THD+N | Total harmonic distortion + noise | vs Frequency | 3-5 |
| | | vs Output power | 6-8 |
| $k_{SVR}$ | Supply ripple rejection ratio | vs Frequency | 9 |
| | Crosstalk | vs Frequency | 10 |
| CMRR | Common-mode rejection ratio | vs Frequency | 11 |
| $R_i$ | Input resistance | vs Gain setting | 12 |

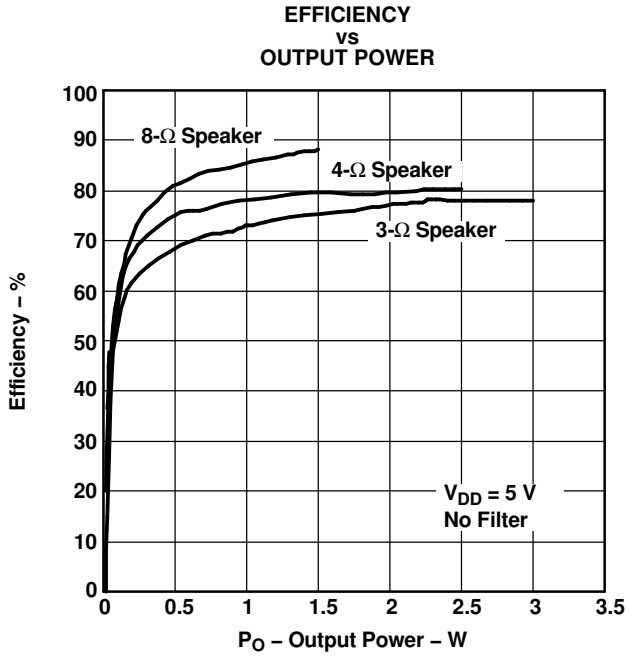



Figure 1.

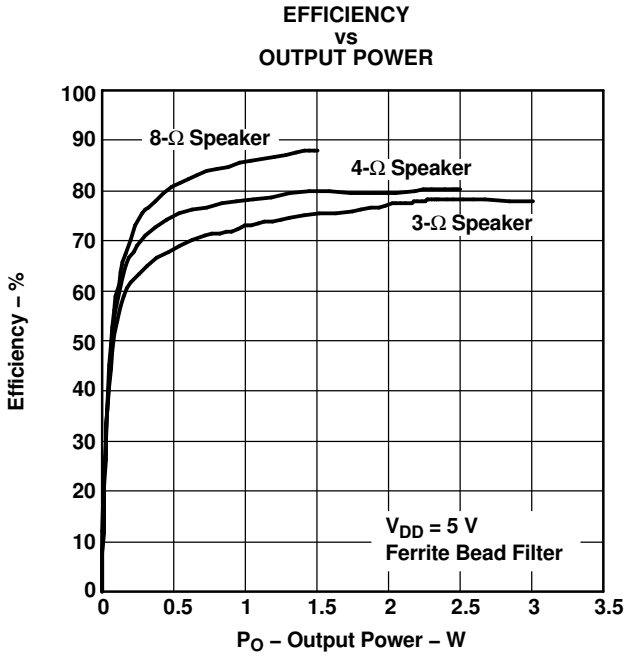



Figure 2.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

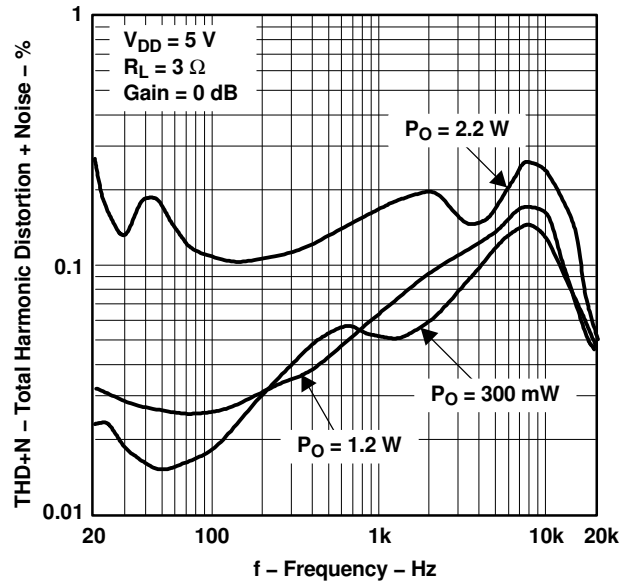



Figure 3.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

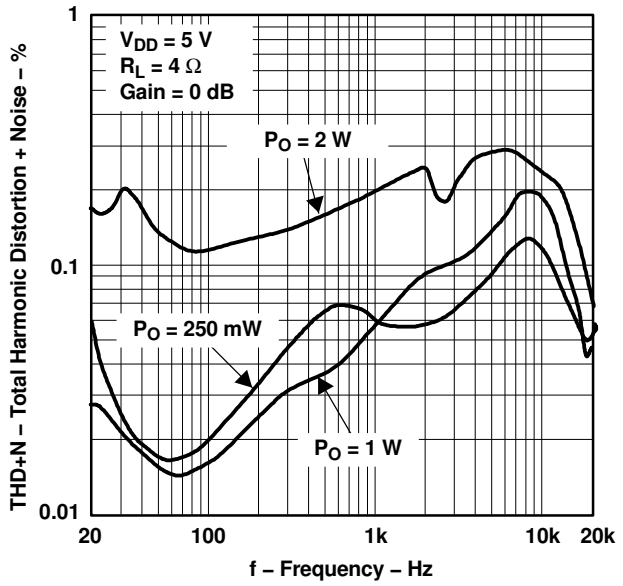



Figure 4.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

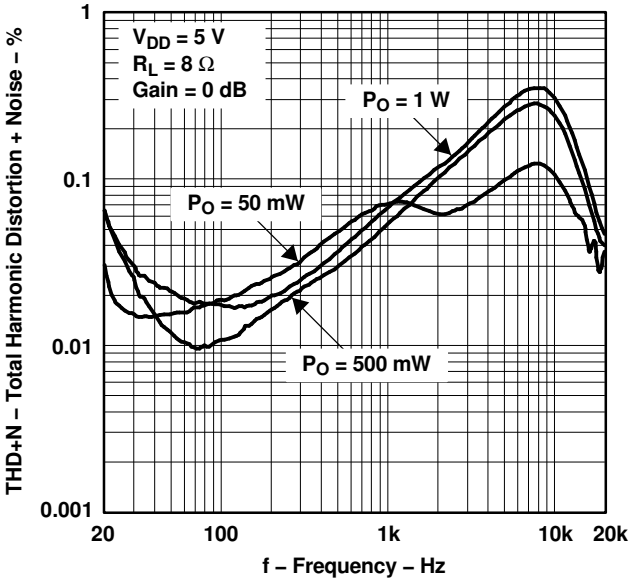



Figure 5.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

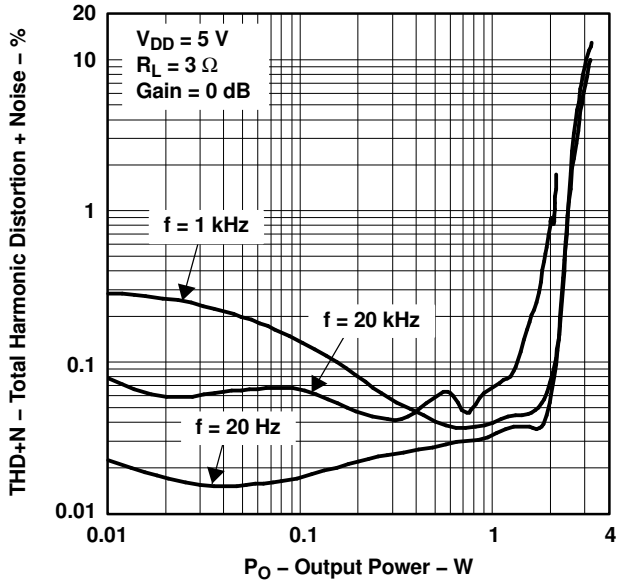



Figure 6.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

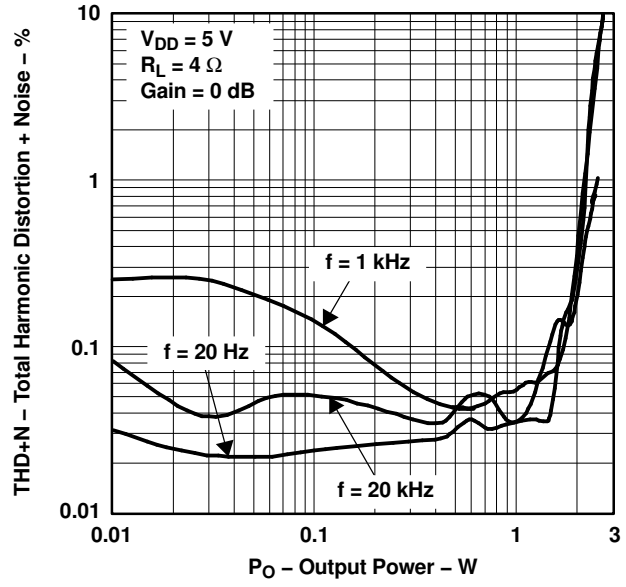



Figure 7.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

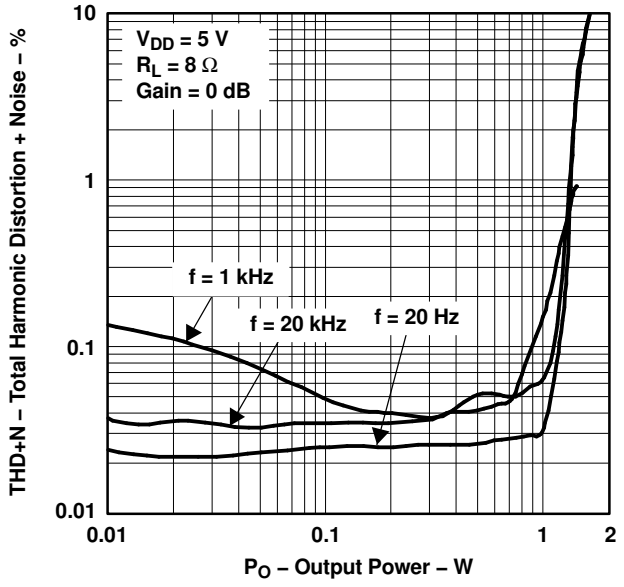



Figure 8.

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

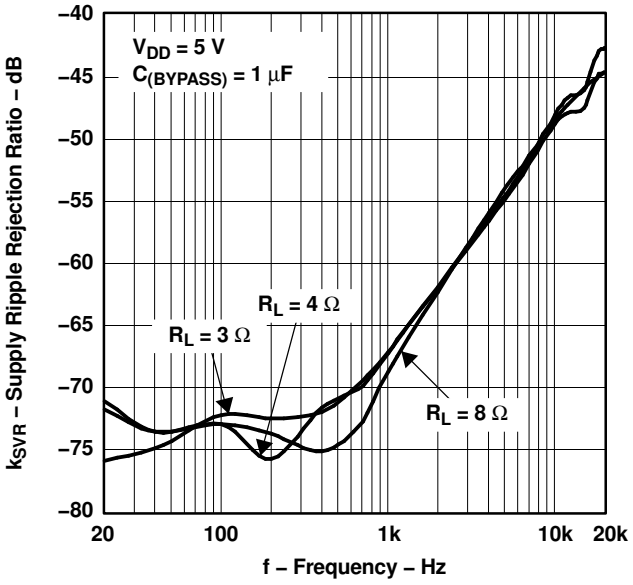



Figure 9.

CROSSTALK
vs
FREQUENCY

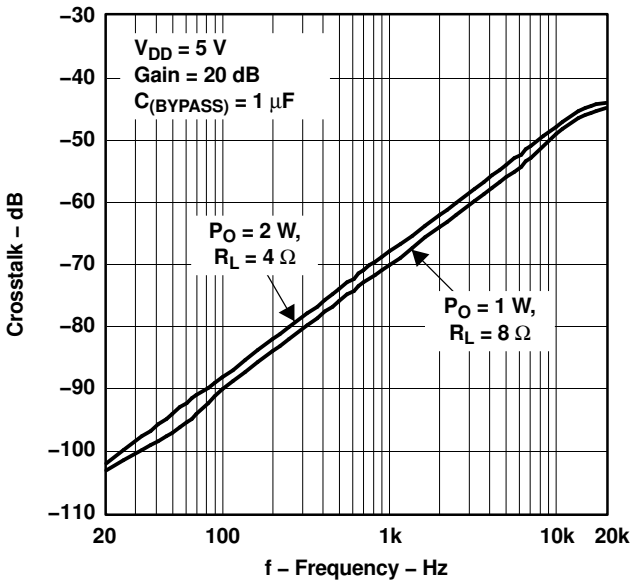



Figure 10.

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

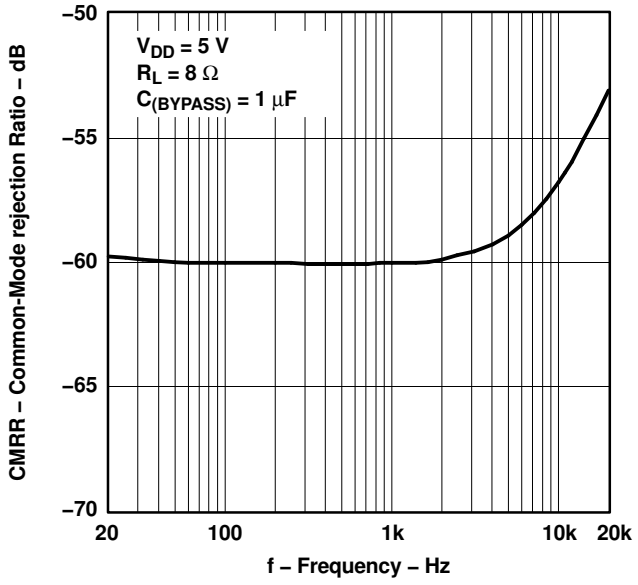



Figure 11.

**INPUT RESISTANCE vs GAIN SETTING**

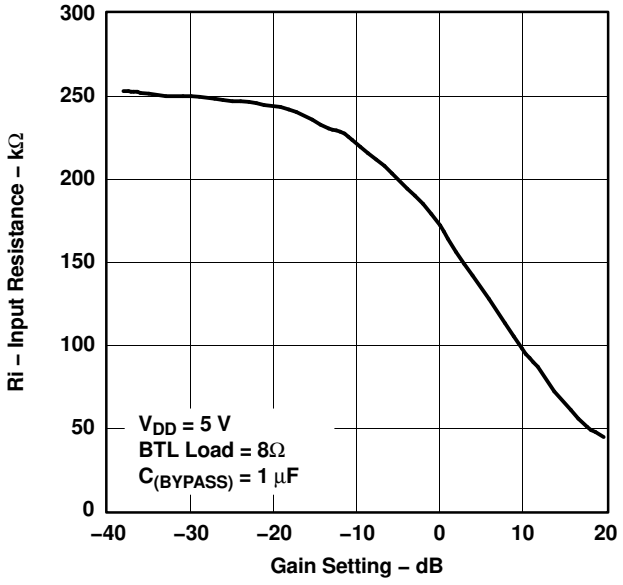



Figure 12.

## APPLICATION INFORMATION

### APPLICATION CIRCUIT

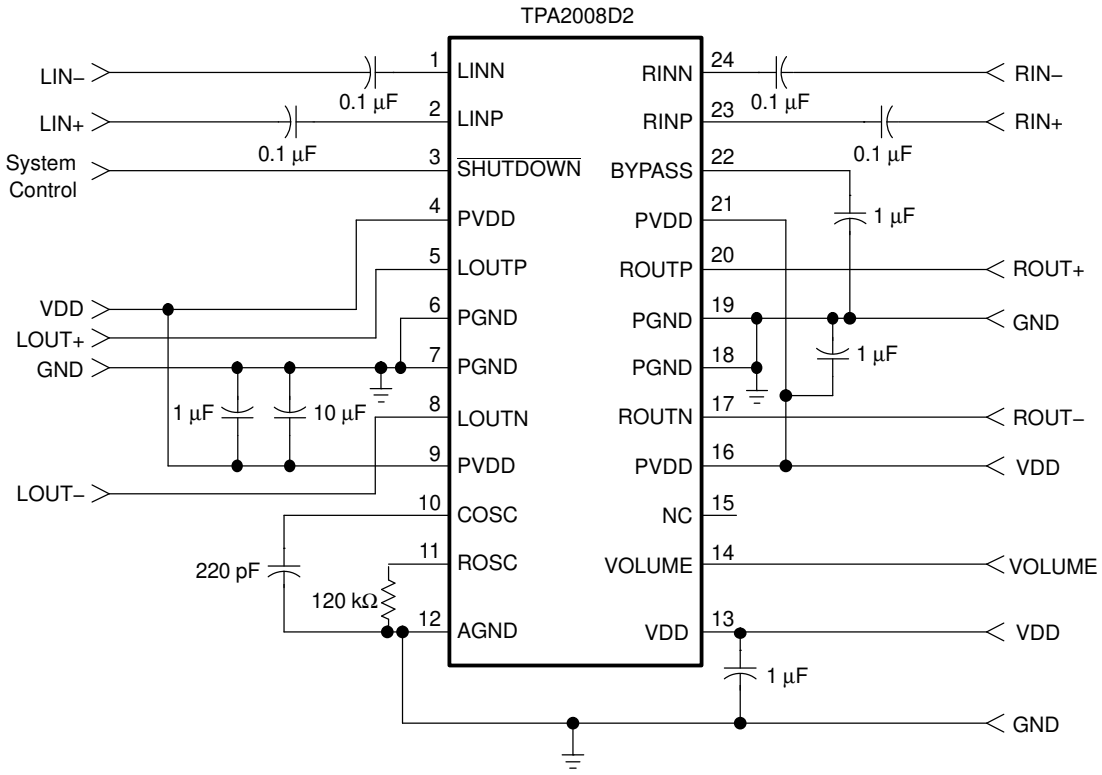



**Figure 13. TPA2008D2 In A Stereo Configuration With Differential Inputs**

## APPLICATION INFORMATION (continued)

### TRADITIONAL CLASS-D MODULATION SCHEME

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, $V_{CC}$. Therefore, the differential prefiltered output varies between positive and negative $V_{CC}$, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 14. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, resulting in a high $I^2R$ loss, thus causing a high supply current.

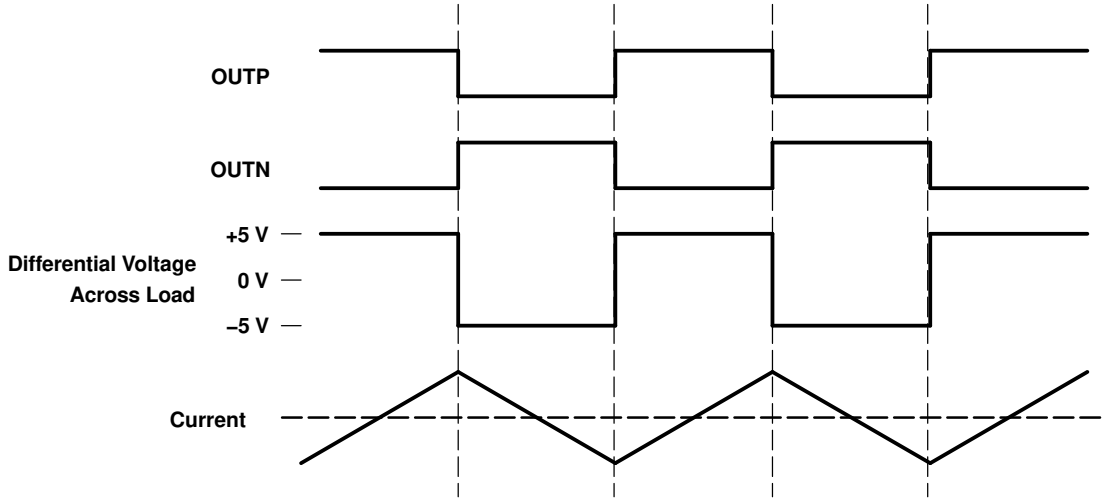



**Figure 14. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input**

## APPLICATION INFORMATION (continued)

### TPA2008D2 MODULATION SCHEME

The TPA2008D2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any $I^2R$ losses in the load.

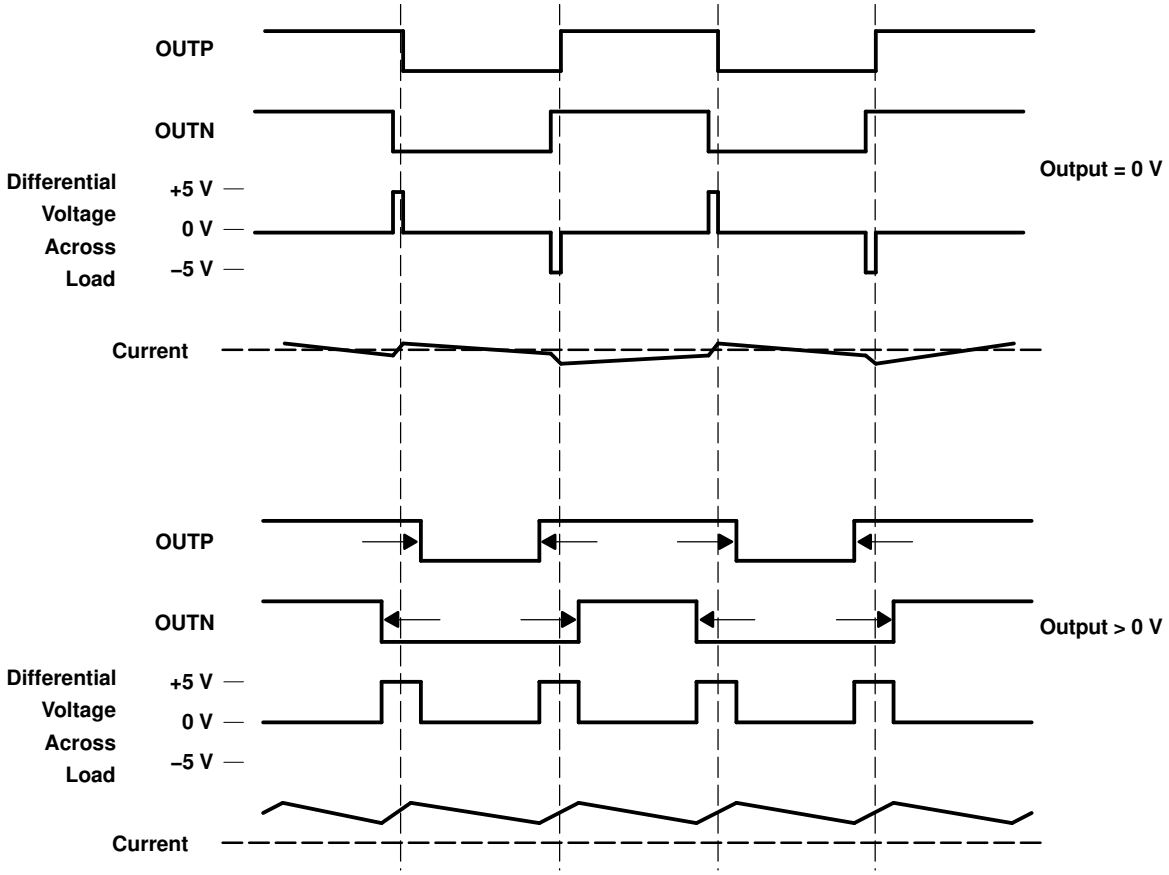



**Figure 15. The TPA2008D2 Output Voltage and Current Waveforms Into an Inductive Load**

### EFFICIENCY: LC FILTER REQUIRED WITH THE TRADITIONAL CLASS-D MODULATION SCHEME

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{DD}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2008D2 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is $V_{DD}$ instead of $2 \times V_{DD}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker, which results in less power dissipation, therefore increasing efficiency.

## APPLICATION INFORMATION (continued)

### EFFECTS OF APPLYING A SQUARE WAVE INTO A SPEAKER

Audio specialists have advised for years not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, does not significantly move the voice coil, as the cone movement is proportional to $1/f^2$ for frequencies beyond the audio band.

Damage may occur if the voice coil cannot handle the additional heat generated from the high-frequency switching current. The amount of power dissipated in the speaker may be estimated by first considering the overall efficiency of the system. If the on-resistance ($r_{ds(on)}$) of the output transistors is considered to cause the dominant loss in the system, then the maximum theoretical efficiency for the TPA2008D2 with an 4-Ω load is as follows:

$$\text{Efficiency (theoretical, \%)} = R_L / \left( R_L + r_{ds(on)} \right) \times 100\% = 4/(4 + 0.45) \times 100\% = 89.9\% \quad (1)$$

The maximum measured output power is approximately 2.5 W with a 5-V power supply. The total theoretical power supplied ($P_{(total)}$) for this worst-case condition would therefore be as follows:

$$P_{(total)} = P_O/\text{Efficiency} = 2.5\ \text{W} / 0.899 = 2.781\ \text{W} \quad (2)$$

The efficiency measured in the lab using a 4-Ω speaker was 80%. The power not accounted for as dissipated across the $r_{ds(on)}$ may be calculated by simply subtracting the theoretical power from the measured power:

$$\text{Other losses} = P_{(total)}\text{(measured)} - P_{(total)}\text{ (theoretical)} = 3.025 - 2.781 = 0.244\ \text{W} \quad (3)$$

The quiescent supply current at 5 V is measured to be 7 mA. It can be assumed that the quiescent current encapsulates all remaining losses in the device, i.e., biasing and switching losses. It may be assumed that any remaining power is dissipated in the speaker and is calculated as follows:

$$P_{(dis)} = 0.244\ \text{W} - (5\ \text{V} \times 7\ \text{mA}) = 0.209\ \text{W} \quad (4)$$

Note that these calculations are for the worst-case condition of 2.5 W delivered to the speaker. Since the 0.209 W is only 7.4% of the power delivered to the speaker, it may be concluded that the amount of power actually dissipated in the speaker is relatively insignificant. Furthermore, this power dissipated is well within the specifications of most loudspeaker drivers in a system, as the power rating is typically selected to handle the power generated from a clipping waveform.

### WHEN TO USE AN OUTPUT FILTER

Design the TPA2008D2 without the filter if the traces from amplifier to speaker are short (< 1 inch). Powered speakers, where the speaker is in the same enclosure as the amplifier, is a typical application for class-D without a filter.

Many applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires from the amplifier to the speaker.

## APPLICATION INFORMATION (continued)

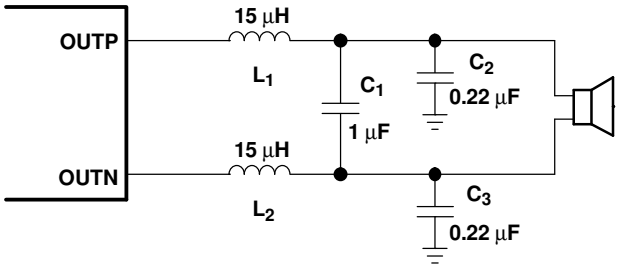



**Figure 16. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance = 4Ω**

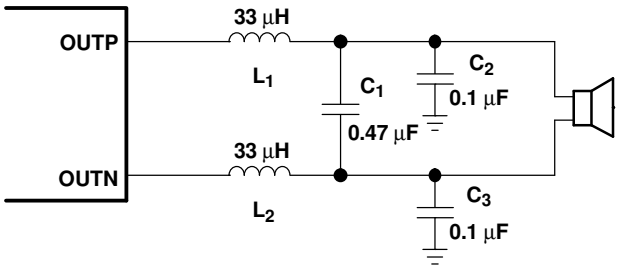



**Figure 17. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance = 8 Ω**

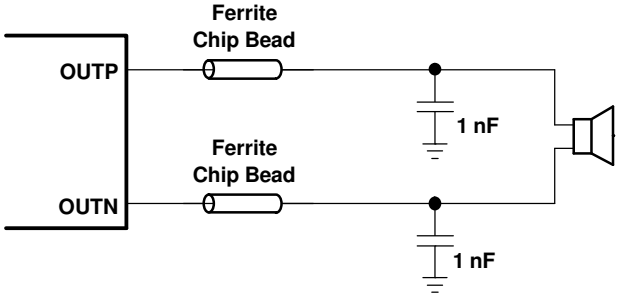



**Figure 18. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)**

## APPLICATION INFORMATION (continued)

### VOLUME CONTROL OPERATION

The VOLUME pin controls the volume of the TPA2008D2. It is controlled with a dc voltage, which should not exceed $V_{DD}$. Table 1 lists the voltage on the VOLUME pin and the corresponding gain.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. A pictorial representation of the volume control can be found in Figure 19. The graph focuses on three gain steps with the trip points defined in the first and second columns of Table 1. The dotted lines represent the hysteresis about each gain step.

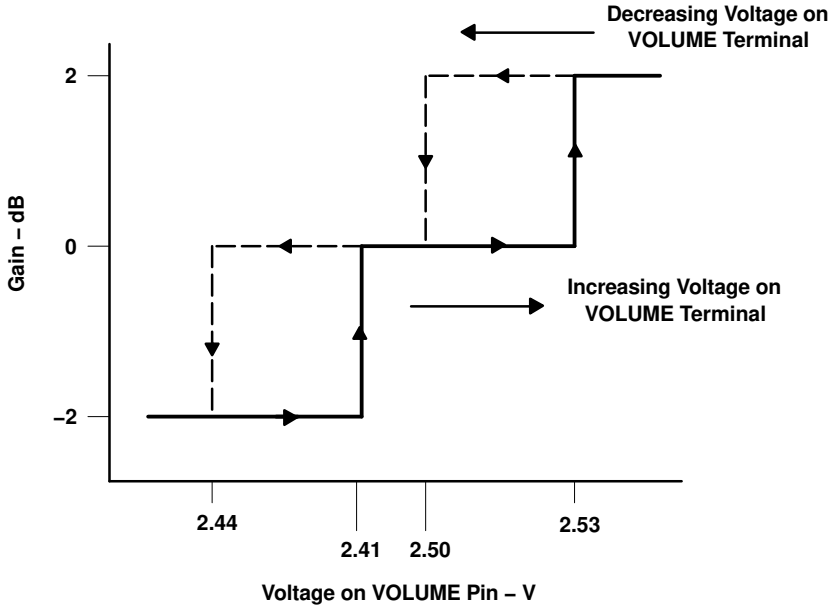



**Figure 19. DC Volume Control Operation**

### SPECIAL LAYOUT CONSIDERATIONS

The voltage on the VOLUME pin must closely track that of the supply voltage, $V_{DD}$. As the output power is increased, the noise on the power supply will increase. The noise seen by the $PV_{DD}$ pin must also be seen by the VOLUME pin. It is for that reason that absolutely no capacitor should be placed on the VOLUME pin. Additional steps should be taken to reduce the line capacitance on the VOLUME pin, such as reducing line length. Any capacitance on the VOLUME pin will act as a filter, thus making the voltage seen by the VOLUME pin and $V_{DD}$ different. If the difference is large enough, the amplifier will change gain steps.

A star point should be used for power, where the supply voltage for $V_{DD}$, $PV_{DD}$, and the volume circuitry can be taken. This point is typically at the bulk decoupling capacitor. The trace connecting the star point to a potentiometer or a DAC should be short. The trace connecting the potentiometer or DAC to the VOLUME pin should be kept as short and straight as possible.

As with the VDD, a star ground should likewise be used. There should exist on the board a point where AGND and PGND converge. This should be the only place where the two grounds are connected. The ground used for the volume control should be AGND. If a potentiometer is to be used to control the volume of the device, it should be connected to AGND. A DAC that has a ground reference should have a short trace to AGND from its ground reference input.

For an example of proper board layout, please refer to the TPA2008D2 EVM User's Guide, document number SLOU116.

## APPLICATION INFORMATION (continued)

### SELECTION OF COSC AND ROSC

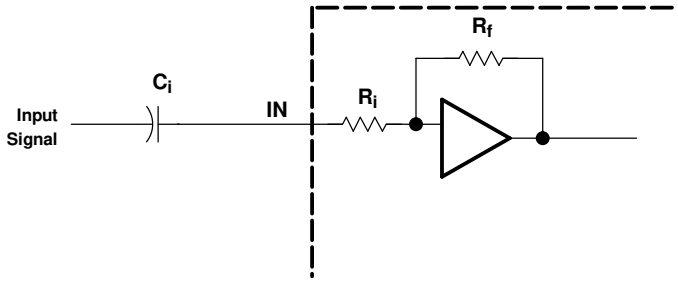
The switching frequency is determined using the values of the components connected to ROSC (pin 11) and COSC (pin 10) and may be calculated with the following equation:

$$f_{OSC} = 6.6 / (R_{OSC} \times C_{OSC}) \quad (5)$$

The frequency may be varied from 200 kHz to 300 kHz by adjusting the values chosen for $R_{OSC}$ and $C_{OSC}$. The recommended values are $C_{OSC}$ = 220 pF, $R_{OSC}$= 120 kΩ for a switching frequency of 250 kHz.

### INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over five times that value. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency also changes by over five times.



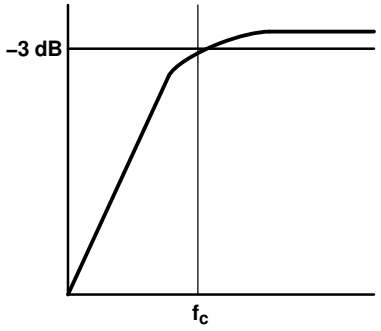

The -3-dB frequency can be calculated using equation Equation 6. See Figure 12. Note that due to process variation, the input resistance, $R_i$, can change by up to 20%.

$$f_{-3\ dB} = \frac{1}{2\pi C_i R_i} \quad (6)$$

### INPUT CAPACITOR, $C_i$

In a typical application, an input capacitor ($C_i$) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, $C_i$ and the input resistance of the amplifier ($R_i$) form a high-pass filter with the corner frequency determined in equation Equation 7.

$$f_c = \frac{1}{2\pi R_i C_i} \quad (7)$$




The value of $C_i$ is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where $R_i$ is 50 kΩ and the specification calls for a flat bass response down to 30 Hz. Equation Equation 5 is reconfigured as equation Equation 8.

$$C_i = \frac{1}{2\pi R_i f_c} \quad (8)$$

In this example, $C_i$ is 0.1 µF, so one would likely choose a value in the range of 0.1 µF to 1 µF. Figure 12 can be used to determine the input impedance for a given gain and can serve to aid in the calculation of $C_i$.

## APPLICATION INFORMATION (continued)

A further consideration for this capacitor is the leakage path from the input source through the input network ($C_i$) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

$C_i$ must be 10 times smaller than the bypass capacitor to reduce clicking and popping noise from power on/off and entering and leaving shutdown. After sizing $C_i$ for a given cutoff frequency, size the bypass capacitor to 10 times that of the input capacitor.

$$C_i \leq C_{BYP} / 10 \quad (9)$$

## POWER SUPPLY DECOUPLING, $C_S$

The TPA2008D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device $V_{DD}$ terminal works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

## MIDRAIL BYPASS CAPACITOR, $C_{BYP}$

The midrail bypass capacitor ($C_{BYP}$) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{BYP}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor ($C_{BYP}$) values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown. To have minimal pop, $C_{BYP}$ should be 10 times larger than $C_i$.

$$C_{BYP} \geq 10 \times C_i \quad (10)$$

## DIFFERENTIAL INPUT

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA2008D2 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA2008D2 with a single-ended source, ac ground either input through a capacitor and apply the audio signal to the remaining input. In a single-ended input application, the unused input should be ac-grounded at the audio source instead of at the device input for best noise performance.

## SHUTDOWN MODES

The TPA2008D2 employs a shutdown mode of operation designed to reduce supply current ($I_{DD}$) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(SD)}$ = 1 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because the amplifier state would be unpredictable.

## APPLICATION INFORMATION (continued)

### USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

### SHORT-CIRCUIT PROTECTION

The TPA2008D2 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-$V_{DD}$ shorts. When a short-circuit is detected on the outputs, the part immediately goes into shutdown. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin to a logic low and back to the logic high, or by cycling the power off and then back on. This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry activates again.

### LOW-SUPPLY VOLTAGE DETECTION

The TPA2008D2 incorporates circuitry designed to detect when the supply voltage is low. When the supply voltage reaches 1.8 V or below, the TPA2008D2 goes into a state of shutdown. The current consumption drops from millamperes to microamperes, leaving the remaining battery power for more essential devices such as microprocessors. When the supply voltage level returns to normal, the device comes out of its shutdown state and starts to draw current again. Note that even though the device is drawing several milliamperes of current, it is not operationally functional until $V_{DD} \geq 4.5$ V.

### THERMAL PROTECTION

Thermal protection on the TPA2008D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 20°C. The device begins normal operation at this point with no external system interaction.

### THERMAL CONSIDERATIONS: OUTPUT POWER AND MAXIMUM AMBIENT TEMPERATURE

To calculate the maximum ambient temperature, the following equation may be used:

$$T_{Amax} = T_J - \Theta_{JA} P_{Dissipated}$$

where: $T_J = 125°C$

$\Theta_{JA} = 45.87°C/W$ (11)

(The derating factor for the 24-pin PWP package is given in the dissipation rating table.)

To estimate the power dissipation, the following equation may be used:

$$P_{Dissipated} = P_{O(average)} \times ((1 / Efficiency) - 1)$$

Efficiency = ~85% for an 8-Ω load

= ~80% for a 4-Ω load

= ~75% for a 3-Ω load (12)

Example. What is the maximum ambient temperature for an application that requires the TPA2008D2 to drive 2 W into a 4-Ω speaker (stereo)?

$P_{Dissipated}$ = 4 W x ((1 / 0.8) - 1) = 1 W

($P_O$ = 2 W x 2)

$T_{Amax}$ = 125°C - (45.87°C/W x 1 W) = 79.13°C

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA2008D2PWP | ACTIVE | HTSSOP | PWP | 24 | 60 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPA2008D2 | Samples |
| TPA2008D2PWPR | ACTIVE | HTSSOP | PWP | 24 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPA2008D2 | Samples |
| TPA2008D2PWPRG4 | ACTIVE | HTSSOP | PWP | 24 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPA2008D2 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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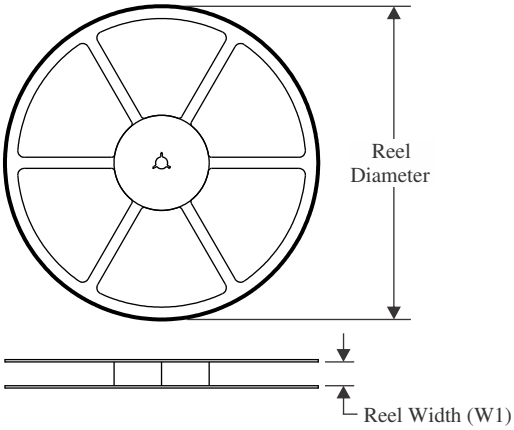
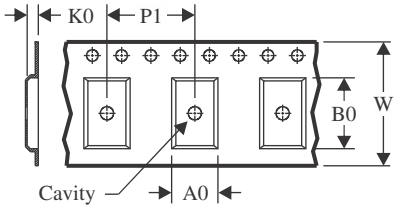
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

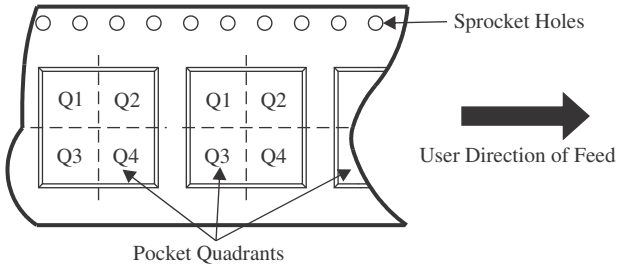



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

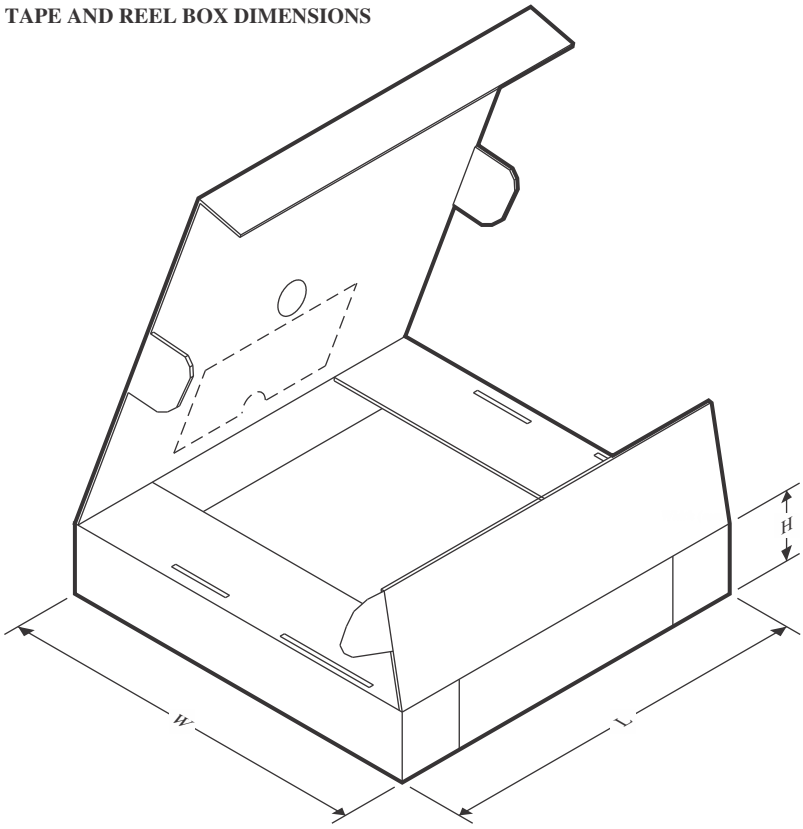
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA2008D2PWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| TPA2008D2PWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

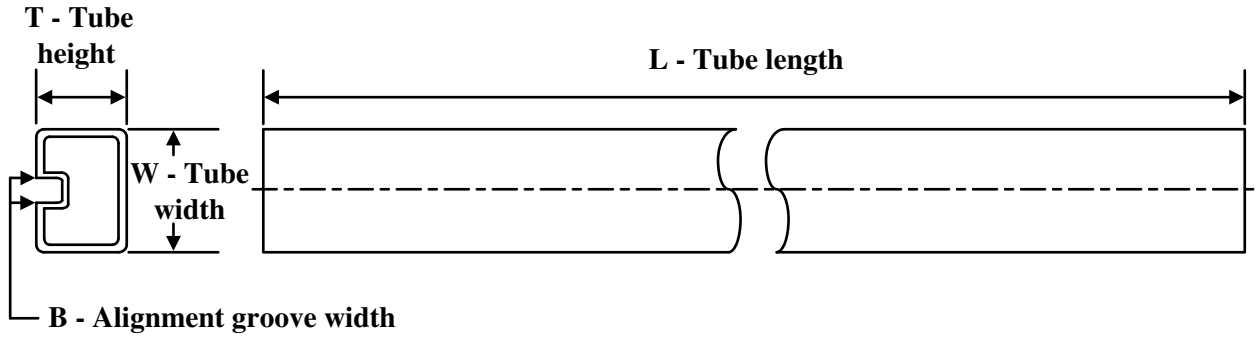
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPA2008D2PWPR | HTSSOP | PWP | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| TPA2008D2PWPR | HTSSOP | PWP | 24 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPA2008D2PWP | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPA2008D2PWP | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

# GENERIC PACKAGE VIEW

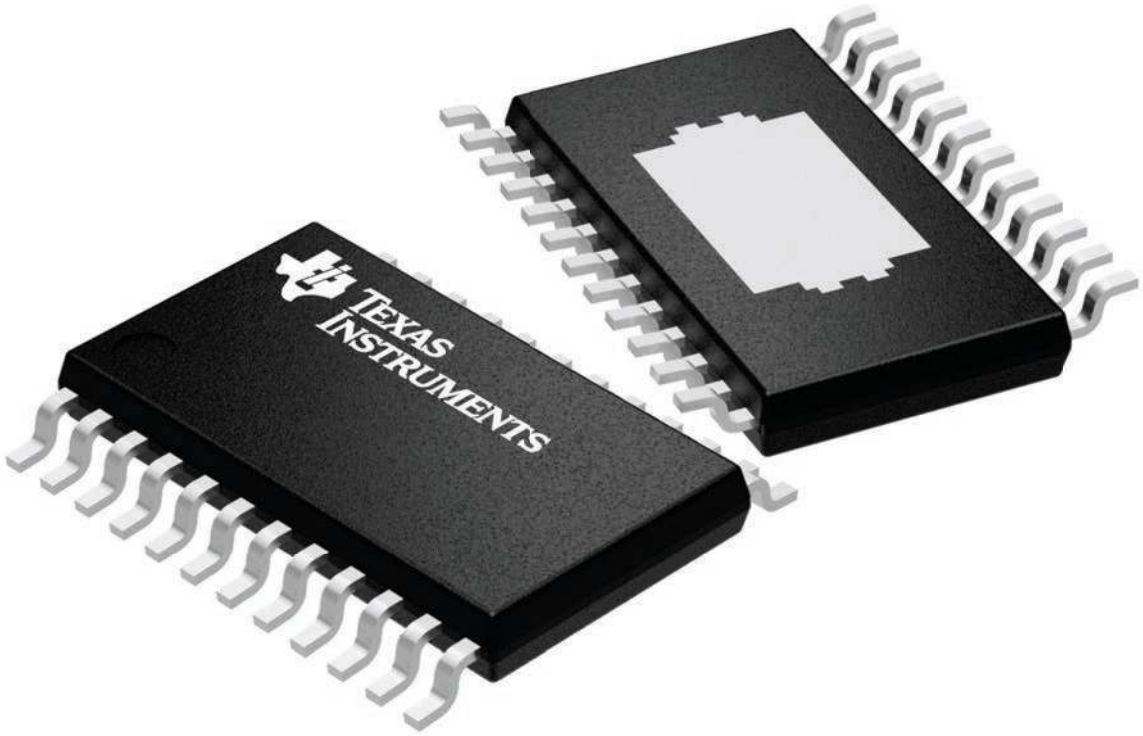
## PWP 24

## PowerPAD™ TSSOP - 1.2 mm max height

**4.4 x 7.6, 0.65 mm pitch**

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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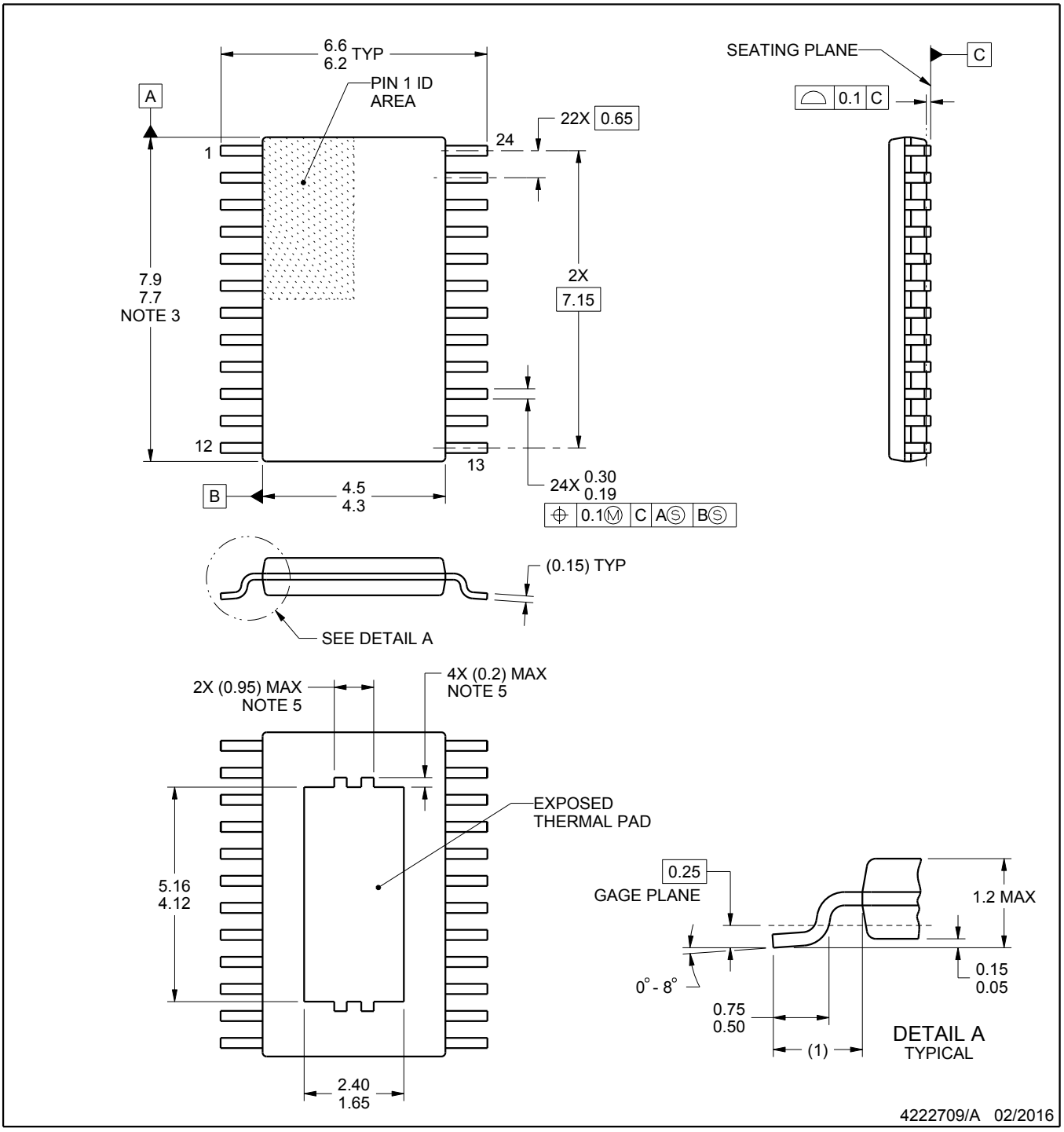
# PACKAGE OUTLINE

## PWP0024B

## PowerPAD™ TSSOP - 1.2 mm max height

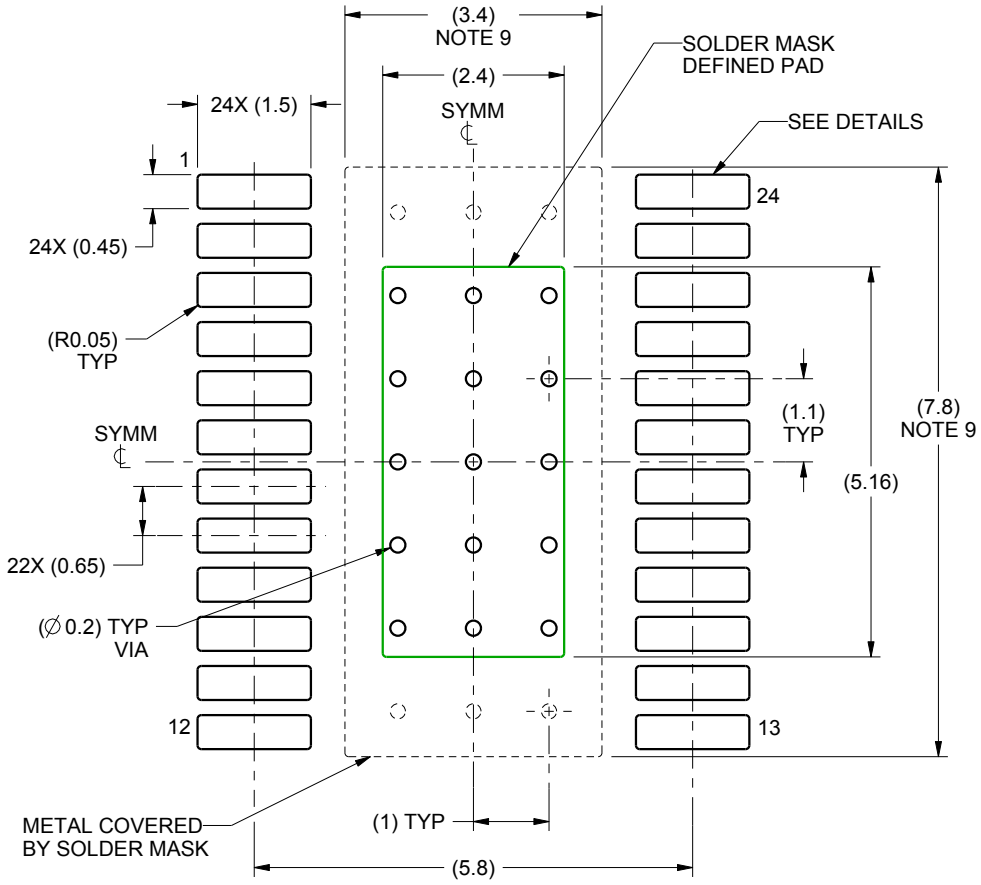
PLASTIC SMALL OUTLINE



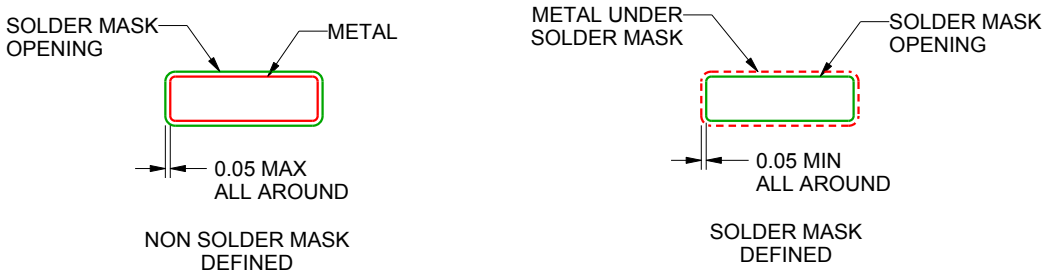

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.




LAND PATTERN EXAMPLE
SCALE:10X

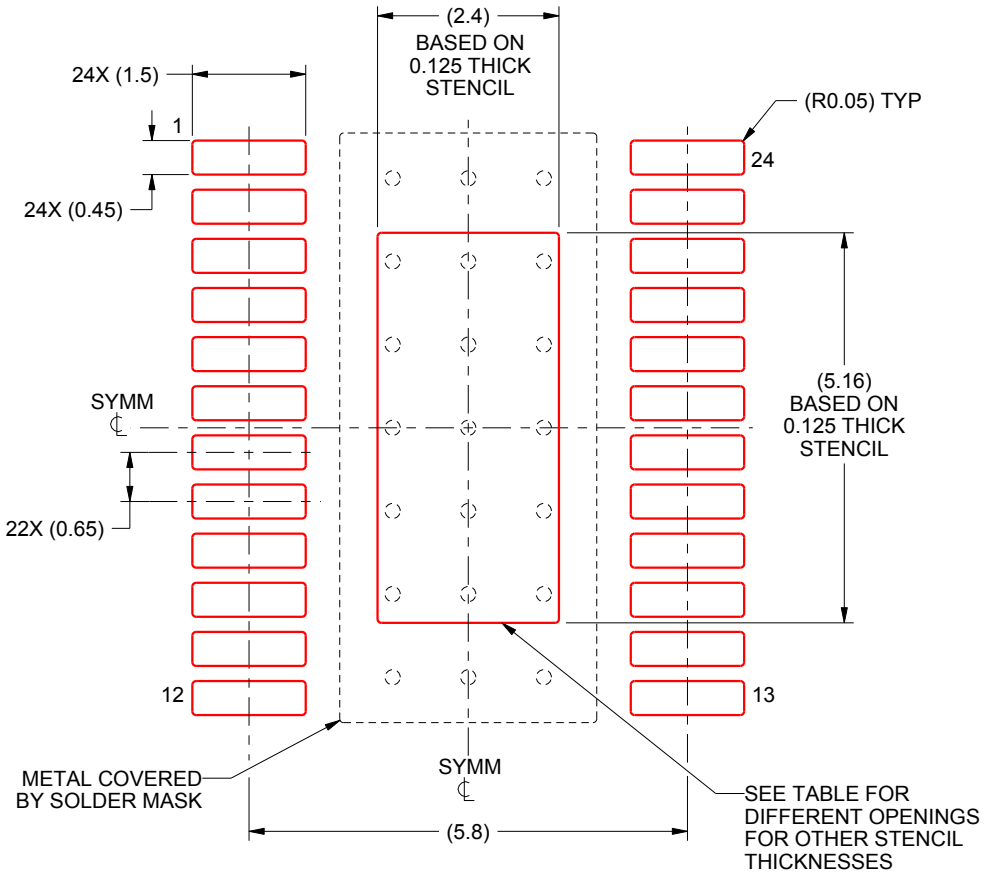



SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 2.68 X 5.77 |
| 0.125 | 2.4 X 5.16 (SHOWN) |
| 0.15 | 2.19 X 4.71 |
| 0.175 | 2.03 X 4.36 |

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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