LT3942
36V 4-Switch Buck-Boost Voltage Regulator

DESCRIPTION

Demonstration circuit DC3103A is a monolithic 4-Switch buck-boost voltage regulator featuring the LT®3942. It has been designed with an output voltage set to 12V with capability of delivering up to 1A when the input voltage is between 7V and 36V. The demonstration circuit continues operating with an input voltage as low as 3V with reduced output power capability. DC3103A is configured for 2MHz switching frequency with spread spectrum frequency modulation (SSFM) disabled. When enabled, SSFM adjusts the switching frequency of the LT3942 between 2MHz and 2.5MHz for improved EMI performance.

The LT3942 has an operating input voltage range of 3V to 36V. It has internal, synchronous 40V switches for high efficiency and small size. It has an adjustable switching frequency between 300kHz and 2MHz. The LT3942 can by synchronized to an external oscillator source, programmed with SSFM enabled for low EMI, or set to normal operation.

The board is designed with ceramic capacitors placed near the PVIN and PVOUT pins to form a compact high frequency hotloop. SMD pads are available to install an optional ferrite bead EMI filter on both the input and output of DC3103A. Small cuts on the top layer copper between the SMD pads of both ferrite bead components are necessary to install the EMI filter correctly. These filters, combined with proper board layout and SSFM, are effective in reducing both radiated and conducted EMI. Please follow the recommended layout and four-layer PCB thickness of DC3103A for low EMI applications.

DC3103A uses the LT3942's voltage regulation loop to program a constant-voltage output of 12V. The LT3942 can operate as a constant voltage regulator as well as a constant current regulator. For LED driver designs, please refer to demonstration circuit DC2404A. DC2404A includes a high-side PMOS disconnect switch to assist with PWM dimming, as well as several other optimizations for LED driver applications.

The LT3942 datasheet gives a complete description of the part, operation, and applications information. The datasheet must be read in conjunction with this User Guide for DC3103A. The LT3942EUFD is assembled in a 28-lead plastic QFN (UFD) package with a thermally-enhanced exposed ground pad. Proper board layout is essential for maximum thermal and low-noise performance. Refer to DC3103A's design files files for recommended layout and routing of the LT3942 for voltage regulator applications.

Design files for this circuit board are available.

PERFORMANCE SUMMARY

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage PV_{IN} Range	Operating	3		36	V
Input Voltage PV_{IN} Range (Full Power)	V_{OUT} = 12V, I_{OUT} = 1A	7		36	V
Switching Frequency (f_{SW})	R4 = 14.3kΩ, JP1 = NO SSFM/SYNC		2.0		MHz
Spread Spectrum (SSFM) Range	R4 = 14.3kΩ, JP1 = SSFM	2.0		2.5	MHz
Output Voltage V_{OUT}	R2 = 110kΩ, R3 = 10kΩ		12		V
Typical Efficiency	PV_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 1A, f_{SW} = 2MHz JP1 = NO SSFM/SYNC		89		%
Peak Switch Current Limit		2.2	2.5	2.8	A
PV_{IN} Undervoltage Lockout (UVLO) Falling	R7 = 402kΩ, R12 = 324kΩ		3.0		V
PV_{IN} Enable Turn-On (EN) Rising	R7 = 402kΩ, R12 = 324kΩ		4.0		V
PV_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.3V, V_{OUT} = 12V $V_{EN/UVLO}$ = 1.3V, V_{OUT} = 12V, Not Switching		0.9 2.6	2 4	µA mA

QUICK START PROCEDURE

Demonstration circuit DC3103A is easy to set up to evaluate the performance of the LT3942. Follow the procedure below.

1. With power off, connect a load capable of 12V 1A operation between the VOUT and GND turrets on the PCB as shown in Figure 1.
2. Connect the EN/UVLO turret to GND.
3. Set JP1 to NO SSFM/SYNC to run without SSFM.
4. With power off, connect an input power supply to the PV_{IN} and GND turrets. Make sure that the DC input voltage will not exceed 40V.
5. Turn the input power supply on and adjust the voltage between 7V and 36V for full output power capability and accurate 12V output regulation. Below 7V, output power capability is reduced.
6. Release the EN/UVLO-to-GND connection.
7. Observe the load running at the programmed output voltage.
8. To enable spread spectrum frequency modulation, set JP1 to SSFM ON.

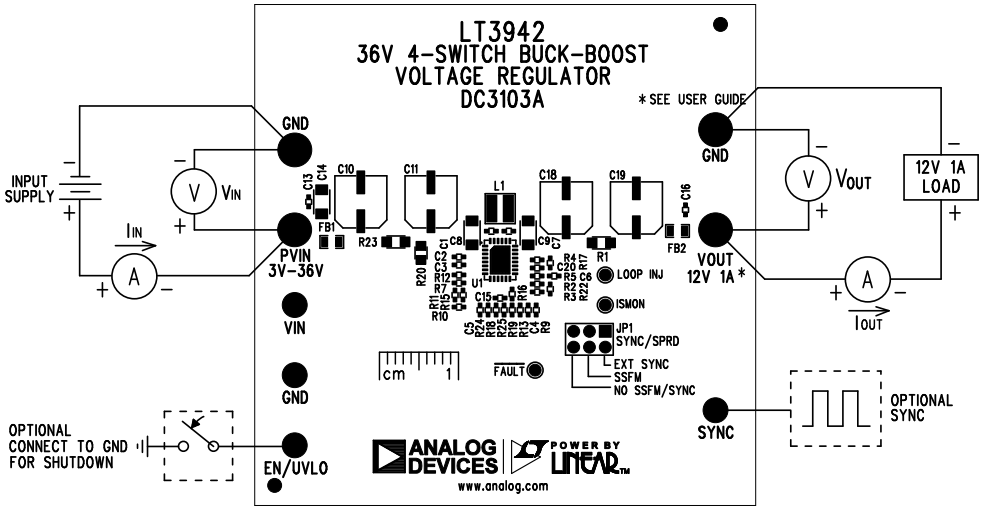


Figure 1. . Test Procedure Setup Drawing for DC3103A

QUICK START PROCEDURE

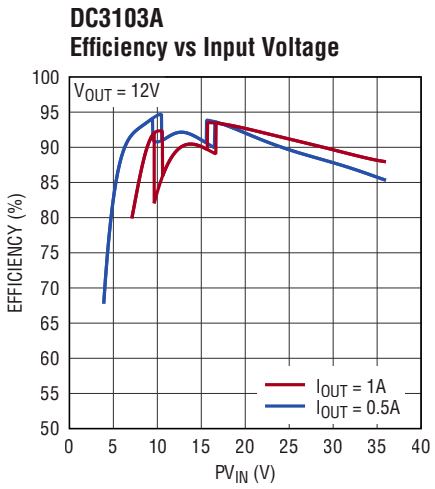


Figure 2. DC3103A Efficiency vs Input Voltage, SSFM OFF

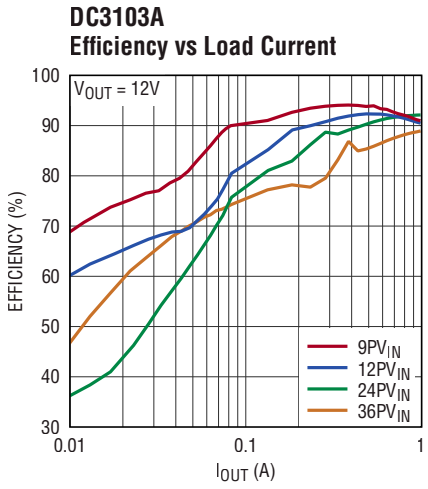


Figure 3. DC3103A Efficiency vs Load Current, SSFM OFF

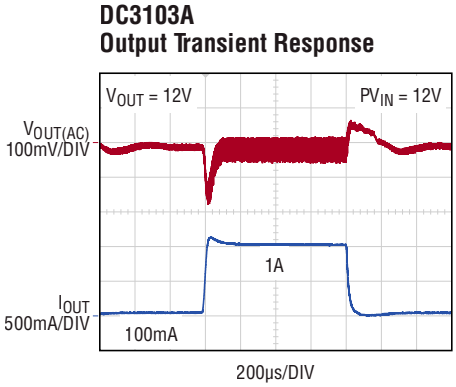


Figure 4. DC3103A 10% to 100% Load Step Transient

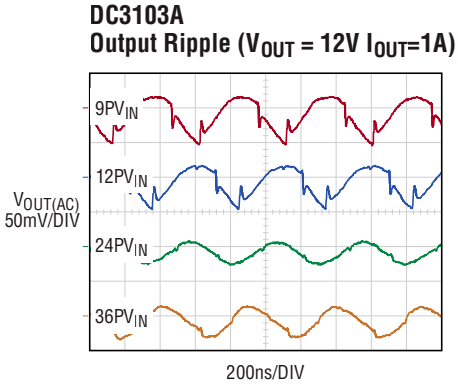


Figure 5. DC3103A Output Ripple (20MHz Bandwidth Limit)

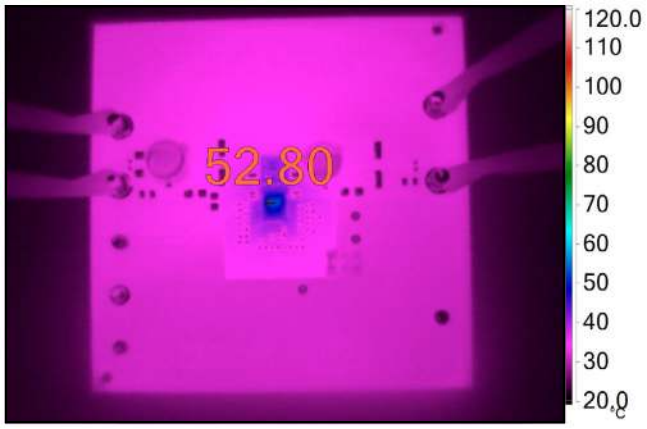
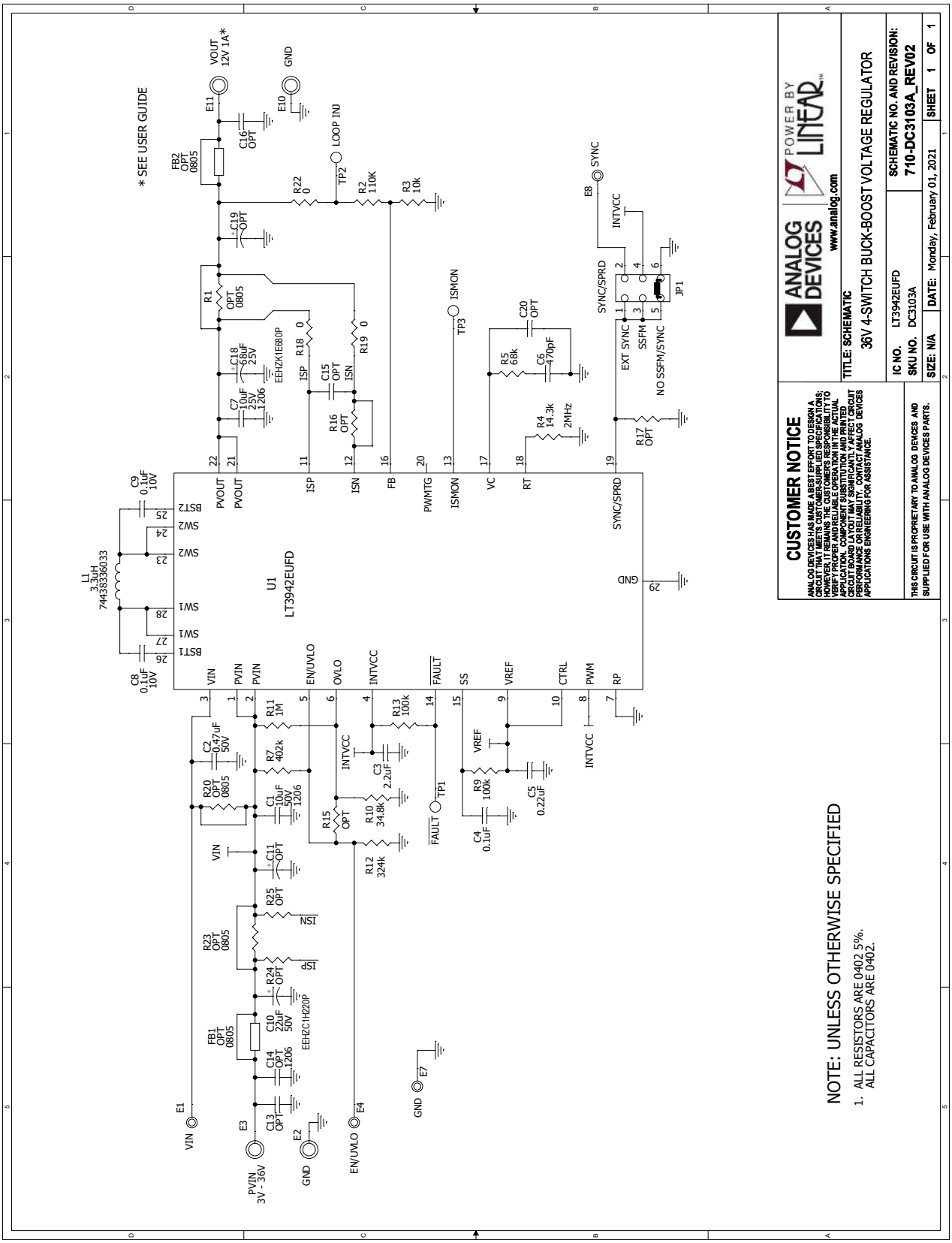


Figure 6. DC3103A Thermal Image, 10 Minute Runtime, 23°C Ambient PV_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 1A, SSFM OFF

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	C1	CAP., 10uF, X5R, 50V, 10%, 1206	TAIYO YUDEN, UMK316BBJ106KL-T
2	1	C2	CAP., 0.47uF, X5R, 50V, 10%, 0402	MURATA, GRM155R61H474KE11D
3	1	C3	CAP., 2.2uF, X5R, 6.3V, 10%, 0402	AVX, 04026D225KAT2A
4	3	C4, C8, C9	CAP., 0.1uF, X7R, 10V, 10%, 0402	AVX, 0402ZC104KAT2A
5	1	C5	CAP., 0.22uF, X7R, 6.3V, 10%, 0402	KEMET, C0402C224K9RACTU
6	1	C6	CAP., 470pF, C0G, 50V, 5%, 0402, AEC-Q200	TDK, CGA2B2C0G1H471J050BA
7	1	C7	CAP., 10uF, X7R, 25V, 10%, 1206	AVX, 12063C106KAT2A
8	1	C18	CAP., 68uF, ALUM POLY HYB, 25V, 20%, 6.3x5.8mm, SMD, RADIAL, AEC-Q200	PANASONIC, EEHZK1E680P
9	1	L1	IND., 3.3uH, WE-MAPI, 20%, 2.2A, 114mOHMS, 3020	WURTH ELEKTRONIK, 74438336033
10	1	R2	RES., 110k OHMS, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402110KFKED
11	1	R3	RES., 10k OHMS, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040210K0JNED
12	1	R4	RES., 14.3k OHMS, 1%, 1/10W, 0402, AEC-Q200	PANASONIC, ERJ2RKF1432X
13	1	R5	RES., 68k OHMS, 5%, 1/16W, 0402	VISHAY, CRCW040268K0JNED
14	1	R7	RES., 402k OHMS, 1%, 1/10W, 0402, AEC-Q200	PANASONIC, ERJ2RKF4023X
15	1	R9	RES., 100k OHMS, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402100KJNED
16	1	R10	RES., 34.8k OHMS, 1%, 1/10W, 0402, AEC-Q200	PANASONIC, ERJ2RKF3482X
17	1	R11	RES., 1M OHM, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04021M00JNED
18	1	R12	RES., 324k OHMS, 1%, 1/10W, 0402, AEC-Q200	PANASONIC, ERJ2RKF3243X
19	1	U1	IC, 36V, 2A SYNC. BUCK-BOOST CVRTR, QFN-28,	ANALOG DEVICES, LT3942EUFD#PBF
Additional Demo Board Circuit Components				
1	1	C10	CAP., 22uF, ALUM POLY HYB, 50V, 20%, 6.3x5.8mm, SMD, RADIAL, AEC-Q200	PANASONIC, EEHZC1H220P
2	0	C11, C19	CAP., OPTION, ALUM. ELECT., SMD	
3	0	C13, C15, C16, C20	CAP., OPTION, 0402	
4	0	C14	CAP., OPTION, 1206	
5	0	FB1, FB2	IND., FERRITE BEAD, OPT, 0805	
6	0	R1, R20, R23	RES., OPTION, 0805	
7	0	R15, R16, R17, R24, R25	RES., OPTION, 0402	
8	2	R18, R19	RES., 0 OHM, 1/10W, 0402, AEC-Q200	PANASONIC, ERJ2GE0R00X
9	1	R22	RES., 0 OHM, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04020000Z0ED
10	1	R13	RES., 100k OHMS, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402100KJNED
Hardware: For Demo Board Only				
1	4	E1, E4, E7, E8	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	4	E2, E3, E10, E11	TEST POINT, TURRET, 0.094" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0
3	1	JP1	CONN., HDR, MALE, 2x3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000621121
4	1	XJP1	CONN., SHUNT, FEMALE, 2 POS, 2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.