AS8506C

Battery Cell Monitor and Balancer IC

General Description

The AS8506C is a battery management IC dedicated to support cell voltage measurement, monitoring, cell balancing and temperature measurement functions in Li-Ion battery stacks for industrial/consumer/PV battery applications.

Ambient temperature range is from -40°C to +85°C.

It features cell voltage diagnosis with externally adjustable upper and lower cell voltage limits, fast cell voltage capture on request through 12-bit SAR ADC, passive cell balancing by simultaneous comparison of actual cell voltages with a reference cell voltage and temperature measurement on two external NTC sensors through 12-bit ADC.

Cells that are above reference will sequentially be discharged through integrated switches and one external resistor.

There is also an active balancing option AS8506C A through factory setting to sequentially charge cells which are below reference from an external DC-DC Flyback converter and an integrated low side driver.

The device can be used flexibly for battery stacks up to 7 cells with a minimum stack voltage of 6V and a maximum stack voltage of 32V.

It can be chained to support battery packs of virtually any number of cells in synchronized mode through chained clock and trigger signal.

The status of the battery stack is communicated to outside world through OR'd voltage_ok signal and balance ready signal.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS8506C, Battery Cell Monitor and Balancer IC are listed below:

Figure 1:
Added Value of using AS8506C

Benefits	Features
Reduce filter / synchronization effort. Acquired data have same time stamp to inherently generate accurate comparison results independent from load transients.	Simultaneous cell voltage capture for safe operating area (SOA) monitoring and balancing.
Strongly reduces data communication and data processing and thereby improves EMC robustness.	Autonomous balancing and SOA monitoring.
To compensate accumulative charge differences only. This mitigates cases of occasional wrong balance decisions due to flat OCV characteristic or mismatch in cell temperature	Autonomous passive balancing in the 100 mA range
Intrinsic inter module balancing through charge redistribution, efficiency improvement in case of leakage path due to defect induced leakage in particular cells.	Option for active charge balancing with very few external components.
For OCV capture, cell impedance calculation, diagnosis	Absolute cell voltage read out, read out of two temperature sensors.
Small form factor, low BOM	40-pin MLF (6x6) package, very low number of external components.

Applications

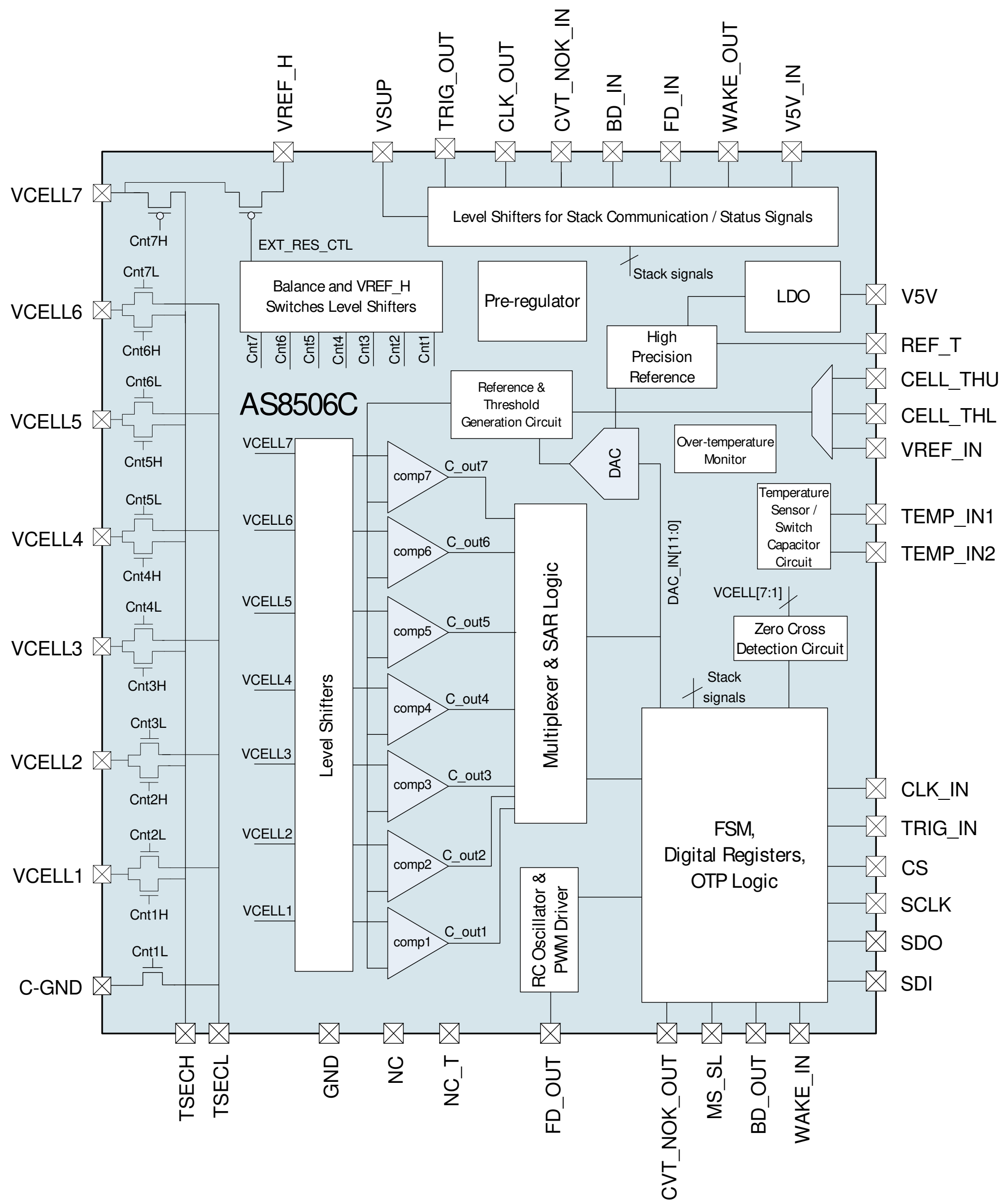
The applications of AS8506C include:

- The AS8506C is ideal for simultaneous cell monitoring and cell balancing in stacked energy storage systems. Current levels in the 100 mA range enables to compensate accumulative SOC mismatch over the entire cell pack.
- Typical applications are
  - Li-Ion batteries up to 200 cells,
  - Energy storage systems to buffer energy from PV panels or for emergency power supplies,
  - Battery management for e-scooters and e-bikes,

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS8506C Block Diagram



Pin Assignment

Figure 3:
Pin Diagram of AS8506C

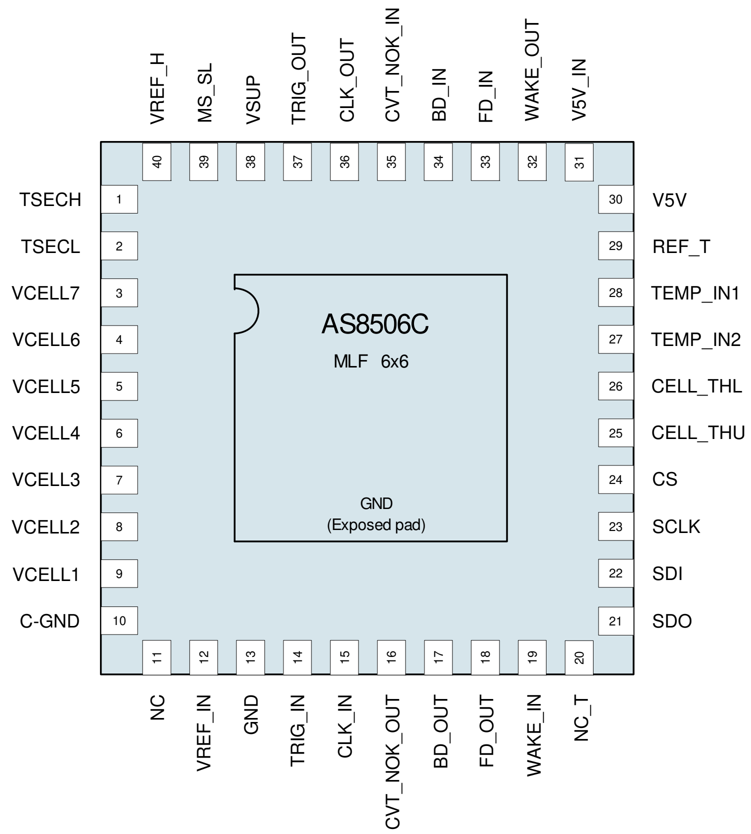


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	TSECH	Analog input / output	Flyback converter transformer secondary high side
2	TSECL		Flyback converter transformer secondary low side
3	VCELL7		Battery cell 7 high level pin
4	VCELL6		Battery cell 6 high level pin
5	VCELL5		Battery cell 5 high level pin
6	VCELL4		Battery cell 4 high level pin
7	VCELL3		Battery cell 3 high level pin
8	VCELL2		Battery cell 2 high level pin
9	VCELL1		Battery cell 1 high level pin
10	C-GND	Power supply input	Battery cell 1 low level pin
11	NC		Not connected
12	VREF_IN	Analog input / output	Cell voltage reference value (cell target voltage of battery)
13	GND	Power supply input	Ground to the IC
14	TRIG_IN	Digital input	This pin triggers the cell balancing in the device. Short pulse is for receiving status and continuous 'High' for cell balancing. It also acts as a data line during 3-wire communication.
15	CLK_IN		Clock input pin in the Slave device. This pin also acts as a clock during 3-wire communication. Scan clock in scan mode.
16	CVT_NOK_OUT	Digital output	This pin alerts when the cell voltage or the device/cell temperature is not within limits. During 3-wire communication, the CRC error is indicated on this pin. The internal device cell voltage or temperature status is ORed with CVT_NOK_IN on this pin.
17	BD_OUT		The 'device internal balance done' and 'balance done from above device' are ANDed on this pin. This pin in Master device indicates the complete system balance done. During address allocation process, this pin will be 'High' if BD_IN is 'High'.
18	FD_OUT		Flyback converter gate/opto coupler drive (pad is push-pull type) can drive up to 12mA.

Pin Number	Pin Name	Pin Type	Description
19	WAKE_IN	Digital input with pull-up	The wake pulse on this pin brings the IC into *NORMAL* mode. This pin has a pull-up resistor to the internal regulator. Should be driven with an open drain or external NMOS.
20	NC_T	Analog input / output	Not connected. Only used in Test mode.
21	SDO	Digital output	SPI data out
22	SDI	Digital input	SPI data in
23	SCLK	Digital input	SPI clock
24	CS	Digital input with pull-up	SPI chip select
25	CELL_THU	Analog input / output	Cell voltage upper threshold
26	CELL_THL	Analog input / output	Cell voltage lower threshold
27	TEMP_IN2	Analog input / output	Temperature input2 to the IC (NTC input; if NTC is not connected, then should be connected to GND with 1K resistor).
28	TEMP_IN1	Analog input / output	Temperature input1 to the IC (NTC input; if NTC is not connected, then should be connected to GND with 1K resistor).
29	REF_T	Analog input / output	Supply to temperature sensor (Reference voltage to DAC and ADC).
30	V5V	Power supply input	LDO 5V output.
31	V5V_IN	Power supply input	Supply to the bottom IC from the cascaded top IC.
32	WAKE_OUT	Digital output open drain	Open drain o/p on the VSUP+5V domain. WAKE_IN information will be transmitted to top device.
33	FD_IN	Digital input	Flyback converter gate drive input in daisy chain connection. (If FD_IN is 'high' then FD_OUT will be PWM o/p in balance mode).
34	BD_IN	Digital input with pull-down	In cell stack system, the device gets balance done status of above device. During address allocation process if this pin is 'High', then the device address is decremented by '1'.
35	CVT_NOK_IN	Digital input with pull-down	Indicates cell voltage or temperature status of above device.

Pin Number	Pin Name	Pin Type	Description
36	CLK_OUT	Digital output	This pin propagates the clock to next device in the stack system. In case of Master device internal RC clock is transmitted on this pin to Slave device.
37	TRIG_OUT		This pin transmits the data fromTRIG_IN for balance and measurement phase. This pin is also used for propagating the data information to next device in stack system in SPI3.
38	VSUP	Power supply input	Supply to the IC.
39	MS_SL	Digital input	This pin informs the device whether it should act as the Master or Slave. If this pin is connected to GND, then device will act as Master. If this pin is connected to VSUP then device will act as Slave.
40	VREF_H	Analog input / output	High sides PMOS switch for external resistive divider. Input to VREF_IN can be taken from external resistive divider in one of the options.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Comments
Electrical Parameters						
V_{VSUP}	Voltage at positive supply pin	-0.3		42	V	VSUP pin
V_{GND}	Voltage at negative supply pin	-0.3		0	V	GND, C-GND; Reference potential
V_{V5V_IN}	Voltage at high side supply	-0.3		VSUP + 0.3	V	MS_SL,VREF_H, TSECH and TSECL
VSUP + V5V_IN	High side supply from top device	VSUP - 0.3		VSUP + 5.5	V	TRIG_OUT, CLK_OUT, CVT_NOK_IN, FD_IN, BD_IN, WAKE_OUT
V_{V5V}	Voltage at on LDO o/p pins	-0.3		7	V	**V5V** pin
V_{ESD}	Voltage on 5V pins	-0.3		V5V+0.3	V	All pins expect VSUP, VCELL1, VCELL2, VCELL3, VCELL4, VCELL5, VCELL6, VCELL7, MS_SL, WAKE_IN
VCELL1 to VCELL7	Voltage on pins VCELL1, VCELL2, VCELL3, VCELL4, VCELL5, VCELL6, VCELL7	-0.3		7	V	Applied cell voltages
I_{SCR}	Latch-up Immunity	-100		+100	mA	

Symbol	Parameter	Min	Typ	Max	Units	Comments
Electrostatic Discharge						
ESD	Electrostatic discharge voltage HBM standard [(1)]	±2			kV	VSUP, VREF_IN, SDI, SDO, CS, SCLK, CELL_THU, CELL_THL, TEMP_IN1, TEMP_IN2, REF_T, V5V, V5V_IN, MS_SL, VREF_H, NC_T
		±4				GND, C-GND, CELL1 – CELL7 (Cell-voltage pins,), TSECH, TSECL, TRIG_IN, TRIG_OUT, CLK_IN, CLK_OUT, CVT_NOK_IN, CVT_NOK_OUT, WAKE_IN, WAKE_OUT, FD_IN, FD_OUT, BD_IN and BD_OUT
Continuous Power Dissipation						
P_{tot}	Maximum power dissipation			1	W	
Temperature Ranges and Storage Conditions						
T_{stg}	Storage temperature	-55		150	ºC	
R_{thj_36}	Thermal resistance package		30		ºC/W	
T_{BODY}	Package body temperature			260	ºC	Norm: IPC/JEDEC J-STD-020 [(2)]
MSL	Moisture Sensitive Level		3			

Note(s) and/or Footnote(s):

1. Human body model: R = 1.5kΩ; C = 100pF.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".

Typical Operating Characteristics

All defined tolerances for external components in this specification need to be assured over the whole operation conditions range and also over lifetime.

Figure 6:
Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
VSUP	Positive supply voltage	6		32	V	Normal operating condition
VSS	Negative supply voltage	-0.3		0	V	With reference to all the voltages
T_{AMB}	Ambient temperature	-40		85	ºC	Maximum junction temperature (T_J) 115ºC
$I_{SUPP, nom}$	Supply current, *NORMAL* mode	2	3	6	mA	VSUP=32V, in *NORMAL* mode
	Supply current, *NORMAL* mode, With External Components	15	20	40	mA	VSUP=32V, in the balancing phase with stack connection (50% PWM duty cycle)
$I_{SUPP, sleep}$	Supply current, *SLEEP* mode	10	17	35	µA	

Electrical Characteristics

Device Level Specifications

-40°C < Tj < 115°C.

Figure 7:
Device Level Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
Vcell_in	Cell Input voltage measurement	1.8		4.5	V	
ADC/DAC	ADC/DAC Reference		±7	±15	mV	0 hour, specification does not include solder stress / board stress effects
DAC_error	Error of the DAC		2		mV	0.1% error because of the DAC/Guaranteed by design
Com_off	Error because of the comparator resolution		1		mV	Guaranteed by design
Sign_path_accuracy	Signal path accuracy		±5	±15	mV	Typical value is from the lab evaluation data. Maximum value is from the test data. 0 hour accuracy, specification does not include solder stress / board stress effects.
$T_{INITIALIZATION}$	Initialization time			50	ms	After Initialization, the system will go to sleep mode and waits for wake signal.
$T_{WAKE-UP}$	Wake up time from the Wake signal to system wait mode			75	ms	After wake signal, device enters into wait mode and stays for two seconds for TRIG_IN signal, if no TRIG_IN event occurs, device goes to sleep mode.
Tmeas	Cell voltage and Temperature measurement time		16		ms	At10KHz clock time
Tspi3_read5k	SPI3 read time for single channel measurement		13.6		ms	At 5KHz clock time
Tspi3_read20k			3.4			At 20KHz clock time
Tspi3_read40k			1.7			At 40KHz clock time

Low Dropout Regulator (5V Output LDO)

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND); positive current flows into the pin, *NORMAL* operating mode, if not otherwise mentioned. The LDO block is a linear voltage regulator, which provides a regulated 5V.

Figure 8:
LDO Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP}	Input supply voltage	6	12	32	V	
V5V	Output voltage range	4.75	5.0	5.25	V	
I_{LOAD}	Load Current			50	mA	
ICC_SH	Output short circuit current		85	250	mA	*NORMAL* mode
PSRR	PSRR		60		dB	f=1kHz / No production test
			35			f=1MHz / No production test
CL1	LDO output Capacitor 1	2.2		10	µF	Electrolytic
ESR1		1		10	Ω	
CL2	LDO output Capacitor 2	100		220	nF	Ceramic
ESR2		0.02		1	Ω	

Note(s) and/or Footnote(s):

1. In *NORMAL* mode, maximum load current will be 50mA. After internal thermal shutdown, current limit is 20mA.
2. The LDO is disabled in *SLEEP* mode.

High-precision Bandgap Reference

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 9:
Bandgap Reference Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
BG_Out	Reference output after trim	1.2	1.235	1.27	V	After temperature trim
$BG\_out\_T_{var}$	Reference variation with respect to Temperature		±2.5	±4	mV	After trim on the absolute
PSRR1K	PSRR at 1KHz	20			dB	No production test
PSRRDC	PSRR at DC	80			dB	

Note(s) and/or Footnote(s):

1. This bandgap output is the reference for the V5V (LDO) regulator.

Digital to Analog Converter

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 10:
Digital to Analog Converter

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP_DAC}	Input supply voltage	4.75	5	5.25	V	LDO output as supply
V_{INREF}	Input reference voltage	4.485	4.5	4.515	V	After absolute trim at 0 hours, specification does not include solder stress/board stress effects
D_{IN}	Resolution		12		bits	Guaranteed by design
F_{DAC}	Update rate		10		KHz	No production test
T_{SETT_DAC}	Settling time		50		µs	
DAC_{INL}	INL		±4		LSB	
DAC_{DNL}	DNL		±0.5		LSB	

Analog to Digital Converter

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 11:
Analog to Digital Converter

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP}	Input supply voltage	4.75	5	5.25	V	LDO output as supply
V_{INREF}	Input reference voltage	4.485	4.5	4.515	V	After absolute trim at 0 hours, specification does not include solder stress/board stress effects
D_{OUT}	Resolution		12		bits	
T_{MEAS_ADC}	Measurement time per channel		1.4		ms	
ADC_{INL}	INL		±4		LSB	No production test.
ADC_{DNL}	DNL		±2		LSB	No production test.

Pre-Regulator

This Pre_reg is an internal regulator which provides supply to digital and a few analog blocks..

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 12:
Pre-reg Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP}	Input supply voltage	6	12	32	V	
P5V	Prereg_output voltage range	4.3	5.0	5.5	V	
3V3	3.3V_output voltage range	2.8	3.3	3.6	V	

PWM Driver

40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 13:
PWM Driver

Symbol	Parameter	Min	Typ	Max	Unit	Note
V5V	Output voltage	4.5	5	5.5	V	
F_{PWM}	Frequency of PWM	25	100	200	KHz	CMOS load mode, Optocoupler load mode
F_{Duty}	Duty cycle	22	25	28	%	
		12	15	18	%	
		17	20	23	%	
		27	30	33	%	
		30	35	38	%	
		37	40	43	%	
		42	45	48	%	
		47	50	53	%	
F_{duty_error}	Duty cycle error	7	12	20	%	
tr_{pwm}	Rise time	30	50	80	ns	CMOS load mode, Optocoupler load mode Guaranteed by design
tf_{pwm}	Fall time	30	50	80	ns	
$Idrive_{opto}$	Driver strength		10	12	mA	Optocoupler load mode
$Cload_{fd\_out}$	Driver switch load capacitance		60	100	pF	

PWM Oscillator

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 14:
PWM Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{OSC}	Frequency	90	100	110	kHz	• After the frequency trim. • Programmable frequency options for 25KHz, 50KHz and 200KHz are available.
f_{OSC_ACC}	Accuracy		±15		%	

Oscillator for Digital Circuit

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 15:
Oscillator for Digital Circuit

Symbol	Parameter	Min	Typ	Max	Unit	Note
$f_{OSC-DIG}$	Frequency	9	10	11	kHz	Oscillator for Digital circuit
f_{OSC_ACC}	Accuracy		±15		%	

External Temperature Thresholds

-40°C < T_J < 115°C; all voltages are with respect to ground (GND).

Figure 16:
External Temperature Thresholds

Symbol	Parameter	Min	Typ	Max	Unit	Note
Ref_ext_warn/sutdown	Code 0000	3.084	3.165	3.238	V	16 reference thresholds are with a step of 66mV.
	Code 0001	3.148	3.231	3.306		
	Code 0010	3.213	3.297	3.373		
	Code 0011	3.277	3.363	3.441		
	Code 0100	3.341	3.429	3.508		
	Code 0101	3.406	3.495	3.576		
	Code 0110	3.470	3.561	3.643		
	Code 0111	3.534	3.627	3.711		
	Code 1000	3.599	3.693	3.779		
	Code 1001	3.663	3.759	3.846		
	Code 1010	3.727	3.825	3.914		
	Code 0011	3.792	3.891	3.981		
	Code 0100	3.856	3.957	4.049		
	Code 0101	3.920	4.023	4.116		
	Code 0110	3.984	4.089	4.184		
	Code 0111	4.049	4.155	4.25		

Ron of the Shuttle Switches (Internal Switch for Charging/Discharging)

-40°C < T_J < 115°C.

Figure 17:
Ron of the Shuttle Switches

Symbol	Parameter	Min	Typ	Max	Unit	Note
Ron_shut	Shuttle switch ON resistance		5	20	Ω	The maximum charging/discharging current limit through shuttle switch is 100mA. Only for Cell1 maximum charging/discharging current is limited to 30mA less than 2V of cell voltage at 115 junction of cell voltage.

Over-Temperature Measurement

Figure 18:
OTM Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{jshut}	Shut down temperature	115	135	145	ºC	Junction temperature for Shutdown
T_{jwarn}	Warning temperature	100	125	140	ºC	Junction temperature for Warning
T_{jrecv}	Recovery temperature	100	115	130	ºC	Junction temperature for Recovery

Weak Cell Detection (Voltage Comparator)

Figure 19:
Weak Cell Detection

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CELL}	Supply voltage	-0.3	3.6	4.5	V	
V_{LOW}	Low voltage detection	-100		100	mV	
TI_spike	Minimum input spike filter		2		µs	No production test. Programmable option.
			4			
			6			
			8			

Power on Voltage Detection

Figure 20:
Power on Voltage Detection

Symbol	Parameter	Min	Typ	Max	Unit	Note
VSUP_POR	VSUP Power-on-Reset threshold ON	5.2	5.5	5.8	V	Rising edge of VSUP
VSUP_RESET	VSUP Power-on-Reset threshold OFF	4.6	4.85	5.1	V	Master reset for device
V5V_IN_POR	V5V_IN Power-on-Reset threshold ON	3.8	4.45	4.8	V	Voltages are with respect to VSUP measure as pass fail test
V5V_IN_RESET	V5V_IN Power-on-Reset threshold OFF	3.6	4.1	4.5	V	
V5V_POR	V5V Power-on-Reset threshold ON	4.1	4.5	4.7	V	Rising edge of V5V
V5V_RESET	V5V Power-on-Reset threshold OFF	3.8	4.1	4.3	V	Falling edge of V5V

Electrical Characteristics for Digital Inputs and Outputs

All pull-up, pull-downs have been implemented with active devices.

Figure 21:
Digital Inputs and Outputs

Port Type	Symbol	Parameter	Min	Typ	Max	Unit	Note
CS							
INPUT Schmitt Trigger	Vt-	Negative-going threshold	1.62		2.22	V	V5V=5V
	Vt+	Positive-going threshold	2.27		3.42	V	
	I_{lil_cs}	Pull-up current	-100		-30	µA	In CS pad, Pulled up to V5V. (ISUP_HV)
SDO							
OUTPUT Tristate	V_{OH}	High level output voltage	2.5			V	
	V_{OL}	Low level output voltage			0.4	V	VSUP ≥ 6V
	V_{IH}	High level input voltage	0.7*V5V			V	
	V_{IL}	Low level input voltage			0.3*V5V	V	
	I_O	Output drive current			4	mA	
SCLK, SDI							
IO Buffer	V_{IH}	High level input voltage	0.7*V5V			V	
	V_{IL}	Low level input voltage			0.3*V5V	V	

Port Type	Symbol	Parameter	Min	Typ	Max	Unit	Note
CVT_NOK_OUT							
OUTPUT Buffer	V_{OH}	High level output voltage	2.4			V	
	V_{OL}	Low level output voltage			0.4	V	VSUP ≥ 6V
	I_O	Output drive current			2	mA	
BD_OUT							
OUTPUT Buffer	V_{OH}	High level output voltage	2.4			V	
	V_{OL}	Low level output voltage			0.4	V	VSUP ≥ 6V
	I_O	Output drive current			1	mA	
TRIG_OUT, CLK_OUT							
OUTPUT Buffer	V_{OH}	High level output voltage	2.4			V	
	V_{OL}	Low level output voltage			0.4	V	VSUP ≥ 6V
	I_O	Output drive current			4	mA	
FD_OUT							
OUTPUT Buffer	V_{OH}	High level input voltage	2.4			V	
	V_{OL}	Low level input voltage			0.4	V	VSUP ≥ 6V
	I_O	Output drive current			24	mA	
MS_SL							
INPUT Buffer	V_{IH}	High level input voltage			VSUP	V	High voltage input pad
	V_{IL}	Low level input voltage			0.3*V5V	V	
CLK_IN, TRIG_IN							
INPUT Schmitt Trigger	Vt-	High level input voltage	1.62		2.22	V	
	Vt+	Low level input voltage	2.27		0.3*V5V	V	

Port Type	Symbol	Parameter	Min	Typ	Max	Unit	Note
FD_IN,BD_IN, CVT_NOK_IN							
INPUT Buffer	V_{IH}	High level input voltage	0.7*V5V			V	
	V_{IL}	Low level input voltage			3.42	V	
WAKE_IN Pull up current	Ipull_up	Pull-up current	-100		-30	µA	Internal pull

Note(s) and/or Footnote(s):

1. Test limits for Iih and Iil are 1.0uA and -1.0uA for input pads.

Detailed Description

The device consists of the following blocks:

- PWM driver
- LDO_5V with 5V / 50mA output
- Temperature monitor block
- High precision bandgap reference
- DAC for the reference voltage generation
- SAR ADC for cell voltage and external temperature measurement
- Oscillators for PWM drive and for the digital logic
- Pre-Regulator
- SC Comparator
- Weak cell detection logic
- PORs on different supplies

Voltage Regulator (LDO_5V)

Power input to the LDO is VSUP pin. It is switched ON when the device is in *NORMAL* mode and switched OFF in *SLEEP* mode. The LDO takes the input from Bandgap and scales it up to the required voltage. It starts charging only after entering *NORMAL* mode. This LDO is the supply for DAC, the PWM driver and Cell voltage comparators.It's additional features are as follows:

- Stability is better than ±2.5% over input range.
- Load current up to 50mA.

High Precision Bandgap (HPBG)

AS8506C has a high precision bandgap to generate accurate reference. This reference voltage is used to generate reference for DAC and ADC.

HPBG is trimmed with respect to temperature. Variation of the bandgap with temperature is ±4mV in the temperature range from -40ºC to 115ºC.

External Temperature Monitor and Measurement

Two sensor inputs TEMP_IN1 and TEMP_IN2 with a comparator on each pin, are available. If the temperature sensor connected to TEMP_IN1 crosses its threshold, then a warning flag is set in the device (status can be read through SPI) and the device will continue balancing.

If the temperature sensor connected to TEMP_IN2 crosses its threshold, then a flag is set in the device and balancing is stopped; but the device continues to stay in *NORMAL* mode for maintaining synchronism. In both the cases, the microcontroller will be interrupted by a pulse on CVT_NOK_OUT pin.

In case the external temperature sensors are not being used, then both the inputs must be connected to GND pin through 1k resistor. In the measurement phase, external temperature is measured through the SAR ADC. Both channels of temperature will be measured and stored in temp_in1_lsb_reg to temp_in2_msb_reg.

Internal Temperature Monitor

The internal temperature monitor has two thresholds at T_{jwarn} 125ºC and T_{jshut} 135ºC. If the internal temperature exceeds 125ºC, then a warning flag is set in the device (status can be read through SPI) and the device will continue balancing.

If the internal temperature exceeds 135ºC, then a flag is set in the device and balancing is stopped; but the device continues to stay in *NORMAL* mode for maintaining synchronism. In both the cases, the microcontroller will be interrupted by a pulse on CVT_NOK_OUT pin. The balance recovery temperature is 115ºC.

PWM Generator

In the Balance phase of the AS8506C, based on the decision made during the Compare phase, some part of the cell is charged with the Flyback converter. To drive the external Flyback converter, AS8506C generates a PWM signal to drive external FET or Optocoupler or Isolation device.

The frequency and of the PWM generator can be controlled by timer_cntl_reg register.

PWM frequency is not used for the passive balancing.

RC Oscillator

The AS8506C has a trimable RC oscillator. It is designed to generate $f_{osc\text{-}dig}$ clock for the digital circuit and for the clocking of the IC. Each oscillator will be trimmed with the process to get the accuracy to $f_{osc\text{-}accy}$ with 5-bit OTP Factory trim code.

DAC for the Reference Generation

AS8506C has a 12-bit DAC to generate the cell reference voltage, cell threshold low and high voltage. The DAC code is written into AS8506C with SPI interface from microcontroller. The output of the DAC is given to one of the inputs of the comparators, to compare the cell voltages synchronously. Reference for the DAC is 4.5V, which is internally generated and is available as reference for temperature inputs on REF_T.

SAR ADC

AS8506C has a 12-bit SAR ADC to measure the cell voltage and external temperature. The SAR ADC uses the 12-bit DAC to generate the digital code. The SAR ADC range is 1.8V to 4.5V for cell voltage measurement and 0.2V to 4.5V for the temperature measurement.

Cell voltage and temperature is measured in the short trigger phase. After the trigger goes 'high', compare phase starts and then all the cell voltages and external temperature are measured and stored in the digital registers.

Pre-Regulator

AS8506C has an internal pre-regulator, which generates supply voltages for the internal blocks. Pre-Regulator output is used as a supply for the oscillators. All the digital logic and the FSM will work on the pre-regulator supply.

In *SLEEP* mode only the pre-regulator will be working along with the WAKE_IN detect circuit.

Cell Threshold

AS8506C has the potential to set the two threshold levels to the cell voltage through pins CELL_THU and CELL_THL. These values can be set externally, (or) through OTP trim bits, (or) from the external microcontroller by writing DAC code into the cell threshold registers in the register space.

Weak Cell Detection

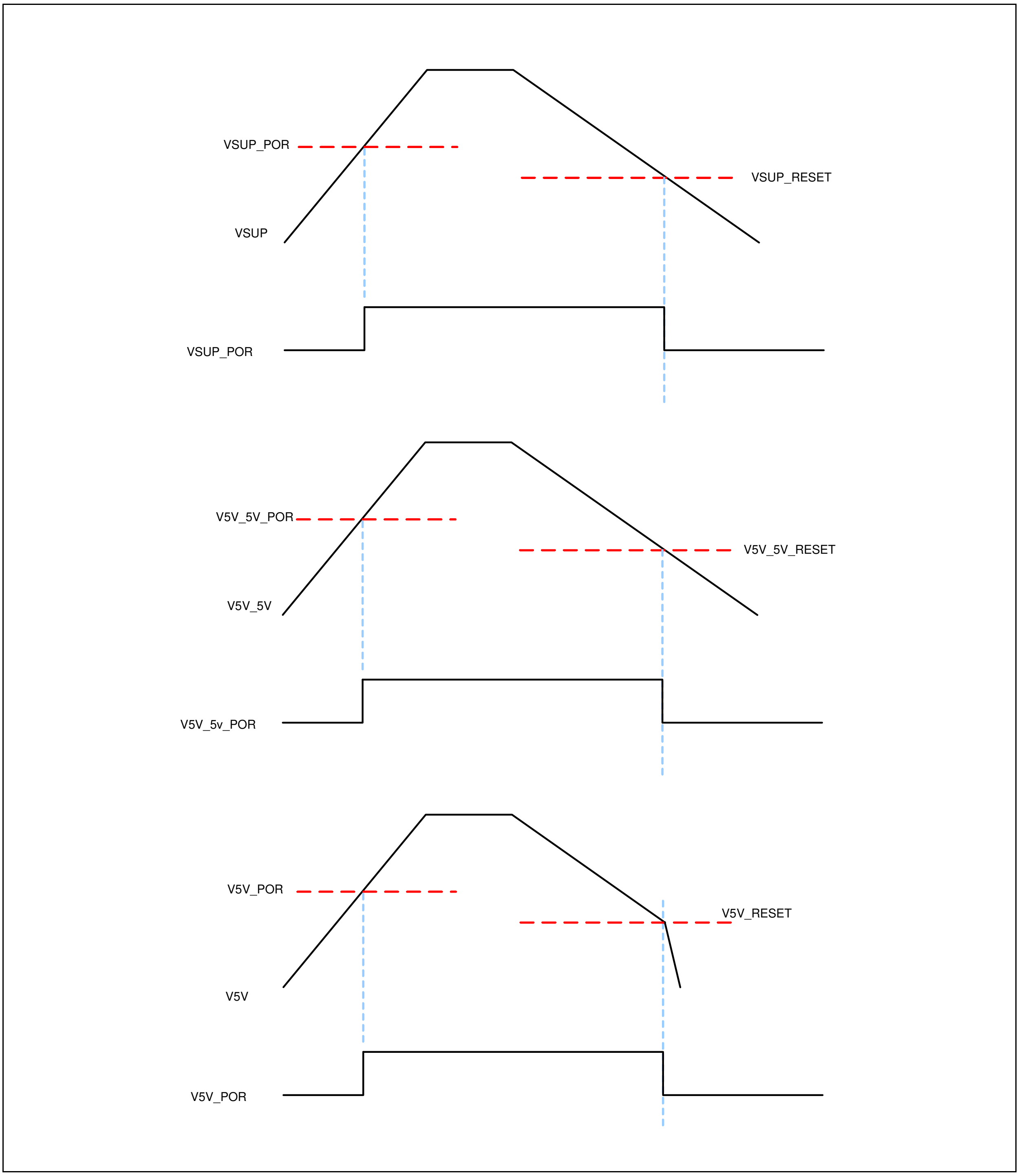
AS8506C has the ability to detect the weak cell. During load conditions, if the cell reaches voltage of about 0.1V to -0.2V, then this variation is detected and stored in the zero cross detection register. This event is indicated to the master device by a pulse on CVT_NOK_OUT pin in Compare and Balance phase. The master device indicates the microcontroller by setting CVT_NOK_OUT 'high'. In *WAIT* mode only this will be stored in the register; there won't be any CVT_NOK_OUT to µC. The register is cleared on µC reading.

External Resister Divider Control

AS8506C has the provision to enable the external divider to give the desired cell voltage to the at VREF_IN pin. External resister divider can be connected between VREF_H pin to ground. Typical internal ON resistance of the VREF_H switch is 30Ω.Calculate the external resister divider values such that the output of the divider will provide the desired reference value. When comparison is not happening, this divider can be disabled using SPI. PORs on Different Supplies

AS8506C has power-on-reset blocks on VSUP, V5Vand V5V_IN supply pins. The values for POR and Reset thresholds are given in Figure 20.

Figure 22:
Power-up Sequence of VSUP, V5V and VSUP+5V



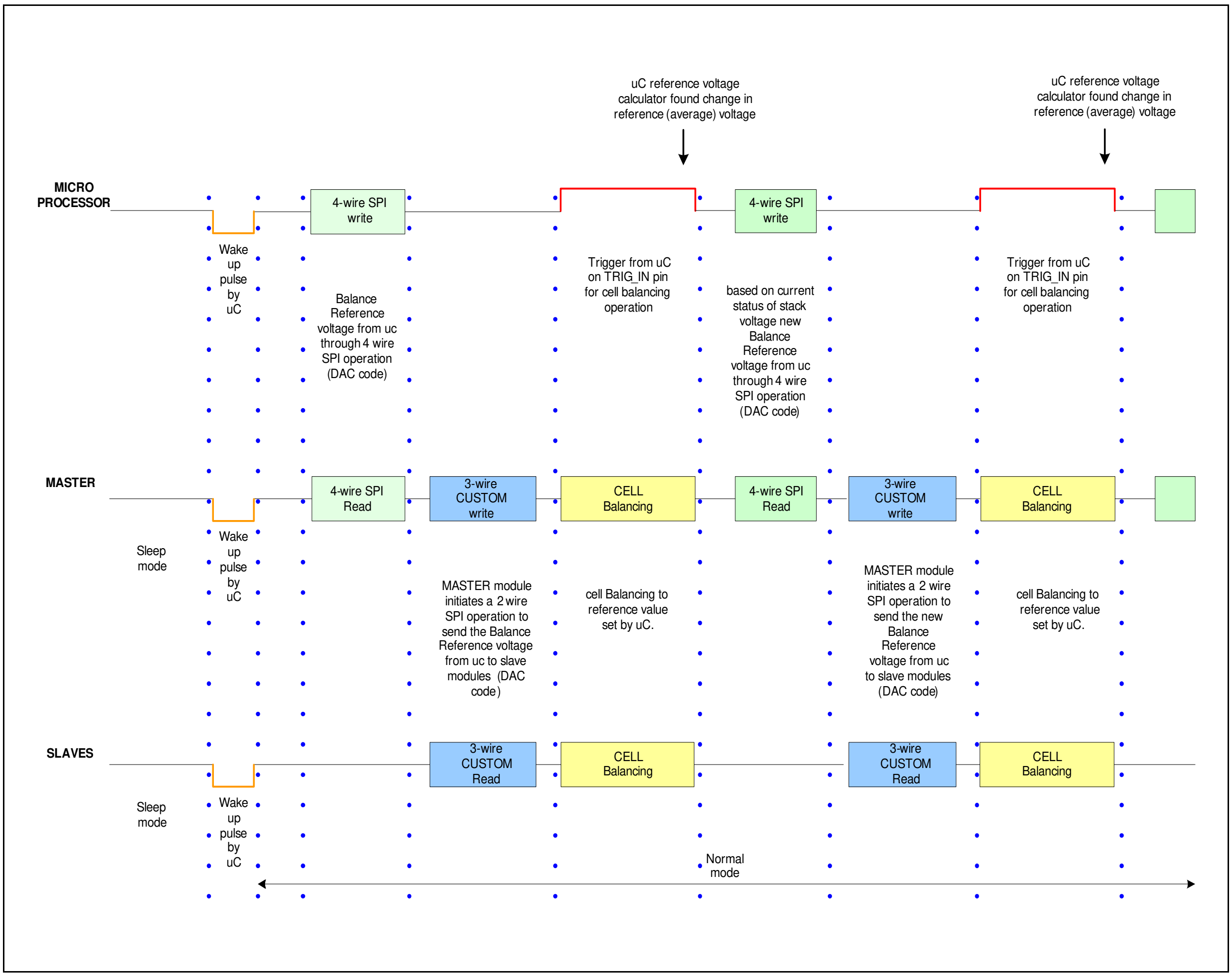
AS8506C System Operation

The AS8506C battery stack system can be set up by configuring one AS8506C device as 'Master' and the rest as 'Slave' devices. The AS8506C Master device is connected to the microcontroller, and the Slave devices are connected to Master through a daisy-chain of 3-wire customized SPI protocol. The microcontroller can communicate to the Slave devices through the Master. On power-up of the system, the microcontroller must assign an address to all AS8506C devices including the Master. The microcontroller can assign the address to AS8506C devices by initiating the address allocation process, by writing a top most Slave device address into dadd_for_allc_reg register of Master and then writing '07' data into spi3_cmd_reg. Once the address allocation process is successful, the microcontroller can start the cell balancing. If cell balancing or check status command is not triggered by the microcontroller, after *WAIT* mode timeout period all devices enter into *SLEEP* mode.

The complete system communication procedure is explained below.

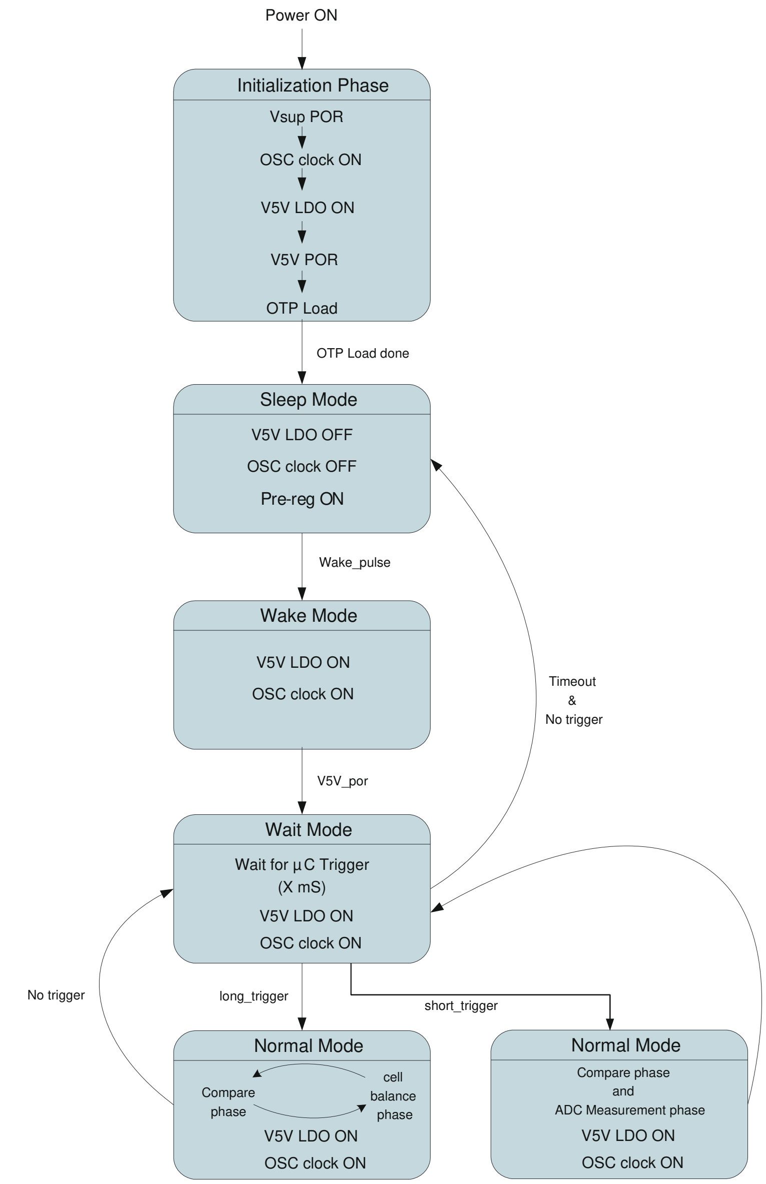
- The microcontroller gives wake pulse on WAKE_IN to bring the Master and Slaves in *NORMAL* mode.
- After the wake-up time period, the microcontroller (µC) sends the reference voltage digital code to the Master device through a 4-wire SPI.
- After receiving the digital reference code from µC, the Master device initiates a 3-wire custom SPI operation to send the digital reference code to the Slave devices.
- The microcontroller waits for the 3-wire SPI operation time period. After the 3-wire SPI time period, it initiates the cell balancing through TRIG_IN. The balancing will continue as long as TRIG_IN is 'High'.
- The microcontroller can change the reference value at any time by making TRIG_IN 'Low' and initiating a 4-wire SPI with new value of reference code. From here on, the procedure is same as from point 3.
- The balance done is indicated on BD_OUT pin.
- The failure in the 3-wire SPI operation is indicated on CVT_NOK_OUT pin.

Figure 23:
Functional Diagram of AS8506C



Functional State Diagram

Figure 24:
Finite State Machine Mode



Operating Modes

The AS8506C has two main operating modes *NORMAL* and *SLEEP*, and has two transition modes *WAIT* and *WAKE*. The transition modes are intermediate modes for switching from *SLEEP* to *NORMAL* and vice versa. The detailed operation of each mode is explained in subsequent sections. The initialization phase is explained in Initialization Sequence.

NORMAL Mode

The device enters into *NORMAL* from *WAKE* when it receives a short or long trigger. The *NORMAL* mode is a full functional mode, where all the power supply and analog blocks are in ON-state and the digital is fully functional.

The *NORMAL* mode has two phases of operation:

- Diagnosis phase
- Compare and Balance phase

Diagnosis Phase

In Diagnosis phase AS8506C detects the number of cells connected to the device. The connected cell voltages are then compared with upper & lower thresholds and target cell voltage of all cells connected. Upper and lower cell voltage thresholds as well as target cell voltages are provided from external in analog or digital format. The Diagnosis phase sequence of operation is explained below.

- Detects number of cells connected to the device by comparing each cell terminals to cell detect threshold voltage.
- Simultaneously compares each connected cell voltage with set lower operating voltage threshold Vlimit_L. If any of the cell voltages is less than the set lower operating threshold, then an indication is given on CVT_NOK_OUT pin stating that one/more cell voltages are not within the operating voltage threshold range. Each cell status is stored in cel_low_thsld_stat_reg register.
- Simultaneously compares each connected cell voltage with set higher operating voltage threshold Vlimit_H. If any of the cell voltages is greater than the set higher operating threshold, then an indication is given on CVT_NOK_OUT pin stating that one/more cell voltages are not within the operating voltage threshold range. Each cell status is stored in cel_high_thsld_stat_reg register.
- Simultaneously compares each connected cell voltage with reference value. This result is stored in cel_ref_stat_reg register and used in balance phase. Cell reference can be provided by microcontroller by writing into register or by providing input at external pin VREF_IN.
- Enables the SAR ADC and measures each cell voltage and two temperature inputs sequentially. The 12 bits cell voltage and temperature inputs information is stored in respective registers.

At the end of the Diagnosis phase, if trigger signal is 'High' then it enters into Balance phase. If trigger signal is 'Low' it enters into *WAIT* mode.

The Diagnosis phase without the cell voltage and temperature measurement with SAR ADC is called **Compare phase**.

Compare and Balance Phase

The Balance phase is basically a charging cycle in case of active balancing and a discharging cycle in case of passive balancing. The Balance phase is divided into 7 time slots. The device will move through all 7 time slots irrespective of number of cells connected to the device. This is done to keep synchronization between each module in case of battery stack system. One time slot is assigned to each cell (sequential order) for charging or discharging. The period of time slots is programmable (see Status Registers).

In each time slot, following operations are done.

- Check CVT_NOK flag status. If CVT_NOK flag is set, then no operation is done till time slot is over. If CVT_NOK flag is not set, then move to the next step.
- Based on Diagnosis phase results, shuttle switch corresponding to current time slot cell is switched ON for charging that cell in case of active balancing, and discharging in case of passive balancing.
- The PWM generator is enabled and PWM driver start driving the Flyback converter FET (external component) in case of active balancing. The PWM frequency and duty cycles are factory programmable and also register controllable. In case of stack system, the bottom module PWM driver is enabled when there is a request of charging or discharging from top module on FD_OUT pin.
- At the end of the current time slot, stop the PWM generator and then open the corresponding shuttle switches. The device moves to the next time slot.

In the Balance phase, at any point, if the trigger input goes 'Low', then the device suspends balancing operation and enters into *WAIT* mode.

An example of Compare and Balance (active balance) phase sequence with respect to time is given in Figure 25. In this example it is assumed that only 6 cells are connected to AS8506C and comparators' outputs at Diagnosis phase is "**010010X**";

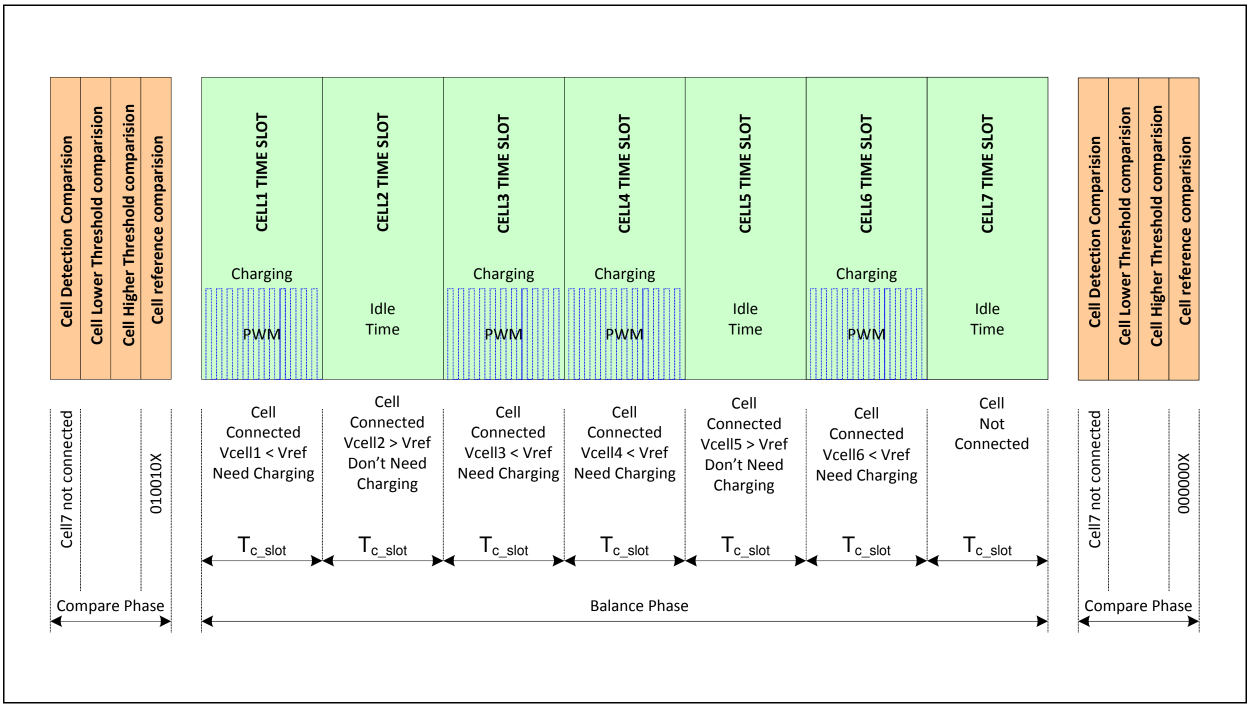
Where:

'0' indicates respective cell voltage is less than target voltage and needs charging.

'1' indicates respective cell voltage is more than target voltage and charging is not needed.

'X' indicates no cell is connected to respective comparator and output is neglected.

Figure 25:
Diagnosis and Compare and Balance Phase with Time Sequence for AS8506C



Sleep Mode

This is the least power consumption mode of AS8506C. In this mode only pre-reg is ON, rest all analog blocks are OFF and digital clock is disabled. Only a digital wake detection circuit is active. The device enters into this mode when there is no trigger from microcontroller for time greater than *WAIT* mode timeout period.

Wait Mode

This mode is a transition mode, where the device waits for command on TRIG_IN pin either from microcontroller, (or) from below module in case of stack system. The device will be in this state for T_{WMODE_TOUT} period. After the timeout, the device enters into *SLEEP* mode. In the *WAIT* period all power blocks are ON, all analog blocks are ON and digital is also functional. In this mode, power consumption is lesser than *NORMAL* mode because there are no charge balancing activities being carried out.

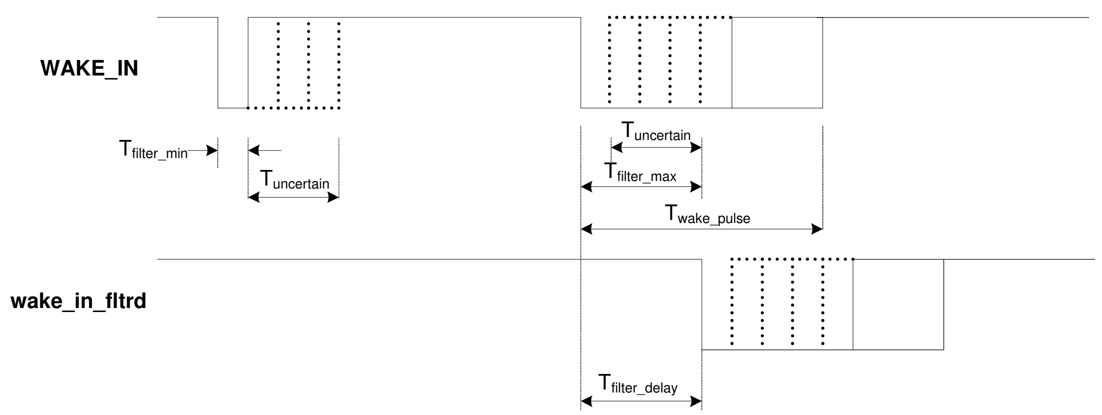
Wake Mode

This is also a transition mode, where the device does initialization after exiting *SLEEP* mode. In the *SLEEP* mode if AS8506C receives a wake pulse of width T_{WAKE}, the device enters into *WAKE* mode. In the *WAKE* mode device enables the V5V LDO and waits for V5V_por_n signal. Once V5V_por_n signal becomes 'High', the device enters into *WAIT* mode.

Wake-up Event

The AS8506C device comes out of *SLEEP* mode by a wake pulse on the WAKE_IN pin. To avoid false wake by noises on the WAKE_IN, the wake signal (Low pulse) is taken through a low-pass filter from WAKE_IN pin. When a pulse of width T_{wake_pulse} is given on the WAKE_IN by the microcontroller, the device wakes up and enters into *WAKE* mode. The low-pass filter discards all signals having width less than T_{filter_min} and allows all signals with width greater than T_{filter_max}. The filter is uncertain in $T_{uncertain}$ region. The negative edge which is passing through the filter will wake the device from *SLEEP* mode. In chain of AS8506C devices, to propagate the negative edge the microcontroller has to give minimum low pulse of width T_{wake_pulse}. Before entering into *SLEEP* mode the wake pin must be 'High'.

Figure 26:
WAKE-UP Signaling



Trigger Event

The AS8506C device enters into *NORMAL* mode only when a valid command is present on the TRIG_IN pin. There are two commands in the device.

- Diagnosis command
- Cell balance command

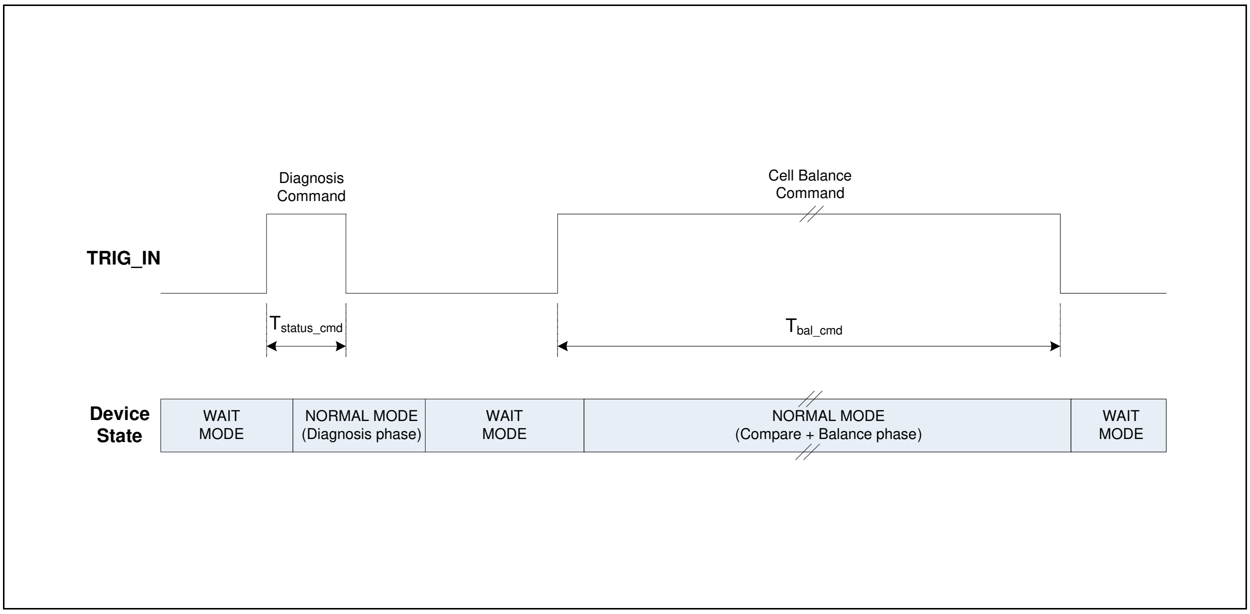
When a high pulse of width T_{diag_cmd} as shown in Figure 27, is given on TRIG_IN pin, the device performs the following operations.

- Compares all connected cell voltages with the set lower operating voltage threshold, and if any of the cell voltage is less than lower threshold, then sets a corresponding flag in the cel_low_thsld_stat_reg register. This is indicated by high pulse on CVT_NOK_OUT pin.
- Compares all connected cell voltages with the set higher operating voltage threshold, and if any of the cell voltage is more than higher threshold, then sets a corresponding flag in the cel_high_thsld_stat_reg register. This is indicated by high pulse on CVT_NOK_OUT pin.
- Sets a corresponding flag in the temp_stat_reg register if ambient temperature or internal chip temperature is higher than respective thresholds. This is indicated by high pulse on CVT_NOK_OUT pin.
- It will enable SAR ADC and starts measuring each cell voltage, and then measures temperature channel measurement. The 12 bits digital value will be stored in corresponding registers.

Thus, on diagnosis command the device gives the cell operating voltage, ambient temperature and internal temperature status with respect to its safe operating range.

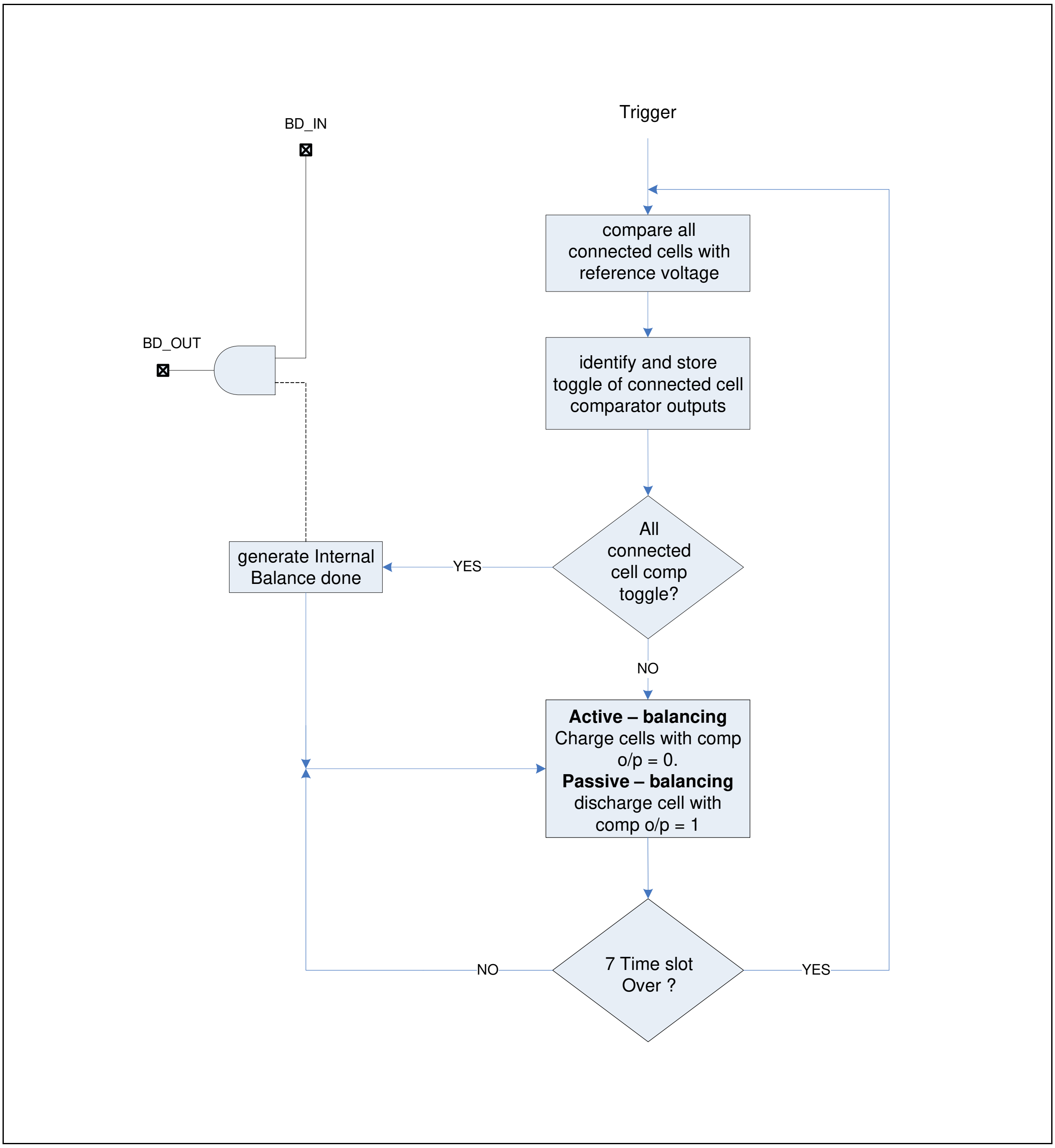
When the TRIG_IN pin is 'High' for longer than the status command, the device enters into Balance phase. Depending upon cell voltage status, the device starts balancing the cell voltages. The cell voltage balancing is continued till the high voltage on the TRIG_IN pin. As soon as TRIG_IN goes 'Low', the device stops balancing and enters into *WAIT* mode. Thus, the microcontroller has full control over the balancing time and stop balancing whenever required.

Figure 27:
TRIG_IN Command Signaling



Balancing Algorithm

Figure 28:
Cell Balancing Algorithm

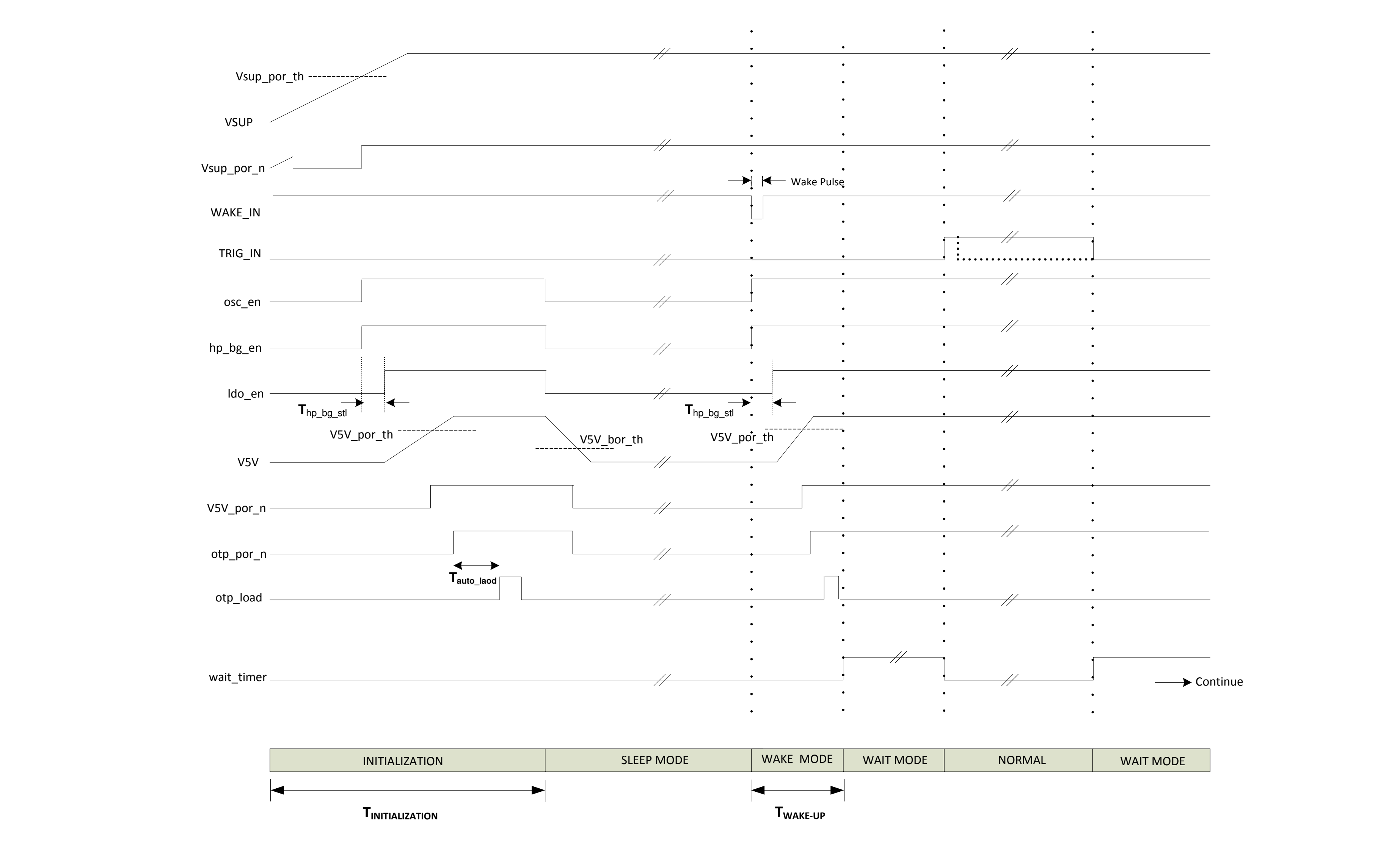


Initialization Sequence

The power-up initialization sequence diagram for AS8506C is shown in Figure 29.

- When the power supply is switched ON, initially VSUP POR output Vsup_por_n is 'Low'; hence all the digital logic will be in reset state.
- Once the VSUP crosses the Vsup_por_th, the VSUP POR output becomes 'High' enabling the oscillator and high-precision bandgap (HPBG) block.
- The digital block is now operational. It will now enable the V5V LDO and waits for V5V_por_n high signal from the V5V POR block.
- Once the V5V crosses V5V_por_th, the V5V_por_n will be 'High'. The OTP auto load command is generated by 'High' on otp_por_n signal. Now the device waits for T_{auto_load} period for OTP contents to load into digital local registers.
- After the OTP contents are loaded into digital local registers, the device power-up sequence is completed. The device enters into *SLEEP* mode. In *SLEEP* mode, the LDO, oscillator and HPBG are disabled.
- The wake-up circuit monitors the WAKE_IN pin for wake-up pulse. When a wake-up pulse is received, the oscillator and HPBG block are enabled and device enters into *WAKE* mode. In the *WAKE* mode, the device enables V5V LDO and waits for V5V_por_n high signal.
- Once the V5V crosses V5V_por_th, the V5V_por_n will be 'High' and the device enters into *WAIT* mode. In *WAIT* mode the device waits for trigger pulse on TRIG_IN pin from microcontroller. In this state, if a short or long pulse trigger signal is received on TRIG_IN within T_{wmode_tout} period, the AS8506C enters into *NORMAL* mode and performs required operations based on trigger pulse.

Figure 29:
Power-up Initialization Sequence



Device Interface

A 4-wire SPI is used to communicate with the device. Pins **CS**, **SCLK**, **SDI**, and **SDO** are used for SPI interface.

Serial Peripheral Interface

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller. The SPI is configured for half-duplex data transfer. The SPI in AS8506C provides access to the status registers, control registers and test registers. The SPI is also used to enter into test and OTP modes. This interface is only Slave interface and only Master can initiate the SPI operation. The SPI also supports block data transfer where sequential register data can be accessed with single SPI command.

The SPI can work on both the clock polarities. The polarity of the clock is dependent on the value of SCLK at the falling edge of CS.

At the falling edge of CS,

- If SCLK is "1", then the SPI is negative edge triggered.
- If the SCLK is "0", then SPI is positive edge triggered logic. see Figure 30 for more details.

Figure 30:
SPI Clock Polarity Table

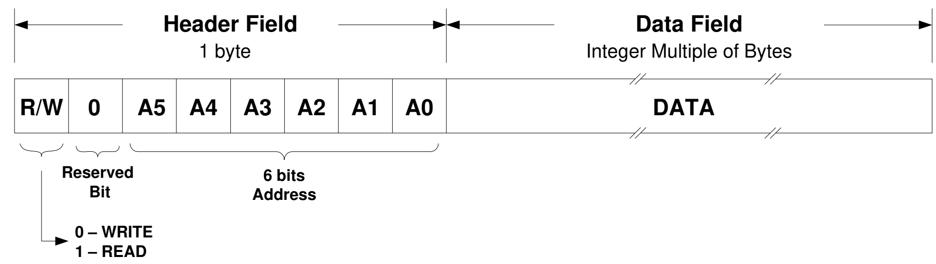
CS	SCLK	Description
↓	Low	Serial data is transferred at rising edge and sampled at falling edge of SCLK.
↓	High	Serial data is transferred at falling edge and sampled at rising edge of SCLK.

The SPI protocol frame is divided into two fields.

- The header field
- The data field

The header field is 1 byte long; containing a read/write command bit, 1 reserved bit, and 6 address bits. The SPI frame format is shown in Figure 31. In the data phase MSB is sent first and LSB is sent last.

Figure 31:
SPI Frame Format



SPI Write Operation

The SPI write operation begins with clock polarity selection at negative edge of CS (see Figure 30). Once the clock polarity is selected, the SPI write command is given by providing ‘0’ in R/W bit of the header field in first sampling edge at SDI pin. The next bit in header field is reserved and set to ‘0’. The 6 bits address of register to be written is provided at SDI pin in next six consecutive sampling edges of SCLK. The data to be written is followed by last bit of header field. With each sampling edge a bit is sampled starting from MSB to LSB. During complete SPI write operation the SCSN has to be ‘Low’. The SPI write operation ends with positive edge of SCSN. The waveform for SPI write operation with single data byte is shown in Figure 32 and Figure 33.

Figure 32:
SPI Write Operation with Negative Clock Polarity and 1 Byte of Data Field

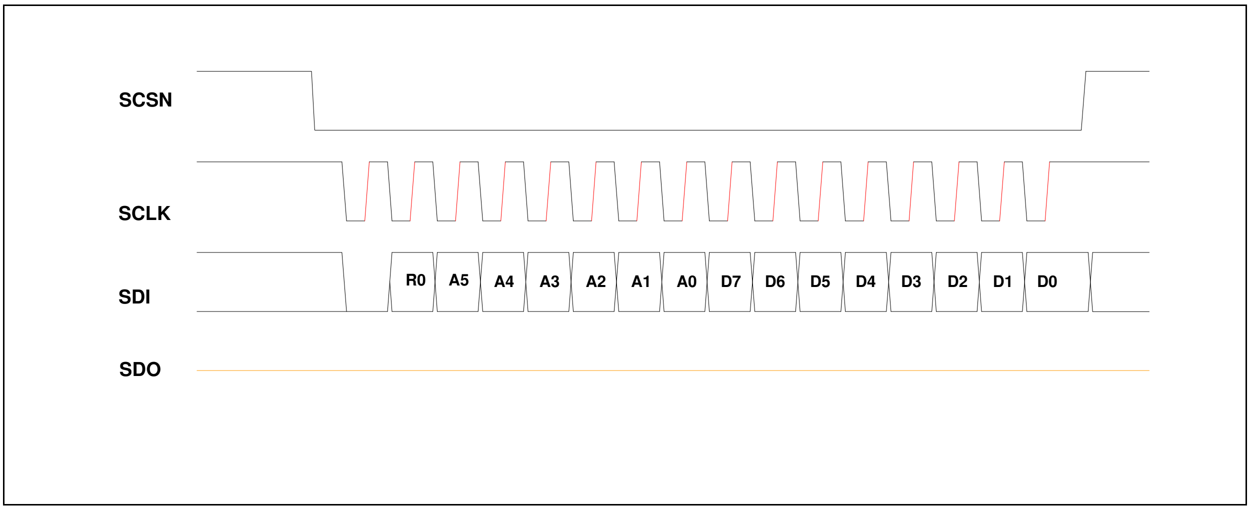
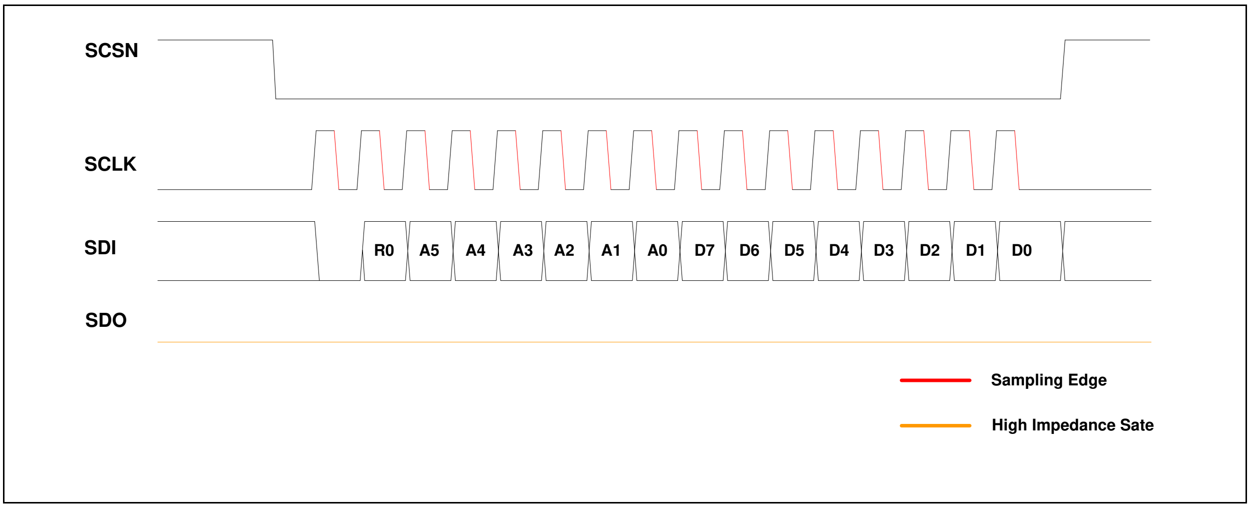
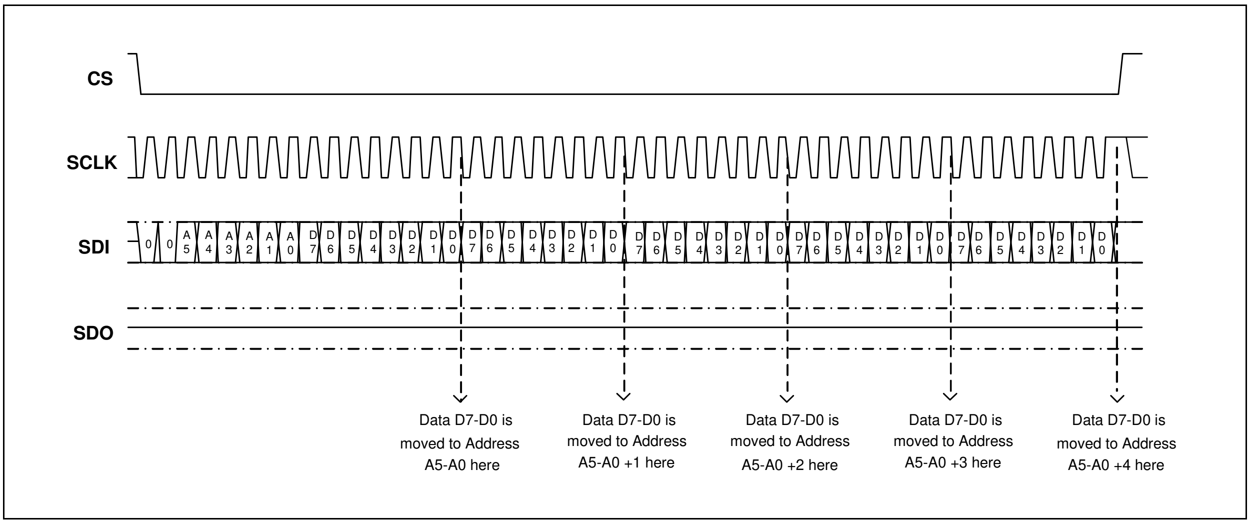


Figure 33:
SPI Write Operation with Positive Clock Polarity and 1 Byte of Data Field



In case of SPI block write operation, first data byte is written into addressed register same as single byte write operation. After first data byte, Master can send next data byte by keeping CS 'Low' and giving clock on SCLK as per polarity selection. At the end of every eighth data bit, the byte is written into next consecutive address location (internally address is incremented by one location). In this way, Master can continue writing into consecutive address locations. The waveform is shown in Figure 34.

Figure 34:
SPI Block Write Operation with Negative Clock Polarity



SPI Read Operation

The SPI read operation also begins with clock polarity selection at negative edge of SCSN (see Figure 30). Once the clock polarity is selected, the SPI read command is given by providing '1' in R/W bit of the header field in first sampling edge at SDI pin. The next bit in header fields is reserved and set to '0'. The 6 bits address of register to be read is provided at SDI pin in next six consecutive sampling edges of SCLK. The read data is followed by last bit of header field on SDO pin. With each sampling edge a bit can be read on SDO pin starting from MSB to LSB. In case of multi-data bytes, MSB of next data byte can be read after the LSB of previous data byte. During complete SPI read operation the SCSN has to be 'Low'. The SPI read operation ends with positive edge of SCSN. The wave form for SPI read operation with single data byte is shown in Figure 35 and Figure 36.

Figure 35:
SPI Read Operation with Negative Clock Polarity and 1 Byte of Data Field

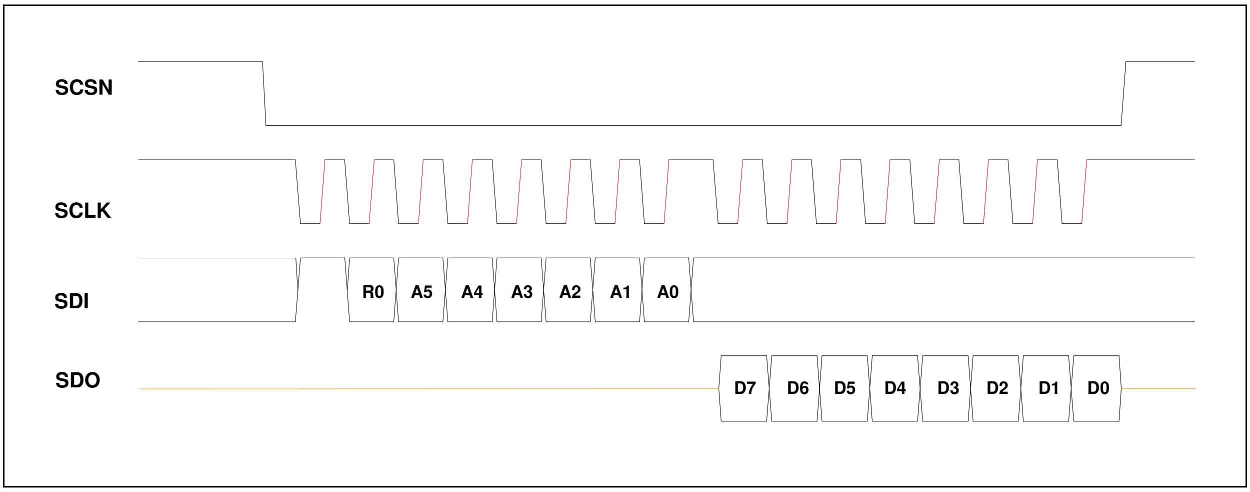
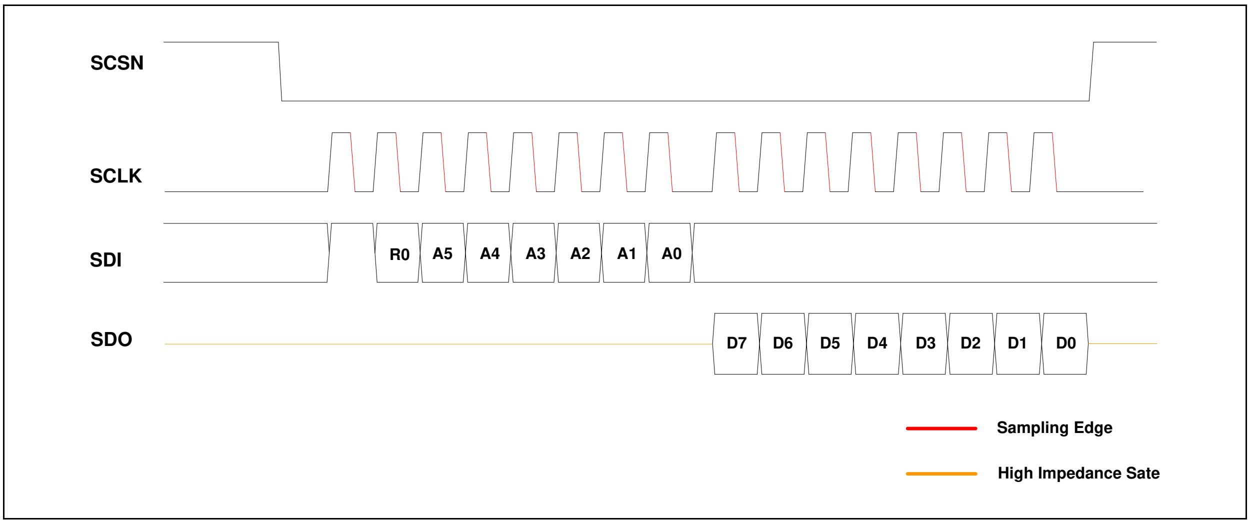
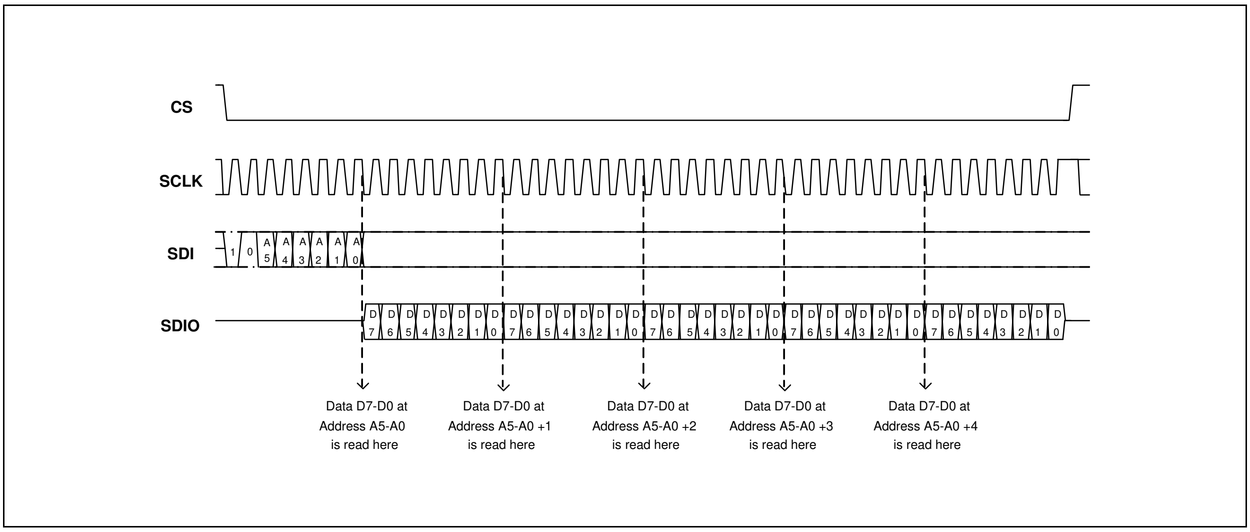


Figure 36:
SPI Read Operation with Positive Clock Polarity and 1 Byte of Data Field



In case of SPI block read operation, first data byte is read from addressed register same as single byte read operation. After first data byte read, Master can read next consecutive addressed data by keeping CS 'Low' and giving clock on SCLK as per clock polarity selection. At the end of every eighth data bit, the address pointer is incremented to next consecutive address location. In this way Master can continue reading from consecutive register address locations. The waveform is shown in Figure 37.

Figure 37:
SPI Block Read Operation with Negative Clock Polarity



Address Allocation Process

During the system configuration the microcontroller has to initiate the address allocation process for the AS8506C master and the stacked slave devices.

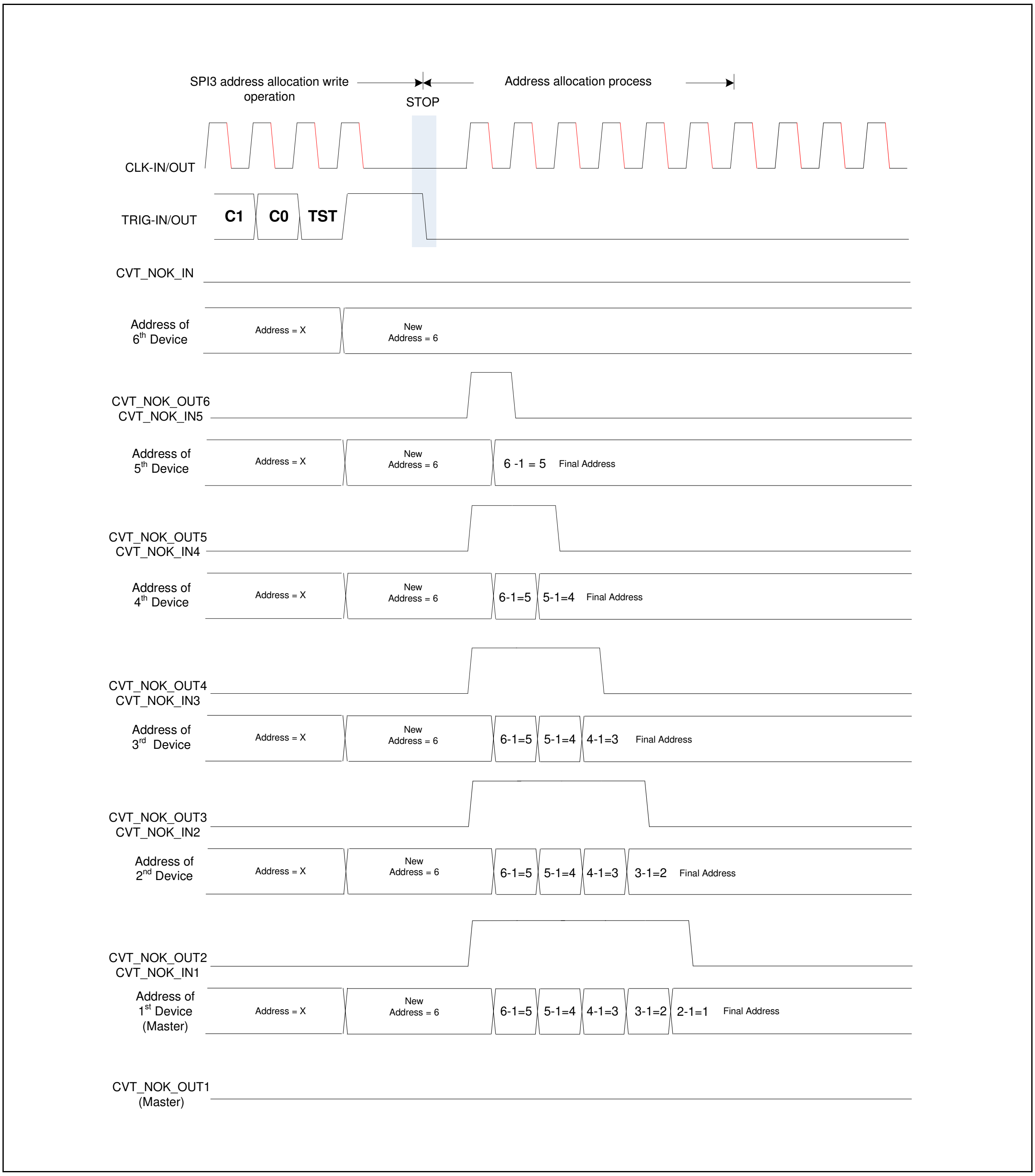
This process is started by writing the number of stacked IC's into address 0x1A (master register dadd_for_allc_reg) through the 4 wire SPI. After that the microcontroller needs to initiate the auto address allocation process by writing the datum 0x07 to master address 0x28 (register spi3_cmd_reg).

After the successful SPI3 address allocation write operation, all AS8506C devices including master will store their allocated device addresses as their address.

The device address "000000" is reserved as broadcast address seen by all devices.

The address allocation process is explained for 6 AS8506C devices (including master) in Figure 38.

Figure 38:
Address Allocation Process



In the address allocation process, the CVT_NOK_IN/CVT_NOK_OUT pins of AS8506C are used. After the successful SPI3 address allocation write operation, all AS8506C devices including Master will store the top device address (sent by Master in SPI3 address allocation write) as its address. The top device identifies itself as top most device and registers the address as its final address and at first rising edge of clock all devices force 'High' on its CVT_NOK_OUT pin. The concept of address allocation is: after the STOP of SPI3, at every falling edge of the clock each device will sample its CVT_NOK_IN pin. If CVT_NOK_IN pin is 'High', the device will decrement the assigned address by '1' and continue to force 'High' on its CVT_NOK_OUT pin at rising edge of clock. If CVT_NOK_IN is sampled to be 'Low', then the address value at register will be stored as its final device address and it stops forcing 'High' on its CVT_NOK_OUT pin and makes it 'Low' at next rising edge of clock.

In Figure 38, top most device pins are suffixed with '6' down to lower most device (Master) pins suffixed with '1' in descending order. There is no device above topmost device, CVT_NOK_IN6 is always 'Low'; therefore the address sent by Master is final address for the top device. For the fifth device the CVT_NOK_IN5 is 'Low' for one clock cycle, the address is decremented once. For the fourth device CVT_NOK_IN4 is 'Low' for two clock cycles, the address is decremented twice before registering it as final address. This procedure is continued and finally the Master device CVT_ONK_IN1 is 'Low' for 5 clock cycles, the address is decremented five times and finally address register will have value of "000001" as its final address. The microcontroller can identify the end of address allocation procedure in two ways:

- One way is by probing CVT_NOK_OUT of Master after initiating address allocation process for a pulse.
- The other method is by polling bit0 of spi3_cmd_reg register for '0' (Low) and no CRC errors.

During SPI3 address allocation write operation, if a CRC error occurs in the any of the Slaves, the Master indicates this failure of SPI3 transaction to all Slaves by driving TST bit 'High'. All Slaves should terminate the address allocation process if a 'High' TST bit is seen during start address allocation process SPI3 write operation. The Master will indicate the failure of address allocation process to µC by asserting a flag in the spi3_sts_reg register and sending interrupt pulse on its CVT_NOK_OUT pin.

Communication to Slaves

There are two modes of communication between the Master and Slaves in the AS8506C stack system:

- Broadcast Communication
- Communication with Individual Slave

Broadcast Communication

The Broadcast of communication is used to send the reference, lower, upper threshold limit codes and timer control register values for all the slaves.

Reference and thresholds can be set by one of the two methods:

- Through the external pins
- Through the Internal DAC

In case of the stacked system, reference and thresholds can be set by writing DAC values though broadcast SPI command.

Write the corresponding data in the registers of timer_cntl_reg, ref_dcod_lsb_reg/ref_dcod_msb_reg, hlmt_dcod_lsb_reg/hlmt_dcod_msb_reg and llmt_dcod_lsb_reg/llmt_dcod_msb_reg and command in the Command Registers spi3_cmd_reg and spop_dadd_bcmd_reg.

Example:

To write DAC code of 0x0666 in the lower threshold register of all the devices, initiate a broadcast command as given in the below sequence.

Figure 39:
Threshold Setting through Broadcast Command to Slaves

Command	Register Name	Address	Data
To set low threshold	llmt_dcod_lsb_reg	0x23	0x66
	llmt_dcod_msb_reg	0x24	0x06
Broadcast the cell lower limit DAC code	spop_dadd_bcmd_reg	0x25	0x03
Broadcast communication command	spi3_cmd_reg	0x28	0x09

Each broadcast write operation takes 35 clock cycles of the communication frequency. The default communication frequency is 5KHz.

Broadcast slave register write is also possible other than above registers.

If there any specific register of all the slaves to be written with the same content of Master then this feature is useful.

Write register address in the spop_reg_add_reg.

Example:

To set the external temperature thresholds to 4.15V, initiate a broadcast command as given in the below sequence.

Figure 40:
External Temperature Threshold Setting through Broadcast Command to Slaves

Command	Register Name	Address	Data
To set the external temperature threshold	tflg_tshld_setg_reg	0x1D	0xFF
Address of the register to broadcast	spop_reg_add_reg	0x26	0x1D
Broadcast communication command	spi3_cmd_reg	0x28	0x0B

Communication with Individual Slave

Communication with an individual slave is done as SPI write or read.

Write operation.

To perform the write operation to one of the slave device, corresponding data should be written in these registers spop_dadd_bcmd_reg, spop_reg_add_reg, wrop_data_reg and spi3_cmd_reg.

Example:

To set the external temperature threshold of the slave device address 0x06 to 4.15V, initiate a broadcast command as given in the below sequence.

Figure 41:
Write Operation to the Individual Slave

Command	Register Name	Address	Data
Slave device address	spop_dadd_bcmd_reg	0x25	0x06
Address of the slave register	spop_reg_add_reg	0x26	0x1D
To set the external temperature threshold	wrop_data_reg	0x27	0xFF
Slave write command	spi3_cmd_reg	0x28	0x05

Read operation.

To perform the read operation to one of the slave device, corresponding data should be written in these registers spop_dadd_bcmd_reg, spop_reg_add_reg and spi3_cmd_reg.

Data from the slave device will be written in the register rdop_data_reg.

Example:

To read the temperature status register of the slave device address 0x06, initiate a broadcast command as given in the below sequence.

Figure 42:
Read Operation to the Individual Slave

Command	Register Name	Address	Data
Slave device address Slave	spop_dadd_bcmd_reg	0x25	0x06
Address of the slave register	spop_reg_add_reg	0x26	0x05
write command	spi3_cmd_reg	0x28	0x03

SPI Timing Diagrams

Figure 43:
Timing Diagram for Write Operation

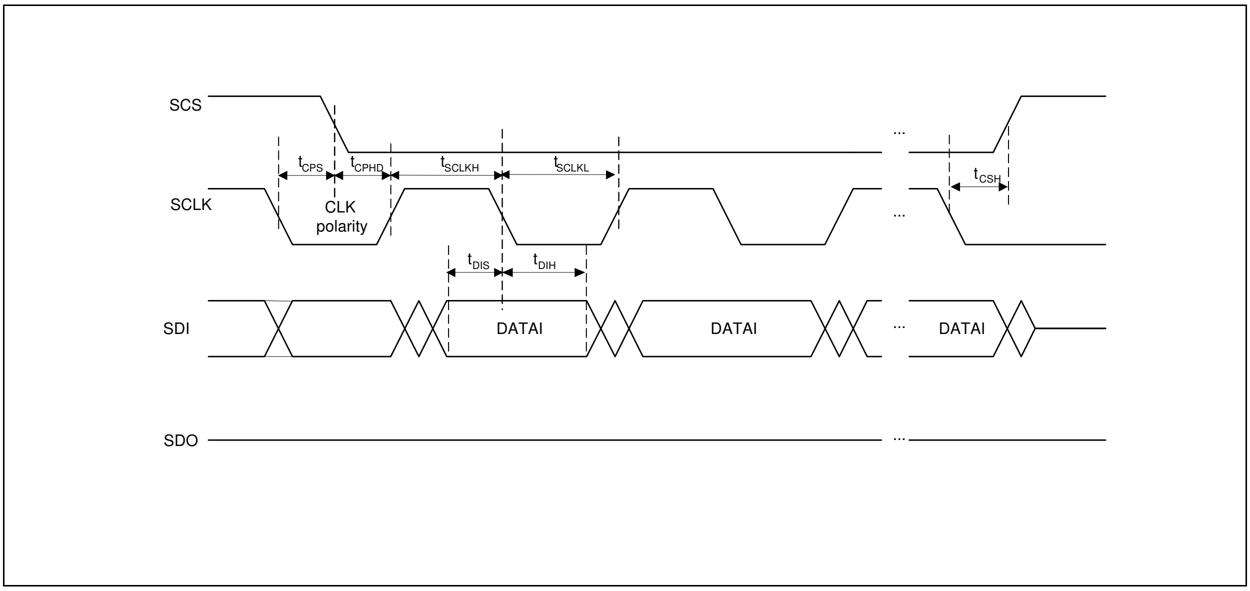
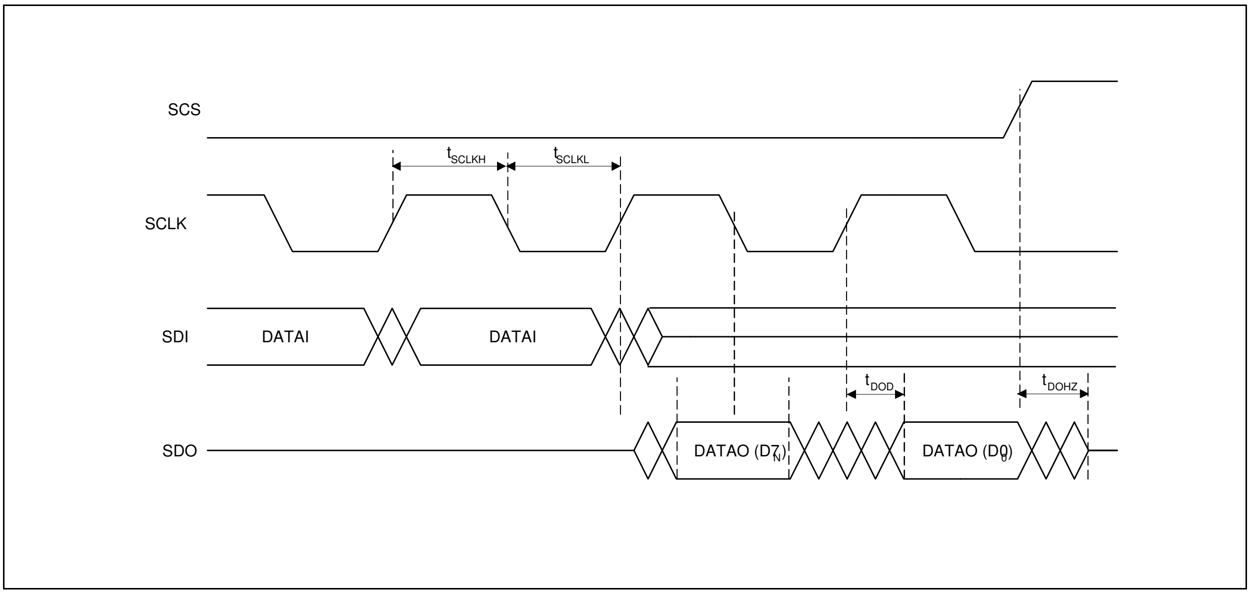


Figure 44:
Timing Diagram for Read Operation



SPI Protocol

Figure 45:
SPI Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
General						
BR_{SPI}	Bit rate			1	Mbps	
T_{SCLKH}	Clock high time	400			ns	
T_{SCLKL}	Clock low time	400			ns	
Write Operation Parameters						
t_{DIS}	Data in setup time	20			ns	
t_{DIH}	Data in hold time	20			ns	
T_{CSH}	SCSN hold time	20			ns	
Read Operation Parameters						
t_{DOD}	Data out delay			80	ns	
t_{DOHZ}	Data out to high impedance delay			80	ns	Time for the SPI to release the SDO bus
Timing Parameters for SCLK Polarity Identification						
t_{CPS}	Clock setup time (CLK polarity)	20			ns	Setup time of SCLK with respect to SCSN falling edge.
t_{CPHD}	Clock hold time (CLK polarity)	20			ns	Hold time of SCLK with respect to SCSN falling edge.

System Timings

Figure 46:
System Timings

Symbol	Parameter	Min	Typ	Max	Unit	Note
Wake-up Timing						
T_{wake_pulse}	Wake pulse width	100			µs	
T_{filter_delay}	Time between edge on TRIG_IN pin to trig_in_fltrd signal			4	µs	
T_{filter}	WAKE_IN pin filter specification	1		4	µs	
Trigger Timing						
T_{status_cmd}	Status request command pulse	500		1000	µs	
T_{bal_cmd}	Cell balance command pulse	7000			µs	
Wait Mode Timing						
T_{wmode_tout}	*WAIT* mode timeout		2000		ms	

Register Space Description

The AS8506C register space is divided into control registers and test registers. All of these registers are accessed through SPI.

Status Registers

Figure 47:
Cell Detection Status Register

Address	Register Name	Features and Bit Description		SPI 4	SPI 3	POR Value
0x00	cel_det_stat_reg	Indicates the detected cells.		R	R	0000_0000 POR_V5V
		D0	**0** → Cell 1 is not detected **1** → Cell 1 is detected			
		D1	**0** → Cell 2 is not detected **1** → Cell 2 is detected			
		D2	**0** → Cell 3 is not detected **1** → Cell 3 is detected			
		D3	**0** → Cell 4 is not detected **1**→ Cell 4 is detected			
		D4	**0** → Cell 5 is not detected **1** → Cell 5 is detected			
		D5	**0** → Cell 6 is not detected **1** → Cell 6 is detected			
		D6	**0** → Cell 7 is not detected **1** → Cell 7 is detected			
		D7	Reserved			

Figure 48:
Diagnostic Status Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x01	diag_sts_reg	Diagnostic register. µC can read this register if pulse is detected on **CVT_NOK_OUT** pin, to diagnose cause of indication.		R	R	0000_0000 POR_V5V
		D0	**1** → Low Threshold limit cross Indicator [(1)]			
		D1	**1** → High Threshold limit cross indicator [(2)]			
		D2	**1** → Over-temperature indicator			
		D3	**1** → Address allocation procedure fail			
		D4	**1** → SPI3 read operation fail			
		D5	**1** → SPI3 write operation fail			
		D6	**1** → SPI3 Broadcast operation fail			
		D7	Reserved			

Note(s) and/or Footnote(s):

1. This bit is only valid if all 7 cells are connected. If the cells connected are less than 7, use the cel_low_thsld_stat_reg (0x02) to detect a low threshold crossing.
2. This bit is only valid if all 7 cells are connected. If the cells connected are less than 7, use the cel_high_thsld_stat_reg (0x03) to detect a high threshold crossing.

Figure 49:
Cell Lower Threshold Status Register

<table>
<tr><th>Address</th><th>Register Name</th><th colspan="2">Features and Bit Description</th><th>SPI4</th><th>SPI3</th><th>POR Value</th></tr>
<tr><td rowspan="9">0x02</td><td rowspan="9">cel_low_thsld_stat_reg</td><td colspan="2">Indicates if a cell voltage crossed the lower threshold limit set by µC.</td><td rowspan="9">R</td><td rowspan="9">R</td><td rowspan="9">0000_0000
POR_V5V</td></tr>
<tr><td>D0</td><td>0 → Cell 1 voltage is more than Low Threshold limit set
1 → Cell 1 voltage is less than Low Threshold limit set</td></tr>
<tr><td>D1</td><td>0 → Cell 2 voltage is more than Low Threshold limit set
1 → Cell 2 voltage is less than Low Threshold limit set</td></tr>
<tr><td>D2</td><td>0 → Cell 3 voltage is more than Low Threshold limit set
1 → Cell 3 voltage is less than Low Threshold limit set</td></tr>
<tr><td>D3</td><td>0 → Cell 4 voltage is more than Low Threshold limit set
1 → Cell 4 voltage is less than Low Threshold limit set</td></tr>
<tr><td>D4</td><td>0 → Cell 5 voltage is more than Low Threshold limit set
1 → Cell 5 voltage is less than Low Threshold limit set</td></tr>
<tr><td>D5</td><td>0 → Cell 6 voltage is more than Low Threshold limit set
1 → Cell 6 voltage is less than Low Threshold limit set</td></tr>
<tr><td>D6</td><td>0 → Cell 7 voltage is more than Low Threshold limit set
1 → Cell 7 voltage is less than Low Threshold limit set</td></tr>
<tr><td>D7</td><td>Reserved</td></tr>
</table>

Figure 50:
Cell Higher Threshold Status Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x03	cel_high_thsld_stat_reg	Indicates if a cell voltage crossed the lower threshold limit set by µC.		R	R	0000_0000 POR_V5V
		D0	**0** → Cell 1 voltage is less than High Threshold limit set **1** → Cell 1 voltage is more than High Threshold limit			
		D1	**0** → Cell 2 voltage is less than High Threshold limit set **1** → Cell 2 voltage is more than High Threshold limit			
		D2	**0** → Cell 3 voltage is less than High Threshold limit set **1** → Cell 3 voltage is more than High Threshold limit			
		D3	**0** → Cell 4 voltage is less than High Threshold limit set **1** → Cell 4 voltage is more than High Threshold limit			
		D4	**0** → Cell 5 voltage is less than High Threshold limit set **1** → Cell 5 voltage is more than High Threshold limit			
		D5	**0** → Cell 6 voltage is less than High Threshold limit set **1** → Cell 6 voltage is more than High Threshold limit			
		D6	**0** → Cell 7 voltage is less than High Threshold limit set **1** → Cell 7 voltage is more than High Threshold limit			
		D7	Reserved			

Figure 51:
Cell Reference Status Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x04	cel_ref_stat_reg	Indicates which cell has reached the reference value at least once. This status is cleared when new reference is selected.		R	R	0000_0000 POR_V5V
		D0	**0** → Cell 1 voltage is less than reference voltage **1** → Cell 1 voltage is more than reference voltage			
		D1	**0** → Cell 2 voltage is less than reference voltage **1** → Cell 2 voltage is more than reference voltage			
		D2	**0** → Cell 3 voltage is less than reference voltage **1** → Cell 3 voltage is more than reference voltage			
		D3	**0** → Cell 4 voltage is less than reference voltage **1** → Cell 4 voltage is more than reference voltage			
		D4	**0** → Cell 5 voltage is less than reference voltage **1** → Cell 5 voltage is more than reference voltage			
		D5	**0** → Cell 6 voltage is less than reference voltage **1** → Cell 6 voltage is more than reference voltage			
		D6	**0** → Cell 7 voltage is less than reference voltage **1** → Cell 7 voltage is more than reference voltage			
		D7	Reserved			

Figure 52:
Temperature Status Register

<table>
<tr><th>Address</th><th>Register Name</th><th colspan="2">Features and Bit Description</th><th>SPI4</th><th>SPI3</th><th>POR Value</th></tr>
<tr><td rowspan="6">0x05</td><td rowspan="6">temp_stat_reg</td><td colspan="2">Indicates the status of temperature monitors.</td><td rowspan="6">R</td><td rowspan="6">R</td><td rowspan="6">0000_0000
POR_V5V</td></tr>
<tr><td>D0</td><td>0 → Ambient temperature is less than warning threshold
1 → Ambient temperature is more than warning threshold</td></tr>
<tr><td>D1</td><td>0 → Internal temperature is less than warning threshold
1 → Internal temperature is more than warning threshold</td></tr>
<tr><td>D2</td><td>0 → Ambient temperature is less than maximum threshold
1 → Ambient temperature is more than maximum threshold</td></tr>
<tr><td>D3</td><td>0 → Internal temperature is less than maximum threshold
1 → Internal temperature is more than maximum threshold</td></tr>
<tr><td>D7:D4</td><td>Reserved</td></tr>
</table>

Figure 53:
Zero Cross Status Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x06	zero_crs_stat_reg	Indicates which cell voltage has crossed zero voltage and reached negative during sudden loading condition. This indirectly indicates the increasing status of cell internal impedance.		R	R	
		D0	**0** → Cell 1 voltage is normal **1** → Cell 1 voltage has crossed zero voltage towards negative direction			
		D1	**0** → Cell 2 voltage is normal **1** → Cell 2 voltage has crossed zero voltage towards negative direction			
		D2	**0** → Cell 3 voltage is normal **1** → Cell 3 voltage has crossed zero voltage towards negative direction			
		D3	**0** → Cell 4 voltage is less than reference voltage **1** → Cell 4 voltage is more than reference voltage			
		D4	**0** → Cell 5 voltage is normal **1** → Cell 5 voltage has crossed zero voltage towards negative direction			
		D5	**0** → Cell 6 voltage is normal **1** → Cell 6 voltage has crossed zero voltage towards negative direction			
		D6	**0** → Cell 7 voltage is normal **1** → Cell 7 voltage has crossed zero voltage towards negative direction			
		D7	Reserved			

Figure 54:
Cell1 Voltage LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x07	cell1_volt_lsb_reg	Cell1 voltage measured. 8 least significant bits of 12-bit ADC code of Cell1		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 55:
Cell1 Voltage MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x08	cell1_volt_msb_reg	Cell1 voltage measured. 4 most significant bits of 12-bit ADC code of Cell1		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 56:
Cell2 Voltage LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x09	Cell2_volt_lsb_reg	Cell2 voltage measured. 8 least significant bits of 12-bit ADC code of Cell2		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 57:
Cell2 Voltage MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x0A	cell2_volt_msb_reg	Cell2 voltage measured. 4 most significant bits of 12-bit ADC code of Cell2		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 58:
Cell3 Voltage LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x0B	cell3_volt_lsb_reg	Cell3 voltage measured. 8 least significant bits of 12-bit ADC code of Cell3		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 59:
Cell3 Voltage MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x0C	cell3_volt_msb_reg	Cell3 voltage measured. 4 most significant bits of 12-bit ADC code of Cell3		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 60:
Cell4 Voltage LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x0D	cell4_volt_lsb_reg	Cell4 voltage measured. 8 least significant bits of 12-bit ADC code of Cell4		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 61:
Cell4 Voltage MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x0E	cell4_volt_msb_reg	Cell4 voltage measured. 4 most significant bits of 12-bit ADC code of Cell4		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 62:
Cell5 Voltage LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x0F	cell5_volt_lsb_reg	Cell5 voltage measured. 8 least significant bits of 12-bit ADC code of Cell5		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 63:
Cell5 Voltage MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x10	cell5_volt_msb_reg	Cell5 voltage measured. 4 most significant bits of 12-bit ADC code of Cell5		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 64:
Cell6 Voltage LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x11	cell6_volt_lsb_reg	Cell6 voltage measured. 8 least significant bits of 12-bit ADC code of Cell6		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 65:
Cell6 Voltage MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x12	cell6_volt_msb_reg	Cell6 voltage measured. 4 most significant bits of 12-bit ADC code of Cell6		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 66:
Cell7 Voltage LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x13	cell7_volt_lsb_reg	Cell7 voltage measured. 8 least significant bits of 12-bit ADC code of Cell7		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 67:
Cell7 Voltage MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x14	cell7_volt_msb_reg	Cell7 voltage measured. 4 most significant bits of 12-bit ADC code of Cell7		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 68:
Temperature Input1 LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x15	temp_in1_lsb_reg	Temperature sensor input1 measured. 8 least significant bits of 12-bit ADC code of temperature input1.		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 69:
Temperature Input1 MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x16	temp_in1_msb_reg	Temperature sensor input1 measured. 4 most significant bits of 12-bit ADC code of temperature input1.		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 70:
Temperature Input2 LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x17	temp_in2_lsb_reg	Temperature sensor input2 measured. 8 least significant bits of 12-bit ADC code of temperature input1.		R	R	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of ADC code			

Figure 71:
Temperature Input2 MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x18	temp_in2_msb_reg	Temperature sensor input2 measured. 4 most significant bits of 12-bit ADC code of temperature input2.		R	R	0000_0000 POR_V5V
		D3:D0	Bit11 to Bit8 of ADC code			
		D7:D4	Reserved			

Figure 72:
SPI3 Status Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x19	spi3_sts_reg	This register has status of the latest SPI3 operation.		R	R	0000_0000 POR_V5V
		D0	**0** → No CRC error. **1** → CRC error for data from Master to Slave			
		D1	**0** → No CRC error. **1** → CRC error for data from Slave to Master			
		D2	**0** → Start address allocation process write pass **1** → Start address allocation process write fail			
		D7:D3	Reserved			

Configuration and 3-Wire SPI Interface Related Registers

Figure 73:
Device Address for Address Allocation Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x1A	dadd_for_allc_reg	The device address for address allocation. In the address allocation process the µC writes top device address in this register. Address "00000" is reserved as broadcast address.		R/W	R/W	0000_0000 POR_VSUP
		D5:D0	Device address			
		D7:D6	Reserved			

Figure 74:
Allocated Device Address Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x1B	allcd_dev_add_reg	Final device address after address allocation process is completed		R	R	0000_0000 POR_VSUP
		D5:D0	Device address			
		D7:D6	Reserved			

Figure 75:
Device Configuration Setting Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x1C	dev_cnfg_setg_reg	Selects SPI3 frequency of operation.		R/W	-	0000_0000 POR_VSUP
		D1:D0	**00** → 5 KHz **01** → 20 KHz **10** → 40 KHz **11** → Reserved			
		D7:D2	Reserved			

Figure 76:
Temperature Threshold Setting Register

<table>
<tr><th>Address</th><th>Register Name</th><th colspan="2">Features and Bit Description</th><th>SPI4</th><th>SPI3</th><th>POR Value</th></tr>
<tr><td rowspan="3">0x1D</td><td rowspan="3">tflg_tshld_setg_reg</td><td colspan="2">Sets over-temperature warning flag and shutdown flag threshold.</td><td rowspan="3">R/W</td><td rowspan="3">R/W</td><td rowspan="3">XXXX_XXXX POR_VSUP</td></tr>
<tr><td>D3:D0</td><td>Over temperature warning flag threshold selection
<table>
<tr><th>Code</th><th>Value</th><th>Code</th><th>Value</th><th>Code</th><th>Value</th></tr>
<tr><td>0000</td><td>3.165</td><td>0110</td><td>3.561</td><td>1100</td><td>3.957</td></tr>
<tr><td>0001</td><td>3.231</td><td>0111</td><td>3.627</td><td>1101</td><td>4.023</td></tr>
<tr><td>0010</td><td>3.297</td><td>1000</td><td>3.693</td><td>1110</td><td>4.089</td></tr>
<tr><td>0011</td><td>3.363</td><td>1001</td><td>3.759</td><td>1111</td><td>4.155</td></tr>
<tr><td>0100</td><td>3.429</td><td>1010</td><td>3.825</td><td>-</td><td>-</td></tr>
<tr><td>0101</td><td>3.495</td><td>1011</td><td>3.891</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>D7:D4</td><td>Over temperature shutdown flag threshold selection
<table>
<tr><th>Code</th><th>Value</th><th>Code</th><th>Value</th><th>Code</th><th>Value</th></tr>
<tr><td>0000</td><td>3.165</td><td>0110</td><td>3.561</td><td>1100</td><td>3.957</td></tr>
<tr><td>0001</td><td>3.231</td><td>0111</td><td>3.627</td><td>1101</td><td>4.023</td></tr>
<tr><td>0010</td><td>3.297</td><td>1000</td><td>3.693</td><td>1110</td><td>4.089</td></tr>
<tr><td>0011</td><td>3.363</td><td>1001</td><td>3.759</td><td>1111</td><td>4.155</td></tr>
<tr><td>0100</td><td>3.429</td><td>1010</td><td>3.825</td><td>-</td><td></td></tr>
<tr><td>0101</td><td>3.495</td><td>1011</td><td>3.891</td><td>-</td><td></td></tr>
</table></td></tr>
</table>

Figure 77:
Timer Control Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x1E	timer_cntl_reg	D2:D0	**000** → 25% duty cycle **001** → 15% duty cycle **010** → 20% duty cycle **011** → 30% duty cycle **100** → 35% duty cycle **101** → 40% duty cycle **110** → 45% duty cycle **111** → 50% duty cycle	R/W	R/W	0000_0000 POR_VSUP
		D4:D3	**00** → 1s time slot **01** → 8s time slot **10** → 16s time slot **11** → 32s time slot			
		D6:D5	**00** → 100 KHz **01** → 25 KHz **10** → 50 KHz **11** → 200 KHz			
		D7	**0** → 5 clock cycles for comparator **1** → 15 clock cycles for comparator			

Figure 78:
Reference DAC Code LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x1F	ref_dcod_lsb_reg	Least Significant byte of 12-bit DAC code for setting reference voltage.		R/W	R/W	0000_0000 POR_VSUP
		D7:D0	Bit7 to Bit0 of DAC code			

Figure 79:
Reference DAC Code MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x20	ref_dcod_msb_reg	Most Significant byte of 12-bit DAC code for setting reference voltage.		R/W	R/W	0000_0000 POR_VSUP
		D3:D0	Bit11 to Bit8 of DAC code			
		D7:D4	Reserved			

Figure 80:
Higher Limit DAC Code LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x21	hlmt_dcod_lsb_reg	Least Significant byte of 12-bit DAC code for setting high limit voltage.		R/W	R/W	0000_0000 POR_VSUP
		D7:D0	Bit7 to Bit0 of DAC code			

Figure 81:
Higher Limit DAC Code MSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x22	hlmt_dcod_msb_reg	Most Significant byte of 12-bit DAC code for setting high limit voltage.		R/W	R/W	0000_0000 POR_VSUP
		D3:D0	Bit11 to Bit8 of DAC code			
		D7:D4	Reserved			

Figure 82:
Lower Limit DAC Code LSB Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x23	llmt_dcod_lsb_reg	Least Significant byte of 12-bit DAC code for setting low limit voltage.		R/W	R/W	0000_0000 POR_VSUP
		D7:D0	Bit7 to Bit0 of DAC code			

Figure 83:
Lower Limit DAC Code MSB Register

<table>
<tr><th>Address</th><th>Register Name</th><th colspan="2">Features and Bit Description</th><th>SPI4</th><th>SPI3</th><th>POR Value</th></tr>
<tr><td rowspan="3">0x24</td><td rowspan="3">llmt_dcod_msb_reg</td><td colspan="2">Most Significant byte of 12-bit DAC code for setting low limit voltage.</td><td rowspan="3">R/W</td><td rowspan="3">R/W</td><td rowspan="3">0000_0000
POR_VSUP</td></tr>
<tr><td>D3:D0</td><td>Bit11 to Bit8 of DAC code</td></tr>
<tr><td>D7:D4</td><td>Reserved</td></tr>
</table>

Figure 84:
Device Address and Broadcast Command SPI Operation Register

<table>
<tr><th>Address</th><th>Register Name</th><th colspan="2">Features and Bit Description</th><th>SPI4</th><th>SPI3</th><th>POR Value</th></tr>
<tr><td rowspan="5">0x25</td><td rowspan="5">spop_dadd_bcmd_reg</td><td colspan="2">Device address/ broadcast command register</td><td rowspan="5">R/W</td><td rowspan="5">-</td><td rowspan="5">0000_0000
POR_V5V</td></tr>
<tr><td rowspan="3">D5:D0</td><td>If spi3_cmd_reg [D3-D1] = 001/010
Address of Device to be accessed.
(000000 address is broadcast address)</td></tr>
<tr><td>If spi3_cmd_reg [D3-D1] = 100
Broadcast communication commands.
000000 → No operation
000001 → Timer control register write
000010 → Cell reference DAC code write
000011 Cell lower limit DAC code write
000100 → Cell higher limit DAC code write</td></tr>
<tr><td>If spi3_cmd_reg [D3-D1] = 101
000000 → Data of register wrop_data_reg is written to address stored in spop_reg_add_reg in all devices.</td></tr>
<tr><td>D7:D6</td><td>Reserved
(accessible only in Master mode)</td></tr>
</table>

Figure 85:
SPI Operation Register Address Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x26	spop_reg_add_reg	Address of register to be accessed during 3-wire read/write operation in the device selected in spop_dadd_bcmd_reg		R/W	-	0000_0000 POR_V5V
		D6:D0	Address of Register to be accessed (R/W)			
		D7:D4	Reserved (accessible only in Master mode)			

Figure 86:
SPI Write Operation Data Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x27	wrop_data_reg	Data to be written in the register addressed by spop_reg_add_reg of device selected in spop_dadd_bcmd_reg during SPI3 write operation.		R/W	-	0000_0000 POR_V5V
		D7:D0	Bit7 to Bit0 of accessed register (accessible only in Master mode)			

Figure 87:
SPI3 Command Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x28	spi3_cmd_reg	3-wire SPI command register. Register is cleared once the SPI3 transaction is done.		R/W	-	0000_0000 POR_V5V
		D0	**0** → No SPI3 operation **1** → Start SPI3 operation corresponding to command code			
		D3:D1	**000** → Reserved **001** → Slave register Read **010** → Slave register Write **011** → Start address allocation process **100** → Broadcast configuration command **101** → Broadcast Slave register Write **110** → Reserved **111** → Reserved			
		D7:D4	Reserved			

Figure 88:
SPI Read Operation Data Register

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x29	rdop_data_reg	Read data from the register addressed by spop_reg_add_reg of device selected in spop_dadd_bcmd_reg during SPI3 read operation.		R/W	R/W	0000_0000 POR_VSUP
		D7:D0	Bit7 to Bit0 of accessed register (accessible only in Master mode)			

Figure 89:
Feature Selection Register 1

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x2A	feat_sel_reg_1	Feature selection register1.		R/W	R/W	0000_0000 POR_VSUP
		D0	**1** → Zero cross detection enable			
		D2:D1	Zero cross detection filter setting **00** → 8µs **01** → 6µs **10** → 4µs **11** → 2µs			
		D3	Reserved			
		D4	**1** → External resistor divider enable			
		D5	**0** → Cell reference is generated from DAC **1** → Cell reference is supplied externally on VREF_IN pin			
		D6	**0** → Cell Lower/Higher limit is generated from DAC **1** → Cell Lower/Higher limit is supplied externally on CELL_THL and CELL_THU pins			
		D7	Reserved			

Figure 90:
Feature Selection Register 2

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x2B	feat_sel_reg_2	Feature selection register2.		R/W	-	0000_0010 POR_V5V
		D1:D0	FD_OUT pad configuration **10** → Optocoupler driver **11** → Normal Pad			
		D7:D2	Reserved			

Note(s) and/or Footnote(s):

1. Registers from address 0x2C to 0x2F are 'Reserved'.

OTP Reflection Registers

Figure 91:
OTP Reflection Register 1

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x30	otp_refln_reg_1	D7:D0	OTP bits [0:7] Chip ID [0:7]	R	R	0000_0000 POR_V5V

Figure 92:
OTP Reflection Register 2

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x31	otp_refln_reg_2	D7:D0	OTP bits [8:15] Chip ID [8:15]	R	R	0000_0000 POR_V5V

Figure 93:
OTP Reflection Register 3

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x32	otp_refln_reg_3	D7:D0	OTP bits [16:23] Chip ID [16:18], OTP bits [19:23]	R	R	0000_0000 POR_V5V

Figure 94:
OTP Reflection Register 4

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x33	otp_refln_reg_4	D7:D0	OTP bits [24:31]	R	R	0000_0000 POR_V5V

Figure 95:
OTP Reflection Register 5

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x34	otp_refln_reg_5	D7:D0	OTP bits [32:39]	R	R	0000_0000 POR_V5V

Figure 96:
OTP Reflection Register 6

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x35	otp_refln_reg_6	D7:D0	OTP bits [40:47]	R	R	0000_0000 POR_V5V

Figure 97:
OTP Reflection Register 7

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x36	otp_refln_reg_7	D7:D0	OTP bits [48:55]	R	R	0000_0000 POR_V5V

Figure 98:
OTP Reflection Register 8

Address	Register Name	Features and Bit Description		SPI4	SPI3	POR Value
0x37	otp_refln_reg_8	D7:D0	OTP bits [56:63]	R	R	0000_0000 POR_V5V

Note(s) and/or Footnote(s):

1. Registers from address 0x38 to 0x39 are 'Reserved'.
2. Registers from address 0x3A to 0x4E are OTP and Test registers. These are for factory use.

Application Information

Figure 99:
Application Schematic with Single Device

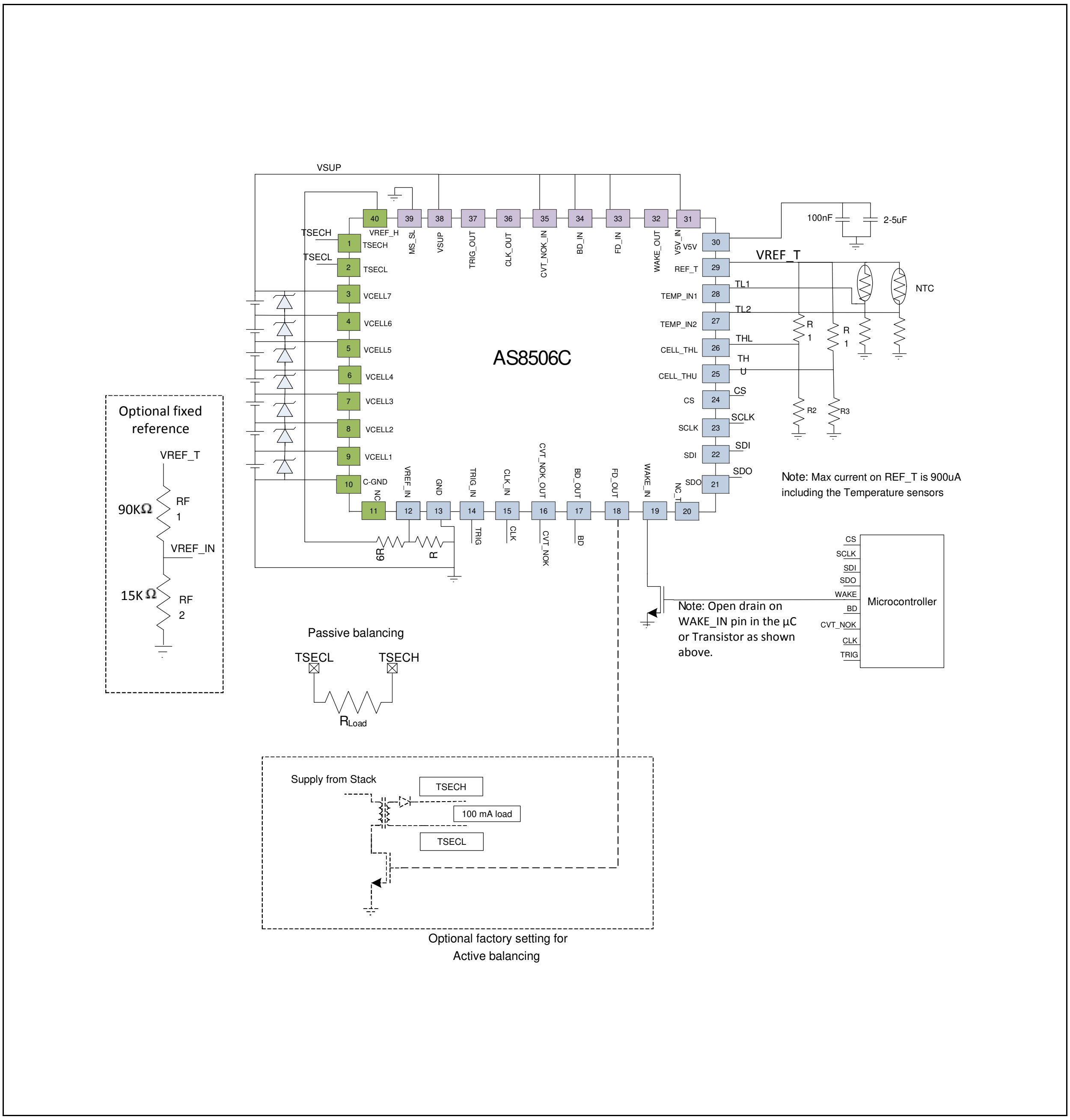


Figure 100:
Application Schematic with Single Device Passive Balancing-Option 1

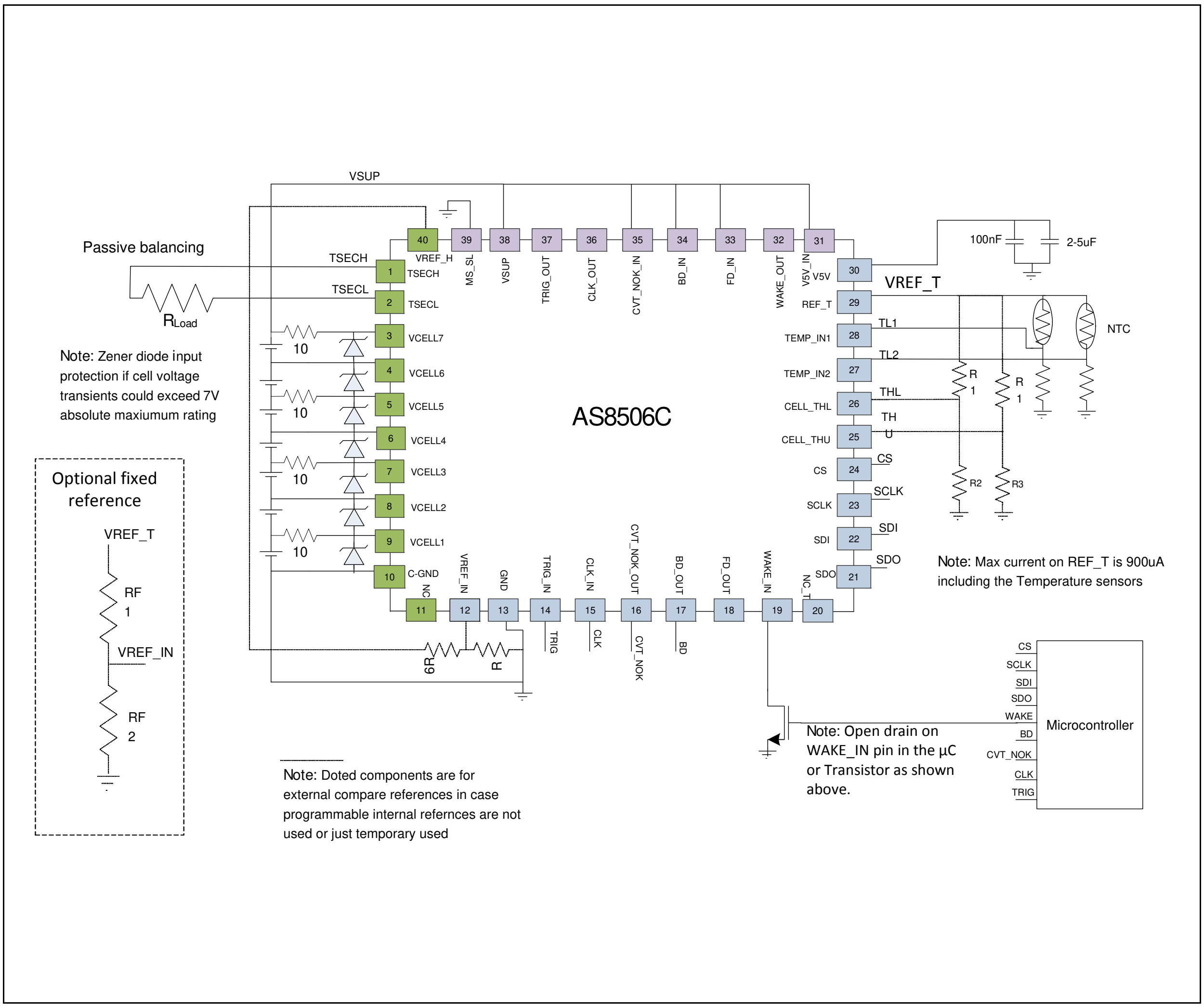
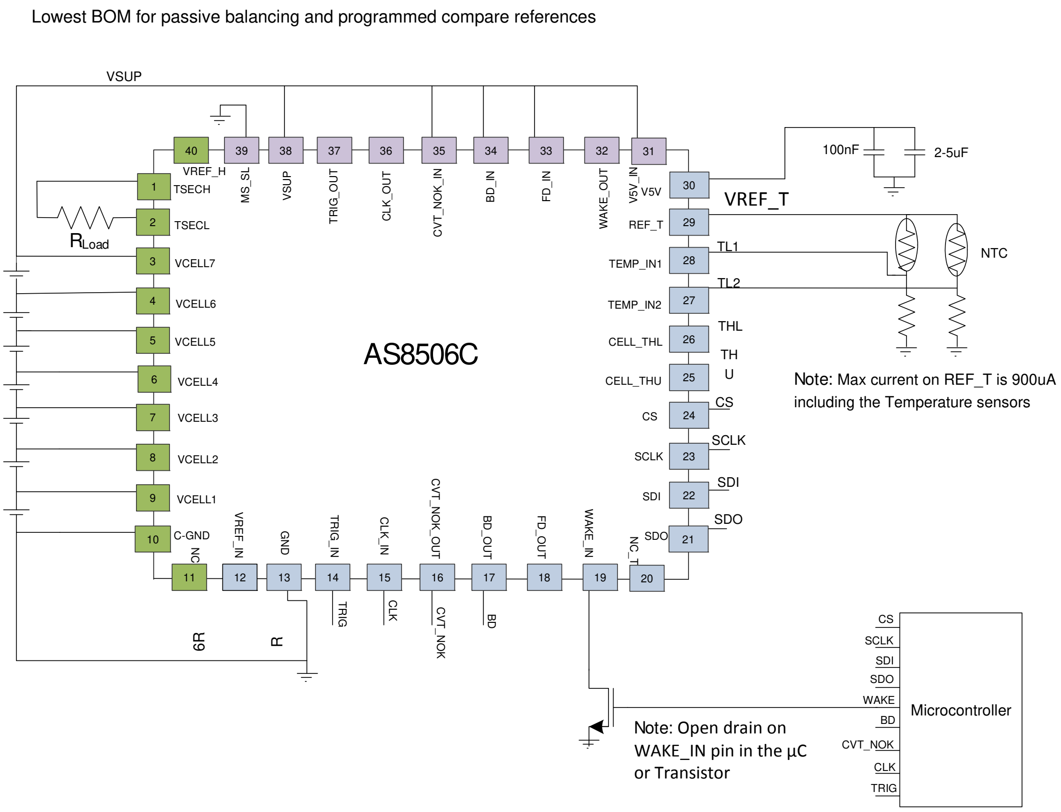


Figure 101:
Application Schematic with Single Device Passive Balancing-Option 2



Passive balance

Passive balance is to dissipate the energy from the cell with the higher cell voltage to the reference value (average of the stack e.g. max cell voltage in constant voltage charge phase or mean cell voltage as genertaed by resitor divider).

Resistor value should be selected based on the cell chemistry and voltage limits. Maximum current capability of internal shuttle switch is 100mA. Internal resistance of the shuttle switch typically is 5Ω..

Active balance

In the active balance device charge the cells which are lower than the reference voltage. This is a method of charge transfer from the stack to the cell.

Flyback converter is used for this charge transfer. Active balancing mode need to be enabled by factory setting. It is not available for the default ASSP.

Flyback Converter (with external Transformer)

The high-efficiency, high-voltage, DC-DC Flyback converter delivers current of 100mA to the lithium ion cell when the secondary side of the Flyback transformer is connected to the cell terminals. This also gives the isolation between the primary supply and the load cell. The Flyback converter is designed to charge the lithium-ion battery cells during the balancing mode of the IC. It consists of a PWM waveform generator with variable duty cycle and a driver. This driver can drive an external MOSFET, (or) the optocoupler, (or) an isolation device based on the requirement. During the ON-state of the PWM waveform, the primary side of the Flyback transformer conducts and stores the energy. In the other phase the stored energy in the secondary is transferred to the cell which will be connected to the secondary side of the transformer. The converter always works in discontinuous current mode (DCM).

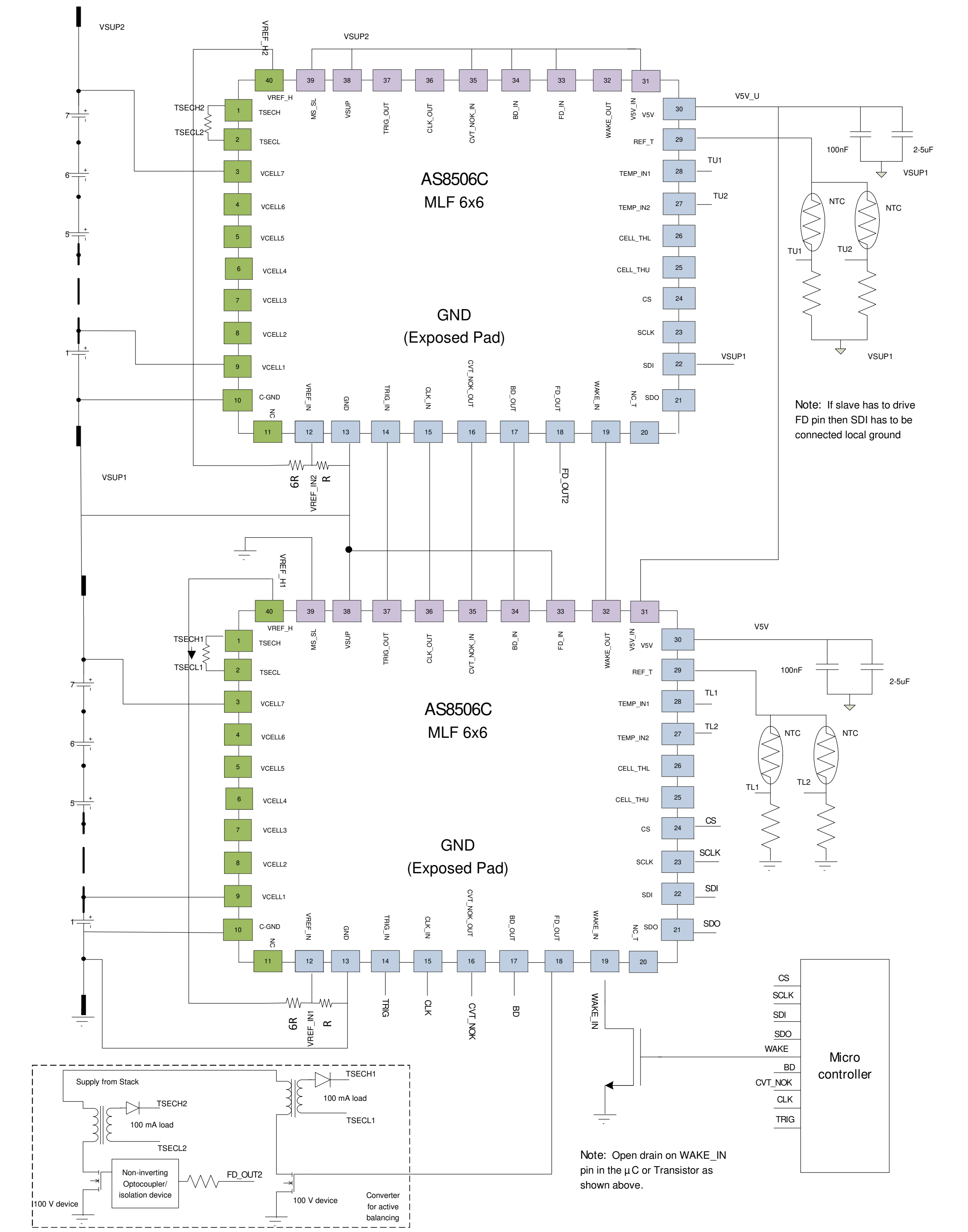
The advantages of this type of control system can be summarized as following:

- High-efficiency even at light load
- Intrinsically stable
- Simplicity

Figure 102:
External Components

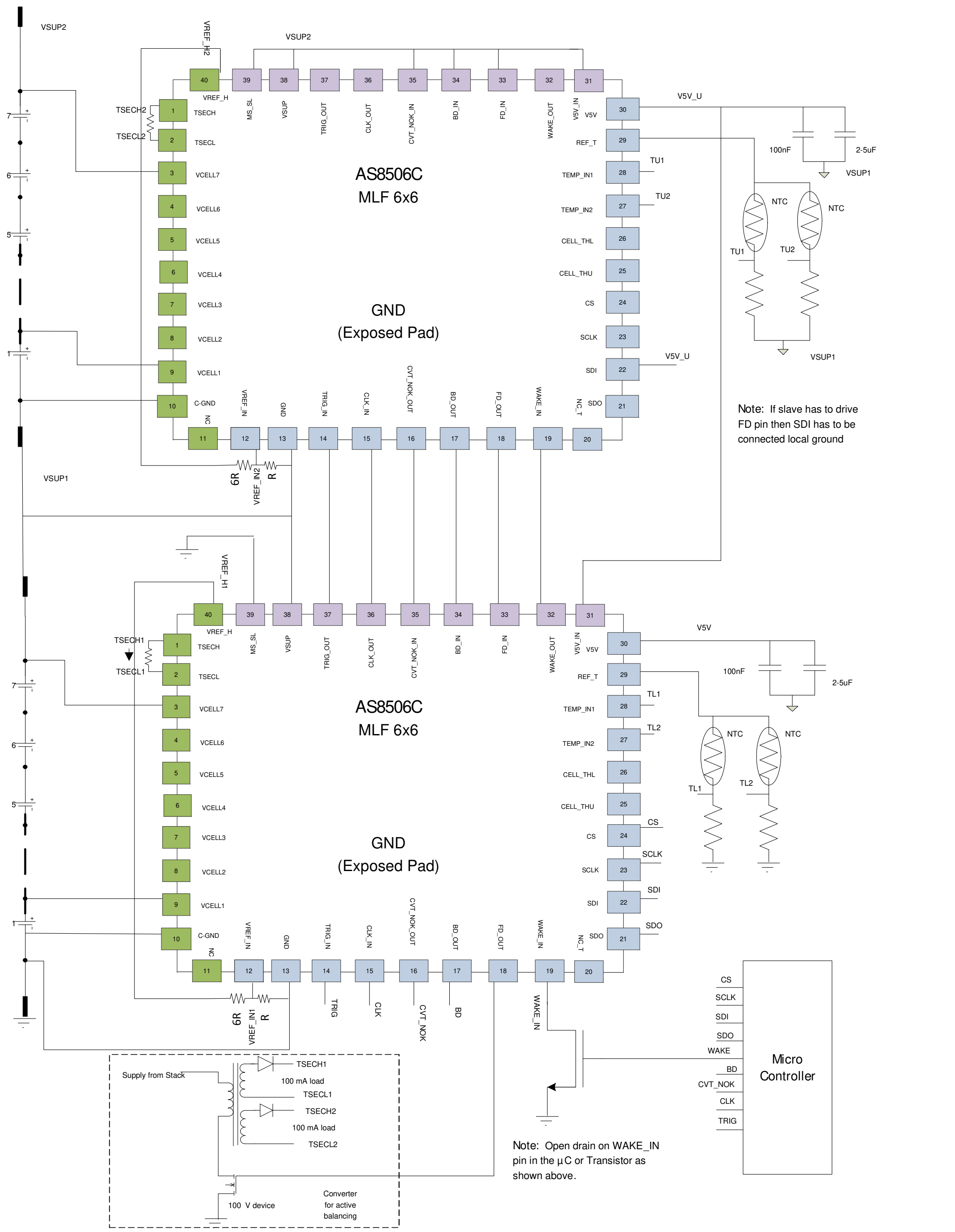
Component	Manufacturer Part Number	Manufacturer
Transformer	WE-FLEX 749196111	WURTH ELECTRONICS
Optocoupler	ACPL-M72T-000E	AVAGO TECHNOLOGIES

Figure 103:
Application with Opto-Coupler/ Isolation Device



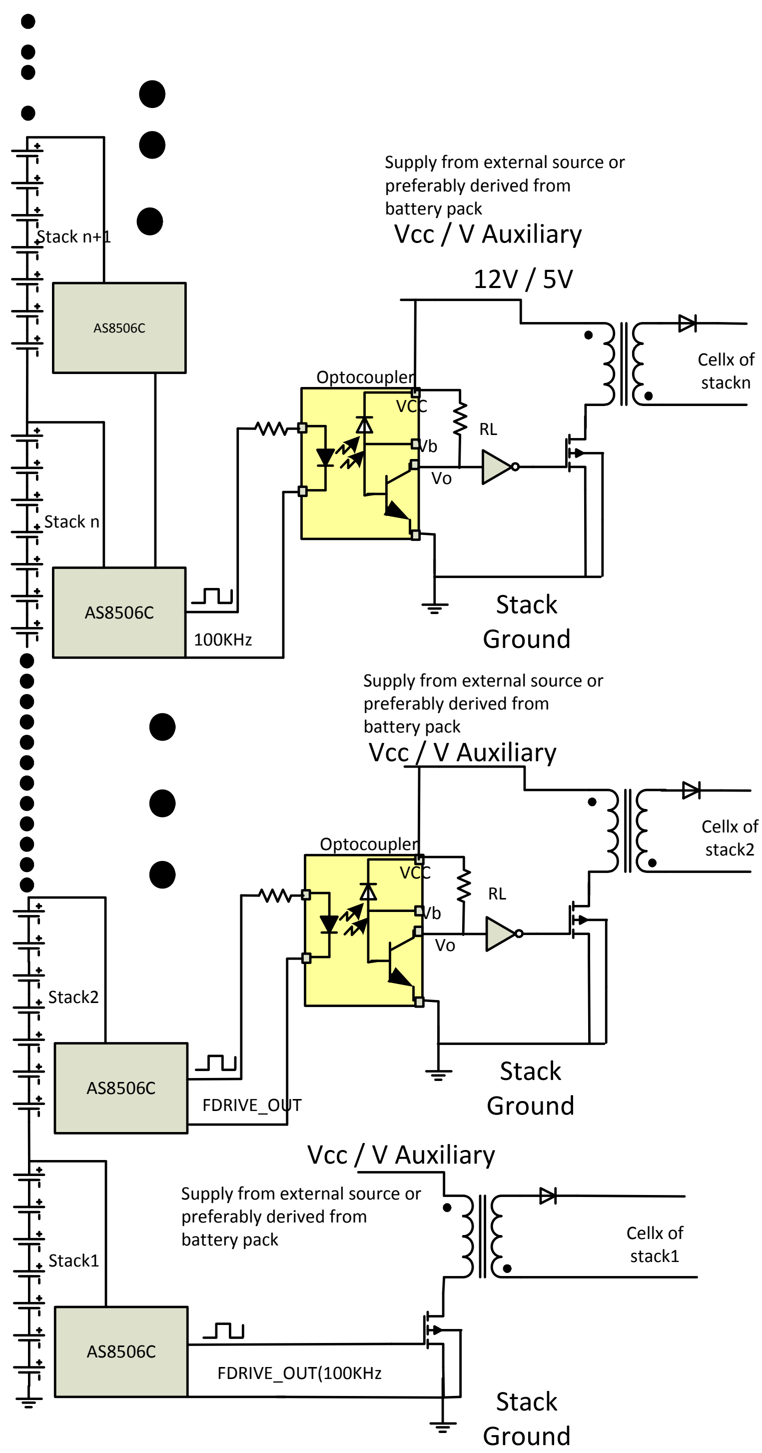
Caution: In the application it's recommended to connect the AS8506C devices stacked first and connect the battery stack from bottom to top in sequence to avoid any possible damage of the system. While removing the battery pack its strictly recommended to remove the battery pack from the top. Removing the battery pack from bottom will damage the system.

Figure 104:
Application Schematic



Caution: In the application it’s recommended to connect the AS8506C devices stacked first and connect the battery stack from bottom to top in sequence to avoid any possible damage of the system. While removing the battery pack its strictly recommended to remove the battery pack from the top. Removing the battery pack from bottom will damage the system.

Figure 105:
Application with Opto-Coupler Device Stackable to Higher Numbers

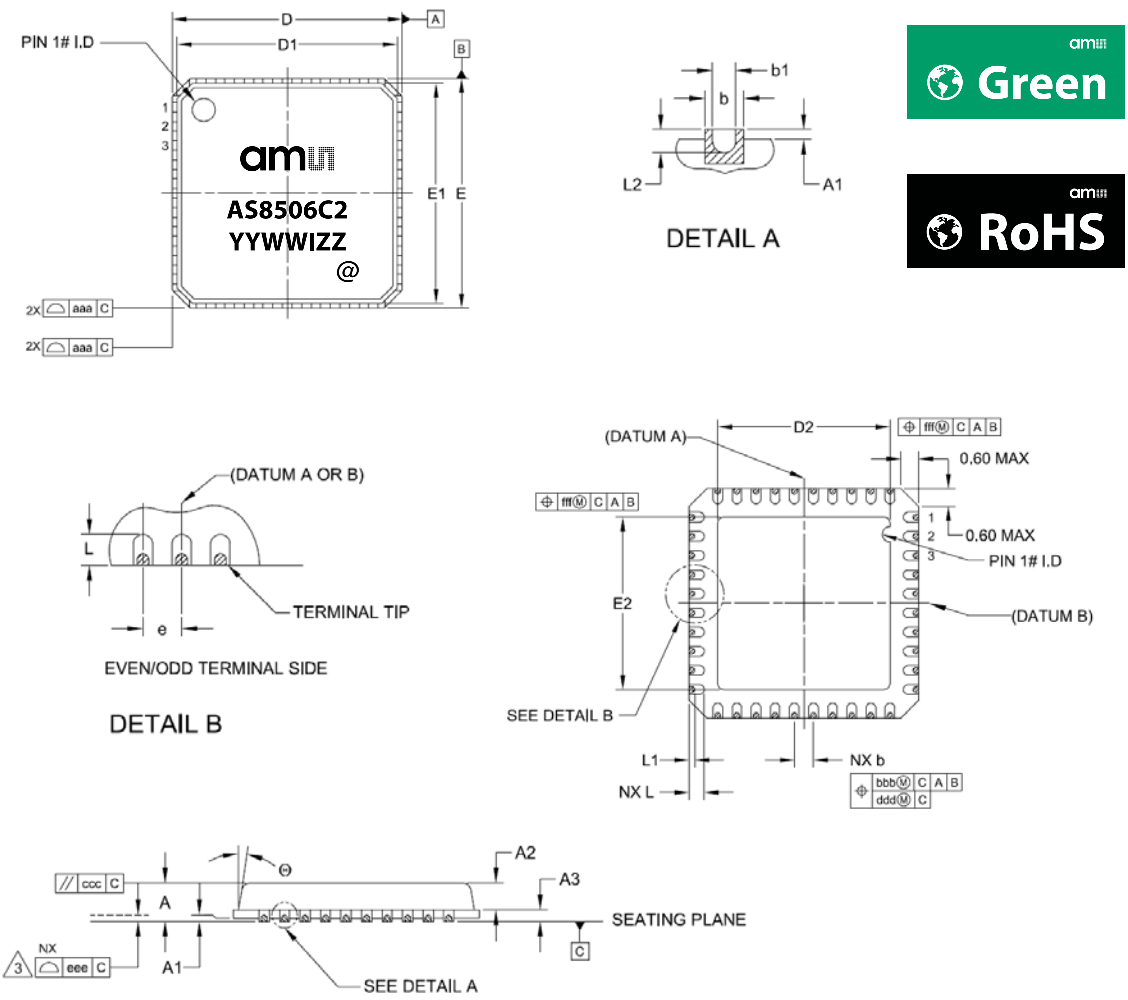


Caution:: In the application it's recommended to connect the AS8506C devices stacked first and connect the battery stack from bottom to top in sequence to avoid any possible damage of the system. While removing the battery pack its strictly recommended to remove the battery pack from the top. Removing the battery pack from bottom will damage the system.

Package Drawings & Markings

The AS8506C device is available in a 40-pin MLF (6x6) package.

Figure 106:
AS8506C Package Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.30	0.40	0.50
L1	0.05	0.15	0.25
L2	0.05	0.10	0.15
Θ	0º	-	14º
b	0.20	0.25	0.30
b1	0.10	0.15	0.20
D		6.00 BSC	
E		6.00 BSC	

Symbol	Min	Nom	Max
e		0.50 BSC	
D1		5.75 BSC	
E1		5.75 BSC	
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		40	

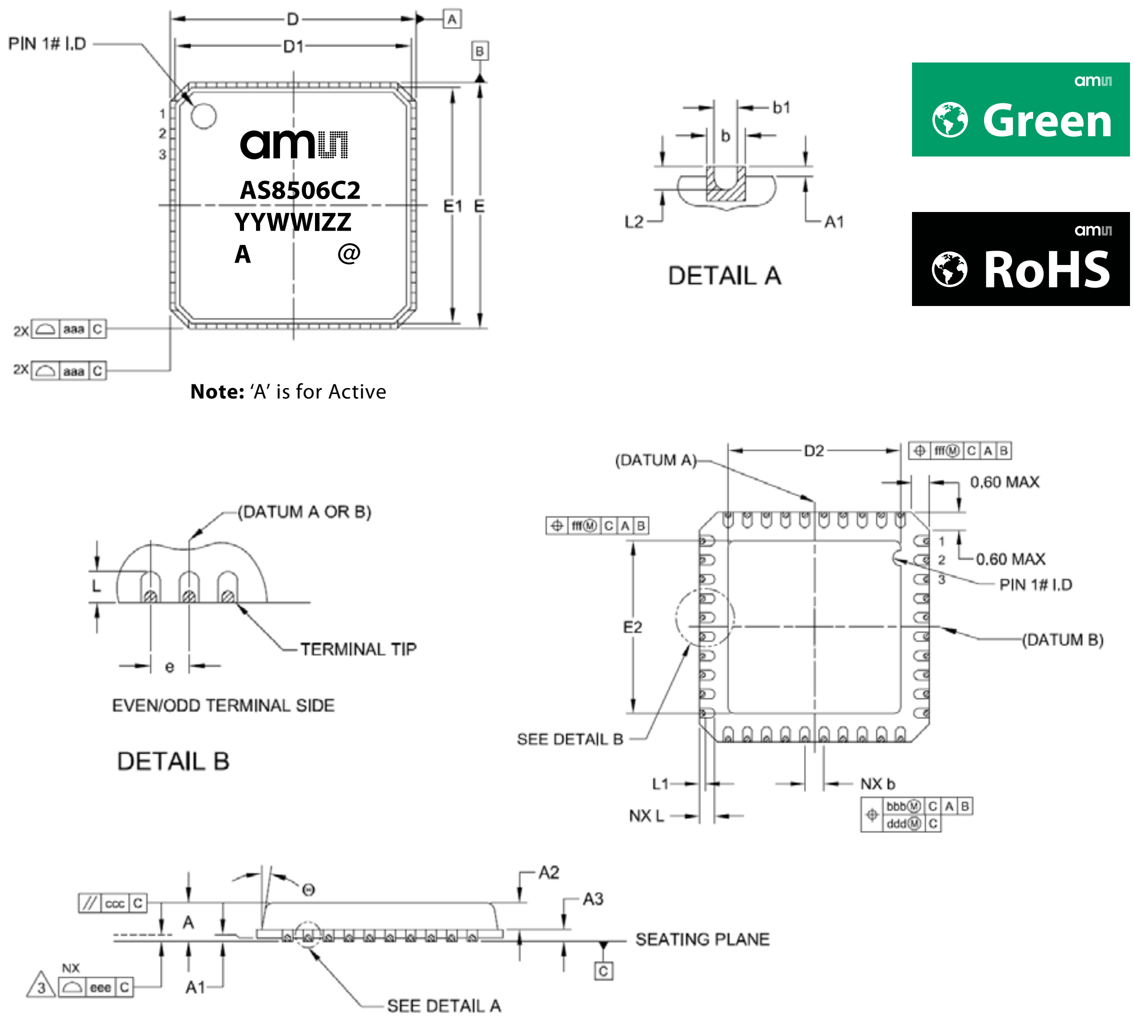
Note(s) and/or Footnote(s):

1. Dimensions and toleranceing conform to ASME Y14.5M. - 1994.
2. All dimensions are in millimeters (angles in degrees).
3. Bilateral coplanarity zone applies to the exposed pad as well as the terminal.
4. Radius on terminal is optional.
5. N is the number of terminals.

Figure 107:
AS8506C Packaging Code YYWWIZZ

YY	WW	I	ZZ	@
Last two digits of the year	Manufacturing week	Plant identifier	Assembly traceability code	Sublot identifier

Figure 108:
AS8506C A Package Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3	0.20 REF		
L	0.30	0.40	0.50
L1	0.05	0.15	0.25
L2	0.05	0.10	0.15
Θ	0º	-	14º
b	0.20	0.25	0.30
b1	0.10	0.15	0.20
D	6.00 BSC		
E	6.00 BSC		

Symbol	Min	Nom	Max
e	0.50 BSC		
D1	5.75 BSC		
E1	5.75 BSC		
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		40	

Note(s) and/or Footnote(s):

1. Dimensions and toleranceing conform to ASME Y14.5M. - 1994.
2. All dimensions are in millimeters (angles in degrees).
3. Bilateral coplanarity zone applies to the exposed pad as well as the terminal.
4. Radius on terminal is optional.
5. N is the number of terminals.

Figure 109:
AS8506C A Packaging Code YYWWIZZ

YY	WW	I	ZZ	@
Last two digits of the year	Manufacturing week	Plant identifier	Assembly traceability code	Sublot identifier

Ordering & Contact Information

The devices are available as the standard products shown in Ordering Information.

Figure 110:
Ordering Information

Ordering Code	Description	Delivery Form	Package	Reel Size
AS8506C-BQFP	Monitor and Balancer IC (1)	Tape and Reel	40-Pin MLF (6x6)	4000
AS8506C-BQFM	Monitor and Balancer IC (1)	Tape and Reel	40-Pin MLF (6x6)	1000
AS8506C-BQFP-A	Monitor and Balancer IC (2)	Tape and Reel	40-Pin MLF (6x6)	4000
AS8506C-BQFM-A	Monitor and Balancer IC (2)	Tape and Reel	40-Pin MLF (6x6)	1000

Note(s) and/or Footnote(s):

1. For Passive balancing.
2. For Active balancing.

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Document Status	Product Status	Definition
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Revision Information

Changes from 1-00 (2014-Jun-23) to current revision 1-02 (2014-Nov-06)	Page
Content was updated to the latest **ams** design	
Added sublot identifier & device marking has been changed from AS8506C to AS8506C2 in Figures 106 & 108	84; 86

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide