16-Bit, 1 MSPS, 8-Channel Data Acquisition System

Enhanced Product

ADAS3022-EP

FEATURES

Ease of use—16-bit, 1 MSPS complete data acquisition system
High impedance, 8-channel input: >500 MΩ
Differential input voltage range: ±24.576 V maximum
High input common-mode rejection: >100 dB
User-programmable input ranges
Channel sequencer with individual channel gains
On-chip 4.096 V reference and buffer
Auxiliary input—direct interface to PulSAR® ADC inputs
No latency or pipeline delay (SAR architecture)
Serial 4-wire, 1.8 V to 5 V SPI-/SPORT-compatible interface
40-Lead LFCSP package (6 mm × 6 mm)

ENHANCED FEATURES

Supports defense and aerospace applications (AQEC standard)
Military temperature range (such as −55°C to +105°C)
Controlled manufacturing baseline
One assembly/test site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Multichannel data acquisition and system monitoring
Process controls
Power line monitoring
Automated test equipment
Instrumentation

GENERAL DESCRIPTION

The ADAS3022-EP is a complete 16-bit, 1 MSPS, successive approximation–based, analog-to-digital data acquisition system that is manufactured on Analog Devices, Inc., proprietary *i*CMOS® high voltage industrial process technology. The device integrates an 8-channel, low leakage multiplexer; a high impedance programmable gain instrumentation amplifier (PGIA) stage with high common-mode rejection; a precision, low drift 4.096 V reference and buffer; and a 16-bit charge redistribution analog-to-digital converter (ADC) with a successive approximation register (SAR) architecture. The ADAS3022-EP can resolve eight single-ended inputs or four fully differential inputs up to ±24.576 V when using ±15 V supplies. In addition, the device can accept the commonly used bipolar differential, bipolar single-ended, pseudo bipolar, or pseudo unipolar input signals, as shown in Table 1, thus enabling the use of almost any direct sensor interface.

The ADAS3022-EP simplifies design challenges by eliminating signal buffering, level shifting, amplification/attenuation, common-mode rejection, settling time, and any other analog signal conditioning challenge while allowing a smaller form factor, faster time to market, and lower cost.

Additional application and technical information can be found in the ADAS3022 data sheet.

Table 1. Typical Input Range Selection

Signal (V)	Input Range, V_{IN} (V)
Differential	
±1	±1.28
±2.5	±2.56
±5	±5.12
±10	±10.24
Single Ended	
0 to 1	±1.28
0 to 2.5	±2.56
0 to 5	±5.12
0 to 10	±10.24

Rev. 0 Document Feedback

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REVISION HISTORY

6/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

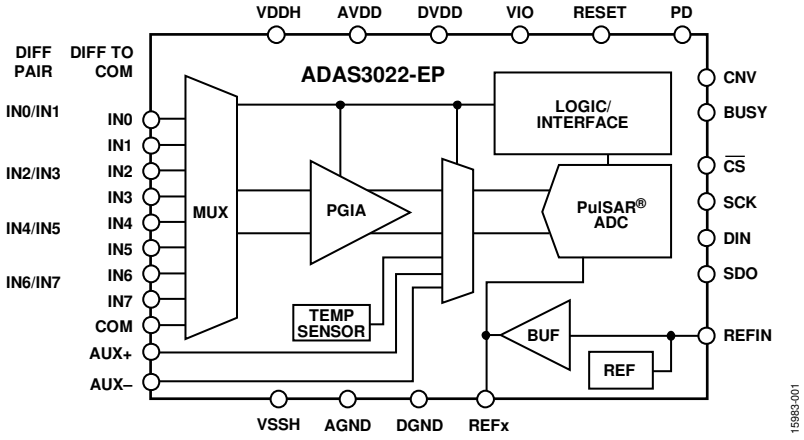


Figure 1.

SPECIFICATIONS

VDDH = 15 V ± 5%, VSSH = −15 V ± 5%, AVDD = DVDD = 5 V ± 5%, VIO = 1.8 V to AVDD, internal voltage reference (V_{REF}) = 4.096 V, sampling frequency (f_S) = 1 MSPS unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
RESOLUTION		16			Bits
ANALOG INPUTS—IN[7:0], COM					
Operating Input Voltage Range	V_{IN}	−VSSH + 2.5		VDDH − 2.5	V
Differential Input Voltage Range, V_{IN}	$V_{IN+} - V_{IN-}$				
	PGIA gain = 0.16, V_{IN} = 49.15 V p-p	$-6 \times V_{REF}$		$+6 \times V_{REF}$	V
	PGIA gain = 0.2, V_{IN} = 40.96 V p-p	$-5 \times V_{REF}$		$+5 \times V_{REF}$	V
	PGIA gain = 0.4, V_{IN} = 20.48 V p-p	$-2.5 \times V_{REF}$		$+2.5 \times V_{REF}$	V
	PGIA gain = 0.8, V_{IN} = 10.24 V p-p	$-1.25 \times V_{REF}$		$+1.25 \times V_{REF}$	V
	PGIA gain = 1.6, V_{IN} = 5.12 V p-p	$-0.625 \times V_{REF}$		$+0.625 \times V_{REF}$	V
	PGIA gain = 3.2, V_{IN} = 2.56 V p-p	$-0.3125 \times V_{REF}$		$+0.3125 \times V_{REF}$	V
	PGIA gain = 6.4, V_{IN} = 1.28 V p-p	$-0.1563 \times V_{REF}$		$+0.1563 \times V_{REF}$	V
Input Impedance, Z_{IN}		500			MΩ
Channel Off Leakage			±0.6		nA
Channel On Leakage			±0.02		nA
Common-Mode Voltage Range (V_{CM})[2]	V_{IN+}, V_{IN-}; full-scale differential inputs				
	PGIA gain = 0.4	−5.12		+5.12	V
	PGIA gain = 0.8	−7.68		+7.68	V
	PGIA gain = 1.6	−8.96		+8.96	V
	PGIA gain = 3.2	−9.60		+9.60	V
	PGIA gain = 6.4	−9.92		+9.92	V
ANALOG INPUTS—AUX+, AUX−					
Differential Input Voltage Range		$-V_{REF}$		$+V_{REF}$	V
THROUGHPUT					
Conversion Rate	One channel and one pair	0		1000	kSPS
	Two channels and two pairs	0		500	kSPS
	Four channels and four pairs	0		250	kSPS
	Eight channels	0		125	kSPS
Transient Response	Full-scale step			520	ns
DC ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error	PGIA gain = 0.16, 0.2, 0.4, 0.8, and 1.6	−2	±0.6	+2	LSB
	PGIA gain = 3.2	−3	±1.0	+3	LSB
	PGIA gain = 6.4	−5	±1.5	+5	LSB
Differential Linearity Error	PGIA gain = 0.16, 0.2, 0.4, 0.8, and 1.6	−0.9	±0.6	+1.0	LSB
	PGIA gain = 3.2	−0.9	±0.75	+1.25	LSB
	PGIA gain = 6.4	−0.9	±0.75	+1.25	LSB
Transition Noise	External reference				
	PGIA gain = 0.16, 0.2, 0.4, 0.8, and 1.6		5		LSB
	PGIA gain = 3.2		7		LSB
	PGIA gain = 6.4		11		LSB
Gain Error	External reference, all PGIA gains, T_A = 25°C	−9		+9	LSB
Gain Error Temperature Drift	External reference, all PGIA gains			0.1	ppm/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
Offset Error	External reference, T_A = 25°C				
	PGIA gain = 0.16, 0.2, 0.4, and 0.8	−3.0	+0.2	+3.0	LSB
	PGIA gain = 1.6	−4.0	+0.2	+4.0	LSB
	PGIA gain = 3.2	−7.5	+0.2	+7.5	LSB
	PGIA gain = 6.4	−12.5	+0.2	+12.5	LSB
Offset Error Temperature Drift	External reference				
	PGIA gain = 0.16, 0.2, 0.4, and 0.8		0.1	0.5	ppm/°C
	PGIA gain = 1.6		0.2	1.0	ppm/°C
	PGIA gain = 3.2		0.4	2.0	ppm/°C
	PGIA gain = 6.4		0.8	4.0	ppm/°C
Total Unadjusted Error	External reference, ambient temperature (T_A) = 25°C				
	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6, and 3.2	−9		+9	LSB
	PGIA gain = 6.4	−15		+15	LSB
AC ACCURACY[3]					
Signal-to-Noise Ratio (SNR)	f_{IN} = 10 kHz				
	PGIA gain = 0.16	90.0	91.5		dB
	PGIA gain = 0.2	90.0	91.5		dB
	PGIA gain = 0.4	89.5	91.5		dB
	PGIA gain = 0.8	89.0	91.0		dB
	PGIA gain = 1.6	88.0	89.7		dB
	PGIA gain = 3.2	86.0	86.8		dB
	PGIA gain = 6.4	83.0	84.5		dB
Signal-to-Noise-and-Distortion (SINAD)	Input frequency (f_{IN}) = 10 kHz				
	PGIA gain = 0.16	88.0	90.0		dB
	PGIA gain = 0.2	88.0	90.0		dB
	PGIA gain = 0.4	88.5	91.0		dB
	PGIA gain = 0.8	88.5	90.5		dB
	PGIA gain = 1.6	87.5	89.5		dB
	PGIA gain = 3.2	85.5	86.5		dB
	PGIA gain = 6.4	82.5	84.0		dB
Dynamic Range	f_{IN} = 10 kHz, −60 dB input				
	PGIA gain = 0.16	91.0	92.0		dB
	PGIA gain = 0.2	91.0	92.0		dB
	PGIA gain = 0.4	90.5	91.5		dB
	PGIA gain = 0.8	90.0	91.0		dB
	PGIA gain = 1.6	89.0	90.0		dB
	PGIA gain = 3.2	86.0	87.0		dB
	PGIA gain = 6.4	83.5	85.0		dB
Total Harmonic Distortion (THD)	f_{IN} = 10 kHz, all PGIA gains		−100		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 10 kHz, all PGIA gains		101		dB
Channel to Channel Crosstalk	f_{IN} = 10 kHz, all channels inactive		−120		dB
Common-Mode Rejection Ratio (CMRR)	f_{IN} = 2 kHz				
	PGIA gain = 0.16, 0.2, 0.4, and 0.8	90.0	110.0		dB
	PGIA gain = 1.6	90.0	105.0		dB
	PGIA gain = 3.2	90.0	98.0		dB
	PGIA gain = 6.4	90.0	98.0		dB
−3 dB Input Bandwidth	−40 dBFS		8		MHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
AUXILIARY ADC INPUT CHANNEL					
DC Accuracy	External reference				
Integral Nonlinearity Error		−1.5	±0.5	+1.5	LSB
Differential Nonlinearity Error		−0.8	±0.6	+1.0	LSB
Gain Error		−2.5	±0.2	+2.5	LSB
Offset Error		−5	±0.2	+5	LSB
AC Performance	Internal reference				
SNR		90.0	93.0		dB
SINAD		89.5	92.5		dB
THD			−105		dB
SFDR			110		dB
INTERNAL REFERENCE					
REF1 and REF2 Output Voltage	T_A = 25°C	4.088	4.096	4.104	V
REF1 and REF2 Output Current	T_A = 25°C		250		µA
REF1 and REF2 Temperature Drift	REFEN = 1		±5		ppm/°C
	REFEN = 0		±1		ppm/°C
REF1 and REF2 Line Regulation	AVDD = 5 V ± 5%				
Internal Reference			20		µV/V
Buffer Only			4		µV/V
REFIN Output Voltage[4]	T_A = 25°C	2.495	2.500	2.505	V
Turn-On Settling Time	C_{REFIN}, C_{REF1}, C_{REF2} = 10 µF and 0.1 µF		100		ms
EXTERNAL REFERENCE					
Voltage Range	REFx input	4.000	4.096	4.104	V
	REFIN input (buffered)		2.5	2.505	V
Current Drain	V_{REF} = 4.096 V		100		µA
TEMPERATURE SENSOR					
Output Voltage	T_A = 25 °C		275		mV
Temperature Sensitivity			800		µV/°C
DIGITAL INPUTS					
Logic Levels					
Input Voltage Low, V_{IL}	VIO > 3 V	−0.3		+0.3 × VIO	V
	VIO ≤ 3 V	−0.3		+0.1 × VIO	V
Input Voltage High, V_{IH}	VIO > 3 V	0.7 × VIO		VIO + 0.3	V
	VIO ≤ 3 V	0.9 × VIO		VIO + 0.3	V
Input Low Current, I_{IL}		−1		+1	µA
Input High Current, I_{IH}		−1		+1	µA
DIGITAL OUTPUTS[5]					
Data Format			Twos complement		
Output Low Voltage, V_{OL}	I_{SINK} = +500 µA			0.4	V
Output High Voltage, V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES	PD = 0				
VIO		1.8		AVDD + 0.3	V
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
VDDH[6]	VDDH > input voltage + 2.5 V	14.25	15	15.75	V
VSSH[6]	VSSH < input voltage − 2.5 V	−15.75	−15	−14.25	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
VDDH Capacitance, I_{VDDH}	PGIA gain = 0.16		3.0	3.5	mA
	PGIA gain = 0.2		3.0	3.5	mA
	PGIA gain = 0.4		3.5	4.0	mA
	PGIA gain = 0.8		5.0	5.5	mA
	PGIA gain = 1.6		8.5	9.5	mA
	PGIA gain = 3.2		15.5	17.5	mA
	PGIA gain = 6.4		15.5	17.5	mA
	All PGIA gains, PD = 1		100		µA
Current at VSSH Supply, I_{VSSH}	PGIA gain = 0.16	−3.0	−2.5		mA
	PGIA gain = 0.2	−3.0	−2.5		mA
	PGIA gain = 0.4	−3.5	−3.0		mA
	PGIA gain = 0.8	−5.5	−4.5		mA
	PGIA gain = 1.6	−9.5	−8.0		mA
	PGIA gain = 3.2	−17.5	−15		mA
	PGIA gain = 6.4	−17.5	−15		mA
	All PGIA gains, PD = 1		10		µA
Current at AVDD, I_{AVDD}	PGIA gain = 6.4, reference buffer enabled		18	21.0	mA
	All other PGIA gains, reference buffer enabled		16	19.0	mA
	PGIA gain = 6.4, reference buffer disabled		14	17.5	mA
	All other PGIA gains, reference buffer disabled		12	16.0	mA
	All PGIA gains, PD = 1		100		µA
Current at DVDD, I_{DVDD}	All PGIA gains, PD = 0		2.5	3.5	mA
	All PGIA gains, PD = 1		10		µA
Current at VIO, I_{VIO}	VIO = 3.3 V, PD = 0		0.30	1.2	mA
	PD = 1		10		µA
Power Supply Sensitivity					
At T_A = 25°C	External reference				
	PGIA gain = 0.16, 0.2, 0.4, and 0.8; VDDH/VSSH ± 5%		±0.5		LSB
	PGIA gain = 3.2, VDDH/VSSH ± 5%		±1.0		LSB
	PGIA gain = 6.4, VDDH/VSSH ± 5%		±2.0		LSB
	PGIA gain = 0.16, AVDD/DVDD ± 5%		±0.6		LSB
	PGIA gain = 0.2, AVDD/DVDD ± 5%		±0.8		LSB
	PGIA gain = 0.4, AVDD/DVDD ± 5%		±1.0		LSB
	PGIA gain = 0.8, AVDD/DVDD ± 5%		±1.5		LSB
	PGIA gain = 1.6, AVDD/DVDD ± 5%		±2.0		LSB
	PGIA gain = 3.2, AVDD/DVDD ± 5%		±3.5		LSB
	PGIA gain = 6.4, AVDD/DVDD ± 5%		±7.0		LSB
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−55		+105	°C

[1] LSB means least significant bit and changes depending on the voltage range.
[2] The common-mode voltage (V_{CM}) for a PGIA gain of 0.16 or 0.2 is 0 V.
[3] All ac accuracy specifications expressed in decibels are referred to a full-scale range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise noted.
[4] This is the output from the internal band gap reference.
[5] There is no pipeline delay. Conversion results are available immediately after a conversion is complete.
[6] The differential input common-mode voltage (V_{CM}) range changes according to the maximum input range selected and the high voltage power supplies (VDDH and VSSH). Note that the specified operating input voltage of any input pin requires 2.5 V of headroom from the VDDH and VSSH supplies; therefore, (VSSH + 2.5 V) ≤ INx/COM ≤ (VDDH − 2.5 V).

TIMING SPECIFICATIONS

VDDH = 15 V ± 5%, VSSH = −15 V ± 5%, AVDD = DVDD = 5 V ± 5%, VIO = 1.8 V to AVDD, internal reference, V_{REF} = 4.096 V, f_S = 1 MSPS unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions	t_{CYC}				
Warp Mode,[1] CMS = 0		1		1000	µs
Normal Mode (Default), CMS = 1		1.1			µs
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}				
Warp Mode, CMS = 0			825		ns
Normal Mode (Default), CMS = 1			925	1000	ns
Auxiliary ADC Input Channel Acquisition Time	t_{ACQ}	600			ns
CNV Pulse Width	t_{CH}	10			ns
CNV High to Hold Time (Aperture Delay)	t_{AD}		2		ns
CNV High to Busy Delay	t_{CBD}			520	ns
Safe Data Access Time During Conversion	t_{DDC}			500	ns
Quiet Conversion Time (BUSY High)	t_{QUIET}				
Warp Mode, CMS = 0				400	ns
Normal Mode (Default), CMS = 1				500	ns
Data Access During Quiet Conversion Time	t_{DDCA}				
Warp Mode, CMS = 0				200	ns
Normal Mode (Default), CMS = 1				300	ns
SCK Period	t_{SCK}	15			ns
SCK Low Time	t_{SCKL}	5			ns
SCK High Time	t_{SCKH}	5			ns
SCK Falling Edge to Data Valid	t_{SDOH}	4			ns
SCK Falling Edge to Data Valid Delay	t_{SDOD}				
VIO > 4.5 V				12	ns
VIO > 3.0 V				18	ns
VIO > 2.7 V				24	ns
VIO > 2.3 V				25	ns
VIO > 1.8 V				37	ns
$\overline{CS}$/RESET/PD Low to SDO	t_{EN}				
VIO > 4.5 V				15	ns
VIO > 3.0 V				16	ns
VIO > 2.7 V				18	ns
VIO > 2.3 V				23	ns
VIO > 1.8 V				28	ns
$\overline{CS}$/RESET/PD High to SDO High Impedance	t_{DIS}			25	ns
DIN Valid Setup Time from SCK Rising Edge	t_{DINS}	4			ns
DIN Valid Hold Time from SCK Rising Edge	t_{DINH}	4			ns
CNV Rising to $\overline{CS}$	t_{CCS}	5			ns
RESET/PD High Pulse	t_{RH}	5			ns

[1] Exceeding the maximum time has an effect on the accuracy of the conversion.

Timing Diagrams

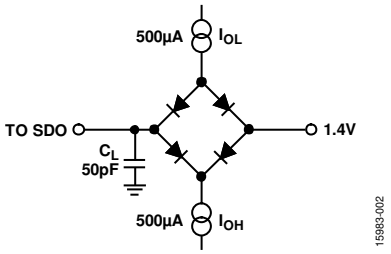


Figure 2. Load Circuit for Digital Interface Timing

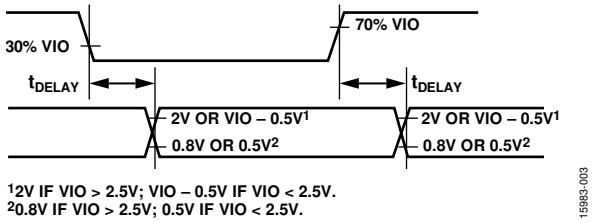
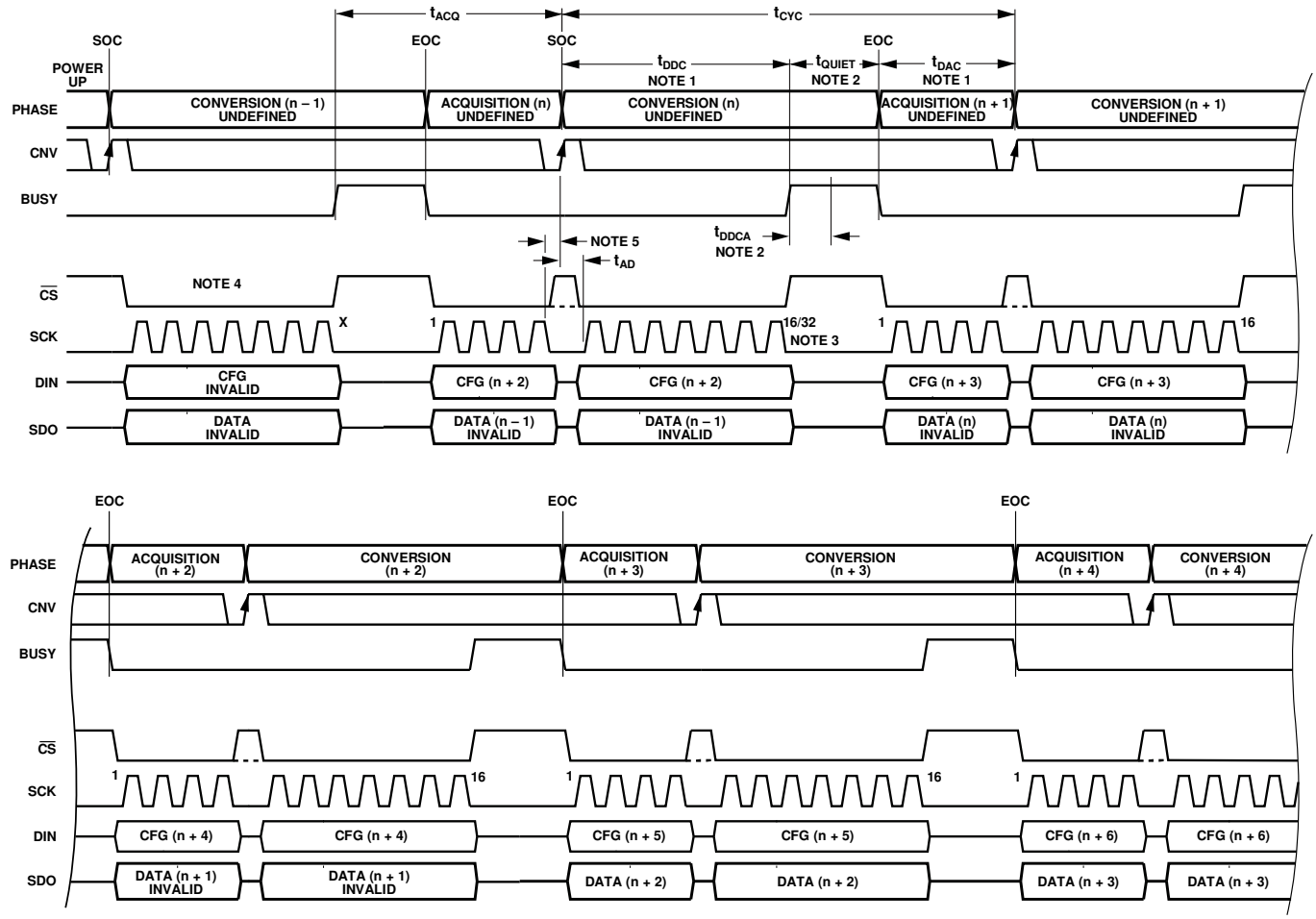


Figure 3. Voltage Levels for Timing



NOTES
1. DATA ACCESS CAN OCCUR DURING A CONVERSION (t_{DDC}), AFTER A CONVERSION (t_{DAC}), OR BOTH DURING AND AFTER A CONVERSION. THE CONVERSION RESULT AND THE CFG REGISTER ARE UPDATED AT THE END OF A CONVERSION (EOC).
2. DATA ACCESS CAN ALSO OCCUR UP TO t_{DDCA} WHILE BUSY IS ACTIVE (SEE THE ADAS3022 DATA SHEET FOR DETAILS). ALL OF THE BUSY TIME CAN BE USED TO ACQUIRE DATA.
3. A TOTAL OF 16 SCK FALLING EDGES IS REQUIRED FOR A CONVERSION RESULT. AN ADDITIONAL 16 EDGES ARE REQUIRED TO READ BACK THE CFG RESULT ASSOCIATED WITH THE CURRENT CONVERSION.
4. $\overline{CS}$ CAN BE HELD LOW OR CONNECTED TO CNV. $\overline{CS}$ WITH FULL INDEPENDENT CONTROL IS SHOWN IN THIS FIGURE.
5. FOR OPTIMAL PERFORMANCE, DATA ACCESS SHOULD NOT OCCUR DURING THE SAMPLING EDGE. A MINIMUM TIME OF THE APERTURE DELAY (t_{AD}) SHOULD ELAPSE PRIOR TO DATA ACCESS.

Figure 4. General Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs/Outputs	
INx, COM to AGND	VSSH − 0.3 V to VDDH + 0.3 V
AUX+, AUX− to AGND	−0.3 V to AVDD + 0.3 V
REFx to AGND	AGND − 0.3 V to AVDD + 0.3 V
REFIN to AGND	AGND − 0.3 V to +2.7 V
REFN to AGND	±0.3 V
Ground Voltage Differences	
AGND, RGND, DGND	±0.3 V
Supply Voltages	
VDDH to AGND	−0.3 V to +16.5 V
VSSH to AGND	+0.3 V to −16.5 V
AVDD, DVDD, VIO to AGND	−0.3 V to +7 V
ACAP, DCAP, RCAP to GND	−0.3 V to +2.7 V
Digital Inputs/Outputs	
CNV, DIN, SCK, RESET, PD, $\overline{CS}$ to DGND	−0.3 V to VIO + 0.3 V
SDO, BUSY to DGND	−0.3 V to VIO + 0.3 V
Internal Power Dissipation	2 W
Junction Temperature	125°C
Storage Temperature Range	−65°C to +125°C
Thermal Impedance	
θ_{JA}	44.1°C/W
θ_{JC}	0.28°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

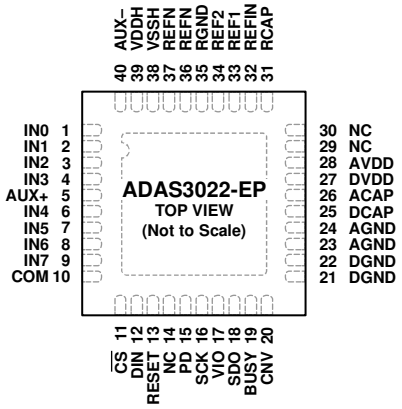


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1 to 4	IN0 to IN3	AI	Input Channel 0 to Input Channel 3.
5	AUX+	AI	Auxiliary Input Channel Positive Input.
6 to 9	IN4 to IN7	AI	Input Channel 4 to Input Channel 7.
10	COM	AI	IN[7:0] Common Channel Input. The IN[7:0] input channels can be referenced to a common point. The maximum voltage on this pin is ±10.24 V for all PGIA gains except for a PGIA gain of 0.16, in which case, the maximum voltage on this pin is ±12.228 V. AUX+ and AUX− are not referenced to COM.
11	$\overline{CS}$	DI	Chip Select. Active low signal. Enables the digital interface for writing and reading data. Use this pin when sharing the serial bus. For a dedicated ADAS3022-EP serial interface, $\overline{CS}$ can be tied to DGND or CNV to simplify the interface.
12	DIN	DI	Data Input. Serial data input used for writing the 16-bit configuration word (CFG) that is latched on SCK rising edges. CFG is an internal register that is updated on the rising edge of the end of a conversion, which is the falling edge of BUSY. The configuration register can be written to during and after a conversion.
13	RESET	DI	Asynchronous Reset. A low to high transition resets the ADAS3022-EP. The current conversion, if active, is aborted and CFG is reset to the default state.
14, 29, 30	NC	N/A	No Connect. This pin is not connected internally.
15	PD	DI	Power-Down. A low to high transition powers down the ADAS3022-EP, minimizing the bias current. Note that this pin must be held high until the user is ready to power on the device; after powering on the device, the user must wait 100 ms until the reference is enabled and then wait for the completion of two dummy conversions before the device is ready to convert.
16	SCK	DI	Serial Clock Input. The DIN and SDO data sent to and from the ADAS3022-EP are synchronized with SCK.
17	VIO	P	Digital Interface Supply. Nominally, this supply is at the same voltage as the supply of the host interface: 1.8 V, 2.5 V, 3.3 V, or 5 V.
18	SDO	DO	Serial Data Output. The conversion result is output on this pin and is synchronized to SCK falling edges. The conversion result is output in twos complement format.
19	BUSY	DO	Busy Output. An active high signal on this pin indicates that a conversion is in process. Reading or writing data during the quiet conversion phase (t_{QUIET}) may cause incorrect bit decisions.
20	CNV	DI	Convert Input. A conversion is initiated on the rising edge of this pin.
21, 22	DGND	P	Digital Ground. Connect these pins to the system digital ground plane.
23, 24	AGND	P	Analog Ground. Connect these pins to the system analog ground plane.
25	DCAP	P	Internal 2.5 V Digital Regulator Output. Decouple this internally regulated output using a 10 µF capacitor and a 0.1 µF local capacitor.
26	ACAP	P	Internal 2.5 V Analog Regulator Output. This regulator supplies power to the internal ADC core and all of the supporting analog circuits with the exception of the internal reference. Decouple this internally regulated output using a 10 µF capacitor and a 0.1 µF local capacitor.

Pin No.	Mnemonic	Type[1]	Description
27	DVDD	P	Digital 5 V Supply. Decouple this supply using a 10 µF capacitor and a 0.1 µF local capacitor.
28	AVDD	P	Analog 5 V Supply. Decouple this supply using a 10 µF capacitor and a 0.1 µF local capacitor.
31	RCAP	P	Internal 2.5 V Analog Regulator Output. This regulator supplies power to the internal reference. Decouple this pin using a 1 µF capacitor connected to RCAP and a 0.1 µF local capacitor.
32	REFIN	AI/O	Internal 2.5 V Band Gap Reference Output, Reference Buffer Input, or Reference Power-Down Input. See the Voltage Reference Input/Output section of the ADAS3022 data sheet for more information.
33, 34	REF1, REF2	AI/O	Reference Input/Output. Regardless of the reference method, these pins need individual decoupling using external 10 µF ceramic capacitors connected as close to REF1, REF2, and REFN as possible. REF1 and REF2 must be tied together externally.
35	RGND	P	Reference Supply Ground. Connect this pin to the system analog ground plane.
36, 37	REFN	P	Reference Input/Output Ground. Connect the 10 µF capacitors on REF1 and REF2 to these pins, and connect these pins to the system analog ground plane.
38	VSSH	P	High Voltage Analog Negative Supply. Nominally, the supply of this pin should be −15 V. Decouple this pin using a 10 µF capacitor and a 0.1 µF local capacitor.
39	VDDH	P	High Voltage Analog Positive Supply. Nominally, the supply of this pin should be +15 V. Decouple this pin using a 10 µF capacitor and a 0.1 µF local capacitor.
40	AUX−	AI	Auxiliary Input Channel Negative Input.
	EPAD		Exposed Paddle. Connect the exposed paddle to VSSH.

[1]AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, N/A = not applicable, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDDH = 15 V, VSSH = −15 V, AVDD = DVDD = 5 V, VIO = 1.8 V to AVDD, unless otherwise noted.

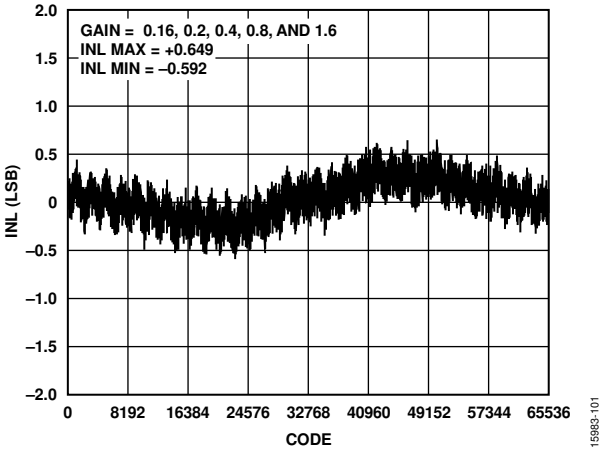


Figure 6. Integral Nonlinearity (INL) vs. Code, PGIA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

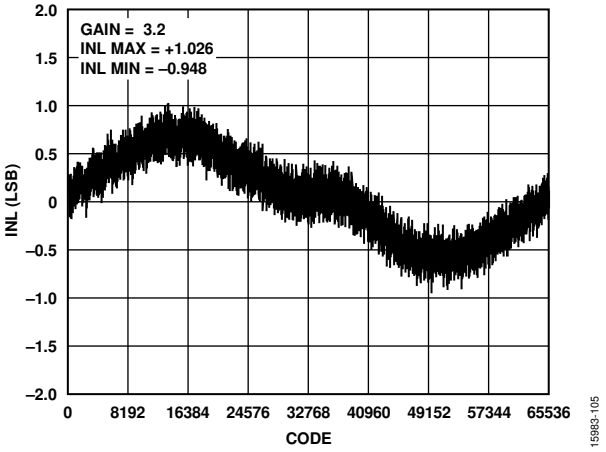


Figure 7. Integral Nonlinearity vs. Code, PGIA Gain = 3.2

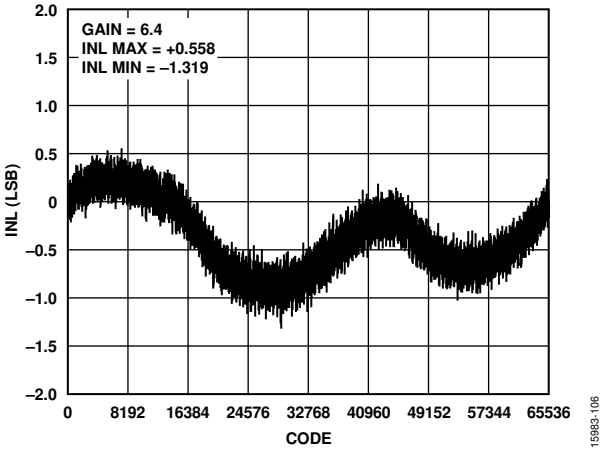


Figure 8. Integral Nonlinearity vs. Code, PGIA Gain = 6.4

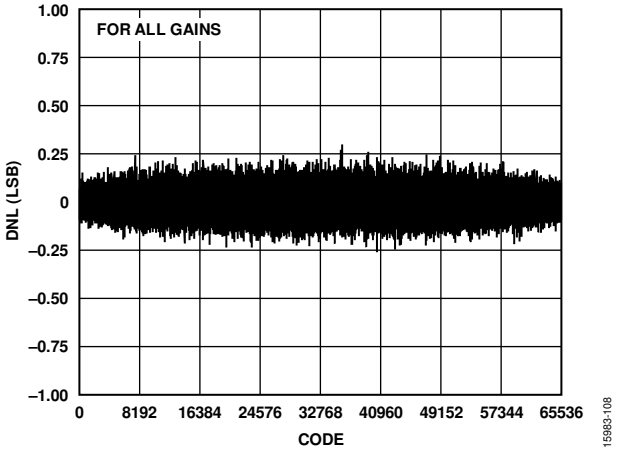


Figure 9. Differential Nonlinearity (DNL) vs. Code for All PGIA Gains

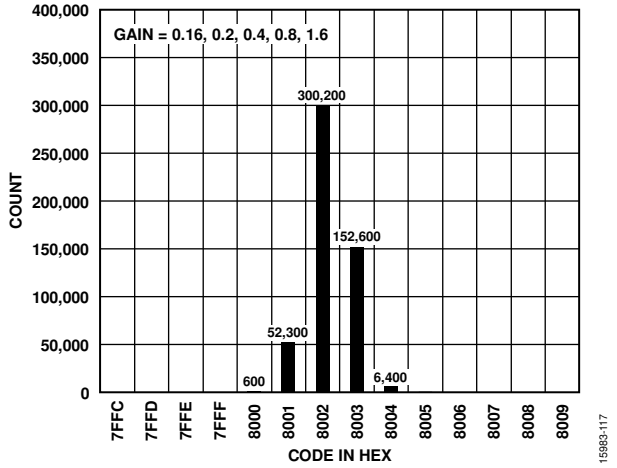


Figure 10. Histogram of a DC Input at Code Center, PGIA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

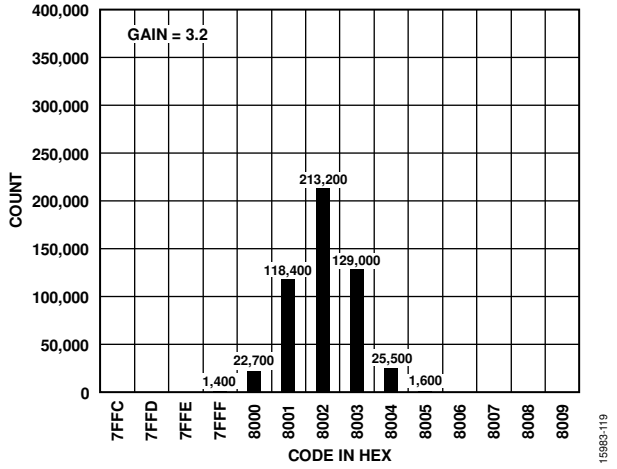


Figure 11. Histogram of a DC Input at Code Center, PGIA Gain = 3.2

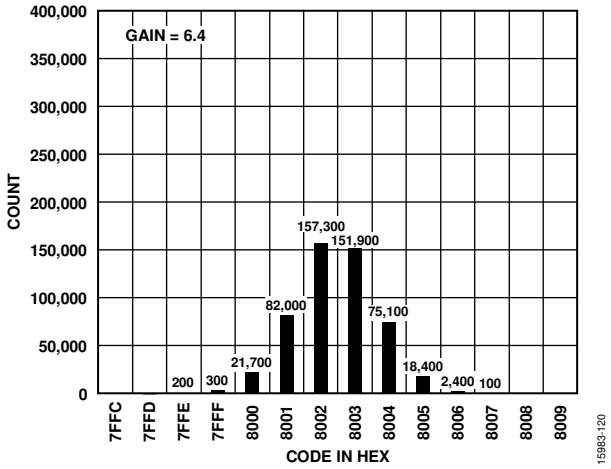


Figure 12. Histogram of a DC Input at Code Center, PGIA Gain = 6.4

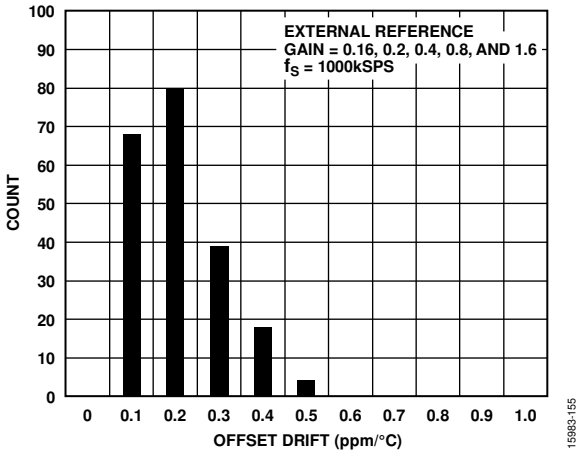


Figure 13. Offset Drift, PGIA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

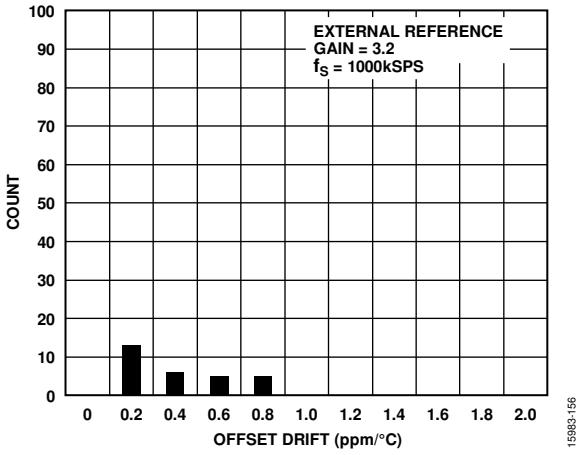


Figure 14. Offset Drift, PGIA Gain = 3.2

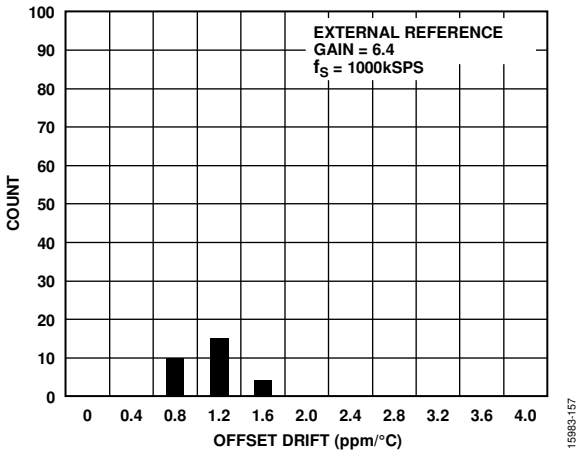


Figure 15. Offset Drift, PGIA Gain = 6.4

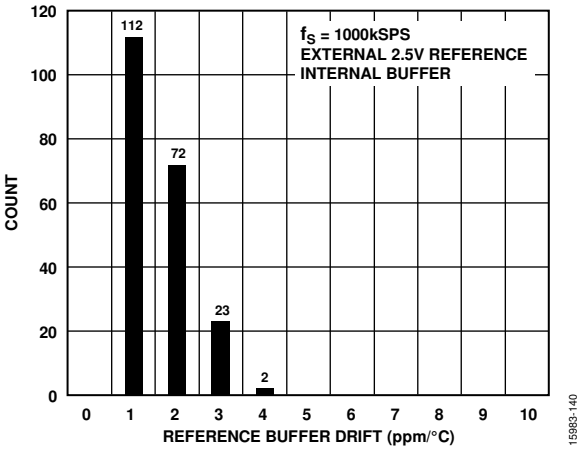


Figure 16. Reference Buffer Drift, External 2.5 V Reference

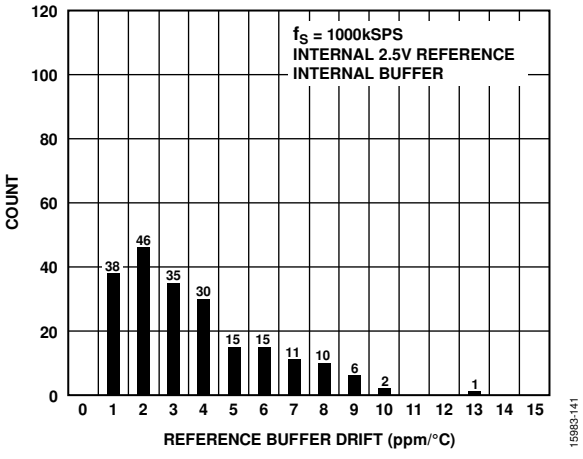


Figure 17. Reference Buffer Drift, Internal 2.5 V Reference

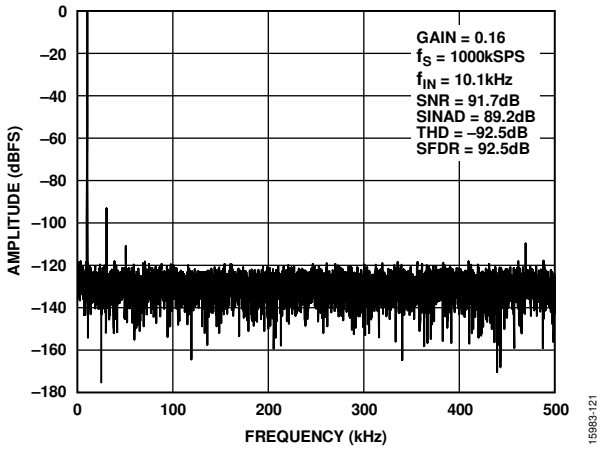


Figure 18. 10 kHz FFT, PGIA Gain = 0.16

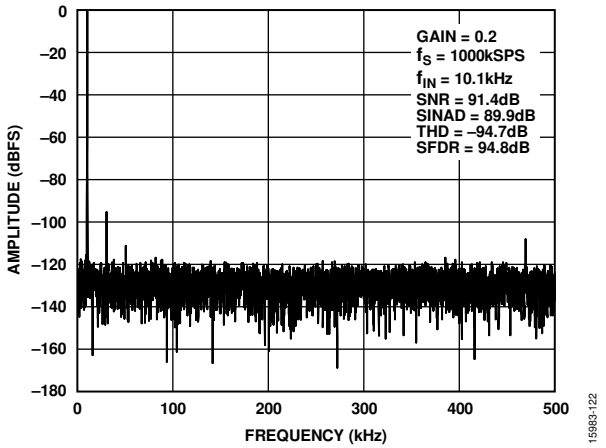


Figure 19. 10 kHz FFT, PGIA Gain = 0.2

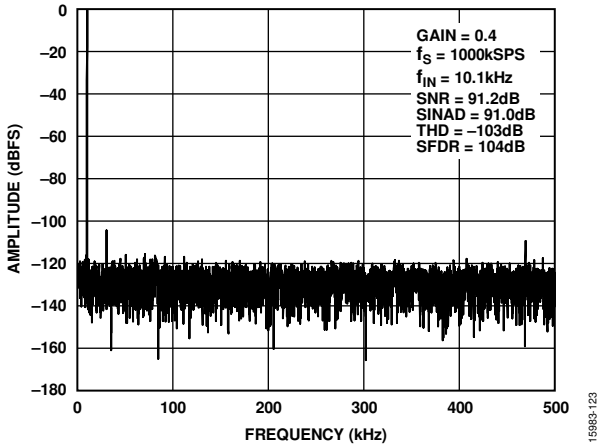


Figure 20. 10 kHz FFT, PGIA Gain = 0.4

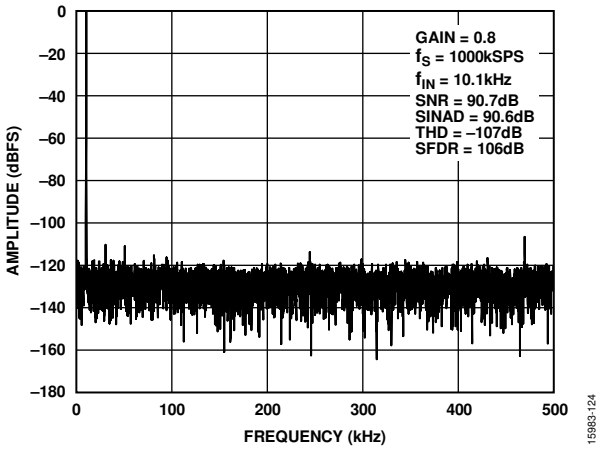


Figure 21. 10 kHz FFT, PGIA Gain = 0.8

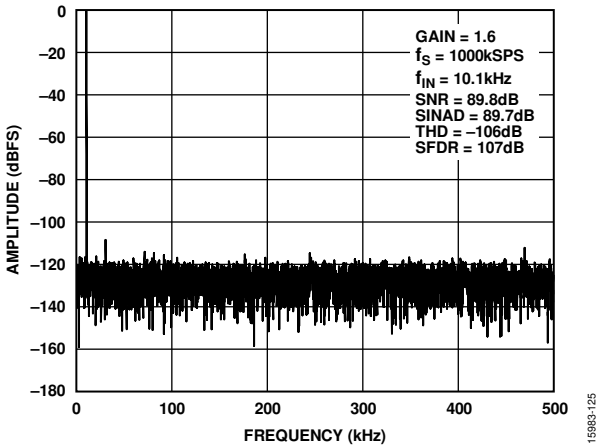


Figure 22. 10 kHz FFT, PGIA Gain = 1.6

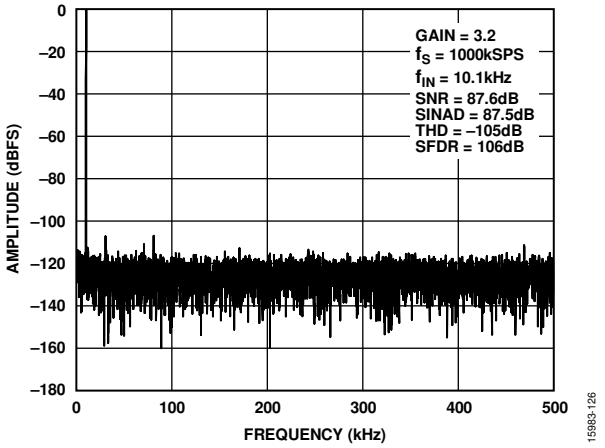


Figure 23. 10 kHz FFT, PGIA Gain = 3.2

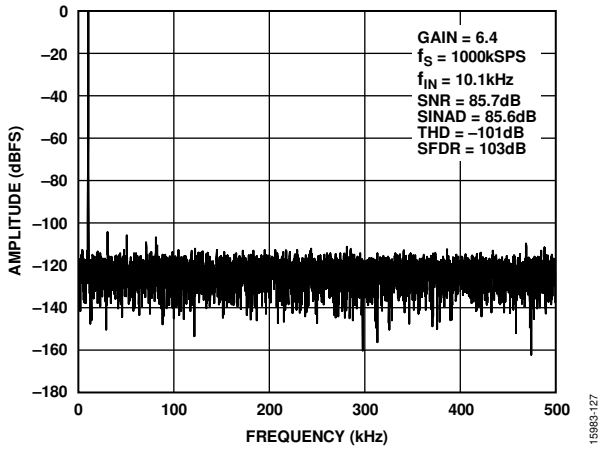


Figure 24. 10 kHz FFT, PGIA Gain = 6.4

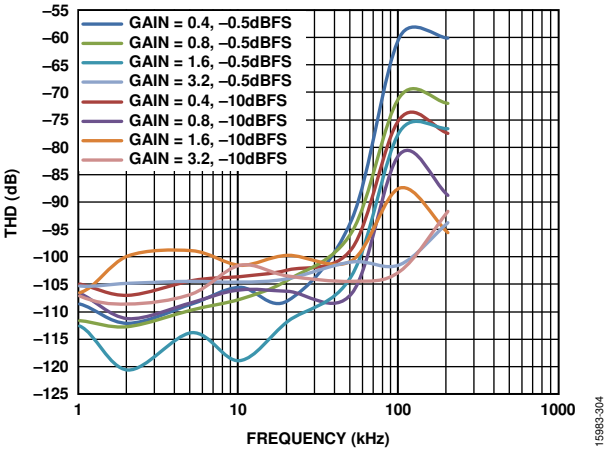


Figure 27. THD vs. Frequency

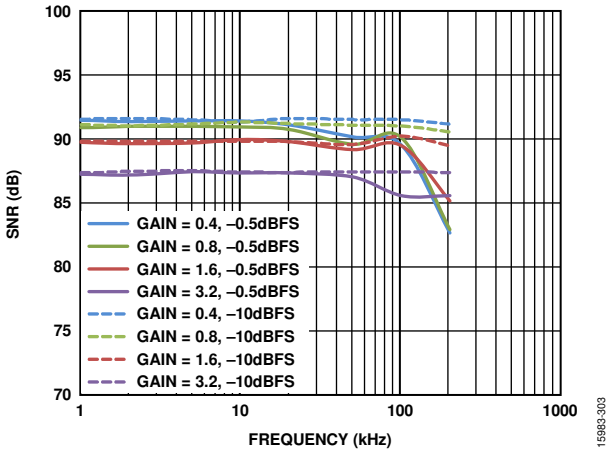


Figure 25. SNR vs. Frequency

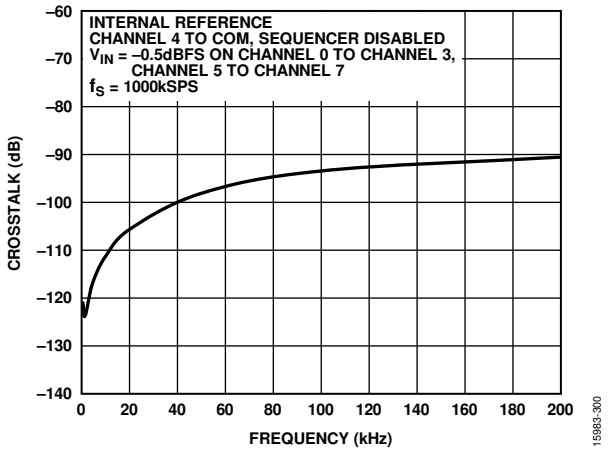


Figure 28. Crosstalk vs. Frequency

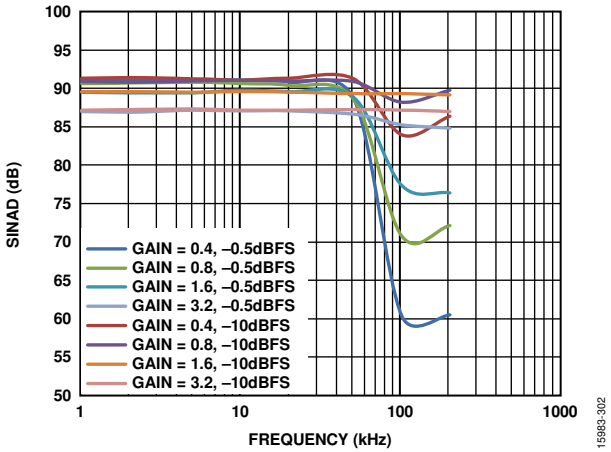


Figure 26. SINAD vs. Frequency

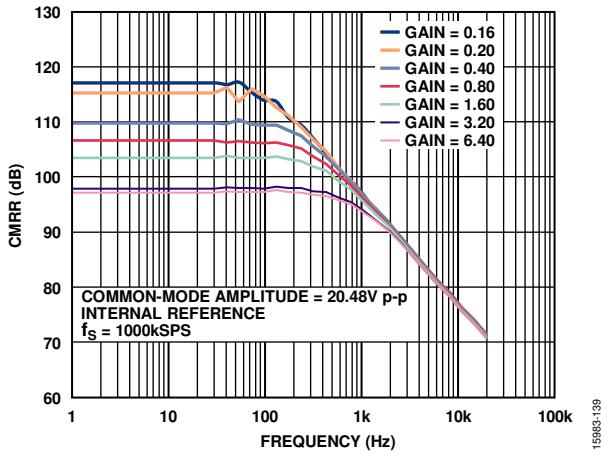


Figure 29. CMRR vs. Frequency

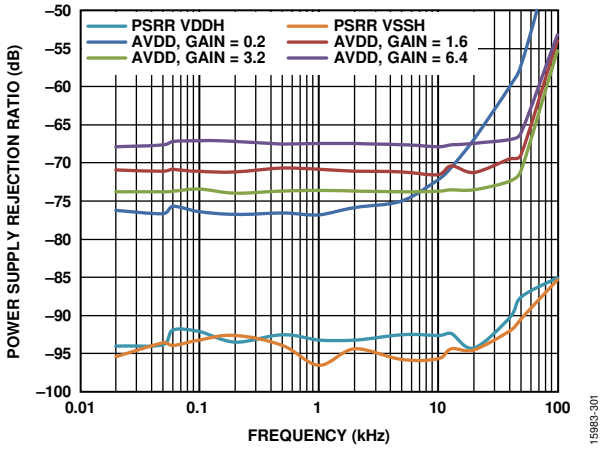


Figure 30. Power Supply Rejection Ration (PSRR) vs. Frequency

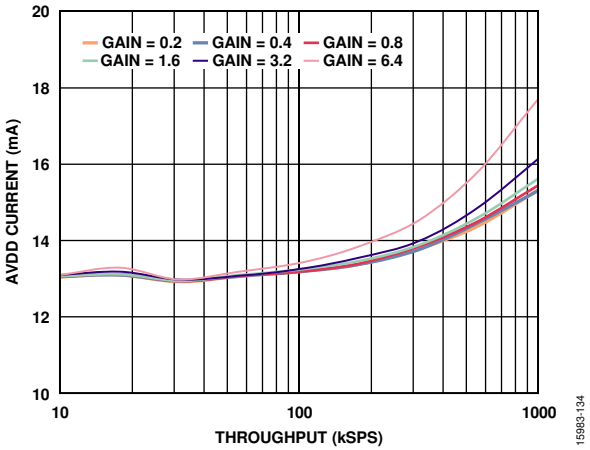


Figure 33. AVDD Current vs. Throughput, Internal Reference

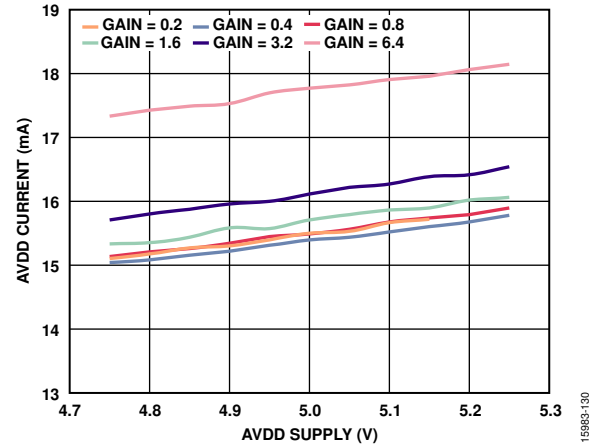


Figure 31. AVDD Current vs. AVDD Supply, Internal Reference

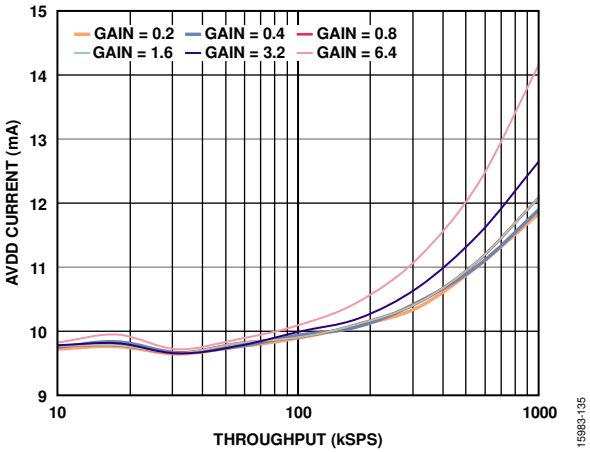


Figure 34. AVDD Current vs. Throughput, External Reference

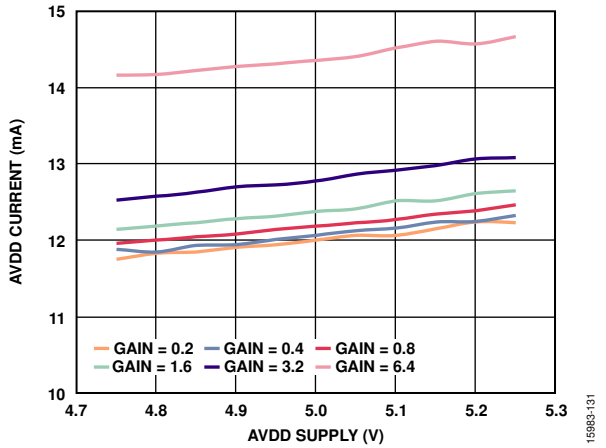


Figure 32. AVDD Current vs. AVDD Supply, External Reference

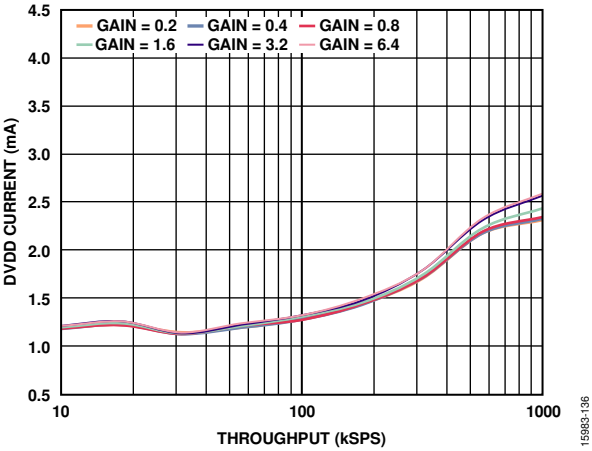


Figure 35. DVDD Current vs. Throughput

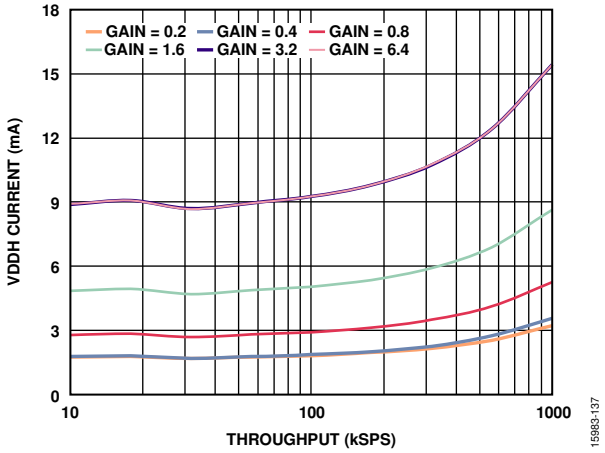


Figure 36. VDDH Current vs. Throughput

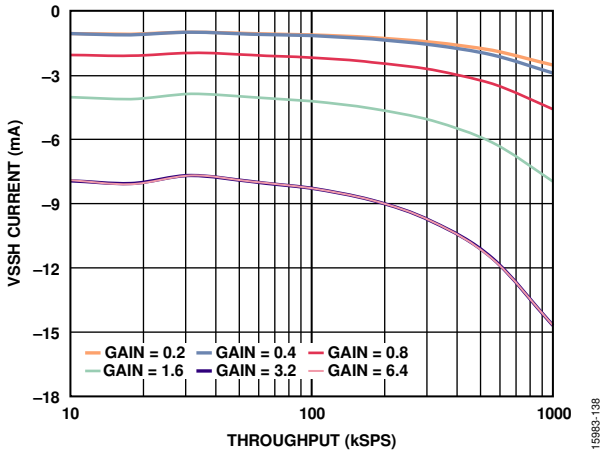


Figure 37. VSSH Current vs. Throughput

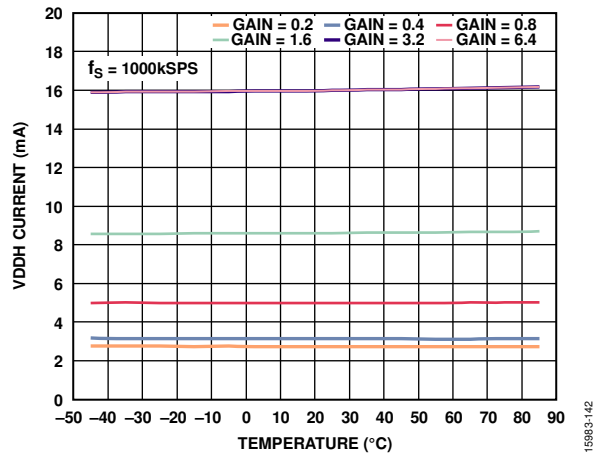


Figure 38. VDDH Current vs. Temperature

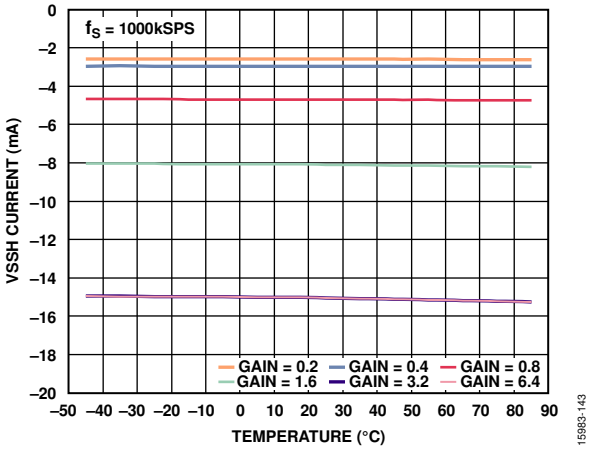


Figure 39. VSSH Current vs. Temperature

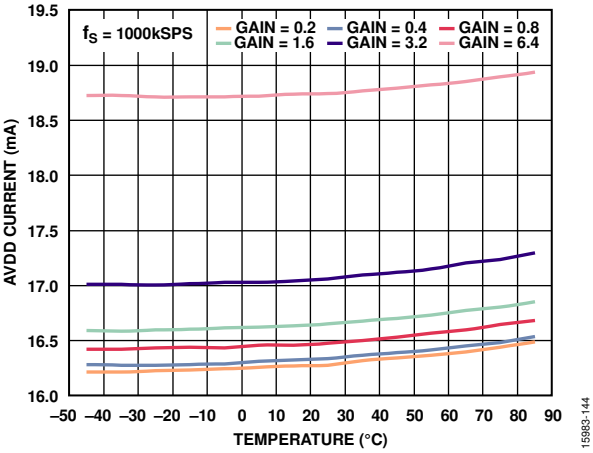


Figure 40. AVDD Current vs. Temperature

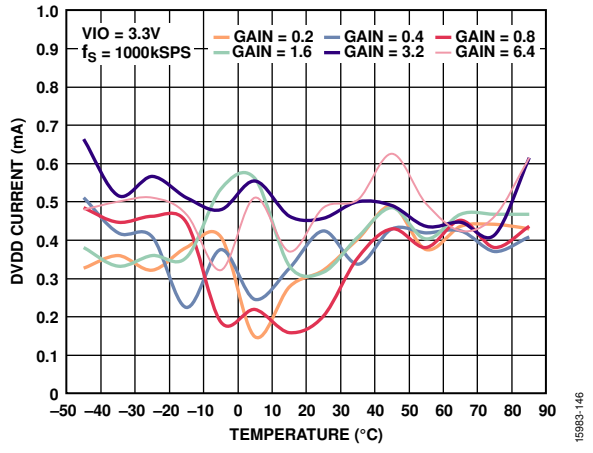


Figure 41. DVDD Current vs. Temperature

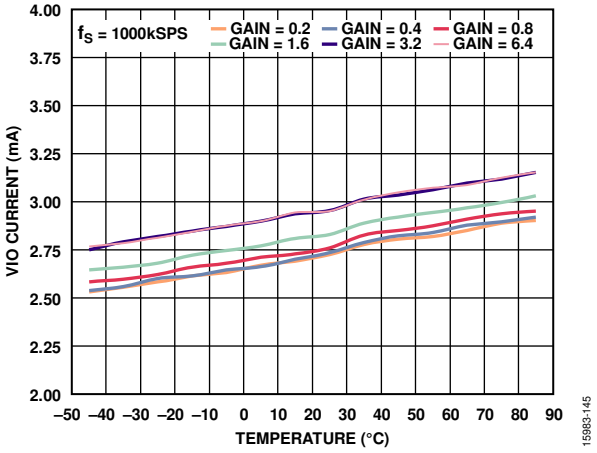


Figure 42. VIO Current vs. Temperature

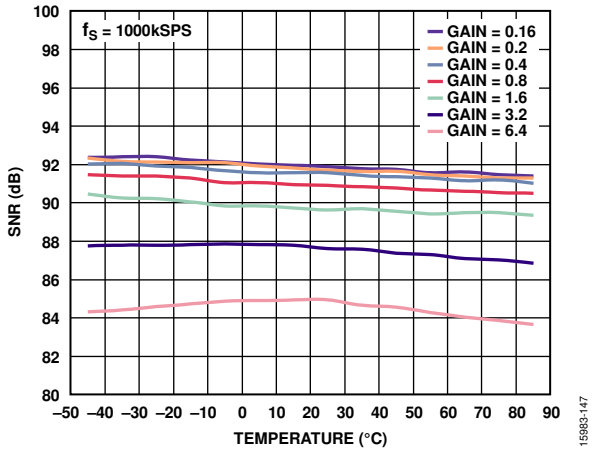


Figure 43. SNR vs. Temperature

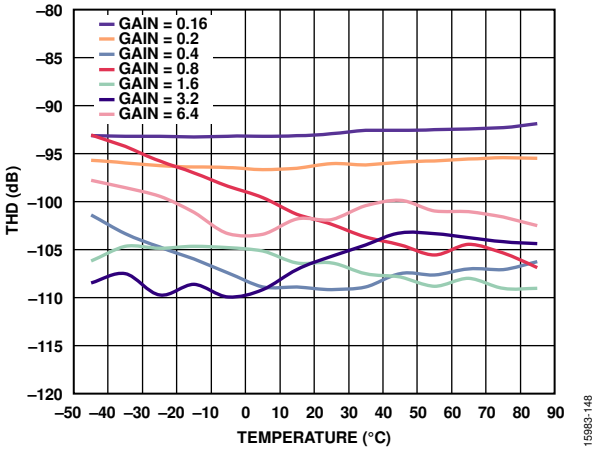


Figure 44. THD vs. Temperature

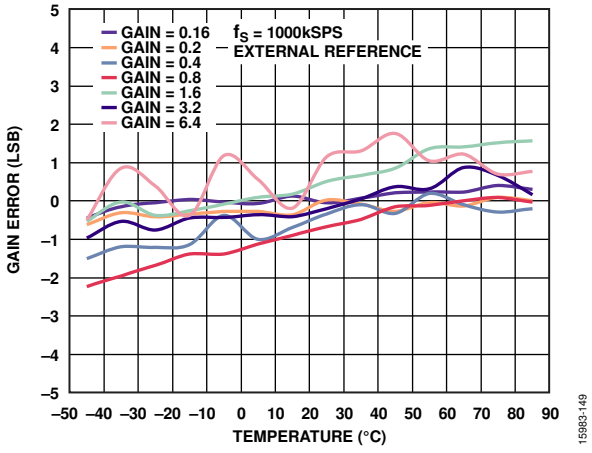


Figure 45. Gain Error vs. Temperature

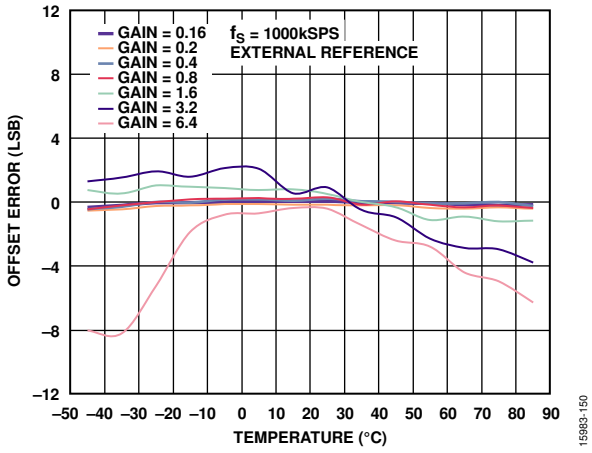


Figure 46. Offset Error vs. Temperature

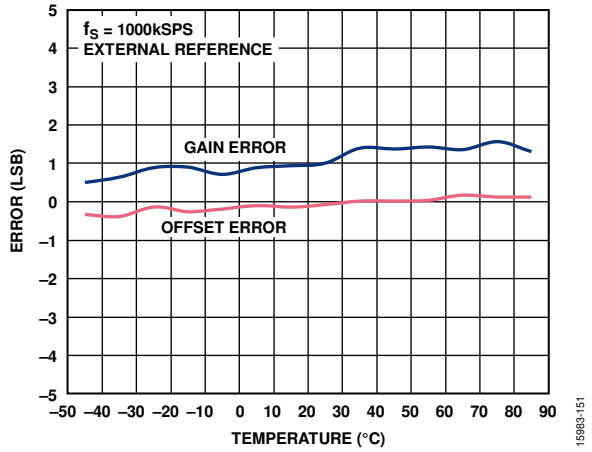


Figure 47. Offset and Gain Errors of the AUX+/AUX– ADC Channel Pair vs. Temperature

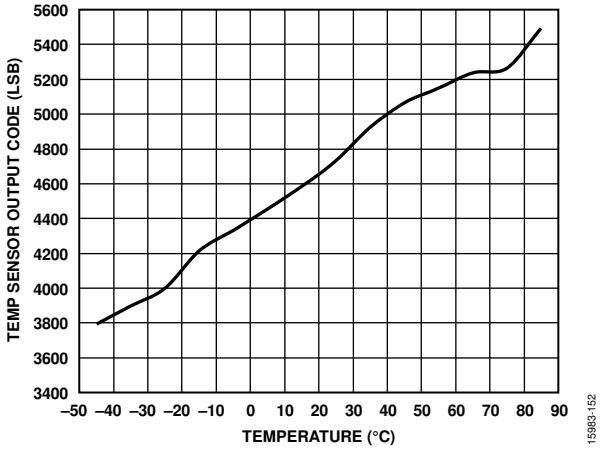


Figure 48. Temperature Sensor Output Code vs. Temperature

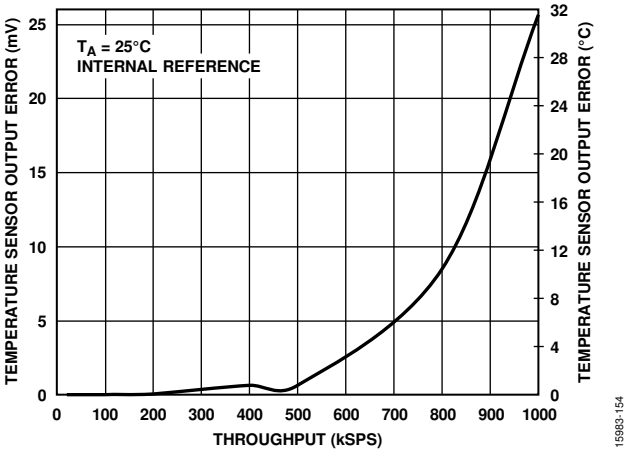


Figure 50. Temperature Sensor Output Error vs. Throughput

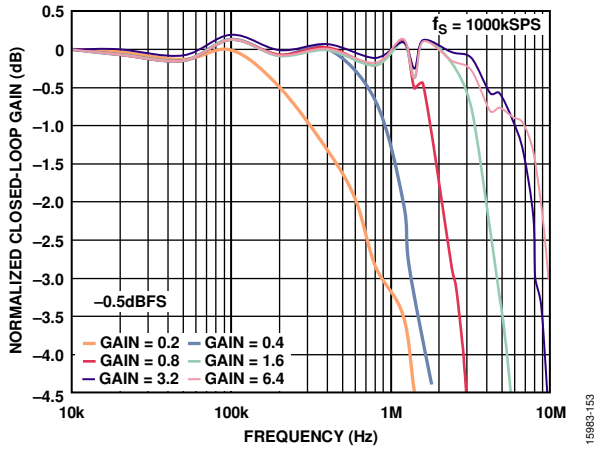


Figure 49. Large Signal Frequency Response vs. Gain

OUTLINE DIMENSIONS

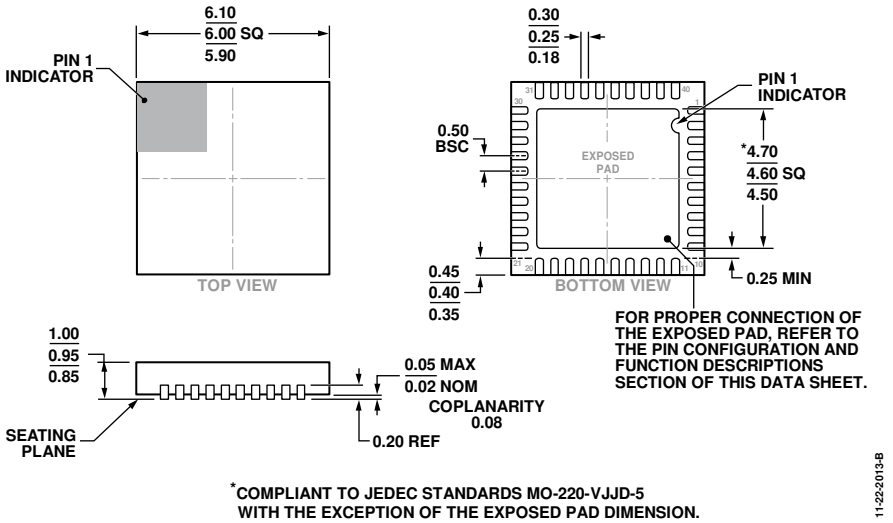


Figure 51. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)
Dimensions shown in millimeters
(See the ADAS3022 Data Sheet for Additional Information)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAS3022SCPZ-EP	−55°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADAS3022SCPZ-EP-RL	−55°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
EVAL-ADAS3022EDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.